

## More Information

Cypress provides a wealth of data at <http://www.cypress.com> to help you to select the right PSoC device for your design, and to help you to quickly and effectively integrate the device into your design. For a comprehensive list of resources, see the introduction page for [Bluetooth® Low Energy \(BLE\) Products](#). Following is an abbreviated list for PRoC BLE:

- Overview: PSoC Portfolio, PSoC Roadmap
- Product Selectors: PSoC 1, PSoC 3, PSoC 4, PRoC BLE, PSoC 4 BLE, PSoC 5LP In addition, PSoC Creator includes a device selection tool.
- Application Notes: Cypress offers a large number of PSoC application notes converting a broad range of topics, from basic to advanced level. Recommended application notes for getting started with PRoC BLE are:
  - [AN94020](#): Getting Started with PRoC BLE
  - [AN97060](#): PSoC 4 BLE and PRoC BLE - Over-The-Air (OTA) Device Firmware Upgrade (DFU) Guide
  - [AN91184](#): PSoC 4 BLE - Designing BLE Applications
  - [AN91162](#): Creating a BLE Custom Profile
  - [AN91445](#): Antenna Design and RF Layout Guidelines
  - [AN96841](#): Getting Started With EZ-BLE Module
  - [AN85951](#): PSoC 4 CapSense Design Guide

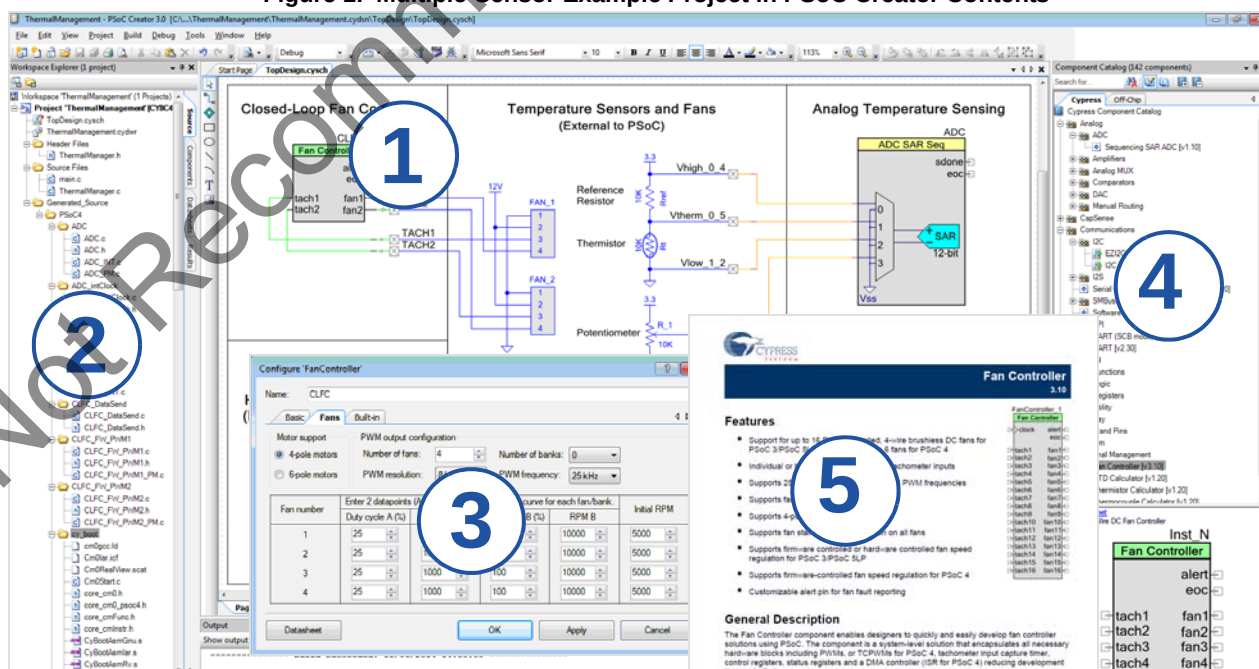
- [AN95089](#): PSoC 4/PRoC BLE Crystal Oscillator Selection and Tuning Techniques
- [AN92584](#): Designing for Low Power and Estimating Battery Life for BLE Applications
- Technical Reference Manual (TRM) is in two documents:
  - [Architecture TRM](#) details each PRoC BLE functional block
  - [Registers TRM](#) describes each of the PRoC BLE registers
- Development Kits:
  - [CY8CKIT-042-BLE](#) Pioneer Kit, is a flexible, Arduino-compatible, Bluetooth LE development kit for PSoC 4 BLE and PRoC BLE.
  - [CY5676](#), PRoC BLE 256KB Module, features a PRoC BLE 256KB device, two crystals for the antenna matching network, a PCB antenna and other passives, while providing access to all GPIOs of the device.
  - [CY8CKIT-142](#), PSoC 4 BLE Module, features a PSoC 4 BLE device, two crystals for the antenna matching network, a PCB antenna and other passives, while providing access to all GPIOs of the device.
  - [CY8CKIT-143](#), PSoC 4 BLE 256KB Module, features a PSoC 4 BLE 256KB device, two crystals for the antenna matching network, a PCB antenna and other passives, while providing access to all GPIOs of the device.
  - The [MiniProg3](#) device provides an interface for flash programming and debug.

## PSoC Creator

[PSoC Creator](#) is a free Windows-based Integrated Design Environment (IDE). It enables concurrent hardware and firmware design of PSoC 3, PSoC 4, and PSoC 5LP based systems. Create designs using classic, familiar schematic capture supported by over 100 pre-verified, production-ready PSoC Components; see the [list of component datasheets](#). With PSoC Creator, you can:

1. Drag and drop component icons to build your hardware system design in the main design workspace
2. Codesign your application firmware with the PSoC hardware, using the PSoC Creator IDE C compiler
3. Configure components using the configuration tools
4. Explore the library of 100+ components
5. Review component datasheets

**Figure 1. Multiple-Sensor Example Project in PSoC Creator Contents**



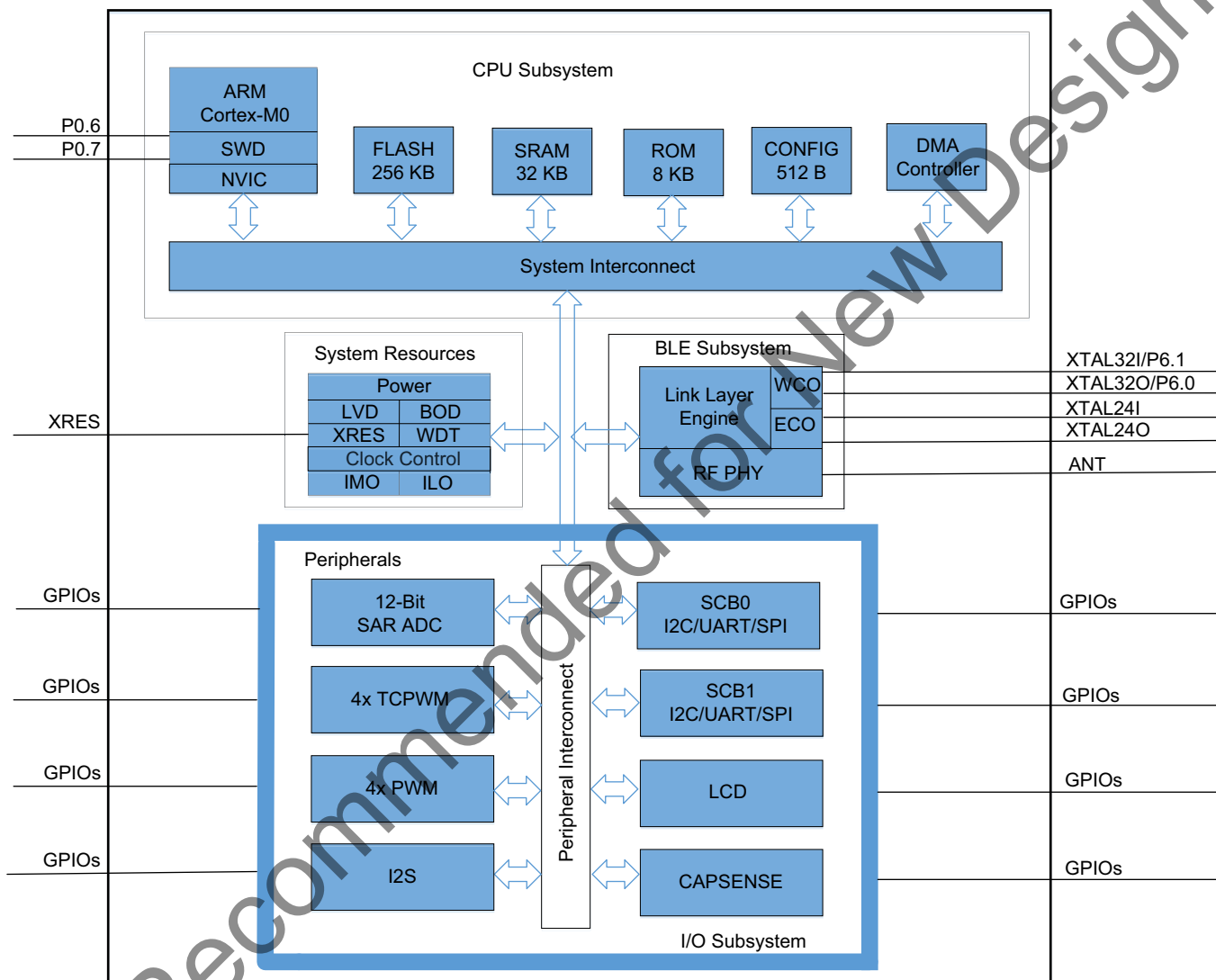
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## Blocks and Functionality

The CYBL1XX7X block diagram is shown in Figure 2. There are five major subsystems: CPU subsystem, BLE subsystem, system resources, peripheral blocks, and I/O subsystem.

Figure 2. Block Diagram



The PRoC BLE family includes extensive support for programming, testing, debugging, and tracing both hardware and firmware. The complete debug-on-chip functionality enables full-device debugging in the final system using the standard production device. It does not require special interfaces, debugging pods, simulators, or emulators. Only the standard programming connections are required to fully support debug.

The PSoC Creator IDE provides fully integrated programming and debug support for PRoC BLE devices. The SWD interface is fully compatible with industry-standard third-party tools. PRoC BLE also supports disabling the SWD interface and has a robust flash-protection feature.

## CPU Subsystem

### CPU

The CYBL1XX7X device is based on an energy-efficient ARM Cortex-M0 32-bit processor, offering low power consumption, high performance, and reduced code size using 16-bit thumb instructions. The Cortex-M0's ability to perform single-cycle 32-bit arithmetic and logic operations, including single-cycle 32-bit multiplication, helps in better performance. The inclusion of the tightly-integrated Nested Vectored Interrupt Controller (NVIC) with 32 interrupt lines enables the Cortex-M0 to achieve a low latency and a deterministic interrupt response.

The CPU also includes a 2-pin interface, the serial wire debug (SWD), which is a 2-wire form of JTAG. The debug circuits are enabled by default and can only be disabled in firmware. If disabled, the only way to re-enable them is to erase the entire device, clear flash protection, and reprogram the device with the new firmware that enables debugging. In addition, it is possible to use the debug pins as GPIO too. The device has four breakpoints and two watchpoints for effective debugging.

### Flash

The device has a 256-KB flash memory with a flash accelerator, tightly coupled to the CPU to improve average access times from flash. The flash is designed to deliver 1-wait-state (WS) access time at 48 MHz and with 0-WS access time at 24 MHz. The flash accelerator delivers 85% of single-cycle SRAM access performance on average. Part of the flash can be used to emulate EEPROM operation, if required.

During flash erase and programming operations (the maximum erase and program time is 20 ms per row), the IMO will be set to 48 MHz for the duration of the operation. This also applies to the emulated EEPROM. System design must take this into account because peripherals operating from different IMO frequencies will be affected. If it is critical that peripherals continue to operate with no change during flash programming, always set the IMO to 48 MHz and derive the peripheral clocks by dividing down from this frequency.

### SRAM

The low-power 32-KB SRAM memory retains its contents even in Hibernation mode.

### ROM

The 8-KB supervisory ROM contains a library of executable functions for flash programming. These functions are accessed through supervisory calls (SVC) and enable in-system programming of the flash memory.

### DMA

DMA controller provides DataWrite (DW) and Direct Memory Access (DMA). The DMA controller has following features

- Supports up to 8 DMA channels with two independent descriptors per channel
- Four levels of priority for each channel
- Byte, half-word (2 bytes), and word (4 bytes) transfers
- Three modes of operation supported for each channel
- Configurable interrupt generation
- Output trigger on completion of transfer (transfer sizes up to 65536 data elements)

## BLE Subsystem

The BLE subsystem consists of the link layer engine and physical layer. The link layer engine supports both master and slave roles. The link layer engine implements time-critical functions such as encryption in the hardware to reduce the power consumption, and provides minimal processor intervention and a high performance. The key protocol elements, such as host control interface (HCI) and link control, are implemented in firmware. The direct test mode (DTM) is included to test the radio performance using a standard Bluetooth tester.

The physical layer consists of a modem and an RF transceiver that transmits and receives BLE packets at the rate of 1 Mbps over the 2.4-GHz ISM band. In the transmit direction, this block performs GFSK modulation and then converts the digital baseband signal of these BLE packets into radio frequency before transmitting them to air through an antenna. In the receive direction, this block converts an RF signal from the antenna to a digital bit stream after performing GFSK demodulation.

The RF transceiver contains an integrated balun, which provides a single-ended RF port pin to drive a 50-Ω antenna terminal through a pi-matching network. The output power is programmable from -18 dBm to +3 dBm to optimize the current consumption for different applications.

The Bluetooth Low Energy protocol stack uses the BLE subsystem and provides the following features:

- Link Layer (LL)
  - Master and Slave roles
  - 128-bit AES engine
  - Encryption
  - Low-duty-cycle advertising
  - LE Ping
  - LE Data Packet Length Extension (Bluetooth 4.2 feature)
  - Link Layer Privacy (with extended scanning filter policy) (Bluetooth 4.2 feature)
- Bluetooth Low Energy 4.2 single-mode protocol stack with logical link control and adaptation protocol (L2CAP), attribute (ATT), and security manager (SM) protocols
- Master and slave roles
- API access to generic attribute profile (GATT), generic access profile (GAP), and L2CAP
- L2CAP connection-oriented channel
- GAP features
  - Broadcaster, Observer, Peripheral, and Central roles
  - Security mode 1: Level 1, 2, 3, and 4
  - Security mode 2: Level 1 and 2
  - User-defined advertising data
  - Multiple-bond support
- GATT features
  - GATT client and server
  - Supports GATT subprocedures
  - 32-bit universally unique identifiers (UUID)
- Security Manager (SM)
  - LE Secure Connections (Bluetooth 4.2 feature)
  - Pairing methods: Just Works, Passkey Entry, Out of Band, and Numeric Comparison
  - Authenticated man-in-the-middle (MITM) protection and data signing
- Supports all SIG-adopted BLE profiles

## System Resources Subsystem

### Power

The power block includes internal LDOs that supply required voltage levels for different blocks. The power system also includes POR, BOD, and LVD circuits. The POR circuit holds the device in the reset state until the power supplies have stabilized at appropriate levels and the clock is ready. The BOD circuit resets the device when the supply voltage is too low for proper device operation. The LVD circuit generates an interrupt if the supply voltage drops below a user-selectable level.

An external active-LOW reset pin (XRES) can be used to reset the device. The XRES pin has an internal pull-up resistor and, in most applications, does not require any additional pull-up resistors. The power system is described in detail in the “Power” section on page 14.

### Clock Control

The PRoC BLE clock control is responsible for providing clocks to all subsystems and also for switching between different clock sources without glitching. The clock control for PRoC BLE consists of the IMO and the internal low-speed oscillator (ILO). It uses the 24-MHz external crystal oscillator (ECO) and the 32-kHz WCO. In addition, an external clock may be supplied from a pin.

The device has 12 dividers with 16 divider outputs. Two dividers have additional fractional division capability. The HFCLK signal is divided down, as shown in Figure 3, to generate the system clock (SYSCLK) and peripheral clock (PERx\_CLK) for different peripherals. The system clock (SYSCLK) driving buses, registers, and the processor must be higher than all the other clocks in the system that are divided off HFCLK. The ECO and WCO are present in the BLE subsystem and the clock outputs are routed to the system resources.

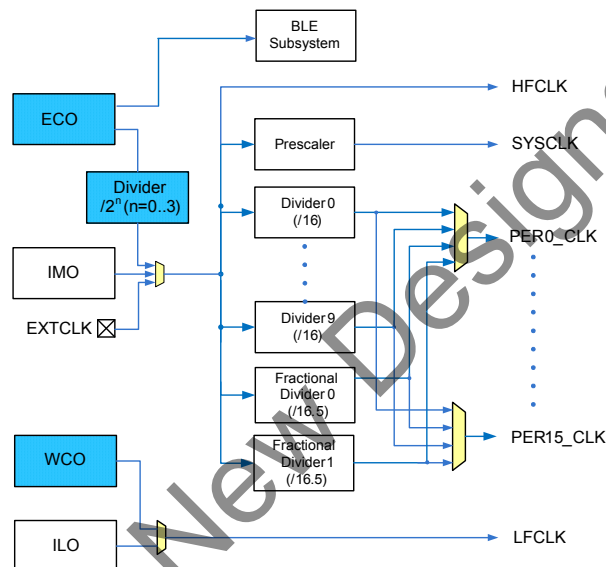
### Internal Main Oscillator (IMO)

The IMO is the primary system clock source, which can be adjusted in the range of 3 MHz to 48 MHz in steps of 1 MHz. The IMO accuracy is  $\pm 2\%$ .

### Internal Low-Speed Oscillator (ILO)

The ILO is a very-low-power 32-kHz oscillator, which is primarily used to generate clocks for peripheral operations in Deep-Sleep mode. The ILO-driven counters can be calibrated to the IMO to improve accuracy. Cypress provides a software component, which does the calibration.

Figure 3. Clock Control



### External Crystal Oscillator (ECO)

The ECO is used as the active clock for the BLE subsystem to meet the  $\pm 50$ -ppm clock accuracy requirement of the Bluetooth Low Energy Specification. The internal tunable load capacitor is provided to tune the crystal clock frequency. The high-accuracy ECO clock can also be used as a system clock.

### Watch Crystal Oscillator (WCO)

The WCO is used as the sleep clock for the BLE subsystem to meet the  $\pm 500$ -ppm clock accuracy requirement of the Bluetooth Low Energy Specification. The sleep clock provides accurate sleep timing and enables wakeup at specified advertisement and connection intervals. With the WCO and firmware, an accurate real-time clock (within the bounds of the 32.768-kHz crystal accuracy) can be realized.

### Voltage Reference

The internal bandgap reference circuit with 1% accuracy provides the voltage reference for the 12-bit SAR ADC. To enable better SNRs and absolute accuracy, it will be possible to bypass the internal bandgap reference using a REF pin and to use an external reference for the SAR.

### Watchdog Timer (WDT)

A watchdog timer is implemented in the system resources subsystem running from the ILO; this allows watchdog operations during Deep-Sleep mode and generates a watchdog reset if not serviced before the timeout occurs. The watchdog reset is recorded in the 'Reset Cause' register.

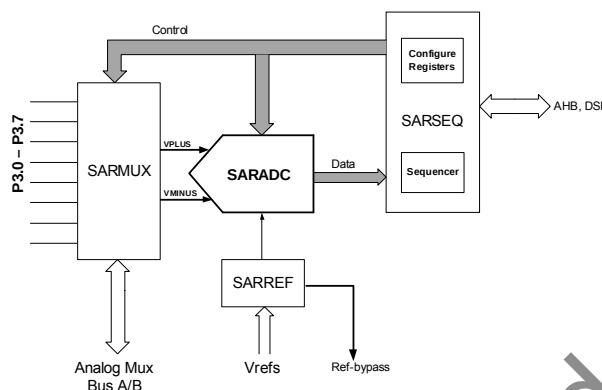
## Peripheral Blocks

### 12-Bit SAR ADC

The ADC is a 12-bit, 1-Msps SAR ADC with a built-in sample-and-hold (S/H) circuit. The ADC can operate with either an internal voltage reference or an external voltage reference.

Preceding the SAR ADC is the SARMUX, which can route external pins and internal signals (analog mux bus and temperature sensor output) to the eight internal channels of the SAR ADC. The sequencer controller (SARSEQ) is used to control the SARMUX and SAR ADC to do an automatic scan on all enabled channels without CPU intervention and for preprocessing tasks such as averaging the output data. A Cypress-supplied software driver (Component) is used to control the ADC peripheral.

**Figure 4. SAR ADC System Diagram**



A diode based, on-chip temperature sensor is used to measure the die temperature. The temperature sensor is connected to the ADC, which digitizes the reading and produces a temperature value using the Cypress-supplied software that includes calibration and linearization.

### 4x Timer Counter PWM (TCPWM)

The 16-bit TCPWM module can be used to generate the PWM output or to capture the timing of edges of input signals or to provide a timer functionality. TCPWM can also be used as a 16-bit counter that supports up, down, and up/down counting modes.

Rising edge, falling edge, combined rising/falling edge detection, or pass-through on all hardware input signals can be used to derive counter events. Three routed output signals are available to indicate underflow, overflow, and counter/compare match events. A maximum of four TCPWMs are available.

### 4x PWM

These PWMs are in addition to the TCPWMs. The PWM peripheral can be configured as 8-bit or 16-bit resolution. The PWM provides compare outputs to generate single or continuous timing and control signals in hardware. It also provides an easy method of generating complex real-time events accurately with minimal CPU intervention. A maximum of four 8-bit PWMs or two 16-bit PWMs are available.

### Serial Communication Block (SCB0/SCB1)

The SCB can be configured as an I<sup>2</sup>C, UART, or SPI interface. It supports an 8-byte FIFO for receive and transmit buffers to reduce CPU intervention. A maximum of two SCBs (SCB0, SCB1) are available.

**I<sup>2</sup>C mode:** The I<sup>2</sup>C peripheral is compatible with the I<sup>2</sup>C Standard-mode, Fast-mode, and Fast-Mode-Plus devices as defined in the NXP I<sup>2</sup>C-bus specification and user manual (UM10204). The I<sup>2</sup>C bus I/O is implemented with GPIOs in open-drain modes.

The hardware I<sup>2</sup>C block implements a full multimaster and slave interface (it is capable of multimaster arbitration). This block is capable of operating at speeds of up to 1 Mbps (Fast-Mode Plus) and has flexible buffering options to reduce the interrupt overhead and latency for the CPU. The I<sup>2</sup>C function is implemented using the Cypress-provided software Component (EzI2C) that creates a mailbox address range in the memory of PROc BLE and effectively reduces the I<sup>2</sup>C communication to reading from and writing to an array in memory. In addition, the block supports an 8-byte FIFO for receive and transmit, which, by increasing the time given for the CPU to read data, greatly reduces the need for clock stretching caused by the CPU not having read the data on time.

When SCB0 is used, Serial Data (SDA) and Serial Clock (SCL) of I<sup>2</sup>C can be connected to P0.4 and P0.5, or P1.4 and P1.5, or P3.0 and P3.1.

When SCB1 is used, SDA and SCL can be connected to P0.0 and P0.1, or P3.4 and P3.5, or P5.0 and P5.1.

Configurations for I<sup>2</sup>C are as follows:

- SCB1 is fully compliant with the Standard-mode (100 kHz), Fast-mode (400 kHz), and Fast-Mode-Plus (1 MHz) I<sup>2</sup>C signaling specifications when routed to GPIO pins P5.0 and P5.1, except for hot-swap capability during I<sup>2</sup>C active communication.
- SCB1 is compliant only with Standard mode (100 kHz) when not used with P5.0 and P5.1.
- SCB0 is compliant with Standard mode (100 kHz) only.

**UART mode:** This is a full-feature UART operating up to 1 Mbps. It supports automotive single-wire interface (LIN), infrared interface (IrDA), and SmartCard (ISO7816) protocols. In addition, it supports the 9-bit multiprocessor mode, which allows addressing of peripherals connected over common RX and TX lines. The UART hardware flow control is supported to allow slow and fast devices to communicate with each other over UART without the risk of losing data. Refer to Table 4 on page 13 for possible UART connections to the GPIOs.

**SPI Mode:** The SPI mode supports full Motorola® SPI, Texas Instruments® Secure Simple Pairing (SSP) (essentially adds a start pulse used to synchronize SPI Codecs), and National Microwire (half-duplex form of SPI). The block supports an 8-byte FIFO for receive and transmit. Refer to Table 4 on page 13 for the possible SPI connections to the GPIOs.

#### Inter-IC Sound Bus (I<sup>2</sup>S)

Inter-IC Sound Bus (I<sup>2</sup>S) is a serial bus interface standard used for connecting digital audio devices. The specification is from Philips® Semiconductor (I<sup>2</sup>S bus specification; February 1986, revised June 5, 1996).

I<sup>2</sup>S operates only in the Master mode, supporting the transmitter (TX) and the receiver (RX), which have independent data byte streams. These byte streams are packed with the most significant byte first. The number of bytes used for each sample (a sample for the left or right channel) is the minimum number of bytes to hold a sample.

#### LCD

The LCD controller can drive up to four commons and up to 32 segments. It uses full digital methods to drive the LCD segments providing ultra-low power consumption. The two methods used are referred to as digital correlation and PWM.

The digital correlation method modulates the frequency and signal levels of the commons and segments to generate the highest RMS voltage across a segment to light it up or to maintain the RMS signal as zero. This method is good for STN displays but may result in reduced contrast in TN (cheaper) displays.

The PWM method drives the panel with PWM signals to effectively use the capacitance of the panel to provide the integration of the modulated pulse-width to generate the desired LCD voltage. This method results in higher power consumption but provides better results in driving TN displays.

LCD operation is supported during Deep Sleep mode by refreshing a small display buffer (four bits; one 32-bit register per port).

#### CapSense

CapSense is supported on all GPIOs through a Capacitive Sigma-Delta (CSD) block, which can be connected to any GPIO through an analog mux bus. Any GPIO pin can be connected to the analog mux bus via an analog switch. The CapSense function can thus be provided on any pin or group of pins in a

system under software control. A software Component in PSoC Creator is provided for the CapSense block to make it easy for the user. The shield voltage can be driven on another mux bus to provide liquid-tolerance capability. Driving the shield electrode in phase with the sense electrode keeps the shield capacitance from attenuating the sensed input.

The CapSense trackpad/touchpad with gestures has the following features:

- Supports 1-finger and 2-finger touch applications
- Supports up to 36 X/Y sensor inputs
- Includes a gesture-detection library:
  - 1-finger touch: Finger tracking, scroll, inertial scroll, click, double-click, edge swipe
  - 2-finger touch: Scroll, inertial scroll, zoom-in, zoom-out

#### I/O Subsystem

The I/O subsystem, which comprises the GPIO block, implements the following:

- Eight drive-strength modes:
  - Analog input mode (input and output buffers disabled)
  - Input only
  - Weak pull-up with strong pull-down
  - Weak pull-up with weak pull-down
  - Strong pull-up with weak pull-down
  - Strong pull-up with strong pull-down
  - Open drain with strong pull-down
  - Open drain with strong pull-up
- Port pins: 36
- Input threshold select (CMOS or LVTTTL)
- Individual control of input and output buffers (enabling/disabling) in addition to drive-strength modes
- Hold mode for latching the previous state (used for retaining the I/O state in Deep Sleep and Hibernate modes)
- Selectable slew rates for dV/dt to improve EMI
- The GPIO pins P5.0 and P5.1 are overvoltage-tolerant
- The GPIO cells, including P5.0 and P5.1, cannot be hot-swapped or powered up independent of the rest of the system.

## Pinouts

Table 1 shows the pin list for the CYBL1XX7X device.

**Table 1. CYBL1XX7X Pin List (QFN Package)**

| Pin | Name         | Type    | Description                                 |
|-----|--------------|---------|---------------------------------------------|
| 1   | VDDD         | POWER   | 1.71-V to 5.5-V digital supply              |
| 2   | XTAL32O/P6.0 | CLOCK   | 32.768-kHz crystal                          |
| 3   | XTAL32I/P6.1 | CLOCK   | 32.768-kHz crystal or external clock input  |
| 4   | XRES         | RESET   | Reset, active LOW                           |
| 5   | P4.0         | GPIO    | Port 4 Pin 0, analog/digital/lcd/csd        |
| 6   | P4.1         | GPIO    | Port 4 Pin 1, analog/digital/lcd/csd        |
| 7   | P5.0         | GPIO    | Port 5 Pin 0, analog/digital/lcd/csd        |
| 8   | P5.1         | GPIO    | Port 5 Pin 1, analog/digital/lcd/csd        |
| 9   | VSSD         | GROUND  | Digital ground                              |
| 10  | VDDR         | POWER   | 1.9-V to 5.5-V radio supply                 |
| 11  | GANT1        | GROUND  | Antenna shielding ground                    |
| 12  | ANT          | ANTENNA | Antenna pin                                 |
| 13  | GANT2        | GROUND  | Antenna shielding ground                    |
| 14  | VDDR         | POWER   | 1.9-V to 5.5-V radio supply                 |
| 15  | VDDR         | POWER   | 1.9-V to 5.5-V radio supply                 |
| 16  | XTAL24I      | CLOCK   | 24-MHz crystal or external clock input      |
| 17  | XTAL24O      | CLOCK   | 24-MHz crystal                              |
| 18  | VDDR         | POWER   | 1.9-V to 5.5-V radio supply                 |
| 19  | P0.0         | GPIO    | Port 0 Pin 0, analog/digital/lcd/csd        |
| 20  | P0.1         | GPIO    | Port 0 Pin 1, analog/digital/lcd/csd        |
| 21  | P0.2         | GPIO    | Port 0 Pin 2, analog/digital/lcd/csd        |
| 22  | P0.3         | GPIO    | Port 0 Pin 3, analog/digital/lcd/csd        |
| 23  | VDDD         | POWER   | 1.71-V to 5.5-V digital supply              |
| 24  | P0.4         | GPIO    | Port 0 Pin 4, analog/digital/lcd/csd        |
| 25  | P0.5         | GPIO    | Port 0 Pin 5, analog/digital/lcd/csd        |
| 26  | P0.6         | GPIO    | Port 0 Pin 6, analog/digital/lcd/csd        |
| 27  | P0.7         | GPIO    | Port 0 Pin 7, analog/digital/lcd/csd        |
| 28  | P1.0         | GPIO    | Port 1 Pin 0, analog/digital/lcd/csd        |
| 29  | P1.1         | GPIO    | Port 1 Pin 1, analog/digital/lcd/csd        |
| 30  | P1.2         | GPIO    | Port 1 Pin 2, analog/digital/lcd/csd        |
| 31  | P1.3         | GPIO    | Port 1 Pin 3, analog/digital/lcd/csd        |
| 32  | P1.4         | GPIO    | Port 1 Pin 4, analog/digital/lcd/csd        |
| 33  | P1.5         | GPIO    | Port 1 Pin 5, analog/digital/lcd/csd        |
| 34  | P1.6         | GPIO    | Port 1 Pin 6, analog/digital/lcd/csd        |
| 35  | P1.7         | GPIO    | Port 1 Pin 7, analog/digital/lcd/csd        |
| 36  | VDDA         | POWER   | 1.71-V to 5.5-V analog supply               |
| 37  | P2.0         | GPIO    | Port 2 Pin 0, analog/digital/lcd/csd        |
| 38  | P2.1         | GPIO    | Port 2 Pin 1, analog/digital/lcd/csd        |
| 39  | P2.2         | GPIO    | Port 2 Pin 2, analog/digital/lcd/csd/WAKEUP |
| 40  | P2.3         | GPIO    | Port 2 Pin 3, analog/digital/lcd/csd        |

**Table 1. CYBL1XX7X Pin List (QFN Package) (continued)**

| Pin | Name | Type   | Description                                         |
|-----|------|--------|-----------------------------------------------------|
| 41  | P2.4 | GPIO   | Port 2 Pin 4, analog/digital/lcd/csd                |
| 42  | P2.5 | GPIO   | Port 2 Pin 5, analog/digital/lcd/csd                |
| 43  | P2.6 | GPIO   | Port 2 Pin 6, analog/digital/lcd/csd                |
| 44  | P2.7 | GPIO   | Port 2 Pin 7, analog/digital/lcd/csd                |
| 45  | VREF | REF    | 1.024-V reference                                   |
| 46  | VDDA | POWER  | 1.71-V to 5.5-V analog supply                       |
| 47  | P3.0 | GPIO   | Port 3 Pin 0, analog/digital/lcd/csd                |
| 48  | P3.1 | GPIO   | Port 3 Pin 1, analog/digital/lcd/csd                |
| 49  | P3.2 | GPIO   | Port 3 Pin 2, analog/digital/lcd/csd                |
| 50  | P3.3 | GPIO   | Port 3 Pin 3, analog/digital/lcd/csd                |
| 51  | P3.4 | GPIO   | Port 3 Pin 4, analog/digital/lcd/csd                |
| 52  | P3.5 | GPIO   | Port 3 Pin 5, analog/digital/lcd/csd                |
| 53  | P3.6 | GPIO   | Port 3 Pin 6, analog/digital/lcd/csd                |
| 54  | P3.7 | GPIO   | Port 3 Pin 7, analog/digital/lcd/csd                |
| 55  | VSSA | GROUND | Analog ground                                       |
| 56  | VCCD | POWER  | Regulated 1.8-V supply, connect to 1.3-μF capacitor |
| 57  | EPAD | GROUND | Ground paddle for the QFN package                   |

Table 2 shows the pin list for the CYBL1XX7X device (WLCSP package).

**Table 2. CYBL1XX7X Pin List (WLCSP Package)**

| Pin | Name         | Type    | Description                                       |
|-----|--------------|---------|---------------------------------------------------|
| A1  | NC           | NC      | Do not connect                                    |
| A2  | VREF         | REF     | 1.024-V reference                                 |
| A3  | VSSA         | GROUND  | Analog ground                                     |
| A4  | P3.3         | GPIO    | Port 3 Pin 3, analog/digital/lcd/csd              |
| A5  | P3.7         | GPIO    | Port 3 Pin 7, analog/digital/lcd/csd              |
| A6  | VSSD         | GROUND  | Digital ground                                    |
| A7  | VSSA         | GROUND  | Analog ground                                     |
| A8  | VCCD         | POWER   | Regulated 1.8-V supply, connect to 1-μF capacitor |
| A9  | VDDD         | POWER   | 1.71-V to 5.5-V digital supply                    |
| B1  | NB           | NO BALL | No Ball                                           |
| B2  | P2.3         | GPIO    | Port 2 Pin 3, analog/digital/lcd/csd              |
| B3  | VSSA         | GROUND  | Analog ground                                     |
| B4  | P2.7         | GPIO    | Port 2 Pin 7, analog/digital/lcd/csd              |
| B5  | P3.4         | GPIO    | Port 3 Pin 4, analog/digital/lcd/csd              |
| B6  | P3.5         | GPIO    | Port 3 Pin 5, analog/digital/lcd/csd              |
| B7  | P3.6         | GPIO    | Port 3 Pin 6, analog/digital/lcd/csd              |
| B8  | XTAL32I/P6.1 | CLOCK   | 32.768-kHz crystal or external clock input        |
| B9  | XTAL32O/P6.0 | CLOCK   | 32.768-kHz crystal                                |
| C1  | NC           | NC      | Do not connect                                    |
| C2  | VSSA         | GROUND  | Analog ground                                     |

**Table 2. CYBL1XX7X Pin List (WLCSP Package) (continued)**

| Pin | Name | Type   | Description                          |
|-----|------|--------|--------------------------------------|
| C3  | P2.2 | GPIO   | Port 2 Pin 2, analog/digital/lcd/csd |
| C4  | P2.6 | GPIO   | Port 2 Pin 6, analog/digital/lcd/csd |
| C5  | P3.0 | GPIO   | Port 3 Pin 0, analog/digital/lcd/csd |
| C6  | P3.1 | GPIO   | Port 3 Pin 1, analog/digital/lcd/csd |
| C7  | P3.2 | GPIO   | Port 3 Pin 2, analog/digital/lcd/csd |
| C8  | XRES | RESET  | Reset, active LOW                    |
| C9  | P4.0 | GPIO   | Port 4 Pin 0, analog/digital/lcd/csd |
| D1  | NC   | NC     | Do not connect                       |
| D2  | P1.7 | GPIO   | Port 1 Pin 7, analog/digital/lcd/csd |
| D3  | VDDA | POWER  | 1.71-V to 5.5-V analog supply        |
| D4  | P2.0 | GPIO   | Port 2 Pin 0, analog/digital/lcd/csd |
| D5  | P2.1 | GPIO   | Port 2 Pin 1, analog/digital/lcd/csd |
| D6  | P2.5 | GPIO   | Port 2 Pin 5, analog/digital/lcd/csd |
| D7  | VSSD | GROUND | Digital ground                       |
| D8  | P4.1 | GPIO   | Port 4 Pin 1, analog/digital/lcd/csd |
| D9  | P5.0 | GPIO   | Port 5 Pin 0, analog/digital/lcd/csd |
| E1  | NC   | NC     | Do not connect                       |
| E2  | P1.2 | GPIO   | Port 1 Pin 2, analog/digital/lcd/csd |
| E3  | P1.3 | GPIO   | Port 1 Pin 3, analog/digital/lcd/csd |
| E4  | P1.4 | GPIO   | Port 1 Pin 4, analog/digital/lcd/csd |
| E5  | P1.5 | GPIO   | Port 1 Pin 5, analog/digital/lcd/csd |
| E6  | P1.6 | GPIO   | Port 1 Pin 6, analog/digital/lcd/csd |
| E7  | P2.4 | GPIO   | Port 2 Pin 4, analog/digital/lcd/csd |
| E8  | P5.1 | GPIO   | Port 5 Pin 1, analog/digital/lcd/csd |
| E9  | VSSD | GROUND | Digital ground                       |
| F1  | NC   | NC     | Do not connect                       |
| F2  | VSSD | GROUND | Digital ground                       |
| F3  | P0.7 | GPIO   | Port 0 Pin 7, analog/digital/lcd/csd |
| F4  | P0.3 | GPIO   | Port 0 Pin 3, analog/digital/lcd/csd |
| F5  | P1.0 | GPIO   | Port 1 Pin 0, analog/digital/lcd/csd |
| F6  | P1.1 | GPIO   | Port 1 Pin 1, analog/digital/lcd/csd |
| F7  | VSSR | GROUND | Radio ground                         |
| F8  | VSSR | GROUND | Radio ground                         |
| F9  | VDDR | POWER  | 1.9-V to 5.5-V radio supply          |
| G1  | NC   | NC     | Do not connect                       |
| G2  | P0.6 | GPIO   | Port 0 Pin 6, analog/digital/lcd/csd |
| G3  | VDDD | POWER  | 1.71-V to 5.5-V digital supply       |
| G4  | P0.2 | GPIO   | Port 0 Pin 2, analog/digital/lcd/csd |
| G5  | VSSD | GROUND | Digital ground                       |
| G6  | VSSR | GROUND | Radio ground                         |

**Table 2. CYBL1XX7X Pin List (WLCSP Package) (continued)**

| Pin | Name       | Type    | Description                            |
|-----|------------|---------|----------------------------------------|
| G7  | VSSR       | GROUND  | Radio ground                           |
| G8  | GANT       | GROUND  | Antenna shielding ground               |
| G9  | VSSR       | GROUND  | Radio ground                           |
| H1  | NC         | NC      | Do not connect                         |
| H2  | P0.5       | GPIO    | Port 0 Pin 5, analog/digital/lcd/csd   |
| H3  | P0.1       | GPIO    | Port 0 Pin 1, analog/digital/lcd/csd   |
| H4  | XTAL24O    | CLOCK   | 24-MHz crystal                         |
| H5  | XTAL24I    | CLOCK   | 24-MHz crystal or external clock input |
| H6  | VSSR       | GROUND  | Radio ground                           |
| H7  | VSSR       | GROUND  | Radio ground                           |
| H8  | ANT        | ANTENNA | Antenna pin                            |
| J1  | NC         | NC      | Do not connect                         |
| J2  | P0.4       | GPIO    | Port 0 Pin 4, analog/digital/lcd/csd   |
| J3  | P0.0       | GPIO    | Port 0 Pin 0, analog/digital/lcd/csd   |
| J4  | VDDR       | POWER   | 1.9-V to 5.5-V radio supply            |
| J7  | VDDR       | POWER   | 1.9-V to 5.5-V radio supply            |
| J8  | NO CONNECT | —       | —                                      |

The I/O subsystem consists of a high-speed I/O matrix (HSIOM), which is a group of high-speed switches that routes GPIOs to the resources inside the device. These resources include CapSense, TCPWMs, I<sup>2</sup>C, SPI, UART, and LCD. HSIOM\_PORT\_SELx are 32-bit-wide registers that control the routing of GPIOs. Each register controls one port; four dedicated bits are assigned to each GPIO in the port. This provides up to 16 different options for GPIO routing as shown in [Table 3](#).

**Table 3. HSIOM Port Settings**

| Value | Description                         |
|-------|-------------------------------------|
| 0     | Firmware-controlled GPIO            |
| 1     | Reserved                            |
| 2     | Reserved                            |
| 3     | Reserved                            |
| 4     | Pin is a CSD sense pin              |
| 5     | Pin is a CSD shield pin             |
| 6     | Pin is connected to AMUXA           |
| 7     | Pin is connected to AMUXB           |
| 8     | Pin-specific Active function #0     |
| 9     | Pin-specific Active function #1     |
| 10    | Pin-specific Active function #2     |
| 11    | Reserved                            |
| 12    | Pin is an LCD common pin            |
| 13    | Pin is an LCD segment pin           |
| 14    | Pin-specific Deep-Sleep function #0 |
| 15    | Pin-specific Deep-Sleep function #1 |

The selection of peripheral functions for different GPIO pins is given in [Table 4](#).

**Table 4. Port Pin Connections<sup>[1]</sup>**

| Name | Analog   | Digital |             |                  |                           |                 |                  |
|------|----------|---------|-------------|------------------|---------------------------|-----------------|------------------|
|      |          | GPIO    | Active #0   | Active #1        | Active #2                 | Deep Sleep #0   | Deep Sleep #1    |
| P0.0 | —        | GPIO    | TCPWM0_P[3] | SCB1_UART_RX[1]  | —                         | SCB1_I2C_SDA[1] | SCB1_SPI_MOSI[1] |
| P0.1 | —        | GPIO    | TCPWM0_N[3] | SCB1_UART_TX[1]  | —                         | SCB1_I2C_SCL[1] | SCB1_SPI_MISO[1] |
| P0.2 | —        | GPIO    | TCPWM1_P[3] | SCB1_UART_RTS[1] | —                         | —               | SCB1_SPI_SS0[1]  |
| P0.3 | —        | GPIO    | TCPWM1_N[3] | SCB1_UART_CTS[1] | —                         | —               | SCB1_SPI_SCLK[1] |
| P0.4 | —        | GPIO    | TCPWM1_P[0] | SCB0_UART_RX[1]  | EXT_CLK[0]/<br>ECO_OUT[0] | SCB0_I2C_SDA[1] | SCB0_SPI_MOSI[1] |
| P0.5 | —        | GPIO    | TCPWM1_N[0] | SCB0_UART_TX[1]  | —                         | SCB0_I2C_SCL[1] | SCB0_SPI_MISO[1] |
| P0.6 | —        | GPIO    | TCPWM2_P[0] | SCB0_UART_RTS[1] | —                         | SWDIO[0]        | SCB0_SPI_SS0[1]  |
| P0.7 | —        | GPIO    | TCPWM2_N[0] | SCB0_UART_CTS[1] | —                         | SWDCLK[0]       | SCB0_SPI_SCLK[1] |
| P1.0 | —        | GPIO    | TCPWM0_P[1] | —                | —                         | —               | WCO_OUT[2]       |
| P1.1 | —        | GPIO    | TCPWM0_N[1] | —                | —                         | —               | SCB1_SPI_SS1     |
| P1.2 | —        | GPIO    | TCPWM1_P[1] | —                | —                         | —               | SCB1_SPI_SS2     |
| P1.3 | —        | GPIO    | TCPWM1_N[1] | —                | —                         | —               | SCB1_SPI_SS3     |
| P1.4 | —        | GPIO    | TCPWM2_P[1] | SCB0_UART_RX[0]  | —                         | SCB0_I2C_SDA[0] | SCB0_SPI_MOSI[1] |
| P1.5 | —        | GPIO    | TCPWM2_N[1] | SCB0_UART_TX[0]  | —                         | SCB0_I2C_SCL[0] | SCB0_SPI_MISO[1] |
| P1.6 | —        | GPIO    | TCPWM3_P[1] | SCB0_UART_RTS[0] | —                         | —               | SCB0_SPI_SS0[1]  |
| P1.7 | —        | GPIO    | TCPWM3_N[1] | SCB0_UART_CTS[0] | —                         | —               | SCB0_SPI_SCLK[1] |
| P2.0 | —        | GPIO    | —           | —                | —                         | —               | SCB0_SPI_SS1     |
| P2.1 | —        | GPIO    | —           | —                | —                         | —               | SCB0_SPI_SS2     |
| P2.2 | —        | GPIO    | —           | —                | —                         | WAKEUP          | SCB0_SPI_SS3     |
| P2.3 | —        | GPIO    | —           | —                | —                         | —               | WCO_OUT[1]       |
| P2.4 | —        | GPIO    | —           | —                | —                         | —               | —                |
| P2.5 | —        | GPIO    | —           | —                | —                         | —               | —                |
| P2.6 | —        | GPIO    | —           | —                | —                         | —               | —                |
| P2.7 | —        | GPIO    | —           | —                | EXT_CLK[1]/<br>ECO_OUT[1] | —               | —                |
| P3.0 | SARMUX_0 | GPIO    | TCPWM0_P[2] | SCB0_UART_RX[2]  | —                         | SCB0_I2C_SDA[2] | —                |
| P3.1 | SARMUX_1 | GPIO    | TCPWM0_N[2] | SCB0_UART_TX[2]  | —                         | SCB0_I2C_SCL[2] | —                |
| P3.2 | SARMUX_2 | GPIO    | TCPWM1_P[2] | SCB0_UART_RTS[2] | —                         | —               | —                |
| P3.3 | SARMUX_3 | GPIO    | TCPWM1_N[2] | SCB0_UART_CTS[2] | —                         | —               | —                |
| P3.4 | SARMUX_4 | GPIO    | TCPWM2_P[2] | SCB1_UART_RX[2]  | —                         | SCB1_I2C_SDA[2] | —                |
| P3.5 | SARMUX_5 | GPIO    | TCPWM2_N[2] | SCB1_UART_TX[2]  | —                         | SCB1_I2C_SCL[2] | —                |
| P3.6 | SARMUX_6 | GPIO    | TCPWM3_P[2] | SCB1_UART_RTS[2] | —                         | —               | —                |
| P3.7 | SARMUX_7 | GPIO    | TCPWM3_N[2] | SCB1_UART_CTS[2] | —                         | —               | WCO_OUT[0]       |
| P4.0 | CMOD     | GPIO    | TCPWM0_P[0] | SCB1_UART_RTS[0] | —                         | —               | SCB1_SPI_MOSI[0] |

**Note**

1. For devices with only 1 SCB, use pins corresponding to SCB1.

**Table 4. Port Pin Connections<sup>[1]</sup>** (continued)

| Name             | Analog | Digital |             |                  |                           |                 |                  |
|------------------|--------|---------|-------------|------------------|---------------------------|-----------------|------------------|
|                  |        | GPIO    | Active #0   | Active #1        | Active #2                 | Deep Sleep #0   | Deep Sleep #1    |
| P4.1             | CTANK  | GPIO    | TCPWM0_N[0] | SCB1_UART_CTS[0] | —                         | —               | SCB1_SPI_MISO[0] |
| P5.0             | —      | GPIO    | TCPWM3_P[0] | SCB1_UART_RX[0]  | EXTPA_EN                  | SCB1_I2C_SDA[0] | SCB1_SPI_SS0[0]  |
| P5.1             | —      | GPIO    | TCPWM3_N[0] | SCB1_UART_TX[0]  | EXT_CLK[2]/<br>ECO_OUT[2] | SCB1_I2C_SCL[0] | SCB1_SPI_SCLK[0] |
| P6.0_XTAL32<br>O | —      | GPIO    | —           | —                | —                         | —               | —                |
| P6.1_XTAL32I     | —      | GPIO    | —           | —                | —                         | —               | —                |

## Power

PRoC BLE can be supplied from batteries with a voltage range of 1.9 V to 5.5 V by directly connecting to the digital supply ( $V_{DD}$ ), analog supply ( $V_{DDA}$ ), and radio supply ( $V_{DDR}$ ) pins. The internal LDOs in the device regulate the supply voltage to required levels for different blocks. The device has one regulator for the digital circuitry and separate regulators for radio circuitry for noise isolation. The analog circuits run directly from the analog supply ( $V_{DDA}$ ) input. The device uses separate regulators for Deep Sleep and Hibernate modes to minimize the power consumption. The radio stops working below 1.9 V, but the rest of the system continues to function down to 1.71 V without RF.

Bypass capacitors must be used from  $VDDx$  ( $x = A, D, \text{ or } R$ ) to ground. The typical practice for systems in this frequency range is to use a capacitor in the 1- $\mu\text{F}$  range in parallel with a smaller capacitor (for example, 0.1  $\mu\text{F}$ ). Note that these are simply rules of thumb and that, for critical applications, the PCB layout, lead inductance, and the bypass capacitor parasitic should be simulated to design to obtain optimal bypassing.

| Power Supply         | Bypass Capacitors                                                                                |
|----------------------|--------------------------------------------------------------------------------------------------|
| $V_{DD}$             | 0.1- $\mu\text{F}$ ceramic at each pin plus bulk capacitor 1- $\mu\text{F}$ to 10- $\mu\text{F}$ |
| $V_{DDA}$            | 0.1- $\mu\text{F}$ ceramic at each pin plus bulk capacitor 1- $\mu\text{F}$ to 10- $\mu\text{F}$ |
| $V_{DDR}$            | 0.1- $\mu\text{F}$ ceramic at each pin plus bulk capacitor 1- $\mu\text{F}$ to 10- $\mu\text{F}$ |
| $V_{CCD}$            | 1.3- $\mu\text{F}$ ceramic capacitor at the VCCD pin                                             |
| $V_{REF}$ (optional) | The internal bandgap may be bypassed with a 1- $\mu\text{F}$ to 10- $\mu\text{F}$ capacitor      |

## Low-Power Modes

PRoC BLE supports five power modes. Refer to [Table 5](#) for more details on the system status. The PRoC BLE device consumes the lowest current in Stop mode; the device wakeup from stop mode is with a system reset through the XRES or WAKEUP pin. It can retain the SRAM data in Hibernate mode and is capable of retaining the complete system status in Deep-Sleep mode. [Table 5](#) shows the different power modes and the peripherals that are active.

**Table 5. Power Modes System Status**

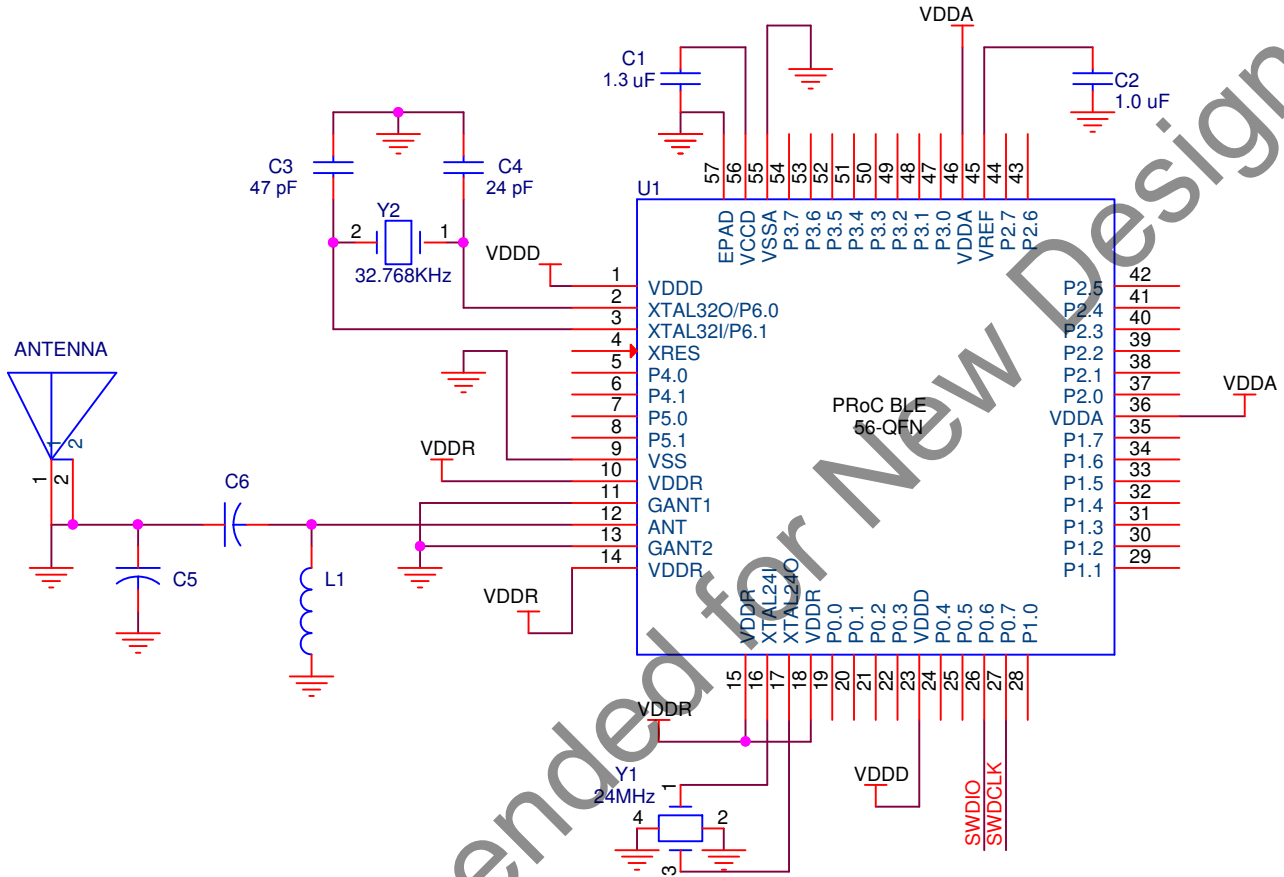
| Power Mode | Current Consumption                                          | Code Execution | Digital Peripherals Available              | Analog Peripherals Available | Clock Sources Available | Wake Up Sources                            | Wake-Up Time     |
|------------|--------------------------------------------------------------|----------------|--------------------------------------------|------------------------------|-------------------------|--------------------------------------------|------------------|
| Active     | 850 $\mu\text{A}$ + 260 $\mu\text{A}$ per MHz <sup>[2]</sup> | Yes            | All                                        | All                          | All                     | —                                          | —                |
| Sleep      | 1.1 mA at 3 MHz                                              | No             | All                                        | All                          | All                     | Any interrupt source                       | 0                |
| Deep Sleep | 1.5 $\mu\text{A}$                                            | No             | WDT, LCD, I <sup>2</sup> C/SPI, Link-Layer | POR, BOD                     | WCO, ILO                | GPIO, WDT, I <sup>2</sup> C/SPI Link Layer | 25 $\mu\text{s}$ |
| Hibernate  | 150 nA                                                       | No             | No                                         | POR, BOD                     | No                      | GPIO                                       | 0.7 ms           |
| Stop       | 60 nA                                                        | No             | No                                         | No                           | No                      | Wake-Up pin, XRES                          | 2.2 ms           |

### Note

2. For CPU subsystem.

A typical system application connection diagram for the 56-QFN package is shown in [Figure 5](#).

**Figure 5. PRoC BLE Applications Diagram**



## Development Support

The CYBL1XX7X family has a rich set of documentation, development tools, and online resources to assist you during your development process. Visit [www.cypress.com/procble](http://www.cypress.com/procble) to find out more.

### Documentation

A suite of documentation supports the CYBL1XX7X family to ensure that you find answers to your questions quickly. This section contains a list of some of the key documents.

**Component Datasheets:** PSoC Creator Components provide hardware abstraction using APIs to configure and control peripheral activity. The Component datasheet covers Component features, its usage and operation details, API description, and electrical specifications. This is the primary documentation used during development. These Components can represent peripherals on the device (such as a timer, I<sup>2</sup>C, or UART) or high-level system functions (such as the [BLE Component](#)).

**Application Notes:** Application notes help you to understand how to use various device features. They also provide guidance on how to solve a variety of system design challenges.

**Technical Reference Manual (TRM):** The TRM describes all peripheral functionality in detail, with register-level descriptions. This document is divided into two parts: the Architecture TRM and the Register TRM.

### Online

In addition to the print documentation, Cypress forums connect you with fellow users and experts from around the world, 24 hours a day, 7 days a week.

### Tools

With industry-standard cores, programming, and debugging interfaces, the CYBL1XX7X family is part of a development tool ecosystem.

Visit us at [www.cypress.com/go/psoccreator](http://www.cypress.com/go/psoccreator) for the latest information on the revolutionary, easy-to-use PSoC Creator IDE, supported third-party compilers, programmers, and debuggers.

### Kits

Cypress provides a portfolio of kits to accelerate time-to-market. Visit us at [www.cypress.com/procble](http://www.cypress.com/procble).

## Electrical Specifications

This section provides detailed electrical characteristics. Absolute maximum rating for the CYBL1XX7X devices is listed in [Table 6](#) through [Table 50](#). Usage above the absolute maximum conditions may cause permanent damage to the device.

Exposure to absolute maximum conditions for extended periods of time may affect device reliability.

The maximum storage temperature is 150 °C in compliance with JEDEC Standard JESD22-A103, High Temperature Storage Life. When used below absolute maximum conditions, but above normal operating conditions, the device may not operate to the specification.

## Absolute Maximum Ratings

**Table 6. Absolute Maximum Ratings**

| Spec ID# | Parameter                   | Description                                                                                                        | Min                 | Typ | Max                   | Units | Details/Conditions                     |
|----------|-----------------------------|--------------------------------------------------------------------------------------------------------------------|---------------------|-----|-----------------------|-------|----------------------------------------|
| SID1     | V <sub>DDD_ABS</sub>        | Analog, digital, or radio supply relative to V <sub>SS</sub> (V <sub>SSD</sub> = V <sub>SSA</sub> )                | −0.5                | −   | 6                     | V     | Absolute max                           |
| SID2     | V <sub>CCD_ABS</sub>        | Direct digital core voltage input relative to V <sub>SSD</sub>                                                     | −0.5                | −   | 1.95                  | V     | Absolute max                           |
| SID3     | V <sub>GPIO_ABS</sub>       | GPIO voltage                                                                                                       | −0.5                | −   | V <sub>DD</sub> + 0.5 | V     | Absolute max                           |
| SID4     | I <sub>GPIO_ABS</sub>       | Maximum current per GPIO                                                                                           | −25                 | −   | 25                    | mA    | Absolute max                           |
| SID5     | I <sub>GPIO_injection</sub> | GPIO injection current, Max for V <sub>IH</sub> > V <sub>DDD</sub> , and Min for V <sub>IL</sub> < V <sub>SS</sub> | −0.5                | −   | 0.5                   | mA    | Absolute max, current injected per pin |
| BID57    | ESD_HBM                     | Electrostatic discharge human body model                                                                           | 2200 <sup>[3]</sup> | −   | −                     | V     | −                                      |
| BID58    | ESD_CDM                     | Electrostatic discharge charged device model                                                                       | 500                 | −   | −                     | V     | −                                      |
| BID61    | LU                          | Pin current for latch up                                                                                           | −200                | −   | 200                   | mA    | −                                      |

## BLE Subsystem

**Table 7. BLE Subsystem**

| Spec ID#                          | Parameter     | Description                                                                         | Min | Typ | Max | Units | Details/Conditions                    |
|-----------------------------------|---------------|-------------------------------------------------------------------------------------|-----|-----|-----|-------|---------------------------------------|
| <b>RF Receiver Specifications</b> |               |                                                                                     |     |     |     |       |                                       |
| SID340                            | RXS, IDLE     | RX sensitivity with idle transmitter                                                | −   | −89 | −   | dBm   | −                                     |
| SID340A                           |               | RX sensitivity with idle transmitter excluding Balun loss                           | −   | −91 | −   | dBm   | Guaranteed by design simulation       |
| SID341                            | RXS, DIRTY    | RX sensitivity with dirty transmitter                                               | −   | −87 | −70 | dBm   | RF-PHY Specification (RCV-LE/CA/01/C) |
| SID342                            | RXS, HIGHGAIN | RX sensitivity in high-gain mode with idle transmitter                              | −   | −91 | −   | dBm   | −                                     |
| SID343                            | PRXMAX        | Maximum input power                                                                 | −10 | −1  | −   | dBm   | RF-PHY Specification (RCV-LE/CA/06/C) |
| SID344                            | CI1           | Co-channel interference, Wanted signal at −67 dBm and Interferer at F <sub>RX</sub> | −   | 9   | 21  | dB    | RF-PHY Specification (RCV-LE/CA/03/C) |

### Note

3. This does not apply to the RF pins (ANT, XTALI, and XTALO). RF pins (ANT, XTALI, and XTALO) are tested for 500-V HBM.

**Table 7. BLE Subsystem (continued)**

| Spec ID#                             | Parameter  | Description                                                                                                                | Min | Typ     | Max | Units | Details/<br>Conditions                                          |
|--------------------------------------|------------|----------------------------------------------------------------------------------------------------------------------------|-----|---------|-----|-------|-----------------------------------------------------------------|
| SID345                               | CI2        | Adjacent channel interference<br>Wanted signal at -67 dBm and<br>Interferer at $F_{RX} \pm 1$ MHz                          | -   | 3       | 15  | dB    | RF-PHY Specification<br>(RCV-LE/CA/03/C)                        |
| SID346                               | CI3        | Adjacent channel interference<br>Wanted signal at -67 dBm and<br>Interferer at $F_{RX} \pm 2$ MHz                          | -   | -29     | -   | dB    | RF-PHY Specification<br>(RCV-LE/CA/03/C)                        |
| SID347                               | CI4        | Adjacent channel interference<br>Wanted signal at -67 dBm and<br>Interferer at $\geq F_{RX} \pm 3$ MHz                     | -   | -39     | -   | dB    | RF-PHY Specification<br>(RCV-LE/CA/03/C)                        |
| SID348                               | CI5        | Adjacent channel interference<br>Wanted signal at -67 dBm and<br>Interferer at Image frequency<br>( $F_{IMAGE}$ )          | -   | -20     | -   | dB    | RF-PHY Specification<br>(RCV-LE/CA/03/C)                        |
| SID349                               | CI6        | Adjacent channel interference<br>Wanted signal at -67 dBm and<br>Interferer at Image frequency<br>( $F_{IMAGE} \pm 1$ MHz) | -   | -30     | -   | dB    | RF-PHY Specification<br>(RCV-LE/CA/03/C)                        |
| SID350                               | OBB1       | Out-of-band blocking,<br>Wanted signal at -67 dBm and<br>Interferer at $F = 30$ –2000 MHz                                  | -30 | -27     | -   | dBm   | RF-PHY Specification<br>(RCV-LE/CA/04/C)                        |
| SID351                               | OBB2       | Out-of-band blocking,<br>Wanted signal at -67 dBm and<br>Interferer at $F = 2,003$ –2,399 MHz                              | -35 | -27     | -   | dBm   | RF-PHY Specification<br>(RCV-LE/CA/04/C)                        |
| SID352                               | OBB3       | Out-of-band blocking,<br>Wanted signal at -67 dBm and<br>Interferer at $F = 2,484$ –2,997 MHz                              | -35 | -27     | -   | dBm   | RF-PHY Specification<br>(RCV-LE/CA/04/C)                        |
| SID353                               | OBB4       | Out-of-band blocking,<br>Wanted signal at -67 dBm and Inter-<br>ferer at $F = 3,000$ –12,750 MHz                           | -30 | -27     | -   | dBm   | RF-PHY Specification<br>(RCV-LE/CA/04/C)                        |
| SID354                               | IMD        | Intermodulation performance<br>Wanted signal at -64 dBm and<br>1-Mbps BLE, third, fourth, and fifth<br>offset channel      | -50 | -       | -   | dBm   | RF-PHY Specification<br>(RCV-LE/CA/05/C)                        |
| SID355                               | RXSE1      | Receiver spurious emission<br>30 MHz to 1.0 GHz                                                                            | -   | -       | -57 | dBm   | 100-kHz<br>measurement<br>bandwidth<br>ETSI EN300 328<br>V1.8.1 |
| SID356                               | RXSE2      | Receiver spurious emission<br>1.0 GHz to 12.75 GHz                                                                         | -   | -       | -47 | dBm   | 1-MHz measurement<br>bandwidth<br>ETSI EN300 328<br>V1.8.1      |
| <b>RF Transmitter Specifications</b> |            |                                                                                                                            |     |         |     |       |                                                                 |
| SID357                               | TXP, ACC   | RF power accuracy                                                                                                          | -   | $\pm 1$ | -   | dB    | -                                                               |
| SID358                               | TXP, RANGE | RF power control range                                                                                                     | -   | 20      | -   | dB    | -                                                               |
| SID359                               | TXP, 0 dBm | Output power, 0-dB gain setting<br>(PA7)                                                                                   | -   | 0       | -   | dBm   | -                                                               |

**Table 7. BLE Subsystem** (continued)

| Spec ID#                        | Parameter        | Description                                         | Min  | Typ  | Max   | Units              | Details/<br>Conditions                                    |
|---------------------------------|------------------|-----------------------------------------------------|------|------|-------|--------------------|-----------------------------------------------------------|
| SID360                          | TXP, MAX         | Output power, maximum power setting (PA10)          | –    | 3    | –     | dBm                | –                                                         |
| SID361                          | TXP, MIN         | Output power, minimum power setting (PA1)           | –    | –18  | –     | dBm                | –                                                         |
| SID362                          | F2AVG            | Average frequency deviation for 10101010 pattern    | 185  | –    | –     | kHz                | RF-PHY Specification (TRM-LE/CA/05/C)                     |
| SID363                          | F1AVG            | Average frequency deviation for 11110000 pattern    | 225  | 250  | 275   | kHz                | RF-PHY Specification (TRM-LE/CA/05/C)                     |
| SID364                          | EO               | Eye opening = $\Delta F2AVG/\Delta F1AVG$           | 0.8  | –    | –     | –                  | RF-PHY Specification (TRM-LE/CA/05/C)                     |
| SID365                          | FTX, ACC         | Frequency accuracy                                  | –150 | –    | 150   | kHz                | RF-PHY Specification (TRM-LE/CA/06/C)                     |
| SID366                          | FTX, MAXDR       | Maximum frequency drift                             | –50  | –    | 50    | kHz                | RF-PHY Specification (TRM-LE/CA/06/C)                     |
| SID367                          | FTX, INITDR      | Initial frequency drift                             | –20  | –    | 20    | kHz                | RF-PHY Specification (TRM-LE/CA/06/C)                     |
| SID368                          | FTX, DR          | Maximum drift rate                                  | –20  | –    | 20    | kHz/<br>50 $\mu$ s | RF-PHY Specification (TRM-LE/CA/06/C)                     |
| SID369                          | IBSE1            | In-band spurious emission at 2-MHz offset           | –    | –    | –20   | dBm                | RF-PHY Specification (TRM-LE/CA/03/C)                     |
| SID370                          | IBSE2            | In-band spurious emission at $\geq 3$ -MHz offset   | –    | –    | –30   | dBm                | RF-PHY Specification (TRM-LE/CA/03/C)                     |
| SID371                          | TXSE1            | Transmitter spurious emissions (average), <1.0 GHz  | –    | –    | –55.5 | dBm                | FCC-15.247                                                |
| SID372                          | TXSE2            | Transmitter spurious emissions (average), >1.0 GHz  | –    | –    | –41.5 | dBm                | FCC-15.247                                                |
| <b>RF Current Specification</b> |                  |                                                     |      |      |       |                    |                                                           |
| SID373                          | IRX              | Receive current in normal mode                      | –    | 18.7 | –     | mA                 | –                                                         |
| SID373A                         | IRX_RF           | Receive current in normal mode                      | –    | 16.4 | –     | mA                 | Measured at V <sub>DDR</sub>                              |
| SID374                          | IRX, HIGHGAIN    | Receive current in high-gain mode                   | –    | 21.5 | –     | mA                 | –                                                         |
| SID375                          | ITX, 3 dBm       | TX current at 3-dBm setting (PA10)                  | –    | 20   | –     | mA                 | –                                                         |
| SID376                          | ITX, 0 dBm       | TX current at 0-dBm setting (PA7)                   | –    | 16.5 | –     | mA                 | –                                                         |
| SID376A                         | ITX_RF, 0 dBm    | TX current at 0-dBm setting (PA7)                   | –    | 15.6 | –     | mA                 | Measured at V <sub>DDR</sub>                              |
| SID376B                         | ITX_RF, 0 dBm    | TX current at 0 dBm excluding Balun loss            | –    | 14.2 | –     | mA                 | Guaranteed by design simulation                           |
| SID377                          | ITX, -3 dBm      | TX current at –3-dBm setting (PA4)                  | –    | 15.5 | –     | mA                 | –                                                         |
| SID378                          | ITX, -6 dBm      | TX current at –6-dBm setting (PA3)                  | –    | 14.5 | –     | mA                 | –                                                         |
| SID379                          | ITX, -12 dBm     | TX current at –12-dBm setting (PA2)                 | –    | 13.2 | –     | mA                 | –                                                         |
| SID380                          | ITX, -18 dBm     | TX current at –18-dBm setting (PA1)                 | –    | 12.5 | –     | mA                 | –                                                         |
| SID380A                         | Iavg_1sec, 0 dBm | Average current at 1-second BLE connection interval | –    | 17.1 | –     | $\mu$ A            | TXP: 0 dBm; $\pm 20$ -ppm master and slave clock accuracy |

**Table 7. BLE Subsystem (continued)**

| Spec ID#                        | Parameter           | Description                                         | Min  | Typ  | Max  | Units | Details/<br>Conditions                              |
|---------------------------------|---------------------|-----------------------------------------------------|------|------|------|-------|-----------------------------------------------------|
| SID380B                         | Iavg_4sec,<br>0 dBm | Average current at 4-second BLE connection interval | –    | 6.1  | –    | μA    | TXP: 0 dBm; ±20-ppm master and slave clock accuracy |
| <b>General RF Specification</b> |                     |                                                     |      |      |      |       |                                                     |
| SID381                          | FREQ                | RF operating frequency                              | 2400 | –    | 2482 | MHz   | –                                                   |
| SID382                          | CHBW                | Channel spacing                                     | –    | 2    | –    | MHz   | –                                                   |
| SID383                          | DR                  | On-air data rate                                    | –    | 1000 | –    | kbps  | –                                                   |
| SID384                          | IDLE2TX             | BLE Radio Idle to BLE Radio TX transition time      | –    | 120  | 140  | μs    | –                                                   |
| SID385                          | IDLE2RX             | BLE Radio Idle to BLE Radio RX transition time      | –    | 75   | 120  | μs    | –                                                   |
| <b>RSSI Specification</b>       |                     |                                                     |      |      |      |       |                                                     |
| SID386                          | RSSI, ACC           | RSSI accuracy                                       | –    | ±5   | –    | dB    | –                                                   |
| SID387                          | RSSI, RES           | RSSI resolution                                     | –    | 1    | –    | dB    | –                                                   |
| SID388                          | RSSI, PER           | RSSI sample period                                  | –    | 6    | –    | μs    | –                                                   |

**Device-Level Specifications**

All specifications are valid for  $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$  and  $T_J \leq 100\text{ }^{\circ}\text{C}$ , except where noted. Specifications are valid for 1.71-V to 5.5-V, except where noted.

**Table 8. DC Specifications**

| Spec ID#                                             | Parameter         | Description                                                                                     | Min  | Typ | Max  | Units | Details/<br>Conditions             |
|------------------------------------------------------|-------------------|-------------------------------------------------------------------------------------------------|------|-----|------|-------|------------------------------------|
| SID6                                                 | V <sub>DD</sub>   | Power supply input voltage (V <sub>DDA</sub> = V <sub>DDD</sub> = V <sub>DD</sub> )             | 1.8  | –   | 5.5  | V     | With regulator enabled             |
| SID7                                                 | V <sub>DD</sub>   | Power supply input voltage unregulated (V <sub>DDA</sub> = V <sub>DDD</sub> = V <sub>DD</sub> ) | 1.71 | 1.8 | 1.89 | V     | Internally unregulated supply      |
| SID8                                                 | V <sub>DDR</sub>  | Radio supply voltage (Radio on)                                                                 | 1.9  | –   | 5.5  | V     | –                                  |
| SID8A                                                | V <sub>DDR</sub>  | Radio supply voltage (Radio off)                                                                | 1.71 | –   | 5.5  | V     | –                                  |
| SID9                                                 | V <sub>CCD</sub>  | Digital regulator output voltage (for core logic)                                               | –    | 1.8 | –    | V     | –                                  |
| SID10                                                | C <sub>VCCD</sub> | Digital regulator output bypass capacitor                                                       | 1    | 1.3 | 1.6  | μF    | X5R ceramic or better              |
| <b>Active Mode, V<sub>DD</sub> = 1.71 V to 5.5 V</b> |                   |                                                                                                 |      |     |      |       |                                    |
| SID13                                                | I <sub>DD3</sub>  | Execute from flash; CPU at 3 MHz                                                                | –    | 2.1 | –    | mA    | T = 25 °C, V <sub>DD</sub> = 3.3 V |
| SID14                                                | I <sub>DD4</sub>  | Execute from flash; CPU at 3 MHz                                                                | –    | –   | –    | mA    | T = –40 °C to 85 °C                |
| SID15                                                | I <sub>DD5</sub>  | Execute from flash; CPU at 6 MHz                                                                | –    | 2.5 | –    | mA    | T = 25 °C, V <sub>DD</sub> = 3.3 V |
| SID16                                                | I <sub>DD6</sub>  | Execute from flash; CPU at 6 MHz                                                                | –    | –   | –    | mA    | T = –40 °C to 85 °C                |
| SID17                                                | I <sub>DD7</sub>  | Execute from flash; CPU at 12 MHz                                                               | –    | 4   | –    | mA    | T = 25 °C, V <sub>DD</sub> = 3.3 V |
| SID18                                                | I <sub>DD8</sub>  | Execute from flash; CPU at 12 MHz                                                               | –    | –   | –    | mA    | T = –40 °C to 85 °C                |
| SID19                                                | I <sub>DD9</sub>  | Execute from flash; CPU at 24 MHz                                                               | –    | 7.1 | –    | mA    | T = 25 °C, V <sub>DD</sub> = 3.3 V |

**Table 8. DC Specifications** (continued)

| Spec ID#                                                                     | Parameter         | Description                           | Min | Typ  | Max | Units | Details/<br>Conditions                                    |
|------------------------------------------------------------------------------|-------------------|---------------------------------------|-----|------|-----|-------|-----------------------------------------------------------|
| SID20                                                                        | I <sub>DD10</sub> | Execute from flash; CPU at 24 MHz     | –   | –    | –   | mA    | T = –40 °C to 85 °C                                       |
| SID21                                                                        | I <sub>DD11</sub> | Execute from flash; CPU at 48 MHz     | –   | 13.4 | –   | mA    | T = 25 °C,<br>V <sub>DD</sub> = 3.3 V                     |
| SID22                                                                        | I <sub>DD12</sub> | Execute from flash; CPU at 48 MHz     | –   | –    | –   | mA    | T = –40 °C to 85 °C                                       |
| <b>Sleep Mode, V<sub>DD</sub> = 1.8 to 5.5 V</b>                             |                   |                                       |     |      |     |       |                                                           |
| SID23                                                                        | I <sub>DD13</sub> | IMO on                                | –   | –    | –   | mA    | T = 25 °C,<br>V <sub>DD</sub> = 3.3 V,<br>SYSCLK = 3 MHz  |
| <b>Sleep Mode, V<sub>DD</sub> and V<sub>DDR</sub> = 1.9 to 5.5 V</b>         |                   |                                       |     |      |     |       |                                                           |
| SID24                                                                        | I <sub>DD14</sub> | ECO on                                | –   | –    | –   | mA    | T = 25 °C,<br>V <sub>DD</sub> = 3.3 V, SYSCLK<br>= 3 MHz  |
| <b>Deep-Sleep Mode, V<sub>DD</sub> = 1.8 to 3.6 V</b>                        |                   |                                       |     |      |     |       |                                                           |
| SID25                                                                        | I <sub>DD15</sub> | WDT with WCO on                       | –   | 1.5  | –   | μA    | T = 25 °C,<br>V <sub>DD</sub> = 3.3 V                     |
| SID26                                                                        | I <sub>DD16</sub> | WDT with WCO on                       | –   | –    | –   | μA    | T = –40 °C to 85 °C                                       |
| <b>Deep-Sleep Mode, V<sub>DD</sub> = 3.6 to 5.5 V</b>                        |                   |                                       |     |      |     |       |                                                           |
| SID27                                                                        | I <sub>DD17</sub> | WDT with WCO on                       | –   | –    | –   | μA    | T = 25 °C,<br>V <sub>DD</sub> = 5 V                       |
| SID28                                                                        | I <sub>DD18</sub> | WDT with WCO on                       | –   | –    | –   | μA    | T = –40 °C to 85 °C                                       |
| <b>Deep-Sleep Mode, V<sub>DD</sub> = 1.71 to 1.89 V (Regulator Bypassed)</b> |                   |                                       |     |      |     |       |                                                           |
| SID29                                                                        | I <sub>DD19</sub> | WDT with WCO on                       | –   | –    | –   | μA    | T = 25 °C                                                 |
| SID30                                                                        | I <sub>DD20</sub> | WDT with WCO on                       | –   | –    | –   | μA    | T = –40 °C to 85 °C                                       |
| <b>Hibernate Mode, V<sub>DD</sub> = 1.8 to 3.6 V</b>                         |                   |                                       |     |      |     |       |                                                           |
| SID37                                                                        | I <sub>DD27</sub> | GPIO and reset active                 | –   | 150  | –   | nA    | T = 25 °C,<br>V <sub>DD</sub> = 3.3 V                     |
| SID38                                                                        | I <sub>DD28</sub> | GPIO and reset active                 | –   | –    | –   | nA    | T = –40 °C to 85 °C                                       |
| <b>Hibernate Mode, V<sub>DD</sub> = 3.6 to 5.5 V</b>                         |                   |                                       |     |      |     |       |                                                           |
| SID39                                                                        | I <sub>DD29</sub> | GPIO and reset active                 | –   | –    | –   | nA    | T = 25 °C,<br>V <sub>DD</sub> = 5 V                       |
| SID40                                                                        | I <sub>DD30</sub> | GPIO and reset active                 | –   | –    | –   | nA    | T = –40 °C to 85 °C                                       |
| <b>Hibernate Mode, V<sub>DD</sub> = 1.71 to 1.89 V (Regulator Bypassed)</b>  |                   |                                       |     |      |     |       |                                                           |
| SID41                                                                        | I <sub>DD31</sub> | GPIO and reset active                 | –   | –    | –   | nA    | T = 25 °C                                                 |
| SID42                                                                        | I <sub>DD32</sub> | GPIO and reset active                 | –   | –    | –   | nA    | T = –40 °C to 85 °C                                       |
| <b>Stop Mode, V<sub>DD</sub> = 1.8 to 3.6 V</b>                              |                   |                                       |     |      |     |       |                                                           |
| SID43                                                                        | I <sub>DD33</sub> | Stop-mode current (V <sub>DD</sub> )  | –   | 20   | –   | nA    | T = 25 °C,<br>V <sub>DD</sub> = 3.3 V                     |
| SID44                                                                        | I <sub>DD34</sub> | Stop-mode current (V <sub>DDR</sub> ) | –   | 40   | –   | nA    | T = 25 °C,<br>V <sub>DDR</sub> = 3.3 V                    |
| SID45                                                                        | I <sub>DD35</sub> | Stop-mode current (V <sub>DD</sub> )  | –   | –    | –   | nA    | T = –40 °C to 85 °C                                       |
| SID46                                                                        | I <sub>DD36</sub> | Stop-mode current (V <sub>DDR</sub> ) | –   | –    | –   | nA    | T = –40 °C to 85 °C,<br>V <sub>DDR</sub> = 1.9 V to 3.6 V |
| <b>Stop Mode, V<sub>DD</sub> = 3.6 to 5.5 V</b>                              |                   |                                       |     |      |     |       |                                                           |
| SID47                                                                        | I <sub>DD37</sub> | Stop-mode current (V <sub>DD</sub> )  | –   | –    | –   | nA    | T = 25 °C,<br>V <sub>DD</sub> = 5 V                       |

**Table 8. DC Specifications (continued)**

| Spec ID#                                                               | Parameter         | Description                           | Min | Typ | Max | Units | Details/<br>Conditions               |
|------------------------------------------------------------------------|-------------------|---------------------------------------|-----|-----|-----|-------|--------------------------------------|
| SID48                                                                  | I <sub>DD38</sub> | Stop-mode current (V <sub>DDR</sub> ) | –   | –   | –   | nA    | T = 25 °C,<br>V <sub>DDR</sub> = 5 V |
| SID49                                                                  | I <sub>DD39</sub> | Stop-mode current (V <sub>DD</sub> )  | –   | –   | –   | nA    | T = –40 °C to 85 °C                  |
| SID50                                                                  | I <sub>DD40</sub> | Stop-mode current (V <sub>DDR</sub> ) | –   | –   | –   | nA    | T = –40 °C to 85 °C                  |
| <b>Stop Mode, V<sub>DD</sub> = 1.71 to 1.89 V (Regulator Bypassed)</b> |                   |                                       |     |     |     |       |                                      |
| SID51                                                                  | I <sub>DD41</sub> | Stop-mode current (V <sub>DD</sub> )  | –   | –   | –   | nA    | T = 25 °C                            |
| SID52                                                                  | I <sub>DD42</sub> | Stop-mode current (V <sub>DD</sub> )  | –   | –   | –   | nA    | T = –40 °C to 85 °C                  |

**Table 9. AC Specifications**

| Spec ID# | Parameter              | Description                 | Min | Typ | Max | Units | Details/<br>Conditions                           |
|----------|------------------------|-----------------------------|-----|-----|-----|-------|--------------------------------------------------|
| SID53    | F <sub>CPU</sub>       | CPU frequency               | DC  | –   | 48  | MHz   | 1.71 V ≤ V <sub>DD</sub> ≤ 5.5 V                 |
| SID54    | T <sub>SLEEP</sub>     | Wakeup from Sleep mode      | –   | 0   | –   | μs    | Guaranteed by<br>characterization                |
| SID55    | T <sub>DEEPSLEEP</sub> | Wakeup from Deep-Sleep mode | –   | –   | 25  | μs    | 24-MHz IMO.<br>Guaranteed by<br>characterization |
| SID56    | T <sub>HIBERNATE</sub> | Wakeup from Hibernate mode  | –   | –   | 0.7 | ms    | Guaranteed by<br>characterization                |
| SID57    | T <sub>STOP</sub>      | Wakeup from Stop mode       | –   | –   | 2.2 | ms    | Guaranteed by<br>characterization                |

#### GPIO

**Table 10. GPIO DC Specifications**

| Spec ID# | Parameter             | Description                          | Min                   | Typ | Max                   | Units | Details/<br>Conditions                             |
|----------|-----------------------|--------------------------------------|-----------------------|-----|-----------------------|-------|----------------------------------------------------|
| SID58    | V <sub>IH</sub>       | Input voltage HIGH threshold         | 0.7 × V <sub>DD</sub> | –   | –                     | V     | CMOS input                                         |
| SID59    | V <sub>IL</sub>       | Input voltage LOW threshold          | –                     | –   | 0.3 × V <sub>DD</sub> | V     | CMOS input                                         |
| SID60    | V <sub>IH</sub>       | LVTTL input, V <sub>DD</sub> < 2.7 V | 0.7 × V <sub>DD</sub> | –   | –                     | V     | –                                                  |
| SID61    | V <sub>IL</sub>       | LVTTL input, V <sub>DD</sub> < 2.7 V | –                     | –   | 0.3 × V <sub>DD</sub> | V     | –                                                  |
| SID62    | V <sub>IH</sub>       | LVTTL input, V <sub>DD</sub> ≥ 2.7 V | 2.0                   | –   | –                     | V     | –                                                  |
| SID63    | V <sub>IL</sub>       | LVTTL input, V <sub>DD</sub> ≥ 2.7 V | –                     | –   | 0.8                   | V     | –                                                  |
| SID64    | V <sub>OH</sub>       | Output voltage HIGH level            | V <sub>DD</sub> – 0.6 | –   | –                     | V     | I <sub>OH</sub> = 4-mA at 3.3-V<br>V <sub>DD</sub> |
| SID65    | V <sub>OH</sub>       | Output voltage HIGH level            | V <sub>DD</sub> – 0.5 | –   | –                     | V     | I <sub>OH</sub> = 1-mA at 1.8-V<br>V <sub>DD</sub> |
| SID66    | V <sub>OL</sub>       | Output voltage LOW level             | –                     | –   | 0.6                   | V     | I <sub>OL</sub> = 8-mA at 3.3-V<br>V <sub>DD</sub> |
| SID67    | V <sub>OL</sub>       | Output voltage LOW level             | –                     | –   | 0.6                   | V     | I <sub>OL</sub> = 4-mA at 1.8-V<br>V <sub>DD</sub> |
| SID68    | V <sub>OL</sub>       | Output voltage LOW level             | –                     | –   | 0.4                   | V     | I <sub>OL</sub> = 3-mA at 3.3-V<br>V <sub>DD</sub> |
| SID69    | R <sub>PULLUP</sub>   | Pull-up resistor                     | 3.5                   | 5.6 | 8.5                   | kΩ    | –                                                  |
| SID70    | R <sub>PULLDOWN</sub> | Pull-down resistor                   | 3.5                   | 5.6 | 8.5                   | kΩ    | –                                                  |

**Note**

4. V<sub>IH</sub> must not exceed V<sub>DD</sub> + 0.2 V.

**Table 10. GPIO DC Specifications** (continued)

| Spec ID# | Parameter       | Description                                         | Min                  | Typ | Max | Units | Details/<br>Conditions            |
|----------|-----------------|-----------------------------------------------------|----------------------|-----|-----|-------|-----------------------------------|
| SID71    | $I_{IL}$        | Input leakage current (absolute value)              | –                    | –   | 2   | nA    | 25 °C,<br>$V_{DD} = 3.3\text{ V}$ |
| SID72    | $I_{IL\_CTBM}$  | Input leakage on CTBm input pins                    | –                    | –   | 4   | nA    |                                   |
| SID73    | $C_{IN}$        | Input capacitance                                   | –                    | –   | 7   | pF    | –                                 |
| SID74    | $V_{HYSTTL}$    | Input hysteresis LVTTL                              | 25                   | 40  |     | mV    | $V_{DD} > 2.7\text{ V}$           |
| SID75    | $V_{HYSCMOS}$   | Input hysteresis CMOS                               | $0.05 \times V_{DD}$ | –   | –   | mV    | –                                 |
| SID76    | $I_{DIODE}$     | Current through protection diode to $V_{DD}/V_{SS}$ | –                    | –   | 100 | μA    | –                                 |
| SID77    | $I_{TOT\_GPIO}$ | Maximum total source or sink chip current           | –                    | –   | 200 | mA    | –                                 |

**Table 11. GPIO AC Specifications**

| Spec ID# | Parameter     | Description                                                                      | Min | Typ | Max  | Units | Details/<br>Conditions                        |
|----------|---------------|----------------------------------------------------------------------------------|-----|-----|------|-------|-----------------------------------------------|
| SID78    | $T_{RISEF}$   | Rise time in Fast-Strong mode                                                    | 2   | –   | 12   | ns    | 3.3-V $V_{DD}$ ,<br>$C_{LOAD} = 25\text{-pF}$ |
| SID79    | $T_{FALLF}$   | Fall time in Fast-Strong mode                                                    | 2   | –   | 12   | ns    | 3.3-V $V_{DD}$ ,<br>$C_{LOAD} = 25\text{-pF}$ |
| SID80    | $T_{RISES}$   | Rise time in Slow-Strong mode                                                    | 10  | –   | 60   | ns    | 3.3-V $V_{DD}$ ,<br>$C_{LOAD} = 25\text{-pF}$ |
| SID81    | $T_{FALLS}$   | Fall time in Slow-Strong mode                                                    | 10  | –   | 60   | ns    | 3.3-V $V_{DD}$ ,<br>$C_{LOAD} = 25\text{-pF}$ |
| SID82    | $F_{GPIOUT1}$ | GPIO Fout; $3.3\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ .<br>Fast-Strong mode    | –   | –   | 33   | MHz   | 90/10%, 25-pF load,<br>60/40 duty cycle       |
| SID83    | $F_{GPIOUT2}$ | GPIO Fout; $1.7\text{ V} \leq V_{DD} \leq 3.3\text{ V}$ .<br>Fast-Strong mode    | –   | –   | 16.7 | MHz   | 90/10%, 25-pF load,<br>60/40 duty cycle       |
| SID84    | $F_{GPIOUT3}$ | GPIO Fout; $3.3\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ .<br>Slow-Strong mode    | –   | –   | 7    | MHz   | 90/10%, 25-pF load,<br>60/40 duty cycle       |
| SID85    | $F_{GPIOUT4}$ | GPIO Fout; $1.7\text{ V} \leq V_{DD} \leq 3.3\text{ V}$ .<br>Slow-Strong mode    | –   | –   | 3.5  | MHz   | 90/10%, 25-pF load,<br>60/40 duty cycle       |
| SID86    | $F_{GPIOIN}$  | GPIO input operating frequency.<br>$1.71\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | –   | –   | 48   | MHz   | 90/10% $V_{IO}$                               |

**Table 12. OVT GPIO DC Specifications (P5\_0 and P5\_1 Only)**

| Spec ID# | Parameter        | Description                                                          | Min | Typ | Max | Units   | Details/<br>Conditions                             |
|----------|------------------|----------------------------------------------------------------------|-----|-----|-----|---------|----------------------------------------------------|
| SID71A   | $I_{IL}$         | Input leakage (absolute value).<br>$V_{IH} > V_{DD}$                 | –   | –   | 10  | $\mu A$ | 25°C, $V_{DD} = 0 V$ ,<br>$V_{IH} = 3.0 V$         |
| SID66A   | $V_{OL}$         | Output voltage LOW level                                             | –   | –   | 0.4 | V       | $I_{OL} = 20\text{-mA}$ ,<br>$V_{DD} > 2.9 V$      |
| SID78A   | $T_{RISE\_OVFS}$ | Output rise time in Fast-Strong mode                                 | 1.5 | –   | 12  | ns      | 25-pF load,<br>10%–90%,<br>$V_{DD} = 3.3\text{-V}$ |
| SID79A   | $T_{FALL\_OVFS}$ | Output fall time in Fast-Strong mode                                 | 1.5 | –   | 12  | ns      | 25-pF load,<br>10%–90%,<br>$V_{DD} = 3.3\text{-V}$ |
| SID80A   | $T_{RISESS}$     | Output rise time in Slow-Strong mode                                 | 10  | –   | 60  | ns      | 25-pF load,<br>10%–90%,<br>$V_{DD} = 3.3\text{-V}$ |
| SID81A   | $T_{FALLSS}$     | Output fall time in Slow-Strong mode                                 | 10  | –   | 60  | ns      | 25-pF load,<br>10%–90%,<br>$V_{DD} = 3.3\text{-V}$ |
| SID82A   | $F_{GPIOUT1}$    | GPIO $F_{OUT}$ ; $3.3 V \leq V_{DD} \leq 5.5 V$<br>Fast-Strong mode  | –   | –   | 24  | MHz     | 90/10%, 25-pF load,<br>60/40 duty cycle            |
| SID83A   | $F_{GPIOUT2}$    | GPIO $F_{OUT}$ ; $1.71 V \leq V_{DD} \leq 3.3 V$<br>Fast-Strong mode | –   | –   | 16  | MHz     | 90/10%, 25-pF load,<br>60/40 duty cycle            |

**XRES**
**Table 13. XRES DC Specifications**

| Spec ID# | Parameter     | Description                                            | Min                  | Typ | Max                  | Units      | Details/<br>Conditions |
|----------|---------------|--------------------------------------------------------|----------------------|-----|----------------------|------------|------------------------|
| SID87    | $V_{IH}$      | Input voltage HIGH threshold                           | $0.7 \times V_{DDD}$ | –   | –                    | V          | CMOS input             |
| SID88    | $V_{IL}$      | Input voltage LOW threshold                            | –                    | –   | $0.3 \times V_{DDD}$ | V          | CMOS input             |
| SID89    | $R_{PULLUP}$  | Pull-up resistor                                       | 3.5                  | 5.6 | 8.5                  | k $\Omega$ | –                      |
| SID90    | $C_{IN}$      | Input capacitance                                      | –                    | 3   | –                    | pF         | –                      |
| SID91    | $V_{HYSXRES}$ | Input voltage hysteresis                               | –                    | 100 | –                    | mV         | –                      |
| SID92    | $I_{DIODE}$   | Current through protection diode to<br>$V_{DD}/V_{SS}$ | –                    | –   | 100                  | $\mu A$    | –                      |

**Table 14. XRES AC Specifications**

| Spec ID# | Parameter        | Description       | Min | Typ | Max | Units   | Details/<br>Conditions |
|----------|------------------|-------------------|-----|-----|-----|---------|------------------------|
| SID93    | $T_{RESETWIDTH}$ | Reset pulse width | 1   | –   | –   | $\mu s$ | –                      |

## Analog Peripherals

### Temperature Sensor

**Table 15. Temperature Sensor Specifications**

| Spec ID# | Parameter            | Description                 | Min | Typ | Max | Units | Details/Conditions |
|----------|----------------------|-----------------------------|-----|-----|-----|-------|--------------------|
| SID155   | T <sub>SENSACC</sub> | Temperature sensor accuracy | −5  | ±1  | 5   | °C    | −40 to +85 °C      |

### SAR ADC

**Table 16. SAR ADC DC Specifications**

| Spec ID# | Parameter | Description                        | Min             | Typ | Max              | Units | Details/Conditions                      |
|----------|-----------|------------------------------------|-----------------|-----|------------------|-------|-----------------------------------------|
| SID156   | A_RES     | Resolution                         | −               | −   | 12               | bits  | −                                       |
| SID157   | A_CHNIS_S | Number of channels – single-ended  | −               | −   | 16               | −     | 8 full-speed                            |
| SID158   | A-CHNKS_D | Number of channels – differential  | −               | −   | 8                | −     | Differential inputs use neighboring I/O |
| SID159   | A-MONO    | Monotonicity                       | −               | −   | −                | −     | Yes                                     |
| SID160   | A_GAINERR | Gain error                         | −               | −   | ±0.1             | %     | With external reference                 |
| SID161   | A_OFFSET  | Input offset voltage               | −               | −   | 2                | mV    | Measured with 1-V V <sub>REF</sub>      |
| SID162   | A_ISAR    | Current consumption                | −               | −   | 1                | mA    | −                                       |
| SID163   | A_VINS    | Input voltage range – single-ended | V <sub>SS</sub> | −   | V <sub>DDA</sub> | V     | −                                       |
| SID164   | A_VIND    | Input voltage range – differential | V <sub>SS</sub> | −   | V <sub>DDA</sub> | V     | −                                       |
| SID165   | A_INRES   | Input resistance                   | −               | −   | 2.2              | kΩ    | −                                       |
| SID166   | A_INCAP   | Input capacitance                  | −               | −   | 10               | pF    | −                                       |
| SID312   | VREFSAR   | Trimmed internal reference to SAR  | −1              | −   | 1                | %     | Percentage of V <sub>bg</sub> (1.024 V) |

**Table 17. SAR ADC AC Specifications**

| Spec ID# | Parameter              | Description                                                           | Min  | Typ | Max      | Units | Details/Conditions                           |
|----------|------------------------|-----------------------------------------------------------------------|------|-----|----------|-------|----------------------------------------------|
| SID167   | A_PSRR                 | Power supply rejection ratio                                          | 70   | −   | −        | dB    | Measured at 1-V reference                    |
| SID168   | A_CMRR                 | Common-mode rejection ratio                                           | 66   | −   | −        | dB    | −                                            |
| SID169   | A_SAMP                 | Sample rate                                                           | −    | −   | 1        | Msp/s | −                                            |
| SID313   | F <sub>sarintref</sub> | SAR operating speed without external reference bypass                 | −    | −   | 100      | ksps  | 12-bit resolution                            |
| SID170   | A_SNR                  | Signal-to-noise ratio (SNR)                                           | 65   | −   | −        | dB    | F <sub>IN</sub> = 10 kHz                     |
| SID171   | A_BW                   | Input bandwidth without aliasing                                      | −    | −   | A_SAMP/2 | kHz   | −                                            |
| SID172   | A_INL                  | Integral nonlinearity (INL). V <sub>DD</sub> = 1.71 to 5.5 V, 1 Msp/s | −1.7 | −   | 2        | LSB   | V <sub>REF</sub> = 1 V to V <sub>DD</sub>    |
| SID173   | A_INL                  | Integral nonlinearity. V <sub>DDD</sub> = 1.71 to 3.6 V, 1 Msp/s      | −1.5 | −   | 1.7      | LSB   | V <sub>REF</sub> = 1.71 V to V <sub>DD</sub> |
| SID174   | A_INL                  | Integral nonlinearity. V <sub>DD</sub> = 1.71 to 5.5 V, 500 ksp/s     | −1.5 | −   | 1.7      | LSB   | V <sub>REF</sub> = 1 V to V <sub>DD</sub>    |

**Table 17. SAR ADC AC Specifications** (continued)

| Spec ID# | Parameter | Description                                                         | Min | Typ | Max | Units | Details/<br>Conditions         |
|----------|-----------|---------------------------------------------------------------------|-----|-----|-----|-------|--------------------------------|
| SID175   | A_DNL     | Differential nonlinearity (DNL). $V_{DD} = 1.71$ to $5.5$ V, 1 Msps | -1  | -   | 2.2 | LSB   | $V_{REF} = 1$ V to $V_{DD}$    |
| SID176   | A_DNL     | Differential nonlinearity. $V_{DD} = 1.71$ to $3.6$ V, 1 Msps       | -1  | -   | 2   | LSB   | $V_{REF} = 1.71$ V to $V_{DD}$ |
| SID177   | A_DNL     | Differential nonlinearity. $V_{DD} = 1.71$ to $5.5$ V, 500 Ksps     | -1  | -   | 2.2 | LSB   | $V_{REF} = 1$ V to $V_{DD}$    |
| SID178   | A_THD     | Total harmonic distortion                                           | -   | -   | -65 | dB    | $F_{IN} = 10$ kHz              |

CSD

**Table 18. CSD Block Specifications**

| Spec ID# | Parameter  | Description                                    | Min  | Typ | Max | Units   | Details/<br>Conditions                                                                          |
|----------|------------|------------------------------------------------|------|-----|-----|---------|-------------------------------------------------------------------------------------------------|
| SID179   | VCSD       | Voltage range of operation                     | 1.71 | -   | 5.5 | V       | -                                                                                               |
| SID180   | IDAC1      | DNL for 8-bit resolution                       | -1   | -   | 1   | LSB     | -                                                                                               |
| SID181   | IDAC1      | INL for 8-bit resolution                       | -3   | -   | 3   | LSB     | -                                                                                               |
| SID182   | IDAC2      | DNL for 7-bit resolution                       | -1   | -   | 1   | LSB     | -                                                                                               |
| SID183   | IDAC2      | INL for 7-bit resolution                       | -3   | -   | 3   | LSB     | -                                                                                               |
| SID184   | SNR        | Ratio of counts of finger to noise             | 5    | -   | -   | Ratio   | Capacitance range of 9-pF to 35-pF; 0.1-pF sensitivity. Radio is not operating during the scan. |
| SID185   | IDAC1_CRT1 | Output current of IDAC1 (8-bits) in HIGH range | -    | 612 | -   | $\mu$ A | -                                                                                               |
| SID186   | IDAC1_CRT2 | Output current of IDAC1 (8-bits) in LOW range  | -    | 306 | -   | $\mu$ A | -                                                                                               |
| SID187   | IDAC2_CRT1 | Output current of IDAC2 (7-bits) in HIGH range | -    | 305 | -   | $\mu$ A | -                                                                                               |
| SID188   | IDAC2_CRT2 | Output current of IDAC2 (7-bits) in LOW range  | -    | 153 | -   | $\mu$ A | -                                                                                               |

## Digital Peripherals

### 4x TCPWM

**Table 19. Timer DC Specifications**

| Spec ID | Parameter  | Description                         | Min | Typ | Max | Units | Details/Conditions |
|---------|------------|-------------------------------------|-----|-----|-----|-------|--------------------|
| SID189  | $I_{TIM1}$ | Block current consumption at 3 MHz  | –   | –   | 50  | μA    | 16-bit timer       |
| SID190  | $I_{TIM2}$ | Block current consumption at 12 MHz | –   | –   | 175 | μA    | 16-bit timer       |
| SID191  | $I_{TIM3}$ | Block current consumption at 48 MHz | –   | –   | 712 | μA    | 16-bit timer       |

**Table 20. Timer AC Specifications**

| Spec ID | Parameter        | Description                    | Min                | Typ | Max | Units | Details/Conditions |
|---------|------------------|--------------------------------|--------------------|-----|-----|-------|--------------------|
| SID192  | $T_{TIMFREQ}$    | Operating frequency            | $F_{CLK}$          | –   | 48  | MHz   | –                  |
| SID193  | $T_{CAPWINT}$    | Capture pulse width (internal) | $2 \times T_{CLK}$ | –   | –   | ns    | –                  |
| SID194  | $T_{CAPWEXT}$    | Capture pulse width (external) | $2 \times T_{CLK}$ | –   | –   | ns    | –                  |
| SID195  | $T_{TIMRES}$     | Timer resolution               | $T_{CLK}$          | –   | –   | ns    | –                  |
| SID196  | $T_{TENWIDINT}$  | Enable pulse width (internal)  | $2 \times T_{CLK}$ | –   | –   | ns    | –                  |
| SID197  | $T_{TENWIDEXT}$  | Enable pulse width (external)  | $2 \times T_{CLK}$ | –   | –   | ns    | –                  |
| SID198  | $T_{TIMRESWINT}$ | Reset pulse width (internal)   | $2 \times T_{CLK}$ | –   | –   | ns    | –                  |
| SID199  | $T_{TIMRESEXT}$  | Reset pulse width (external)   | $2 \times T_{CLK}$ | –   | –   | ns    | –                  |

### Counter

**Table 21. Counter DC Specifications**

| Spec ID | Parameter  | Description                         | Min | Typ | Max | Units | Details/Conditions |
|---------|------------|-------------------------------------|-----|-----|-----|-------|--------------------|
| SID200  | $I_{CTR1}$ | Block current consumption at 3 MHz  | –   | –   | 50  | μA    | 16-bit Counter     |
| SID201  | $I_{CTR2}$ | Block current consumption at 12 MHz | –   | –   | 175 | μA    | 16-bit Counter     |
| SID202  | $I_{CTR3}$ | Block current consumption at 48 MHz | –   | –   | 712 | μA    | 16-bit Counter     |

**Table 22. Counter AC Specifications**

| Spec ID | Parameter        | Description                    | Min                | Typ | Max | Units | Details/Conditions |
|---------|------------------|--------------------------------|--------------------|-----|-----|-------|--------------------|
| SID203  | $T_{CTRFREQ}$    | Operating frequency            | $F_{CLK}$          | –   | 48  | MHz   | –                  |
| SID204  | $T_{CTRPWINT}$   | Capture pulse width (internal) | $2 \times T_{CLK}$ | –   | –   | ns    | –                  |
| SID205  | $T_{CTRPWEXT}$   | Capture pulse width (external) | $2 \times T_{CLK}$ | –   | –   | ns    | –                  |
| SID206  | $T_{CTRES}$      | Counter resolution             | $T_{CLK}$          | –   | –   | ns    | –                  |
| SID207  | $T_{CENWIDINT}$  | Enable pulse width (internal)  | $2 \times T_{CLK}$ | –   | –   | ns    | –                  |
| SID208  | $T_{CENWIDEXT}$  | Enable pulse width (external)  | $2 \times T_{CLK}$ | –   | –   | ns    | –                  |
| SID209  | $T_{CTBRESWINT}$ | Reset pulse width (internal)   | $2 \times T_{CLK}$ | –   | –   | ns    | –                  |
| SID210  | $T_{CTBRESWEXT}$ | Reset pulse width (external)   | $2 \times T_{CLK}$ | –   | –   | ns    | –                  |

### Pulse Width Modulation (PWM)

**Table 23. PWM DC Specifications**

| Spec ID | Parameter  | Description                         | Min | Typ | Max | Units | Details/Conditions |
|---------|------------|-------------------------------------|-----|-----|-----|-------|--------------------|
| SID211  | $I_{PWM1}$ | Block current consumption at 3 MHz  | –   | –   | 50  | μA    | 16-bit PWM         |
| SID212  | $I_{PWM2}$ | Block current consumption at 12 MHz | –   | –   | 175 | μA    | 16-bit PWM         |
| SID213  | $I_{PWM3}$ | Block current consumption at 48 MHz | –   | –   | 741 | μA    | 16-bit PWM         |

**Table 24. PWM AC Specifications**

| Spec ID | Parameter               | Description                   | Min                  | Typ | Max | Units | Details/Conditions |
|---------|-------------------------|-------------------------------|----------------------|-----|-----|-------|--------------------|
| SID214  | T <sub>PWMFREQ</sub>    | Operating frequency           | F <sub>CLK</sub>     | –   | 48  | MHz   | –                  |
| SID215  | T <sub>PWMPWINT</sub>   | Pulse width (internal)        | 2 × T <sub>CLK</sub> | –   | –   | ns    | –                  |
| SID216  | T <sub>PWMEXT</sub>     | Pulse width (external)        | 2 × T <sub>CLK</sub> | –   | –   | ns    | –                  |
| SID217  | T <sub>PWMKILLINT</sub> | Kill pulse width (internal)   | 2 × T <sub>CLK</sub> | –   | –   | ns    | –                  |
| SID218  | T <sub>PWMKILLEXT</sub> | Kill pulse width (external)   | 2 × T <sub>CLK</sub> | –   | –   | ns    | –                  |
| SID219  | T <sub>PWMEINT</sub>    | Enable pulse width (internal) | 2 × T <sub>CLK</sub> | –   | –   | ns    | –                  |
| SID220  | T <sub>PWMENEXT</sub>   | Enable pulse width (external) | 2 × T <sub>CLK</sub> | –   | –   | ns    | –                  |
| SID221  | T <sub>PWMRESWINT</sub> | Reset pulse width (internal)  | 2 × T <sub>CLK</sub> | –   | –   | ns    | –                  |
| SID222  | T <sub>PWMRESWEXT</sub> | Reset pulse width (external)  | 2 × T <sub>CLK</sub> | –   | –   | ns    | –                  |

*I<sup>2</sup>C*
**Table 25. I<sup>2</sup>C DC Specifications**

| Spec ID | Parameter         | Description                                 | Min | Typ | Max | Units | Details/Conditions |
|---------|-------------------|---------------------------------------------|-----|-----|-----|-------|--------------------|
| SID223  | I <sub>I2C1</sub> | Block current consumption at 100 kHz        | –   | –   | 50  | μA    | –                  |
| SID224  | I <sub>I2C2</sub> | Block current consumption at 400 kHz        | –   | –   | 155 | μA    | –                  |
| SID225  | I <sub>I2C3</sub> | Block current consumption at 1 Mbps         | –   | –   | 390 | μA    | –                  |
| SID226  | I <sub>I2C4</sub> | I <sup>2</sup> C enabled in Deep-Sleep mode | –   | –   | 1.4 | μA    | –                  |

**Table 26. Fixed I<sup>2</sup>C AC Specifications**

| Spec ID | Parameter         | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|-------------------|-------------|-----|-----|-----|-------|--------------------|
| SID227  | F <sub>I2C1</sub> | Bit rate    | –   | –   | 1   | Mbps  | –                  |

*LCD Direct Drive*
**Table 27. LCD Direct Drive DC Specifications**

| Spec ID | Parameter             | Description                                                | Min | Typ  | Max  | Units | Details/Conditions                    |
|---------|-----------------------|------------------------------------------------------------|-----|------|------|-------|---------------------------------------|
| SID228  | I <sub>LCDLOW</sub>   | Operating current in low-power mode                        | –   | 17.5 | –    | μA    | 16 × 4 small-segment display at 50 Hz |
| SID229  | C <sub>LCDCAP</sub>   | LCD capacitance per segment/common driver                  | –   | 500  | 5000 | pF    |                                       |
| SID230  | LCD <sub>OFFSET</sub> | Long-term segment offset                                   | –   | 20   | –    | mV    |                                       |
| SID231  | I <sub>LCDOP1</sub>   | LCD system operating current.<br>V <sub>bias</sub> = 5 V   | –   | 2    | –    | mA    | 32 × 4 segments.<br>50 Hz. 25 °C      |
| SID232  | I <sub>LCDOP2</sub>   | LCD system operating current.<br>V <sub>bias</sub> = 3.3 V | –   | 2    | –    | mA    | 32 × 4 segments.<br>50 Hz. 25 °C      |

**Table 28. LCD Direct Drive AC Specifications**

| Spec ID | Parameter        | Description    | Min | Typ | Max | Units | Details/Conditions |
|---------|------------------|----------------|-----|-----|-----|-------|--------------------|
| SID233  | F <sub>LCD</sub> | LCD frame rate | 10  | 50  | 150 | Hz    | –                  |

**Table 29. Fixed UART DC Specifications**

| Spec ID | Parameter          | Description                            | Min | Typ | Max | Units | Details/Conditions |
|---------|--------------------|----------------------------------------|-----|-----|-----|-------|--------------------|
| SID234  | I <sub>UART1</sub> | Block current consumption at 100 kbps  | –   | –   | 55  | μA    | –                  |
| SID235  | I <sub>UART2</sub> | Block current consumption at 1000 kbps | –   | –   | 360 | μA    | –                  |

**Table 30. Fixed UART AC Specifications**

| Spec ID | Parameter         | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|-------------------|-------------|-----|-----|-----|-------|--------------------|
| SID236  | F <sub>UART</sub> | Bit rate    | –   | –   | 1   | Mbps  | –                  |

*SPI Specifications*
**Table 31. Fixed SPI DC Specifications**

| Spec ID | Parameter         | Description                         | Min | Typ | Max | Units | Details/Conditions |
|---------|-------------------|-------------------------------------|-----|-----|-----|-------|--------------------|
| SID237  | I <sub>SPI1</sub> | Block current consumption at 1 Mbps | –   | –   | 360 | μA    | –                  |
| SID238  | I <sub>SPI2</sub> | Block current consumption at 4 Mbps | –   | –   | 560 | μA    | –                  |
| SID239  | I <sub>SPI3</sub> | Block current consumption at 8 Mbps | –   | –   | 600 | μA    | –                  |

**Table 32. Fixed SPI AC Specifications**

| Spec ID | Parameter        | Description                                       | Min | Typ | Max | Units | Details/Conditions |
|---------|------------------|---------------------------------------------------|-----|-----|-----|-------|--------------------|
| SID240  | F <sub>SPI</sub> | SPI operating frequency (master; 6x oversampling) | –   | –   | 8   | MHz   | –                  |

**Table 33. Fixed SPI Master Mode AC Specifications**

| Spec ID | Parameter        | Description                                                                | Min | Typ | Max | Units | Details/Conditions               |
|---------|------------------|----------------------------------------------------------------------------|-----|-----|-----|-------|----------------------------------|
| SID241  | T <sub>DMO</sub> | MOSI valid after SCLK driving edge                                         | –   | –   | 18  | ns    | –                                |
| SID242  | T <sub>DSI</sub> | MISO valid before SCLK capturing edge. Full clock, late MISO sampling used | 20  | –   | –   | ns    | Full clock, late MISO sampling   |
| SID243  | T <sub>HMO</sub> | Previous MOSI data hold time                                               | 0   | –   | –   | ns    | Referred to Slave capturing edge |

**Table 34. Fixed SPI Slave Mode AC Specifications**

| Spec ID | Parameter            | Description                                                                        | Min | Typ | Max                       | Units |
|---------|----------------------|------------------------------------------------------------------------------------|-----|-----|---------------------------|-------|
| SID244  | T <sub>DMI</sub>     | MOSI valid before SCLK capturing edge                                              | 40  | –   | –                         | ns    |
| SID245  | T <sub>DSO</sub>     | MISO valid after SCLK driving edge                                                 | –   | –   | 42 + 3 × T <sub>CPU</sub> | ns    |
| SID246  | T <sub>DSO_ext</sub> | MISO Valid after SCLK driving edge in external clock mode. V <sub>DD</sub> < 3.0 V | –   | –   | 53                        | ns    |
| SID247  | T <sub>HMO</sub>     | Previous MISO data hold time                                                       | 0   | –   | –                         | ns    |
| SID248  | T <sub>SSELSCK</sub> | SSEL valid to first SCK valid edge                                                 | 100 | –   | –                         | ns    |

## Memory

**Table 35. Flash DC Specifications**

| Spec ID | Parameter         | Description                        | Min  | Typ | Max | Units | Details/Conditions       |
|---------|-------------------|------------------------------------|------|-----|-----|-------|--------------------------|
| SID249  | V <sub>PE</sub>   | Erase and program voltage          | 1.71 | –   | 5.5 | V     | –                        |
| SID309  | T <sub>WS48</sub> | Number of Wait states at 32–48 MHz | 2    | –   | –   | –     | CPU execution from flash |
| SID310  | T <sub>WS32</sub> | Number of Wait states at 16–32 MHz | 1    | –   | –   | –     | CPU execution from flash |
| SID311  | T <sub>WS16</sub> | Number of Wait states for 0–16 MHz | 0    | –   | –   | –     | CPU execution from flash |

**Table 36. Flash AC Specifications**

| Spec ID | Parameter                              | Description                                               | Min   | Typ | Max | Units   | Details/Conditions      |
|---------|----------------------------------------|-----------------------------------------------------------|-------|-----|-----|---------|-------------------------|
| SID250  | T <sub>ROWWRITE</sub> <sup>[5]</sup>   | Row (block) write time (erase and program)                | –     | –   | 20  | ms      | Row (block) = 256 bytes |
| SID251  | T <sub>ROWERASE</sub> <sup>[5]</sup>   | Row erase time                                            | –     | –   | 13  | ms      | –                       |
| SID252  | T <sub>ROWPROGRAM</sub> <sup>[5]</sup> | Row program time after erase                              | –     | –   | 7   | ms      | –                       |
| SID253  | T <sub>BULKERASE</sub> <sup>[5]</sup>  | Bulk erase time (256 KB)                                  | –     | –   | 35  | ms      | –                       |
| SID254  | T <sub>DEVPROG</sub> <sup>[5]</sup>    | Total device program time                                 | –     | –   | 25  | seconds | –                       |
| SID255  | F <sub>END</sub>                       | Flash endurance                                           | 100 K | –   | –   | cycles  | –                       |
| SID256  | F <sub>RET</sub>                       | Flash retention. T <sub>A</sub> ≤ 55 °C, 100 K P/E cycles | 20    | –   | –   | years   | –                       |
| SID257  | F <sub>RET2</sub>                      | Flash retention. T <sub>A</sub> ≤ 85 °C, 10 K P/E cycles  | 10    | –   | –   | years   | –                       |

## System Resources

### Power-on-Reset (POR)

**Table 37. POR DC Specifications**

| Spec ID | Parameter             | Description          | Min  | Typ | Max  | Units | Details/Conditions |
|---------|-----------------------|----------------------|------|-----|------|-------|--------------------|
| SID258  | V <sub>RISEIPOR</sub> | Rising trip voltage  | 0.80 | –   | 1.45 | V     | –                  |
| SID259  | V <sub>FALLIPOR</sub> | Falling trip voltage | 0.75 | –   | 1.40 | V     | –                  |
| SID260  | V <sub>IPORHYST</sub> | Hysteresis           | 15   | –   | 200  | mV    | –                  |

**Table 38. POR AC Specifications**

| Spec ID | Parameter            | Description                                                             | Min | Typ | Max | Units | Details/Conditions |
|---------|----------------------|-------------------------------------------------------------------------|-----|-----|-----|-------|--------------------|
| SID264  | T <sub>PPOR_TR</sub> | Precision power-on reset (PPOR) response time in Active and Sleep modes | –   | –   | 1   | μs    | –                  |

**Table 39. Brown-Out Detect**

| Spec ID# | Parameter              | Description                                | Min  | Typ | Max | Units | Details/Conditions |
|----------|------------------------|--------------------------------------------|------|-----|-----|-------|--------------------|
| SID261   | V <sub>FALLPPOR</sub>  | BOD trip voltage in Active and Sleep modes | 1.64 | –   | –   | V     | –                  |
| SID262   | V <sub>FALLDPSLP</sub> | BOD trip voltage in Deep Sleep             | 1.4  | –   | –   | V     | –                  |

### Note

- It can take as much as 20 ms to write to flash. During this time, the device should not be reset, or flash operations will be interrupted and cannot be relied on to have completed. Reset sources include the XRES pin, software resets, CPU lockup states and privilege violations, improper power supply levels, and watchdogs. Make certain that these are not inadvertently activated.

**Table 40. Hibernate Reset**

| Spec ID# | Parameter            | Description                   | Min | Typ | Max | Units | Details/<br>Conditions |
|----------|----------------------|-------------------------------|-----|-----|-----|-------|------------------------|
| SID263   | V <sub>HBRTRIP</sub> | BOD trip voltage in Hibernate | 1.1 | –   | –   | V     | –                      |

Voltage Monitors (LVD)

**Table 41. Voltage Monitor DC Specifications**

| Spec ID | Parameter          | Description              | Min  | Typ  | Max  | Units | Details/<br>Conditions |
|---------|--------------------|--------------------------|------|------|------|-------|------------------------|
| SID265  | V <sub>LVI1</sub>  | LVI_A/D_SEL[3:0] = 0000b | 1.71 | 1.75 | 1.79 | V     | –                      |
| SID266  | V <sub>LVI2</sub>  | LVI_A/D_SEL[3:0] = 0001b | 1.76 | 1.80 | 1.85 | V     | –                      |
| SID267  | V <sub>LVI3</sub>  | LVI_A/D_SEL[3:0] = 0010b | 1.85 | 1.90 | 1.95 | V     | –                      |
| SID268  | V <sub>LVI4</sub>  | LVI_A/D_SEL[3:0] = 0011b | 1.95 | 2.00 | 2.05 | V     | –                      |
| SID269  | V <sub>LVI5</sub>  | LVI_A/D_SEL[3:0] = 0100b | 2.05 | 2.10 | 2.15 | V     | –                      |
| SID270  | V <sub>LVI6</sub>  | LVI_A/D_SEL[3:0] = 0101b | 2.15 | 2.20 | 2.26 | V     | –                      |
| SID271  | V <sub>LVI7</sub>  | LVI_A/D_SEL[3:0] = 0110b | 2.24 | 2.30 | 2.36 | V     | –                      |
| SID272  | V <sub>LVI8</sub>  | LVI_A/D_SEL[3:0] = 0111b | 2.34 | 2.40 | 2.46 | V     | –                      |
| SID273  | V <sub>LVI9</sub>  | LVI_A/D_SEL[3:0] = 1000b | 2.44 | 2.50 | 2.56 | V     | –                      |
| SID274  | V <sub>LVI10</sub> | LVI_A/D_SEL[3:0] = 1001b | 2.54 | 2.60 | 2.67 | V     | –                      |
| SID2705 | V <sub>LVI11</sub> | LVI_A/D_SEL[3:0] = 1010b | 2.63 | 2.70 | 2.77 | V     | –                      |
| SID276  | V <sub>LVI12</sub> | LVI_A/D_SEL[3:0] = 1011b | 2.73 | 2.80 | 2.87 | V     | –                      |
| SID277  | V <sub>LVI13</sub> | LVI_A/D_SEL[3:0] = 1100b | 2.83 | 2.90 | 2.97 | V     | –                      |
| SID278  | V <sub>LVI14</sub> | LVI_A/D_SEL[3:0] = 1101b | 2.93 | 3.00 | 3.08 | V     | –                      |
| SID279  | V <sub>LVI15</sub> | LVI_A/D_SEL[3:0] = 1110b | 3.12 | 3.20 | 3.28 | V     | –                      |
| SID280  | V <sub>LVI16</sub> | LVI_A/D_SEL[3:0] = 1111b | 4.39 | 4.50 | 4.61 | V     | –                      |
| SID281  | LVI_IDD            | Block current            | –    | –    | 100  | μA    | –                      |

**Table 42. Voltage Monitor AC Specifications**

| Spec ID | Parameter            | Description               | Min | Typ | Max | Units | Details/<br>Conditions |
|---------|----------------------|---------------------------|-----|-----|-----|-------|------------------------|
| SID282  | T <sub>MONTRIP</sub> | Voltage monitor trip time | –   | –   | 1   | μs    | –                      |

SWD Interface

**Table 43. SWD Interface Specifications**

| Spec ID | Parameter               | Description                                   | Min      | Typ | Max     | Units | Details/Conditions               |
|---------|-------------------------|-----------------------------------------------|----------|-----|---------|-------|----------------------------------|
| SID283  | F <sub>SWDCLK1</sub>    | $3.3\text{ V} \leq V_{DD} \leq 5.5\text{ V}$  | –        | –   | 14      | MHz   | SWDCLK ≤ 1/3 CPU clock frequency |
| SID284  | F <sub>SWDCLK2</sub>    | $1.71\text{ V} \leq V_{DD} \leq 3.3\text{ V}$ | –        | –   | 7       | MHz   | SWDCLK ≤ 1/3 CPU clock frequency |
| SID285  | T <sub>SWDI_SETUP</sub> | T = 1/f SWDCLK                                | 0.25 × T | –   | –       | ns    | –                                |
| SID286  | T <sub>SWDI_HOLD</sub>  | T = 1/f SWDCLK                                | 0.25 × T | –   | –       | ns    | –                                |
| SID287  | T <sub>SWDO_VALID</sub> | T = 1/f SWDCLK                                | –        | –   | 0.5 × T | ns    | –                                |
| SID288  | T <sub>SWDO_HOLD</sub>  | T = 1/f SWDCLK                                | 1        | –   | –       | ns    | –                                |

### Internal Main Oscillator

**Table 44. IMO DC Specifications**

| Spec ID | Parameter         | Description                     | Min | Typ | Max  | Units | Details/Conditions |
|---------|-------------------|---------------------------------|-----|-----|------|-------|--------------------|
| SID289  | I <sub>IMO1</sub> | IMO operating current at 48 MHz | –   | –   | 1000 | μA    | –                  |
| SID290  | I <sub>IMO2</sub> | IMO operating current at 24 MHz | –   | –   | 325  | μA    | –                  |
| SID291  | I <sub>IMO3</sub> | IMO operating current at 12 MHz | –   | –   | 225  | μA    | –                  |
| SID292  | I <sub>IMO4</sub> | IMO operating current at 6 MHz  | –   | –   | 180  | μA    | –                  |
| SID293  | I <sub>IMO5</sub> | IMO operating current at 3 MHz  | –   | –   | 150  | μA    | –                  |

**Table 45. IMO AC Specifications**

| Spec ID | Parameter            | Description                          | Min | Typ | Max | Units | Details/Conditions          |
|---------|----------------------|--------------------------------------|-----|-----|-----|-------|-----------------------------|
| SID296  | F <sub>IMOTOL3</sub> | Frequency variation from 3 to 48 MHz | –   | –   | ±2  | %     | With API-called calibration |
| SID297  | F <sub>IMOTOL3</sub> | IMO startup time                     | –   | 12  | –   | μs    | –                           |

### Internal Low-Speed Oscillator

**Table 46. ILO DC Specifications**

| Spec ID | Parameter         | Description                     | Min | Typ | Max  | Units | Details/Conditions |
|---------|-------------------|---------------------------------|-----|-----|------|-------|--------------------|
| SID298  | I <sub>ILO2</sub> | ILO operating current at 32 kHz | –   | 0.3 | 1.05 | μA    | –                  |

**Table 47. ILO AC Specifications**

| Spec ID | Parameter              | Description              | Min | Typ | Max | Units | Details/Conditions |
|---------|------------------------|--------------------------|-----|-----|-----|-------|--------------------|
| SID299  | T <sub>STARTILO1</sub> | ILO startup time         | –   | –   | 2   | ms    | –                  |
| SID300  | F <sub>ILOTRIM1</sub>  | 32-kHz trimmed frequency | 15  | 32  | 50  | kHz   | –                  |

**Table 48. External Clock Specifications**

| Spec ID | Parameter  | Description                                | Min | Typ | Max | Units | Details/Conditions                                |
|---------|------------|--------------------------------------------|-----|-----|-----|-------|---------------------------------------------------|
| SID301  | ExtClkFreq | External clock input frequency             | 0   | –   | 48  | MHz   | CMOS input level only. TTL input is not supported |
| SID302  | ExtClkDuty | Duty cycle; measured at V <sub>DD</sub> /2 | 45  | –   | 55  | %     | CMOS input level only. TTL input is not supported |

**Table 49. ECO Specifications**

| Spec ID# | Parameter           | Description                    | Min | Typ  | Max | Units | Details/Conditions |
|----------|---------------------|--------------------------------|-----|------|-----|-------|--------------------|
| SID389   | F <sub>ECO</sub>    | Crystal frequency              | –   | 24   | –   | MHz   | –                  |
| SID390   | F <sub>TOL</sub>    | Frequency tolerance            | –50 | –    | 50  | ppm   | –                  |
| SID391   | ESR                 | Equivalent series resistance   | –   | –    | 60  | Ω     | –                  |
| SID392   | PD                  | Drive level                    | –   | –    | 100 | μW    | –                  |
| SID393   | T <sub>START1</sub> | Startup time (Fast Charge on)  | –   | –    | 850 | μs    | –                  |
| SID394   | T <sub>START2</sub> | Startup time (Fast Charge off) | –   | –    | 3   | ms    | –                  |
| SID395   | C <sub>L</sub>      | Load capacitance               | –   | 8    | –   | pF    | –                  |
| SID396   | C <sub>0</sub>      | Shunt capacitance              | –   | 1.1  | –   | pF    | –                  |
| SID397   | I <sub>ECO</sub>    | Operating current              | –   | 1400 | –   | μA    | –                  |

**Table 50. WCO Specifications**

| Spec ID# | Parameter   | Description                         | Min | Typ    | Max  | Units      | Details/<br>Conditions |
|----------|-------------|-------------------------------------|-----|--------|------|------------|------------------------|
| SID398   | $F_{WCO}$   | Crystal frequency                   | –   | 32.768 | –    | kHz        | –                      |
| SID399   | $F_{TOL}$   | Frequency tolerance                 | –   | 50     | –    | ppm        | –                      |
| SID400   | ESR         | Equivalent series resistance        | –   | 50     | –    | k $\Omega$ | –                      |
| SID401   | PD          | Drive level                         | –   | –      | 1    | $\mu$ W    | –                      |
| SID402   | $T_{START}$ | Startup time                        | –   | –      | 500  | ms         | –                      |
| SID403   | $C_L$       | Crystal load capacitance            | 6   | –      | 12.5 | pF         | –                      |
| SID404   | $C_0$       | Crystal shunt capacitance           | –   | 1.35   | –    | pF         | –                      |
| SID405   | $I_{WCO1}$  | Operating current (high-power mode) | –   | –      | 8    | $\mu$ A    | –                      |
| SID406   | $I_{WCO2}$  | Operating current (low-power mode)  | –   | –      | 2.6  | $\mu$ A    | –                      |

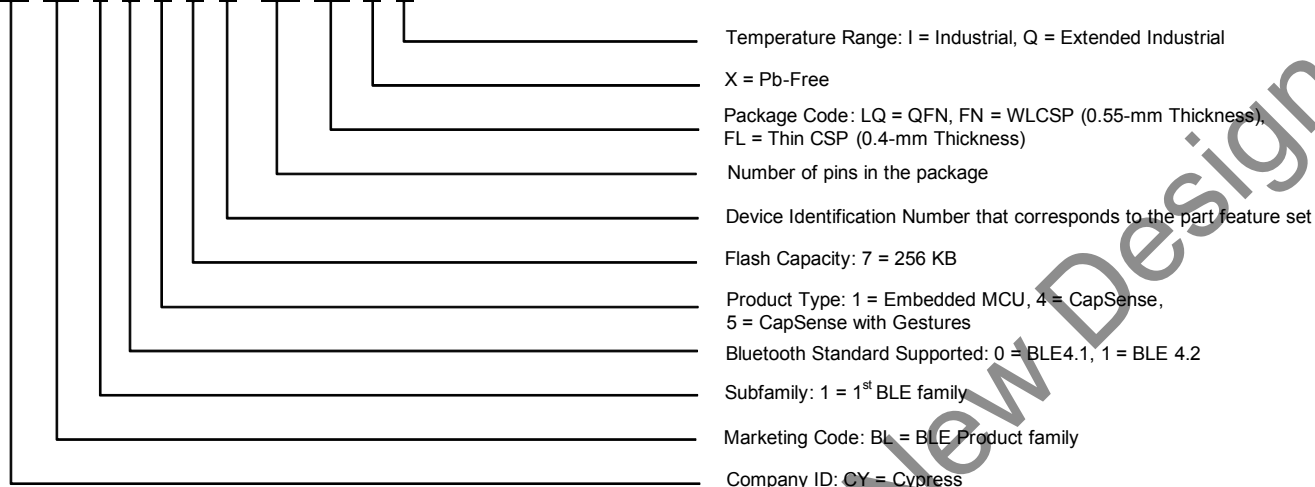
## Ordering Information

The CYBL1XX7X part numbers and features are listed in the following table.

| Part Number      | CPU Speed (MHz) | Flash Size (KB) | DMA | CapSense       | SCB | TCPWM | 12-bit ADC | I2S | PWM | LCD | Package     | Bluetooth Version |
|------------------|-----------------|-----------------|-----|----------------|-----|-------|------------|-----|-----|-----|-------------|-------------------|
| CYBL10573-56LQXI | 48              | 256             | No  | Yes (Gestures) | 2   | 4     | 1 Msps     | Yes | 1   | Yes | 56-QFN      | 4.1               |
| CYBL10573-76FNXI | 48              | 256             | No  | Yes (Gestures) | 2   | 4     | 1 Msps     | Yes | 1   | Yes | 76-WLCSP    | 4.1               |
| CYBL11171-56LQXI | 48              | 256             | Yes | No             | 1   | 2     | 1 Msps     | No  | 0   | No  | 56-QFN      | 4.2               |
| CYBL11172-56LQXI | 48              | 256             | Yes | No             | 2   | 4     | 1 Msps     | No  | 0   | No  | 56-QFN      | 4.2               |
| CYBL11173-56LQXI | 48              | 256             | Yes | No             | 2   | 4     | 1 Msps     | Yes | 0   | No  | 56-QFN      | 4.2               |
| CYBL11471-56LQXI | 48              | 256             | Yes | Yes            | 2   | 4     | 1 Msps     | No  | 0   | No  | 56-QFN      | 4.2               |
| CYBL11472-56LQXI | 48              | 256             | Yes | Yes            | 2   | 4     | 1 Msps     | Yes | 0   | No  | 56-QFN      | 4.2               |
| CYBL11473-56LQXI | 48              | 256             | Yes | Yes            | 2   | 4     | 1 Msps     | No  | 0   | Yes | 56-QFN      | 4.2               |
| CYBL11571-56LQXI | 48              | 256             | Yes | Yes (Gestures) | 2   | 4     | 1 Msps     | No  | 0   | No  | 56-QFN      | 4.2               |
| CYBL11572-56LQXI | 48              | 256             | Yes | Yes (Gestures) | 2   | 4     | 1 Msps     | Yes | 1   | No  | 56-QFN      | 4.2               |
| CYBL11573-56LQXI | 48              | 256             | Yes | Yes (Gestures) | 2   | 4     | 1 Msps     | Yes | 1   | Yes | 56-QFN      | 4.2               |
| CYBL11573-56LQXQ | 48              | 256             | Yes | Yes (Gestures) | 2   | 4     | 1 Msps     | Yes | 1   | Yes | 56-QFN      | 4.2               |
| CYBL11573-76FNXI | 48              | 256             | Yes | Yes (Gestures) | 2   | 4     | 1 Msps     | Yes | 1   | Yes | 76-WLCSP    | 4.2               |
| CYBL11573-76FLXI | 48              | 256             | Yes | Yes (Gestures) | 2   | 4     | 1 Msps     | Yes | 1   | Yes | 76-Thin CSP | 4.2               |
| CYBL11573-76FNXQ | 48              | 256             | Yes | Yes (Gestures) | 2   | 4     | 1 Msps     | Yes | 1   | Yes | 76-WLCSP    | 4.2               |

## Ordering Code Definitions

**CY BL 1 X A B C- DE EG H I**



The Field Values are listed in the following table:

| Field | Description             | Values | Meaning                        |
|-------|-------------------------|--------|--------------------------------|
| CYBL  | Cypress PRoC BLE Family | CYBL   |                                |
| 1X    | Subfamily               | 10, 11 | 1st Generation BLE 4.1, 4.2    |
| A     | Product Type            | 1      | Embedded Only                  |
|       |                         | 4      | CapSense                       |
|       |                         | 5      | Touch                          |
| B     | Flash Capacity          | 7      | 256 KB                         |
| C     | Feature set             |        |                                |
| DE    | Package Pins            | 56     |                                |
|       |                         | 76     |                                |
| FG    | Package code            | LQ     | QFN                            |
|       |                         | FN     | WLCSP                          |
|       |                         | FL     | Thin CSP                       |
| H     | Pb                      | X      | Pb-free                        |
|       |                         |        | X Absent (with Pb)             |
| I     | Temperature Range       | Q      | Extended temp –40 °C to 105 °C |
|       |                         | I      | Industrial –40 °C to 85 °C     |

### Note

6. All part numbers support input voltage from 1.9 V to 5.5 V.

## Packaging

**Table 51. Package Characteristics**

| Parameter       | Description                                | Conditions | Min | Typ  | Max | Units   |
|-----------------|--------------------------------------------|------------|-----|------|-----|---------|
| T <sub>A</sub>  | Operating ambient temperature              | –          | –40 | 25   | 105 | °C      |
| T <sub>J</sub>  | Operating junction temperature             | –          | –40 | –    | 125 | °C      |
| T <sub>JA</sub> | Package $\theta_{JA}$ (56-pin QFN)         | –          | –   | 16.9 | –   | °C/watt |
| T <sub>JC</sub> | Package $\theta_{JC}$ (56-pin QFN)         | –          | –   | 9.7  | –   | °C/watt |
| T <sub>JA</sub> | Package $\theta_{JA}$ (76-ball WLCSP)      | –          | –   | 20.1 | –   | °C/watt |
| T <sub>JC</sub> | Package $\theta_{JC}$ (76-ball WLCSP)      | –          | –   | 0.19 | –   | °C/watt |
| T <sub>JA</sub> | Package $\theta_{JA}$ (76-ball Thin WLCSP) | –          | –   | 20.9 | –   | °C/watt |
| T <sub>JC</sub> | Package $\theta_{JC}$ (76-ball Thin WLCSP) | –          | –   | 0.17 | –   | °C/watt |

**Table 52. Solder Reflow Peak Temperature**

| Package                      | Maximum Peak Temperature | Maximum Time at Peak Temperature |
|------------------------------|--------------------------|----------------------------------|
| 56-pin QFN                   | 260 °C                   | 30 seconds                       |
| 76-ball WLCSP and Thin WLCSP | 260 °C                   | 30 seconds                       |

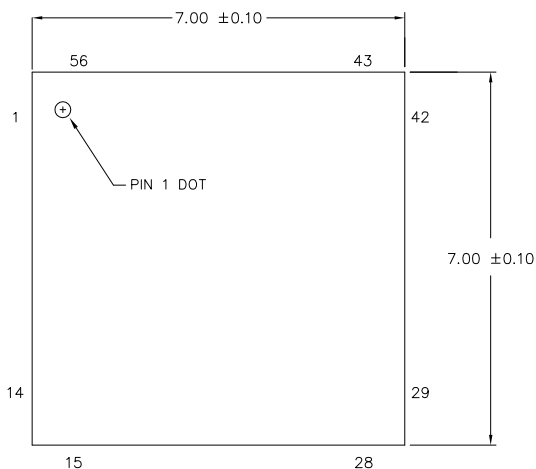
**Table 53. Package Moisture Sensitivity Level (MSL), IPC/JEDEC J-STD-2**

| Package                      | MSL   |
|------------------------------|-------|
| 56-pin QFN                   | MSL 3 |
| 76-ball WLCSP and Thin WLCSP | MSL 1 |

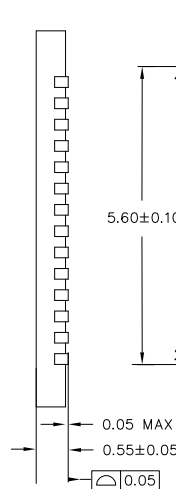
**Table 54. Package Details**

| Spec ID            | Package            | Description                 |
|--------------------|--------------------|-----------------------------|
| 001-58740 Rev. *C  | 56-pin QFN         | 7 mm × 7 mm × 0.6 mm        |
| 001-96603 Rev. *A  | 76-ball WLCSP      | 4.04 mm × 3.87 mm × 0.55 mm |
| 002-10658, Rev. ** | 76-ball thin WLCSP | 4.04 mm X 3.87 mm X 0.4 mm  |

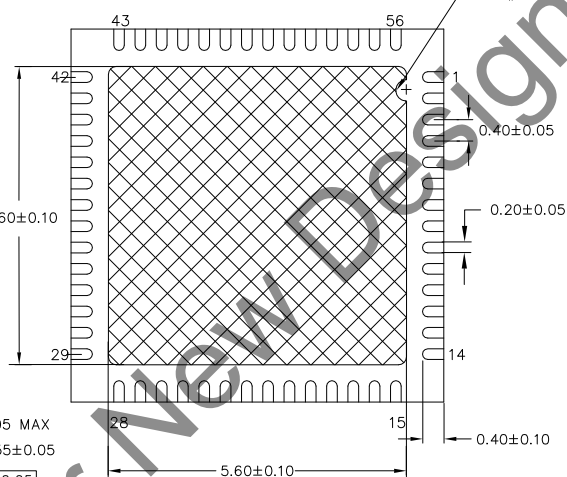
**TOP VIEW**



### SIDE VIEW



**BOTTOM VIEW**



1.  HATCH AREA IS SOLDERABLE EXPOSED PAD  
2. BASED ON REF JEDEC # MO-248  
3. ALL DIMENSIONS ARE IN MILLIMETERS

001-58740 \*C

The center pad on the QFN package must be connected to ground (VSS) for the proper operation of the device.

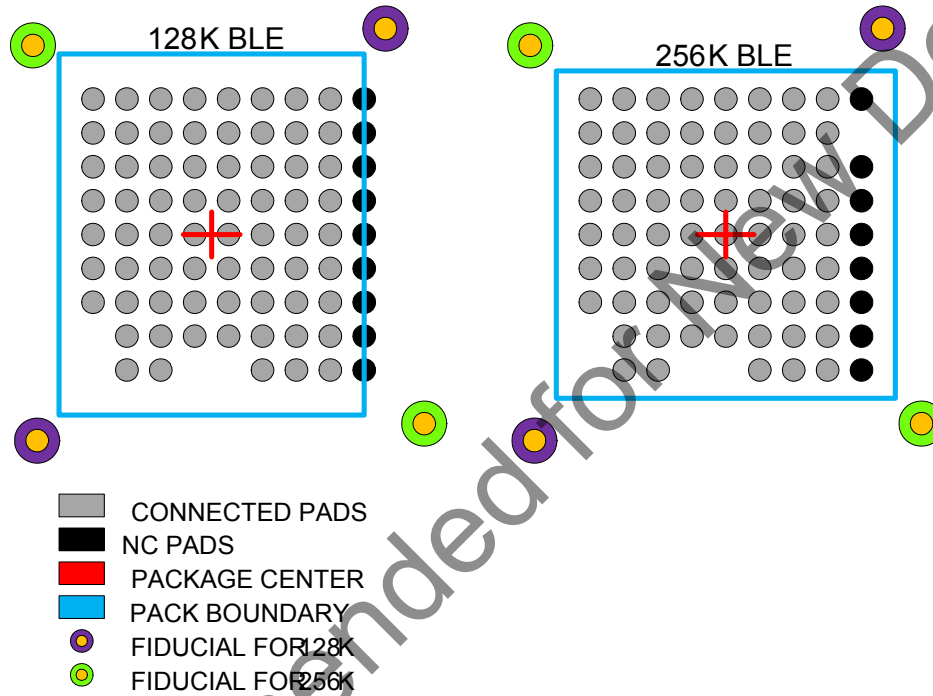
### WLCSP Compatibility

The PRoC BLE family has products with 128 KB (16KB SRAM) and 256 KB (32KB SRAM) Flash. Package pin-outs and sizes are identical for the 56-pin QFN package but are different in one dimension for the 68-ball WLCSP.

The 256KB Flash product has an extra column of balls which are required for mechanical integrity purposes in the Chip-Scale package. With consideration for this difference, the land pattern on the PCB may be designed such that either product may be used with no change to the PCB design.

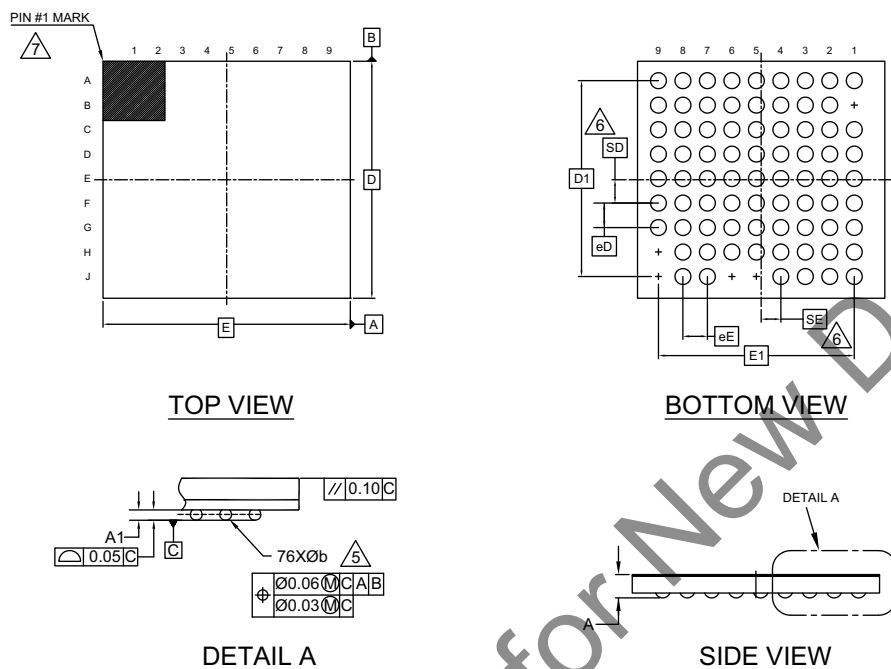
Figure 7 shows the 128KB and 256 KB Flash CSP Packages.

**Figure 7. 128KB and 256 KB Flash CSP Packages**



The rightmost column of (all NC, No Connect) balls in the 256K BLE WLCSP is for mechanical integrity purposes. The package is thus wider (3.2 mm versus 2.8 mm). All other dimensions are identical. Cypress will provide layout symbols for PCB layout.

The scheme in Figure 7 is implemented to design the PCB for the 256K BLE package with the appropriate space requirements thus allowing use of either package at a later time without redesigning the Printed Circuit Board.

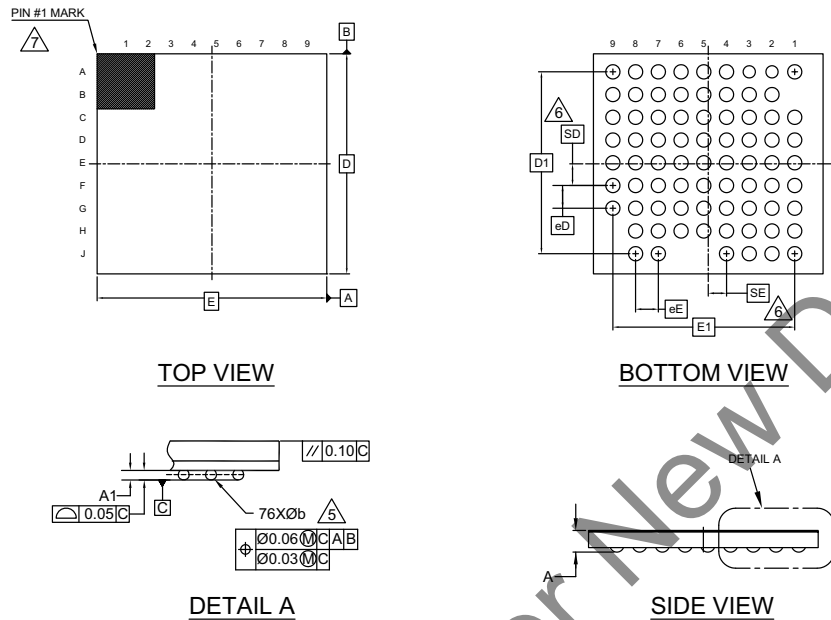
**Figure 8. 76-Ball WLCSP Package Outline**


| SYMBOL | DIMENSIONS |      |      |
|--------|------------|------|------|
|        | MIN.       | NOM. | MAX. |
| A      | -          | -    | 0.55 |
| A1     | 0.18       | 0.21 | 0.24 |
| D      | 3.87 BSC   |      |      |
| E      | 4.04 BSC   |      |      |
| D1     | 3.20 BSC   |      |      |
| E1     | 3.20 BSC   |      |      |
| MD     | 9          |      |      |
| ME     | 9          |      |      |
| N      | 76         |      |      |
| Ø b    | 0.23       | 0.26 | 0.29 |
| eD     | 0.40 BSC   |      |      |
| eE     | 0.40 BSC   |      |      |
| SD     | 0.381 BSC  |      |      |
| SE     | 0.321 BSC  |      |      |

**NOTES:**

- ALL DIMENSIONS ARE IN MILLIMETERS.
- SOLDER BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-020.
- "e" REPRESENTS THE SOLDER BALL GRID PITCH.
- SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.  
SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.  
N IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
- DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
- "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.  
WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" OR "SE" = 0.  
WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.
- A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK METALIZED MARK, INDENTATION OR OTHER MEANS.
- "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED SOLDER BALLS.
- JEDEC SPECIFICATION NO. REF : N/A

001-96603 \*B

**Figure 9. 76-Ball Thin WLCSP Package Outline**


| SYMBOL | DIMENSIONS |      |       |
|--------|------------|------|-------|
|        | MIN.       | NOM. | MAX.  |
| A      | -          | -    | 0.40  |
| A1     | 0.072      | 0.08 | 0.088 |
| D      | 3.87 BSC   |      |       |
| E      | 4.04 BSC   |      |       |
| D1     | 3.20 BSC   |      |       |
| E1     | 3.20 BSC   |      |       |
| MD     | 9          |      |       |
| ME     | 9          |      |       |
| N      | 76         |      |       |
| Ø b    | 0.22       | 0.25 | 0.28  |
| eD     | 0.40 BSC   |      |       |
| eE     | 0.40 BSC   |      |       |
| SD     | 0.381      |      |       |
| SE     | 0.321      |      |       |

**NOTES:**

- ALL DIMENSIONS ARE IN MILLIMETERS.
- SOLDER BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-020.
- "e" REPRESENTS THE SOLDER BALL GRID PITCH.
- SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.  
SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.  
N IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
- DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
- "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW. WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" OR "SE" = 0. WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.
- A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK METALIZED MARK, INDENTATION OR OTHER MEANS.
- "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED SOLDER BALLS.

002-10658 \*\*

## Acronyms

**Table 55. Acronyms Used in This Document**

| Acronym | Description                                                                                     |
|---------|-------------------------------------------------------------------------------------------------|
| abus    | analog local bus                                                                                |
| ADC     | analog-to-digital converter                                                                     |
| AG      | analog global                                                                                   |
| AHB     | AMBA (advanced microcontroller bus architecture) high-performance bus, an ARM data transfer bus |
| ALU     | arithmetic logic unit                                                                           |
| AMUXBUS | analog multiplexer bus                                                                          |
| API     | application programming interface                                                               |
| APSR    | application program status register                                                             |
| ARM®    | advanced RISC machine, a CPU architecture                                                       |
| ATM     | automatic thump mode                                                                            |
| BW      | bandwidth                                                                                       |
| CAN     | Controller Area Network, a communications protocol                                              |
| CMRR    | common-mode rejection ratio                                                                     |
| CPU     | central processing unit                                                                         |
| CRC     | cyclic redundancy check, an error-checking protocol                                             |
| DAC     | digital-to-analog converter, see also IDAC, VDAC                                                |
| DFB     | digital filter block                                                                            |
| DIO     | digital input/output, GPIO with only digital capabilities, no analog. See GPIO.                 |
| DMIPS   | Dhrystone million instructions per second                                                       |
| DMA     | direct memory access, see also TD                                                               |
| DNL     | differential nonlinearity, see also INL                                                         |
| DNU     | do not use                                                                                      |
| DR      | port write data registers                                                                       |
| DSI     | digital system interconnect                                                                     |
| DWT     | data watchpoint and trace                                                                       |
| ECC     | error correcting code                                                                           |
| ECO     | external crystal oscillator                                                                     |
| EEPROM  | electrically erasable programmable read-only memory                                             |
| EMI     | electromagnetic interference                                                                    |
| EMIF    | external memory interface                                                                       |
| EOC     | end of conversion                                                                               |
| EOF     | end of frame                                                                                    |
| EPSR    | execution program status register                                                               |
| ESD     | electrostatic discharge                                                                         |

**Table 55. Acronyms Used in This Document** *(continued)*

| Acronym                  | Description                                            |
|--------------------------|--------------------------------------------------------|
| ETM                      | embedded trace macrocell                               |
| FET                      | field-effect transistor                                |
| FIR                      | finite impulse response, see also IIR                  |
| FPB                      | flash patch and breakpoint                             |
| FS                       | full-speed                                             |
| GPIO                     | general-purpose input/output, applies to a PSoC pin    |
| HCI                      | host controller interface                              |
| HVI                      | high-voltage interrupt, see also LVI, LVD              |
| IC                       | integrated circuit                                     |
| IDAC                     | current DAC, see also DAC, VDAC                        |
| IDE                      | integrated development environment                     |
| I <sup>2</sup> C, or IIC | Inter-Integrated Circuit, a communications protocol    |
| I <sup>2</sup> S         | Inter-IC Sound                                         |
| IIR                      | infinite impulse response, see also FIR                |
| ILO                      | internal low-speed oscillator, see also IMO            |
| IMO                      | internal main oscillator, see also ILO                 |
| INL                      | integral nonlinearity, see also DNL                    |
| I/O                      | input/output, see also GPIO, DIO, SIO, USBIO           |
| IPOR                     | initial power-on reset                                 |
| IPSR                     | interrupt program status register                      |
| IRQ                      | interrupt request                                      |
| ITM                      | instrumentation trace macrocell                        |
| LCD                      | liquid crystal display                                 |
| LIN                      | Local Interconnect Network, a communications protocol. |
| LR                       | link register                                          |
| LUT                      | lookup table                                           |
| LVD                      | low-voltage detect, see also LVI                       |
| LVI                      | low-voltage interrupt, see also HVI                    |
| LVTTTL                   | low-voltage transistor-transistor logic                |
| MAC                      | multiply-accumulate                                    |
| MCU                      | microcontroller unit                                   |
| MISO                     | master-in slave-out                                    |
| NC                       | no connect                                             |
| NMI                      | nonmaskable interrupt                                  |
| NRZ                      | non-return-to-zero                                     |
| NVIC                     | nested vectored interrupt controller                   |

**Table 55. Acronyms Used in This Document** *(continued)*

| Acronym | Description                                                  |
|---------|--------------------------------------------------------------|
| NVL     | nonvolatile latch, see also WOL                              |
| opamp   | operational amplifier                                        |
| PAL     | programmable array logic, see also PLD                       |
| PC      | program counter                                              |
| PCB     | printed circuit board                                        |
| PGA     | programmable gain amplifier                                  |
| PHUB    | peripheral hub                                               |
| PHY     | physical layer                                               |
| PICU    | port interrupt control unit                                  |
| PLA     | programmable logic array                                     |
| PLD     | programmable logic device, see also PAL                      |
| PLL     | phase-locked loop                                            |
| PMDD    | package material declaration data sheet                      |
| POR     | power-on reset                                               |
| PRES    | precise power-on reset                                       |
| PRS     | pseudo random sequence                                       |
| PS      | port read data register                                      |
| PSoC®   | Programmable System-on-Chip™                                 |
| PSRR    | power supply rejection ratio                                 |
| PWM     | pulse-width modulator                                        |
| RAM     | random-access memory                                         |
| RISC    | reduced-instruction-set computing                            |
| RMS     | root-mean-square                                             |
| RTC     | real-time clock                                              |
| RTL     | register transfer language                                   |
| RTR     | remote transmission request                                  |
| RX      | receive                                                      |
| SAR     | successive approximation register                            |
| SC/CT   | switched capacitor/continuous time                           |
| SCL     | I <sup>2</sup> C serial clock                                |
| SDA     | I <sup>2</sup> C serial data                                 |
| S/H     | sample and hold                                              |
| SINAD   | signal to noise and distortion ratio                         |
| SIO     | special input/output, GPIO with advanced features. See GPIO. |
| SOC     | start of conversion                                          |
| SOF     | start of frame                                               |
| SPI     | Serial Peripheral Interface, a communications protocol       |
| SR      | slew rate                                                    |

**Table 55. Acronyms Used in This Document** *(continued)*

| Acronym | Description                                                            |
|---------|------------------------------------------------------------------------|
| SRAM    | static random access memory                                            |
| SRES    | software reset                                                         |
| STN     | super twisted nematic                                                  |
| SWD     | serial wire debug, a test protocol                                     |
| SWV     | single-wire viewer                                                     |
| TD      | transaction descriptor, see also DMA                                   |
| THD     | total harmonic distortion                                              |
| TIA     | transimpedance amplifier                                               |
| TN      | twisted nematic                                                        |
| TRM     | technical reference manual                                             |
| TTL     | transistor-transistor logic                                            |
| TX      | transmit                                                               |
| UART    | Universal Asynchronous Transmitter Receiver, a communications protocol |
| USB     | Universal Serial Bus                                                   |
| USBIO   | USB input/output, PSoC pins used to connect to a USB port              |
| VDAC    | voltage DAC, see also DAC, IDAC                                        |
| WDT     | watchdog timer                                                         |
| WOL     | write once latch, see also NVL                                         |
| WRES    | watchdog timer reset                                                   |
| XRES    | external reset I/O pin                                                 |
| XTAL    | crystal                                                                |

## Document Conventions

### Units of Measure

Table 56. Units of Measure

| Symbol | Unit of Measure        |
|--------|------------------------|
| °C     | degrees Celsius        |
| dB     | decibel                |
| dBm    | decibel-milliwatts     |
| fF     | femtofarads            |
| Hz     | hertz                  |
| KB     | 1024 bytes             |
| kbps   | kilobits per second    |
| Khr    | kilohour               |
| kHz    | kilohertz              |
| kΩ     | kilo ohm               |
| ksps   | kilosamples per second |
| LSB    | least significant bit  |
| Mbps   | megabits per second    |
| MHz    | megahertz              |
| MΩ     | mega-ohm               |
| Msps   | megasamples per second |
| μA     | microampere            |
| μF     | microfarad             |

Table 56. Units of Measure (continued)

| Symbol | Unit of Measure      |
|--------|----------------------|
| μH     | microhenry           |
| μs     | microsecond          |
| μV     | microvolt            |
| μW     | microwatt            |
| mA     | milliampere          |
| ms     | millisecond          |
| mV     | millivolt            |
| nA     | nanoampere           |
| ns     | nanosecond           |
| nV     | nanovolt             |
| Ω      | ohm                  |
| pF     | picofarad            |
| ppm    | parts per million    |
| ps     | picosecond           |
| s      | second               |
| sps    | samples per second   |
| sqrtHz | square root of hertz |
| V      | volt                 |
| W      | watt                 |

## Revision History

| Description Title: PRoC™ BLE: CYBL1XX7X Family Datasheet Programmable Radio-on-Chip With Bluetooth Low Energy<br>Document Number: 001-95464 |         |                 |                 |                                                |
|---------------------------------------------------------------------------------------------------------------------------------------------|---------|-----------------|-----------------|------------------------------------------------|
| Revision                                                                                                                                    | ECN     | Orig. of Change | Submission Date | Description of Change                          |
| *J                                                                                                                                          | 5438827 | DEJO            | 09/16/2016      | Release to web                                 |
| *K                                                                                                                                          | 5669710 | SGUP            | 03/27/2017      | Updated the template.<br>Added NRND watermark. |

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