Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied..... 0°C to +70°C

Maximum Junction Temperature (Under Bias)..... 150°C

Supply Voltage to Ground Potential ..... –2.0V to +7.0V

Maximum Power Dissipation..... 1500 mW

DC V_{CC} or GND Current..... 500 mA

Static Discharge Voltage (per MIL-STD-883, Method 3015)..... >2001V

DC Output Current, per Pin ..... –25 mA to +25 mA

DC Input Voltage[2] ..... –3.0V to +7.0V

DC Program Voltage ..... +13.0V

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±5%
Industrial	–40°C to +85°C	5V ±10%
Military	–55°C to +125°C (Case)	5V ±10%

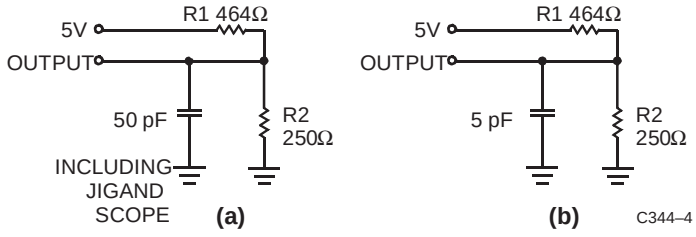
Electrical Characteristics Over the Operating Range[3]

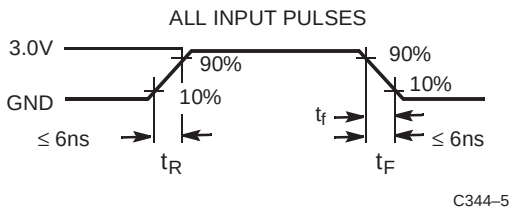
Parameter	Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –4.0 mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8 mA			0.45	V
V_{IH}	Input HIGH Level			2.2	V_{CC}+0.3	V
V_{IL}	Input LOW Level			–0.3	0.8	V
I_{IX}	Input Current	GND ≤ V_{IN} ≤ V_{CC}		–10	+10	µA
I_{OZ}	Output Leakage Current	V_O = V_{CC} or GND		–40	+40	µA
I_{OS}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.5V[4, 5]		–30	–90	mA
I_{CC1}	Power Supply Current (Standby)	V_I = V_{CC} or GND (No Load)	Commercial		150	mA
			Military/Industrial		170	mA
I_{CC2}	Power Supply Current	V_I = V_{CC} or GND (No Load) f = 1.0 MHz[4, 6]	Commercial		200	mA
			Military/Industrial		220	mA
t_R	Recommended Input Rise Time				100	ns
t_F	Recommended Input Fall Time				100	ns

Capacitance

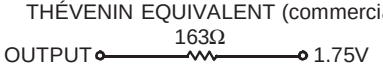
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2V, f = 1.0 MHz	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V, f = 1.0 MHz	10	pF

AC Test Loads and Waveforms[7]





Equivalent to: THÉVENIN EQUIVALENT (commercial/military)



Notes:

2. Minimum DC input is –0.3V. During transitions, the inputs may undershoot to –2.0V for periods less than 20 ns.
3. Typical values are for T_A = 25°C and V_{CC} = 5V.
4. Guaranteed by design but not 100% tested.
5. Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.
6. Measured with device programmed as a 16-bit counter.
7. Part (a) in AC Test Load and Waveforms is used for all parameters except t_{ER} and t_{XZ}, which is used for part (b) in AC Test Load and Waveforms. All external timing parameters are measured referenced to external pins of the device.

Timing Delays

Timing delays within the CY7C344/CY7C344B may be easily determined using *Warp2*®, *Warp2*Sim™, or *Warp3*® software or by the model shown in *Figure 1*. The CY7C344/CY7C344B has fixed internal delays, allowing the user to determine the worst case timing delays for any design. For complete timing information, the *Warp3* software provides a timing simulator.

Design Recommendations

Operation of the devices described herein with conditions above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this datasheet is not implied. Exposure to absolute maximum ratings conditions for extended periods of time may affect device reliability. The CY7C344/CY7C344B contains circuitry to protect device pins from high-static voltages or electric fields; however, normal precautions should be taken to avoid applying any voltage higher than maximum rated voltages.

For proper operation, input and output pins must be constrained to the range GND ≤ (VIN or VOUT) ≤ VCC. Unused inputs must always be tied to an appropriate logic level (either VCC or GND). Each set of VCC and GND pins must be connected together directly at the device. Power supply decoupling capacitors of at least 0.2 µF must be connected between VCC and GND. For the most effective decoupling, each VCC pin should be separately decoupled.

Timing Considerations

Unless otherwise stated, propagation delays do not include expanders. When using expanders, add the maximum expander delay t_{EXP} to the overall delay.

When calculating synchronous frequencies, use t_{S1} if all inputs are on the input pins. t_{S2} should be used if data is applied at an I/O pin. If t_{S2} is greater than t_{CO1}, $1/t_{S2}$ becomes the limiting frequency in the data-path mode unless $1/(t_{WH} + t_{WL})$ is less than $1/t_{S2}$.

When expander logic is used in the data path, add the appropriate maximum expander delay, t_{EXP} to t_{S1}. Determine which of $1/(t_{WH} + t_{WL})$, $1/t_{CO1}$, or $1/(t_{EXP} + t_{S1})$ is the lowest frequency. The lowest of these frequencies is the maximum data-path frequency for the synchronous configuration.

When calculating external asynchronous frequencies, use t_{AS1} if all inputs are on dedicated input pins. If any data is applied to an I/O pin, t_{AS2} must be used as the required set-up time. If $(t_{AS2} + t_{AH})$ is greater than t_{ACO1}, $1/(t_{AS2} + t_{AH})$ becomes the limiting frequency in the data-path mode unless $1/(t_{AWH} + t_{AWL})$ is less than $1/(t_{AS2} + t_{AH})$.

When expander logic is used in the data path, add the appropriate maximum expander delay, t_{EXP} to t_{AS1}. Determine which of $1/(t_{AWH} + t_{AWL})$, $1/t_{ACO1}$, or $1/(t_{EXP} + t_{AS1})$ is the lowest frequency. The lowest of these frequencies is the maximum data-path frequency for the asynchronous configuration.

The parameter t_{OH} indicates the system compatibility of this device when driving other synchronous logic with positive input hold times, which is controlled by the same synchronous clock. If t_{OH} is greater than the minimum required input hold time of the subsequent synchronous logic, then the devices are guaranteed to function properly with a common synchronous clock under worst-case environmental and supply voltage conditions.

The parameter t_{AOH} indicates the system compatibility of this device when driving subsequent registered logic with a positive hold time and using the same clock as the CY7C344/CY7C344B.In general, if t_{AOH} is greater than the minimum required input hold time of the subsequent logic (synchronous or asynchronous), then the devices are guaranteed to function properly under worst-case environmental and supply voltage conditions, provided the clock signal source is the same. This also applies if expander logic is used in the clock signal path of the driving device, but not for the driven device. This is due to the expander logic in the second device's clock signal path adding an additional delay (t_{EXP}), causing the output data from the preceding device to change prior to the arrival of the clock signal at the following device's register.

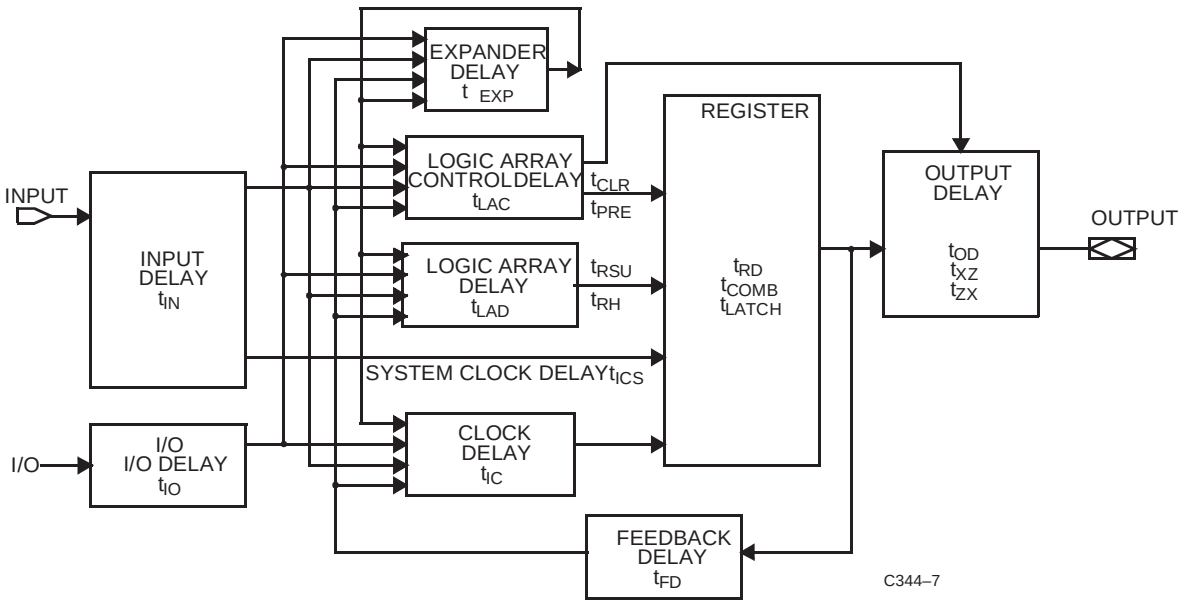


Figure 1. CY7C344/CY7C344B Timing Model

External Synchronous Switching Characteristics[7] Over Operating Range

Parameter	Description		7C344B–10		7C344B–12		7C344–15 7C344B–15		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD1}	Dedicated Input to Combinatorial Output Delay[8]	Com'l /Ind		10		12		15	ns
		Mil				12		15	
t_{PD2}	I/O Input to Combinatorial Output Delay[9]	Com'l/Ind		10		12		15	ns
		Mil				12		15	
t_{PD3}	Dedicated Input to Combinatorial Output Delay with Expander Delay[10]	Com'l /Ind		16		18		30	ns
		Mil				18		30	
t_{PD4}	I/O Input to Combinatorial Output Delay with Expander Delay[4, 11]	Com'l/Ind		16		18		30	ns
		Mil				18		30	
t_{EA}	Input to Output Enable Delay[4]	Com'l/Ind		10		12		20	ns
		Mil				12		20	
t_{ER}	Input to Output Disable Delay[4]	Com'l /Ind		10		12		20	ns
		Mil				12		20	
t_{CO1}	Synchronous Clock Input to Output Delay	Com'l /Ind		5		6		10	ns
		Mil				6		10	
t_{CO2}	Synchronous Clock to Local Feedback to Combinatorial Output[4, 12]	Com'l /Ind		10		12		20	ns
		Mil				12		20	
t_S	Dedicated Input or Feedback Set-Up Time to Synchronous Clock Input	Com'l/Ind	6		8		10		ns
		Mil			8		10		
t_H	Input Hold Time from Synchronous Clock Input[7]	Com'l /Ind	0		0		0		ns
		Mil			0		0		
t_{WH}	Synchronous Clock Input HIGH Time[4]	Com'l/Ind	4		4.5		6		ns
		Mil			4.5		6		
t_{WL}	Synchronous Clock Input LOW Time[4]	Com'l /Ind	4		4.5		6		ns
		Mil			4.5		6		
t_{RW}	Asynchronous Clear Width[4]	Com'l /Ind	10		12		20		ns
		Mil			12		20		
t_{RR}	Asynchronous Clear Recovery Time[4]	Com'l /Ind	10		12		20		ns
		Mil			12		20		
t_{RO}	Asynchronous Clear to Registered Output Delay[4]	Com'l /Ind		10		12		15	ns
		Mil				12		15	
t_{PW}	Asynchronous Preset Width[4]	Com'l /Ind	10		12		20		ns
		Mil			12		20		
t_{PR}	Asynchronous Preset Recovery Time[4]	Com'l /Ind	10		12		20		ns
		Mil			12		20		
t_{PO}	Asynchronous Preset to Registered Output Delay[4]	Com'l /Ind		10		12		15	ns
		Mil				12		15	
t_{CF}	Synchronous Clock to Local Feedback Input[4, 13]	Com'l /Ind		3		3		4	ns
		Mil				3		4	
t_P	External Synchronous Clock Period ($1/f_{MAX3}$)[4]	Com'l/Ind	8		9		13		ns
		Mil			9		13		
f_{MAX1}	External Maximum Frequency($1/(t_{CO1}+t_S)$)[4, 14]	Com'l/Ind	90.9		71.4		50.0		MHz
		Mil			71.4		50.0		

Shaded area contains preliminary information.

External Synchronous Switching Characteristics[7] Over Operating Range (continued)

Parameter	Description		7C344B–10		7C344B–12		7C344–15 7C344B–15		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
f_{MAX2}	Maximum Frequency with Internal Only Feedback $(1/(t_{CF} + t_S))$[4, 15]	Com'l/Ind	111.1		90.9		71.4		MHz
		Mil			90.9		71.4		
f_{MAX3}	Data Path Maximum Frequency, least of $1/(t_{WL} + t_{WH})$, $1/(t_S + t_H)$, or $(1/t_{CO1})$[4, 16]	Com'l/Ind	125.0		111.1		83.3		MHz
		Mil			111.1		83.3		
f_{MAX4}	Maximum Register Toggle Frequency $1/(t_{WL} + t_{WH})$[4, 17]	Com'l/Ind	125.0		111.1		83.3		MHz
		Mil			111.1		83.3		
t_{OH}	Output Data Stable Time from Synchronous Clock Input[4, 18]	Com'l/ Ind	3		3		3		ns
		Mil			3		3		

Shaded area contains preliminary information.

Notes:

8. This parameter is the delay from an input signal applied to a dedicated input pin to a combinatorial output on any output pin. This delay assumes no expander terms are used to form the logic function.
9. This parameter is the delay associated with an input signal applied to an I/O macrocell pin to any output. This delay assumes no expander terms are used to form the logic function.
10. This parameter is the delay associated with an input signal applied to a dedicated input pin to combinatorial output on any output pin. This delay assumes expander terms are used to form the logic function and includes the worst-case expander logic delay for one pass through the expander logic. This parameter is tested periodically by sampling production material.
11. This parameter is the delay associated with an input signal applied to an I/O macrocell pin to any output pin. This delay assumes expander terms are used to form the logic function and includes the worst-case expander logic delay for one pass through the expander logic. This parameter is tested periodically by sampling production material.
12. This specification is a measure of the delay from synchronous register clock input to internal feedback of the register output signal to a combinatorial output for which the registered output signal is used as an input. This parameter assumes no expanders are used in the logic of the combinatorial output and the register is synchronously clocked. This parameter is tested periodically by sampling production material.
13. This specification is a measure of the delay associated with the internal register feedback path. This delay plus the register set-up time, t_S, is the minimum internal period for an internal state machine configuration. This parameter is tested periodically by sampling production material.
14. This specification indicates the guaranteed maximum frequency at which a state machine configuration with external only feedback can operate.
15. This specification indicates the guaranteed maximum frequency at which a state machine with internal-only feedback can operate. If register output states must also control external points, this frequency can still be observed as long as it is less than $1/t_{CO1}$. This specification assumes no expander logic is used. This parameter is tested periodically by sampling production material.
16. This frequency indicates the maximum frequency at which the device may operate in data-path mode (dedicated input pin to output pin). This assumes that no expander logic is used.
17. This specification indicates the guaranteed maximum frequency in synchronous mode, at which an individual output or buried register can be cycled by a clock signal applied to either a dedicated input pin or an I/O pin.
18. This parameter indicates the minimum time after a synchronous register clock input that the previous register output data is maintained on the output pin.

External Synchronous Switching Characteristics[7] Over Operating Range (continued)

Parameter	Description		7C344–20 7C344B–20		7C344–25 7C344B–25		Unit
			Min.	Max.	Min.	Max.	
t_{PD1}	Dedicated Input to Combinatorial Output Delay[8]	Com'l /Ind		20		25	ns
		Mil		20		25	
t_{PD2}	I/O Input to Combinatorial Output Delay[9]	Com'l/Ind		20		25	ns
		Mil		20		25	
t_{PD3}	Dedicated Input to Combinatorial Output Delay with Expander Delay[10]	Com'l /Ind		30		40	ns
		Mil		30		40	
t_{PD4}	I/O Input to Combinatorial Output Delay with Expander Delay[4, 11]	Com'l/Ind		30		40	ns
		Mil		30		40	
t_{EA}	Input to Output Enable Delay[4]	Com'l/Ind		20		25	ns
		Mil		20		25	
t_{ER}	Input to Output Disable Delay[4]	Com'l /Ind		20		25	ns
		Mil		20		25	
t_{CO1}	Synchronous Clock Input to Output Delay	Com'l /Ind		12		15	ns
		Mil		12		15	
t_{CO2}	Synchronous Clock to Local Feedback to Combinatorial Output[4, 12]	Com'l /Ind		22		29	ns
		Mil		22		29	
t_S	Dedicated Input or Feedback Set-Up Time to Synchronous Clock Input	Com'l/Ind	12		15		ns
		Mil	12		15		
t_H	Input Hold Time from Synchronous Clock Input[7]	Com'l /Ind	0		0		ns
		Mil	0		0		
t_{WH}	Synchronous Clock Input HIGH Time[4]	Com'l/Ind	7		8		ns
		Mil	7		8		
t_{WL}	Synchronous Clock Input LOW Time[4]	Com'l /Ind	7		8		ns
		Mil	7		8		
t_{RW}	Asynchronous Clear Width[4]	Com'l /Ind	20		25		ns
		Mil	20		25		
t_{RR}	Asynchronous Clear Recovery Time[4]	Com'l /Ind	20		25		ns
		Mil	20		25		
t_{RO}	Asynchronous Clear to Registered Output Delay[4]	Com'l /Ind		20		25	ns
		Mil		20		25	
t_{PW}	Asynchronous Preset Width[4]	Com'l /Ind	20		25		ns
		Mil	20		25		
t_{PR}	Asynchronous Preset Recovery Time[4]	Com'l /Ind	20		25		ns
		Mil	20		25		
t_{PO}	Asynchronous Preset to Registered Output Delay[4]	Com'l /Ind		20		25	ns
		Mil		20		25	
t_{CF}	Synchronous Clock to Local Feedback Input[4, 13]	Com'l /Ind		4		7	ns
		Mil		4		7	
t_P	External Synchronous Clock Period ($1/f_{MAX3}$)[4]	Com'l/Ind	14		16		ns
		Mil	14		16		

External Synchronous Switching Characteristics[7] Over Operating Range (continued)

Parameter	Description		7C344–20 7C344B–20 Min.	7C344–20 7C344B–20 Max.	7C344–25 7C344B–25 Min.	7C344–25 7C344B–25 Max.	Unit
f_{MAX1}	External Maximum Frequency$(1/(t_{CO1}+t_S))$[4, 14]	Com'l/Ind	41.6		33.3		MHz
		Mil	41.6		33.3		
f_{MAX2}	Maximum Frequency with Internal Only Feedback $(1/(t_{CF}+t_S))$[4, 15]	Com'l/Ind	62.5		45.4		MHz
		Mil	62.5		45.4		
f_{MAX3}	Data Path Maximum Frequency, least of $1/(t_{WL}+t_{WH})$, $1/(t_S+t_H)$, or $(1/t_{CO1})$[4, 16]	Com'l/Ind	71.4		62.5		MHz
		Mil	71.4		62.5		
f_{MAX4}	Maximum Register Toggle Frequency $1/(t_{WL}+t_{WH})$[4, 17]	Com'l/Ind	71.4		62.5		MHz
		Mil	71.4		62.5		
t_{OH}	Output Data Stable Time from Synchronous Clock Input[4, 18]	Com'l/ Ind	3		3		ns
		Mil	3		3		

External Asynchronous Switching Characteristics Over Operating Range[7]

Parameter	Description		7C344B–10 Min.	7C344B–10 Max.	7C344B–12 Min.	7C344B–12 Max.	7C344–15 7C344B–15 Min.	7C344–15 7C344B–15 Max.	Unit
t_{ACO1}	Asynchronous Clock Input to Output Delay	Com'l/ Ind		10		12		15	ns
		Mil				12		15	
t_{ACO2}	Asynchronous Clock Input to Local Feedback to Combinatorial Output[19]	Com'l/Ind		15		18		30	ns
		Mil				18		30	
t_{AS}	Dedicated Input or Feedback Set-Up Time to Asynchronous Clock Input	Com'l/Ind	4		4		7		ns
		Mil			4		7		
t_{AH}	Input Hold Time from Asynchronous Clock Input	Com'l/Ind	3		4		7		ns
		Mil			4		7		
t_{AWH}	Asynchronous Clock Input HIGH Time[4, 20]	Com'l/Ind	4		5		6		ns
		Mil			5		6		
t_{AWL}	Asynchronous Clock Input LOW Time[4]	Com'l/Ind	5		6		7		ns
		Mil			6		7		
t_{ACF}	Asynchronous Clock to Local Feedback Input[4, 21]	Com'l /Ind		7		9		18	ns
		Mil				9		18	
t_{AP}	External Asynchronous Clock Period $(1/f_{MAX4})$[4]	Com'l/Ind	12		12.5		13		ns
		Mil			12.5		13		
f_{MAXA1}	External Maximum Frequency in Asynchronous Mode $1/(t_{ACO1}+t_{AS})$[4, 22]	Com'l/Ind	71.4		62.5		45.4		MHz
		Mil			62.5		45.4		
f_{MAXA2}	Maximum Internal Asynchronous Frequency $1/(t_{ACF}+t_{AS})$ or $1/(t_{AWH}+t_{AWL})$[4, 23]	Com'l/Ind	90.9		76.9		40		MHz
		Mil			76.9		40		
f_{MAXA3}	Data Path Maximum Frequency in Asynchronous Mode[4, 24]	Com'l/Ind	100.0		83.3		66.6		MHz
		Mil			83.3		66.6		
f_{MAXA4}	Maximum Asynchronous Register Toggle Frequency $1/(t_{AWH}+t_{AWL})$[4, 25]	Com'l /Ind	111.1		90.9		76.9		MHz
		Mil			90.9		76.9		
t_{AOH}	Output Data Stable Time from Asynchronous Clock Input[4, 26]	Com'l/Ind	12		12		15		ns
		Mil					15		

Shaded area contains preliminary information.

External Asynchronous Switching Characteristics Over Operating Range[7] (continued)

Parameter	Description		7C344–20 7C344B–20 Min.	7C344–20 7C344B–20 Max.	7C344–25 7C344B–25 Min.	7C344–25 7C344B–25 Max.	Unit
t_{ACO1}	Asynchronous Clock Input to Output Delay	Com'l/ Ind		20		25	ns
		Mil		20		25	
t_{ACO2}	Asynchronous Clock Input to Local Feedback to Combinatorial Output[19]	Com'l/Ind		30		37	ns
		Mil		30		37	
t_{AS}	Dedicated Input or Feedback Set-Up Time to Asynchronous Clock Input	Com'l/Ind	9		12		ns
		Mil	9		12		
t_{AH}	Input Hold Time from Asynchronous Clock Input	Com'l/Ind	9		12		ns
		Mil	9		12		
t_{AWH}	Asynchronous Clock Input HIGH Time[4, 20]	Com'l/Ind	7		9		ns
		Mil	7		9		
t_{AWL}	Asynchronous Clock Input LOW Time[4]	Com'l/Ind	9		11		ns
		Mil	9		11		
t_{ACF}	Asynchronous Clock to Local Feedback Input[4, 21]	Com'l /Ind		18		21	ns
		Mil		18		21	
t_{AP}	External Asynchronous Clock Period ($1/f_{MAX4}$)[4]	Com'l/Ind	16		20		ns
		Mil	16		20		
f_{MAXA1}	External Maximum Frequency in Asynchronous Mode $1/(t_{ACO1} + t_{AS})$[4, 22]	Com'l/Ind	34.4		27		MHz
		Mil	34.4		27		
f_{MAXA2}	Maximum Internal Asynchronous Frequency $1/(t_{ACF} + t_{AS})$ or $1/(t_{AWH} + t_{AWL})$[4, 23]	Com'l/Ind	37		30.3		MHz
		Mil	37		30.3		
f_{MAXA3}	Data Path Maximum Frequency in Asynchronous Mode[4, 23]	Com'l/Ind	50		40		MHz
		Mil	50		40		
f_{MAXA4}	Maximum Asynchronous Register Toggle Frequency $1/(t_{AWH} + t_{AWL})$[4, 25]	Com'l /Ind	62.5		50		MHz
		Mil	62.5		50		
t_{AOH}	Output Data Stable Time from Asynchronous Clock Input[4, 26]	Com'l/Ind	15		15		ns
		Mil	15		15		

Notes:

19. This specification is a measure of the delay from an asynchronous register clock input to internal feedback of the registered output signal to a combinatorial output for which the registered output signal is used as an input. Assumes no expanders are used in logic of combinatorial output or the asynchronous clock input. This parameter is tested periodically by sampling production material.
20. This parameter is measured with a positive-edge-triggered clock at the register. For negative edge triggering, the t_{AWH} and t_{AWL} parameters must be swapped. If a given input is used to clock multiple registers with both positive and negative polarity, t_{AWH} should be used for both t_{AWH} and t_{AWL}.
21. This specification is a measure of the delay associated with the internal register feedback path for an asynchronously clocked register. This delay plus the asynchronous register set-up time, t_{AS}, is the minimum internal period for an asynchronously clocked state machine configuration. This delay assumes no expander logic in the asynchronous clock path. This parameter is tested periodically by sampling production material.
22. This parameter indicates the guaranteed maximum frequency at which an asynchronously clocked state machine configuration with external feedback can operate. It is assumed that no expander logic is employed in the clock signal path or data path.
23. This specification indicates the guaranteed maximum frequency at which an asynchronously clocked state machine with internal-only feedback can operate. If register output states must also control external points, this frequency can still be observed as long as this frequency is less than $1/t_{ACO1}$. This specification assumes no expander logic is utilized. This parameter is tested periodically by sampling production material.
24. This specification indicates the guaranteed maximum frequency at which an individual output or buried register can be cycled in asynchronously clocked mode. This frequency is least of $1/(t_{AWH} + t_{AWL})$, $1/(t_{AS} + t_{AH})$, or $1/t_{ACO1}$. It also indicates the maximum frequency at which the device may operate in the asynchronously clocked data-path mode. Assumes no expander logic is used.
25. This specification indicates the guaranteed maximum frequency at which an individual output or buried register can be cycled in asynchronously clocked mode by a clock signal applied to an external dedicated input or an I/O pin.
26. This parameter indicates the minimum time that the previous register output data is maintained on the output pin after an asynchronous register clock input to an external dedicated input or I/O pin.

Typical Internal Switching Characteristics Over Operating Range[7]

Parameter	Description		7C344B–10		7C344B–12		7C344–15 7C344B–15		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{IN}	Dedicated Input Pad and Buffer Delay	Com'l/Ind		2		2.5		4	ns
		Mil				2.5		4	
t_{IO}	I/O Input Pad and Buffer Delay	Com'l/Ind		2		2.5		4	ns
		Mil				2.5		4	
t_{EXP}	Expander Array Delay	Com'l/Ind		6		6		8	ns
		Mil				6		8	
t_{LAD}	Logic Array Data Delay	Com'l/Ind		5		6		7	ns
		Mil				6		7	
t_{LAC}	Logic Array Control Delay	Com'l/Ind		5		5		5	ns
		Mil				5		5	
t_{OD}	Output Buffer and Pad Delay	Com'l/Ind		3		3		4	ns
		Mil				3		4	
t_{ZX}	Output Buffer Enable Delay[27]	Com'l /Ind		5		5		7	ns
		Mil				5		7	
t_{XZ}	Output Buffer Disable Delay	Com'l/Ind		5		5		7	ns
		Mil				5		7	
t_{RSU}	Register Set-Up Time Relative to Clock Signal at Register	Com'l/Ind	2		2		5		ns
		Mil			2		5		
t_{RH}	Register Hold Time Relative to Clock Signal at Register	Com'l/Ind	4		5		7		ns
		Mil			5		7		
t_{LATCH}	Flow-Through Latch Delay	Com'l/Ind		0.5		0.5		1	ns
		Mil				0.5		1	
t_{RD}	Register Delay	Com'l/Ind		0.5		0.5		1	ns
		Mil				0.5		1	
t_{COMB}	Transparent Mode Delay[28]	Com'l/Ind		0.5		0.5		1	ns
		Mil				0.5		1	
t_{CH}	Clock HIGH Time	Com'l/Ind	3		4		6		ns
		Mil			4		6		
t_{CL}	Clock LOW Time	Com'l/Ind	3		4		6		ns
		Mil			4		6		
t_{IC}	Asynchronous Clock Logic Delay	Com'l/Ind		5		6		7	ns
		Mil				6		7	
t_{ICS}	Synchronous Clock Delay	Com'l/Ind		0.5		0.5		1	ns
		Mil				0.5		1	
t_{FD}	Feedback Delay	Com'l/Ind		1		1		1	ns
		Mil				1		1	
t_{PRE}	Asynchronous Register Preset Time	Com'l/Ind		2		3		5	ns
		Mil				3		5	
t_{CLR}	Asynchronous Register Clear Time	Com'l/Ind		2		3		5	ns
		Mil				3		5	
t_{PCW}	Asynchronous Preset and Clear Pulse Width	Com'l/Ind	2		3		5		ns
		Mil			3		5		
t_{PCR}	Asynchronous Preset and Clear Recovery Time	Com'l/Ind	2		3		5		ns
		Mil			3		5		

Shaded area contains preliminary information.

Notes:

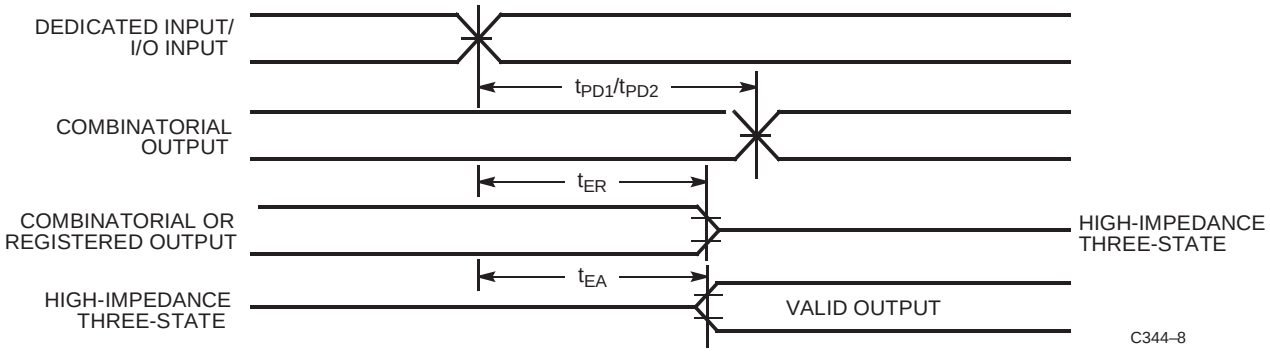
27. Sample tested only for an output change of 500 mV.
28. This specification guarantees the maximum combinatorial delay associated with the macrocell register bypass when the macrocell is configured for combinatorial operation.

Typical Internal Switching Characteristics Over Operating Range[7] (continued)

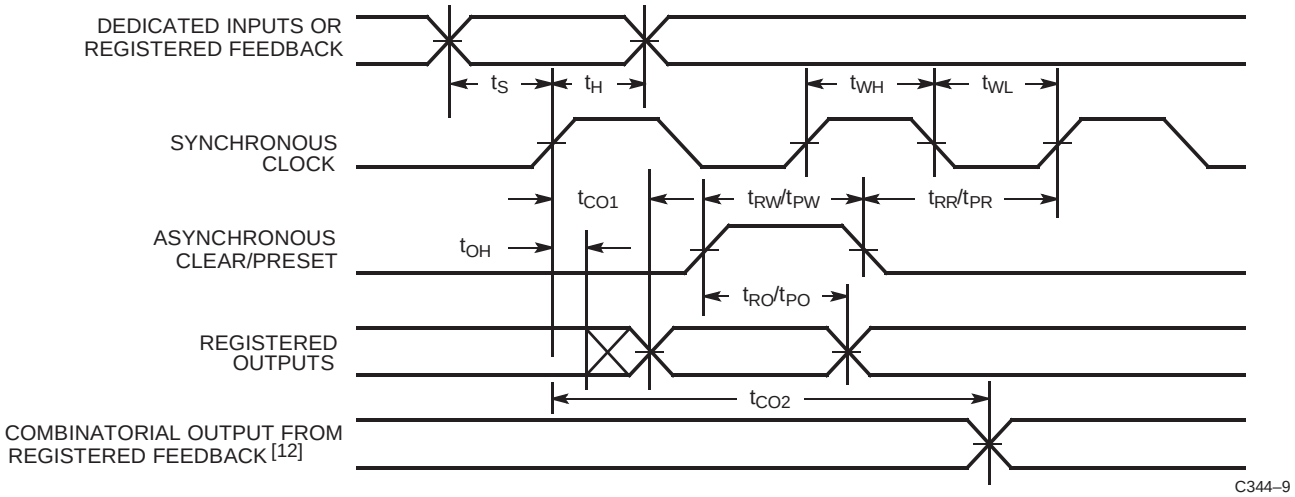
Parameter	Description		7C344–20 7C344B–20		7C344–25 7C344B–25		Unit
			Min.	Max.	Min.	Max.	
t_{IN}	Dedicated Input Pad and Buffer Delay	Com'l/Ind		5		7	ns
		Mil		5		7	
t_{IO}	I/O Input Pad and Buffer Delay	Com'l/Ind		5		7	ns
		Mil		5		7	
t_{EXP}	Expander Array Delay	Com'l/Ind		10		15	ns
		Mil		10		15	
t_{LAD}	Logic Array Data Delay	Com'l/Ind		9		10	ns
		Mil		9		10	
t_{LAC}	Logic Array Control Delay	Com'l/Ind		7		7	ns
		Mil		7		7	
t_{OD}	Output Buffer and Pad Delay	Com'l/Ind		5		5	ns
		Mil		5		5	
t_{ZX}	Output Buffer Enable Delay[27]	Com'l /Ind		8		11	ns
		Mil		8		11	
t_{XZ}	Output Buffer Disable Delay	Com'l/Ind		8		11	ns
		Mil		8		11	
t_{RSU}	Register Set-Up Time Relative to Clock Signal at Register	Com'l/Ind	5		8		ns
		Mil	5		8		
t_{RH}	Register Hold Time Relative to Clock Signal at Register	Com'l/Ind	9		12		ns
		Mil	9		12		
t_{LATCH}	Flow-Through Latch Delay	Com'l/Ind		1		3	ns
		Mil		1		3	
t_{RD}	Register Delay	Com'l/Ind		1		1	ns
		Mil		1		1	
t_{COMB}	Transparent Mode Delay[28]	Com'l/Ind		1		3	ns
		Mil		1		3	
t_{CH}	Clock HIGH Time	Com'l/Ind	7		8		ns
		Mil	7		8		
t_{CL}	Clock LOW Time	Com'l/Ind	7		8		ns
		Mil	7		8		
t_{IC}	Asynchronous Clock Logic Delay	Com'l/Ind		8		10	ns
		Mil		8		10	
t_{ICS}	Synchronous Clock Delay	Com'l/Ind		2		3	ns
		Mil		2		3	
t_{FD}	Feedback Delay	Com'l/Ind		1		1	ns
		Mil		1		1	
t_{PRE}	Asynchronous Register Preset Time	Com'l/Ind		6		9	ns
		Mil		6		9	
t_{CLR}	Asynchronous Register Clear Time	Com'l/Ind		6		9	ns
		Mil		6		9	
t_{PCW}	Asynchronous Preset and Clear Pulse Width	Com'l/Ind	5		7		ns
		Mil	5		7		
t_{PCR}	Asynchronous Preset and Clear Recovery Time	Com'l/Ind	5		7		ns
		Mil	5		7		

Switching Waveforms

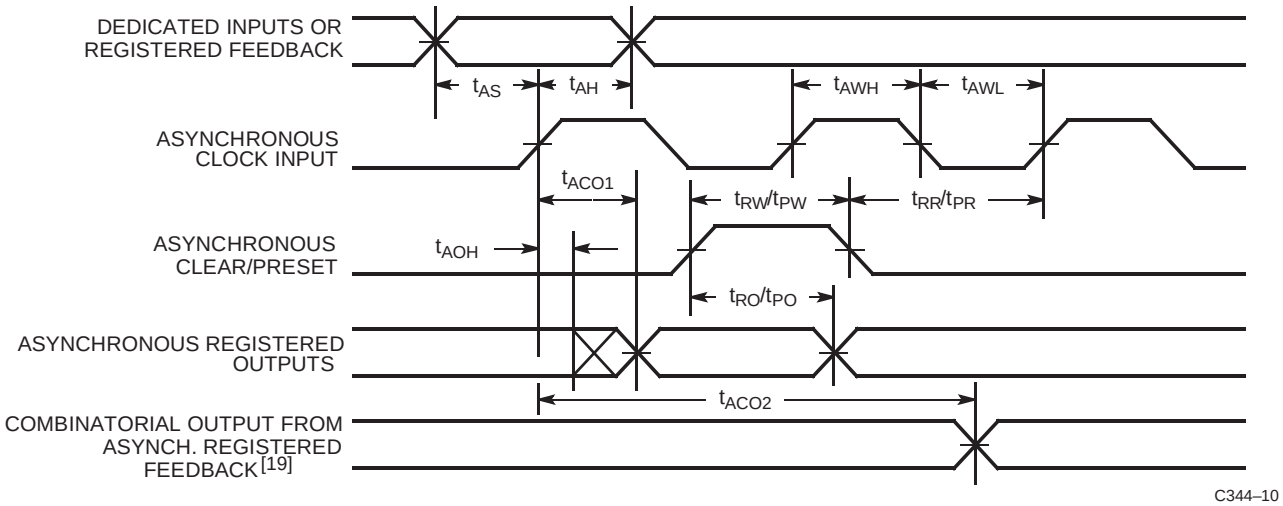
External Combinatorial



External Synchronous

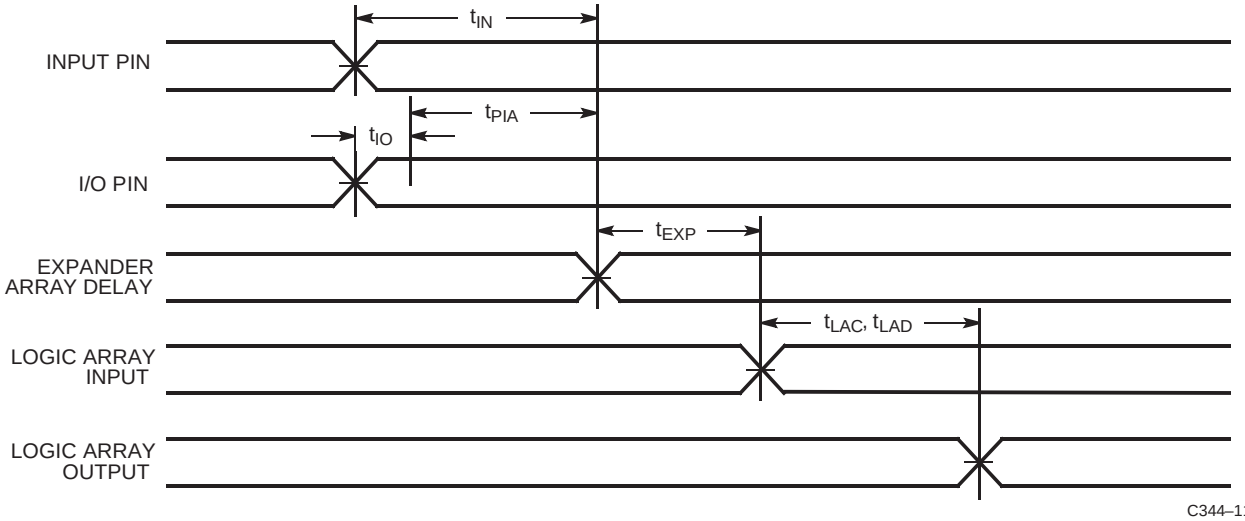


External Asynchronous



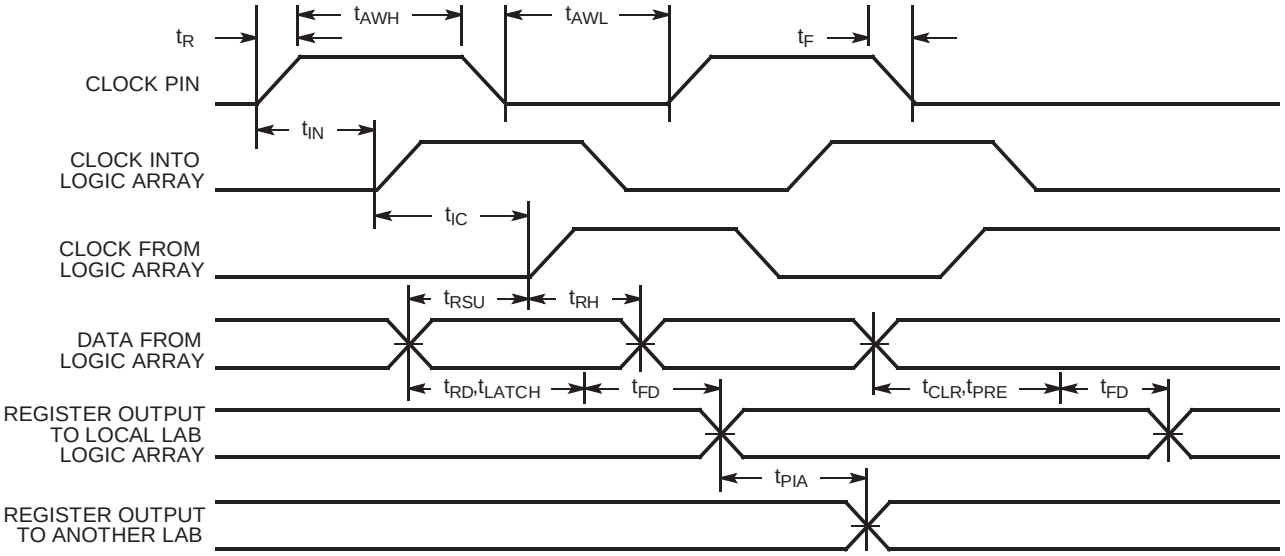
Switching Waveforms (Continued)

Internal Combinatorial



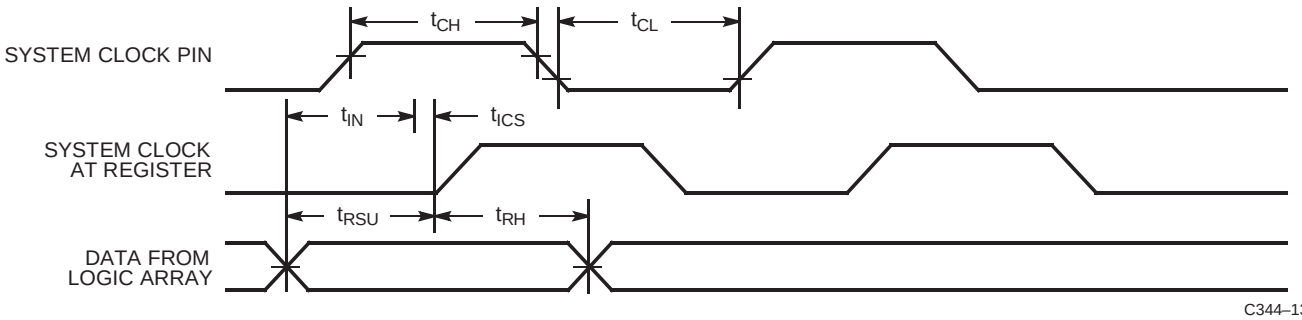
C344–11

Internal Asynchronous



C344–12

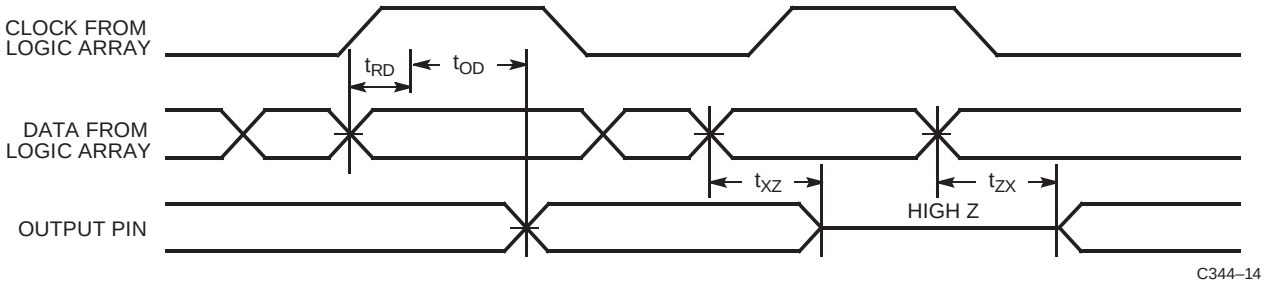
Internal Synchronous (Input Path)



C344–13

Switching Waveforms (Continued)

Internal Synchronous (Output Path)



C344–14

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C344B–10HC	H64	28-Lead Windowed Leaded Chip Carrier	Commercial
	CY7C344B–10JC	J64	28-Lead Plastic Leaded Chip Carrier	
	CY7C344B–10PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C344B–10WC	W22	28-Lead Windowed CerDIP	
12	CY7C344B–12HC/HI	H64	28-Lead Windowed Leaded Chip Carrier	Commercial/Industrial
	CY7C344B–12JC/JI	J64	28-Lead Plastic Leaded Chip Carrier	
	CY7C344B–12PC/PI	P21	28-Lead (300-Mil) Molded DIP	
	CY7C344B–12WC/WI	W22	28-Lead Windowed CerDIP	
	CY7C344B–12HMB	H64	28-Lead Windowed Leaded Chip Carrier	Military
	CY7C344B–12WMB	W22	28-Lead Windowed CerDIP	
15	CY7C344–15HC/HI	H64	28-Lead Windowed Leaded Chip Carrier	Commercial/Industrial
	CY7C344–15JC/JI	J64	28-Lead Plastic Leaded Chip Carrier	
	CY7C344–15PC/PI	P21	28-Lead (300-Mil) Molded DIP	
	CY7C344–15WC/WI	W22	28-Lead Windowed CerDIP	
	CY7C344B–15HC/HI	H64	28-Lead Windowed Leaded Chip Carrier	
	CY7C344B–15JC/JI	J64	28-Lead Plastic Leaded Chip Carrier	
	CY7C344B–15PC/PI	P21	28-Lead (300-Mil) Molded DIP	
	CY7C344B–15WC/WI	W22	28-Lead Windowed CerDIP	
	CY7C344B–15HMB	H64	28-Lead Windowed Leaded Chip Carrier	Military
	CY7C344B–15WMB	W22	28-Lead Windowed CerDIP	
20	CY7C344–20HC/HI	H64	28-Lead Windowed Leaded Chip Carrier	Commercial/Industrial
	CY7C344–20JC/JI	J64	28-Lead Plastic Leaded Chip Carrier	
	CY7C344–20PC/PI	P21	28-Lead (300-Mil) Molded DIP	
	CY7C344–20WC/WI	W22	28-Lead Windowed CerDIP	
	CY7C344B–20HC/HI	H64	28-Lead Windowed Leaded Chip Carrier	
	CY7C344B–20JC/JI	J64	28-Lead Plastic Leaded Chip Carrier	
	CY7C344B–20PC/PI	P21	28-Lead (300-Mil) Molded DIP	
	CY7C344B–20WC/WI	W22	28-Lead Windowed CerDIP	
	CY7C344–20HMB	H64	28-Lead Windowed Leaded Chip Carrier	Military
	CY7C344–20WMB	W22	28-Lead Windowed CerDIP	
	CY7C344B–20HMB	H64	28-Lead Windowed Leaded Chip Carrier	
	CY7C344B–20WMB	W22	28-Lead Windowed CerDIP	

Shaded area contains preliminary information.

Ordering Information (continued)

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
25	CY7C344–25HC/HI	H64	28-Lead Windowed Leaded Chip Carrier	Commercial/Industrial
	CY7C344–25JC/JI	J64	28-Lead Plastic Leaded Chip Carrier	
	CY7C344–25PC/PI	P21	28-Lead (300-Mil) Molded DIP	
	CY7C344–25WC/WI	W22	28-Lead Windowed CerDIP	
	CY7C344B–25HC/HI	H64	28-Lead Windowed Leaded Chip Carrier	
	CY7C344B–25JC/JI	J64	28-Lead Plastic Leaded Chip Carrier	
	CY7C344B–25PC/PI	P21	28-Lead (300-Mil) Molded DIP	
	CY7C344B–25WC/WI	W22	28-Lead Windowed CerDIP	
	CY7C344–25HMB	H64	28-Lead Windowed Leaded Chip Carrier	Military
	CY7C344–25WMB	W22	28-Lead Windowed CerDIP	
	CY7C344B–25HMB	H64	28-Lead Windowed Leaded Chip Carrier	
	CY7C344B–25WMB	W22	28-Lead Windowed CerDIP	

Shaded area contains preliminary information.

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC1}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t_{PD1}	7, 8, 9, 10, 11
t_{PD2}	7, 8, 9, 10, 11
t_{PD3}	7, 8, 9, 10, 11
t_{CO1}	7, 8, 9, 10, 11
t_{S}	7, 8, 9, 10, 11
t_{H}	7, 8, 9, 10, 11
t_{ACO1}	7, 8, 9, 10, 11
t_{ACO1}	7, 8, 9, 10, 11
t_{AS}	7, 8, 9, 10, 11
t_{AH}	7, 8, 9, 10, 11

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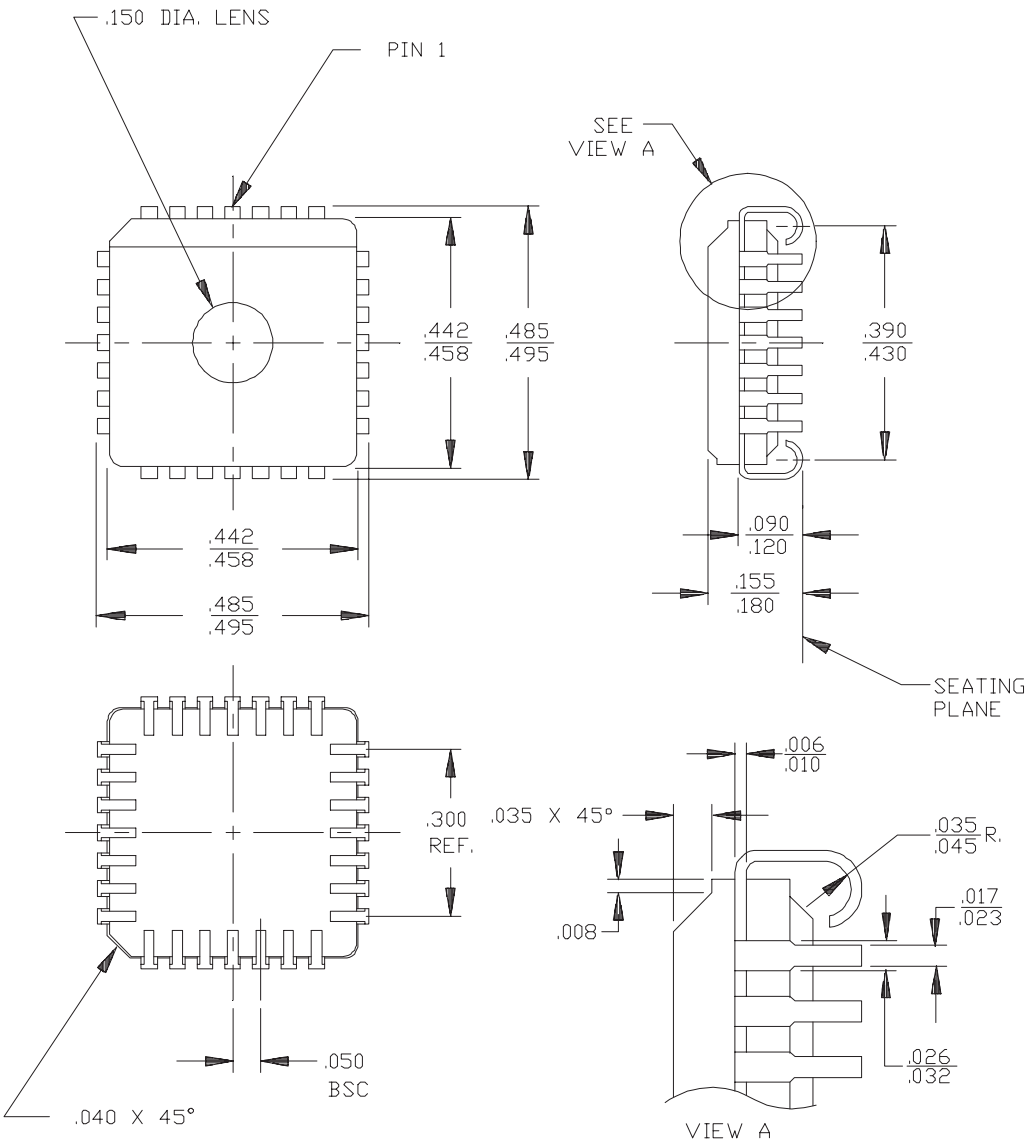
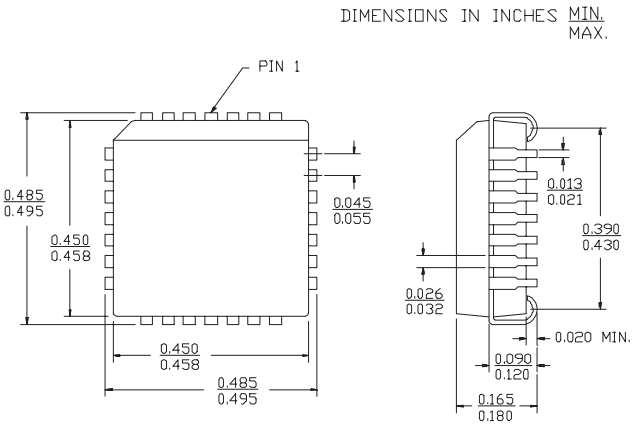
Package Diagrams

28-Pin Windowed Leaded Chip Carrier H64

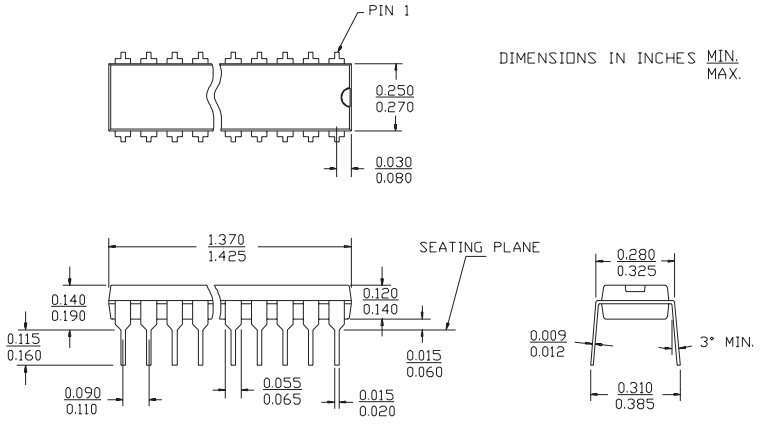


Package Diagrams (Continued)

28-Lead Plastic Leaded Chip Carrier J64



28-Lead (300-Mil) Molded DIP P21



Package Diagrams (Continued)

28-Lead (300-Mil) Windowed CerDIP W22
MIL–STD–1835 D– 15Config.A