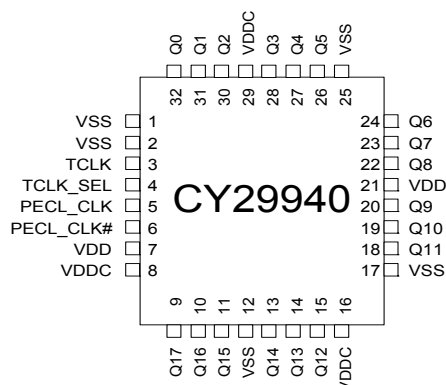


## Pin Configuration



## Pin Description

| Pin   | Name      | PWR  | I/O [1] | Description  |
|---|-----------|------|---------|--|
| 5   | PECL_CLK  |      | I, PU   | PECL input clock   |
| 6   | PECL_CLK# |      | I, PD   | PECL input clock   |
| 3   | TCLK      |      | I, PD   | External reference/test clock input  |
| 9, 10, 11, 13, 14, 15, 18, 19, 20, 22, 23, 24, 26, 27, 28, 30, 31, 32 | Q(17:0)   | VDDC | O       | Clock outputs  |
| 4   | TCLK_SEL  |      | I, PD   | Clock Select Input. When LOW, PECL clock is selected and when HIGH TCLK is selected. |
| 8, 16, 29   | VDDC      |      |         | 3.3 V or 2.5 V power supply for output clock buffers                                 |
| 7, 21   | VDD       |      |         | 3.3 V or 2.5 V power supply  |
| 1, 2, 12, 17, 25  | VSS       |      |         | Common ground  |

### Note

1. PD = Internal Pull-Down, PU = Internal Pull-up

## Maximum Ratings

Exceeding the maximum ratings<sup>[2]</sup> may impair the useful life of the device. User guidelines are not tested.

Maximum input voltage relative to  $V_{SS}$  .....  $V_{SS} - 0.3 \text{ V}$

Maximum input voltage relative to  $V_{DD}$  .....  $V_{DD} + 0.3 \text{ V}$

Storage temperature .....  $-65^\circ\text{C}$  to  $+150^\circ\text{C}$

Operating temperature .....  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$

Maximum ESD protection ..... 2 kV

Maximum power supply ..... 5.5 V

Maximum input current .....  $\pm 20 \text{ mA}$

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range:

$$V_{SS} < (V_{in} \text{ or } V_{out}) < V_{DD}$$

Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{SS}$  or  $V_{DD}$ ).

## DC Parameters

$V_{DD} = 3.3 \text{ V} \pm 5\%$  or  $2.5 \text{ V} \pm 5\%$ ,  $V_{DDC} = 3.3 \text{ V} \pm 5\%$  or  $2.5 \text{ V} \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$

| Parameter <sup>[2]</sup> | Description                                  | Conditions   | Min            | Typ | Max            | Unit          |
|--------------------------|--|--|----------------|-----|----------------|---------------|
| $V_{IL}$                 | Input low voltage                            |  | $V_{SS}$       | –   | 0.8            | V             |
| $V_{IH}$                 | Input high voltage                           |  | 2.0            | –   | $V_{DD}$       | V             |
| $I_{IL}$                 | Input low current <sup>[3]</sup>             |  | –              | –   | –200           | $\mu\text{A}$ |
| $I_{IH}$                 | Input high current <sup>[3]</sup>            |  | –              | –   | 200            | $\mu\text{A}$ |
| $V_{PP}$                 | Peak-to-peak input voltage<br>PECL_CLK       |  | 500            | –   | 1000           | mV            |
| $V_{CMR}$                | Common mode range <sup>[4]</sup><br>PECL_CLK | $V_{DD} = 3.3 \text{ V}$   | $V_{DD} - 1.4$ | –   | $V_{DD} - 0.6$ | V             |
|                          |  | $V_{DD} = 2.5 \text{ V}$   | $V_{DD} - 1.0$ | –   | $V_{DD} - 0.6$ | V             |
| $V_{OL}$                 | Output low voltage <sup>[5, 6, 7]</sup>      | $I_{OL} = 20 \text{ mA}$   | –              | –   | 0.5            | V             |
| $V_{OH}$                 | Output high voltage <sup>[5, 6, 7]</sup>     | $I_{OH} = -20 \text{ mA}$ , $V_{DDC} = 3.3 \text{ V}$                | 2.4            | –   | –              | V             |
|                          |  | $I_{OH} = -20 \text{ mA}$ , $V_{DDC} = 2.5 \text{ V}$                | 1.8            | –   | –              | V             |
| $I_{DDQ}$                | Quiescent supply current                     |  | –              | 5   | 7              | mA            |
| $I_{DD}$                 | Dynamic supply current                       | $V_{DD} = 3.3 \text{ V}$ , Outputs at 150 MHz, $C_L = 15 \text{ pF}$ | –              | 285 | –              | mA            |
|                          |  | $V_{DD} = 3.3 \text{ V}$ , Outputs at 200 MHz, $C_L = 15 \text{ pF}$ | –              | 335 | –              |               |
|                          |  | $V_{DD} = 2.5 \text{ V}$ , Outputs at 150 MHz, $C_L = 15 \text{ pF}$ | –              | 200 | –              |               |
|                          |  | $V_{DD} = 2.5 \text{ V}$ , Outputs at 200 MHz, $C_L = 15 \text{ pF}$ | –              | 240 | –              |               |
| $Z_{out}$                | Output impedance                             | $V_{DD} = 3.3 \text{ V}$   | 8              | 12  | 16             | $\Omega$      |
|                          |  | $V_{DD} = 2.5 \text{ V}$   | 10             | 15  | 20             |               |
| $C_{in}$                 | Input capacitance                            |  | –              | 4   | –              | pF            |

## Thermal Resistance

| Parameter <sup>[8]</sup> | Description                                 | Test Conditions   | 32-pin TQFP | Unit               |
|--------------------------|---|---|-------------|--------------------|
| $\theta_{JA}$            | Thermal resistance<br>(junction to ambient) | Test conditions follow standard test methods and procedures for measuring thermal impedance, in accordance with EIA/JESD51. | 67          | $^\circ\text{C/W}$ |
| $\theta_{JC}$            | Thermal resistance<br>(junction to case)    |   | 28          | $^\circ\text{C/W}$ |

### Notes

- Multiple Supplies:** The Voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is not required.
- Inputs have pull-up/pull-down resistors that effect input current.
- The VCMR is the difference from the most positive side of the differential input signal. Normal operation is obtained when the "High" input is within the VCMR range and the input lies within the VPP specification. Driving series or parallel terminated 50  $\Omega$  (or 50  $\Omega$  to  $V_{DD}/2$ ) transmission lines
- Outputs driving 50  $\Omega$  transmission lines.
- See Figure 1 on page 5 and Figure 2 on page 5.
- 50% input duty cycle.
- These parameters are guaranteed by design and are not tested.

## AC Parameters<sup>[9]</sup>

$V_{DD} = 3.3 \text{ V} \pm 5\%$  or  $2.5 \text{ V} \pm 5\%$ ,  $V_{DDC} = 3.3 \text{ V} \pm 5\%$  or  $2.5 \text{ V} \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$

| Parameter                      | Description   | Conditions                               |                  | Min | Typ | Max | Unit |
|--------------------------------|---|--|------------------|-----|-----|-----|------|
| F <sub>max</sub>               | Input frequency                                       |  | —                | —   | —   | 200 | MHz  |
| t <sub>PD</sub>                | PECL_CLK to Q Delay <sup>[10, 11, 12]</sup> ≤ 150 MHz | V <sub>DD</sub> = 3.3 V, 85 °C           | t <sub>PHL</sub> | 2.0 | —   | 3.2 | ns   |
|                                |   |  | t <sub>PLH</sub> | 2.1 | —   | 3.4 |      |
|                                |   | V <sub>DD</sub> = 3.3 V, 70 °C           | t <sub>PHL</sub> | 1.9 | —   | 3.1 |      |
|                                |   |  | t <sub>PLH</sub> | 2.0 | —   | 3.2 |      |
|                                |   | V <sub>DD</sub> = 2.5 V, 85 °C           | t <sub>PHL</sub> | 2.5 | —   | 5.2 |      |
|                                |   |  | t <sub>PLH</sub> | 2.6 | —   | 5   |      |
|                                |   | V <sub>DD</sub> = 2.5 V, 70 °C           | t <sub>PHL</sub> | 2.5 | —   | 5   |      |
|                                |   |  | t <sub>PLH</sub> | 2.6 | —   | 5   |      |
| t <sub>PD</sub>                | LVCMOS to Q Delay <sup>[10, 11, 12]</sup> ≤ 150 MHz   | V <sub>DD</sub> = 3.3 V, 85 °C           | t <sub>PHL</sub> | 1.9 | —   | 3   | ns   |
|                                |   |  | t <sub>PLH</sub> | 2.0 | —   | 3.2 |      |
|                                |   | V <sub>DD</sub> = 3.3 V, 70 °C           | t <sub>PHL</sub> | 1.8 | —   | 2.9 |      |
|                                |   |  | t <sub>PLH</sub> | 1.8 | —   | 3.1 |      |
|                                |   | V <sub>DD</sub> = 2.5 V, 85 °C           | t <sub>PHL</sub> | 2.5 | —   | 4   |      |
|                                |   |  | t <sub>PLH</sub> | 2.5 | —   | 4   |      |
|                                |   | V <sub>DD</sub> = 2.5 V, 70 °C           | t <sub>PHL</sub> | 2.3 | —   | 3.8 |      |
|                                |   |  | t <sub>PLH</sub> | 2.3 | —   | 3.8 |      |
| t <sub>J</sub>                 | Total jitter  | V <sub>DD</sub> = 3.3 V @ 150 MHz        |                  | —   | —   | 10  | ps   |
| F <sub>outDC</sub>             | Output duty cycle <sup>[10, 11, 13]</sup>             | FCLK < 134 MHz                           |                  | —   | —   | 55  | %    |
|                                |   | FCLK > 134 MHz                           |                  | —   | —   | 60  |      |
| T <sub>skew</sub>              | Output-to-output skew <sup>[10, 11]</sup>             | V <sub>DD</sub> = 3.3 V                  |                  | —   | 60  | 150 | ps   |
|                                |   | V <sub>DD</sub> = 2.5 V                  |                  | —   | —   | 200 |      |
| T <sub>skew</sub> (pp)         | Part-to-part skew <sup>[14]</sup>                     | PECL, V <sub>DDC</sub> = 3.3 V           |                  | —   | —   | 1.4 | ns   |
|                                |   | PECL, V <sub>DDC</sub> = 2.5 V           |                  | —   | —   | 2.2 |      |
| T <sub>skew</sub> (pp)         | Part-to-part skew <sup>[14]</sup>                     | TCLK, V <sub>DDC</sub> = 3.3 V           |                  | —   | —   | 1.2 | ns   |
|                                |   | TCLK, V <sub>DDC</sub> = 2.5 V           |                  | —   | —   | 1.7 |      |
| T <sub>skew</sub> (pp)         | Part-to-part skew <sup>[15]</sup>                     | PECL_CLK                                 |                  | —   | —   | 850 | ps   |
|                                |   | TCLK                                     |                  | —   | —   | 750 |      |
| t <sub>R</sub> /t <sub>F</sub> | Output clocks rise/fall time <sup>[10, 11]</sup>      | 0.7 V to 2.0 V, V <sub>DDC</sub> = 3.3 V |                  | 0.3 | —   | 1.1 | ns   |
|                                |   | 0.5 V to 1.8 V, V <sub>DDC</sub> = 2.5 V |                  | 0.3 | —   | 1.2 |      |

### Notes

9. Parameters are guaranteed by design and characterization. Not 100% tested in production. All parameters specified with loaded outputs.

10. Outputs driving  $50 \Omega$  transmission lines.

11. See Figure 1 on page 5 and Figure 2 on page 5.

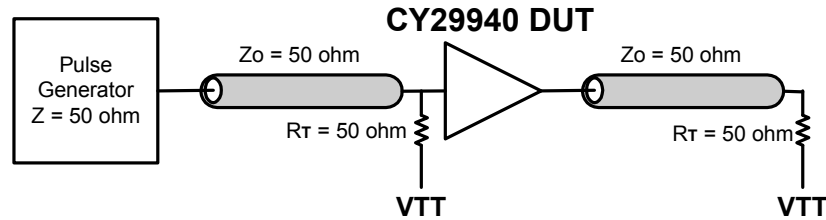
12. Parameters tested @ 150 MHz.

13. 50% input duty cycle.

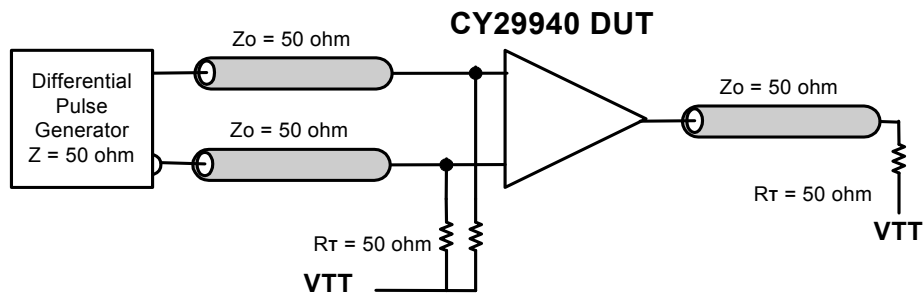
14. Across temperature and voltage ranges, includes output skew.

15. For a specific temperature and voltage, includes output skew.

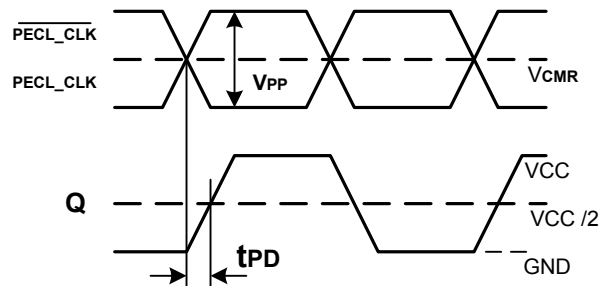
**Figure 1. LVCMOS\_CLK CY29940 Test Reference for  $V_{CC} = 3.3\text{ V}$  and  $V_{CC} = 2.5\text{ V}$**



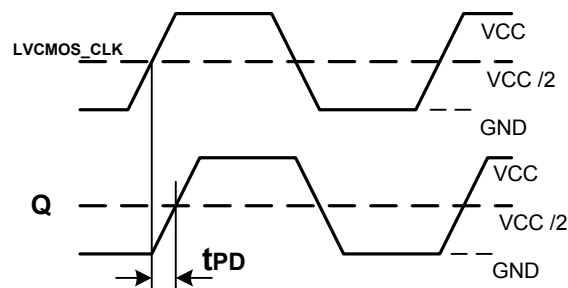
**Figure 2. PECL\_CLK CY29940 Test Reference for  $V_{CC} = 3.3\text{ V}$  and  $V_{CC} = 2.5\text{ V}$**

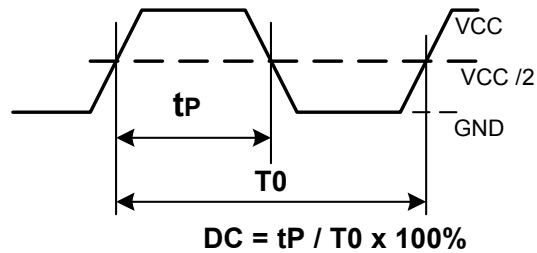
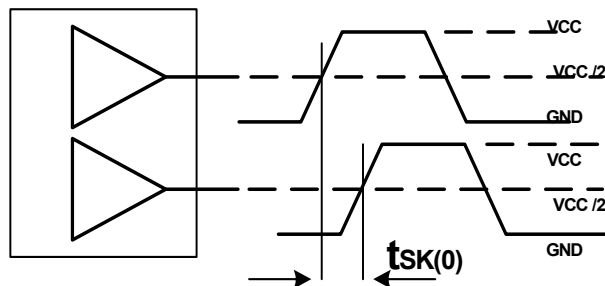


**Figure 3. Propagation Delay (TPD) Test Reference**



**Figure 4. LVCMOS Propagation Delay (TPD) Test Reference**

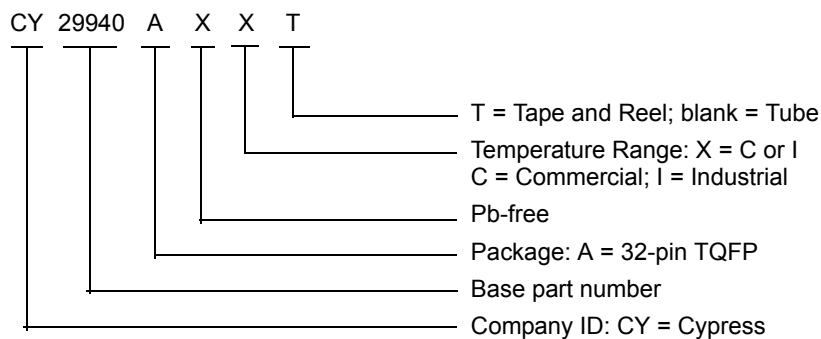


**Figure 5. Output Duty Cycle (FoutDC)**

**Figure 6. Output-to-Output Skew tsk(0)**


## Ordering Information

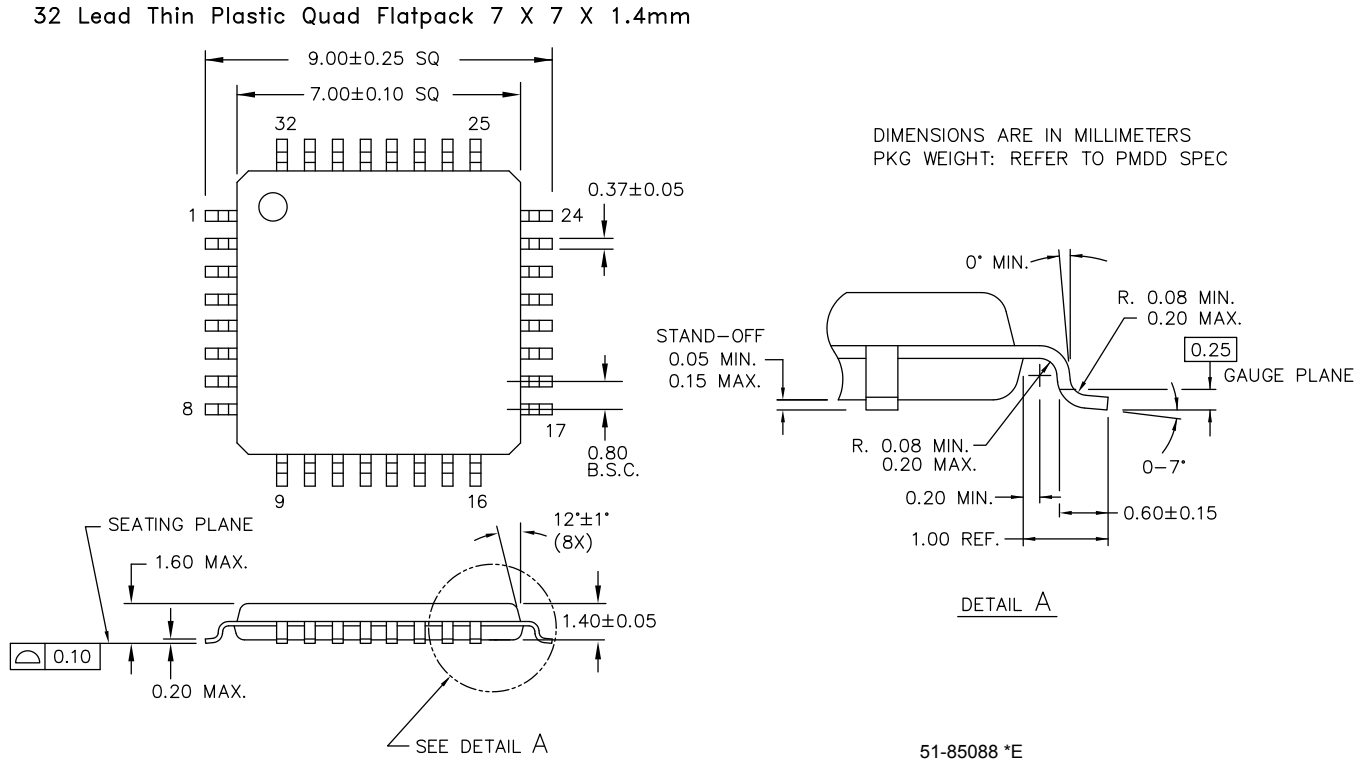
| Part Number    | Package Type                | Production Flow              |
|----------------|-----------------------------|------------------------------|
| <b>Pb-free</b> |                             |                              |
| CY29940AXI     | 32-pin TQFP                 | Industrial, -40 °C to +85 °C |
| CY29940AXIT    | 32-pin TQFP – Tape and Reel | Industrial, -40 °C to +85 °C |
| CY29940AXC     | 32-pin TQFP                 | Commercial, 0 °C to 70 °C    |
| CY29940AXCT    | 32-pin TQFP – Tape and Reel | Commercial, 0 °C to 70 °C    |

## Ordering Code Definitions



## Package Drawing and Dimensions

**Figure 7. 32-pin TQFP 7 × 7 × 1.4 mm A32.14**



## Acronyms

| Acronym | Description   |
|---------|---|
| ESD     | electrostatic discharge                             |
| I/O     | input/output  |
| TQFP    | thin quad flat package                              |
| LVC MOS | low voltage complementary metal oxide semiconductor |
| LVPECL  | low-voltage positive emitter-coupled logic          |
| LVTTTL  | low-voltage transistor-transistor logic             |
| TQFP    | thin quad flat pack                                 |

## Document Conventions

### Units of Measure

| Symbol | Unit of Measure |
|--------|-----------------|
| °C     | degree Celsius  |
| kV     | kilo Volts      |
| MHz    | Mega Hertz      |
| μA     | micro Amperes   |
| mA     | milli Amperes   |
| mm     | milli meter     |
| mV     | milli Volts     |
| ns     | nano seconds    |
| Ω      | ohms            |
| %      | percent         |
| pF     | pico Farad      |
| ps     | pico seconds    |
| V      | Volts           |
| W      | Watts           |

## Document History Page

| Document Title: CY29940, 2.5 V or 3.3 V, 200 MHz, 1:18 Clock Distribution Buffer<br>Document Number: 38-07283 |         |            |                 |  |
|---|---------|------------|-----------------|--|
| Rev.  | ECN No. | Issue Date | Orig. of Change | Description of Change  |
| **  | 111094  | 02/01/02   | BRK             | New data sheet   |
| *A  | 116776  | 08/15/02   | HWT             | Incorporate results of final characterization using corporate methods, added output impedance on page 3 and added output duty cycle on page 4.<br>Updated <a href="#">Ordering Information</a> :<br>Add commercial temperature range part numbers.   |
| *B  | 122875  | 12/21/02   | RBI             | Add power up requirements to maximum rating information  |
| *C  | 448379  | See ECN    | RGL             | Add typical value for output-to-output skew<br>Updated <a href="#">Ordering Information</a> :<br>Added Lead-free devices.  |
| *D  | 2899304 | 03/25/10   | BASH / KVM      | Updated <a href="#">Ordering Information</a> :<br>Removed inactive parts.<br>Updated <a href="#">Package Drawing and Dimensions</a> .  |
| *E  | 3254185 | 05/11/2011 | CXQ             | Added <a href="#">Ordering Code Definitions</a> .<br>Added <a href="#">Acronyms</a> and <a href="#">Units of Measure</a> .<br>Updated to new template.   |
| *F  | 3548252 | 03/12/2012 | PURU            | Changed LQFP to TQFP throughout document.  |
| *G  | 4586288 | 12/03/2014 | PURU            | Updated <a href="#">Functional Description</a> :<br>Added "For a complete list of related documentation, <a href="#">click here</a> ." at the end.<br>Updated <a href="#">Package Drawing and Dimensions</a> :<br>Updated <a href="#">Figure 7</a> (spec 51-85088 – Changed revision from *D to *E). |
| *H  | 4787038 | 06/04/2015 | TAVA            | Updated to new template.<br>Completing Sunset Review.  |
| *I  | 5258862 | 05/04/2016 | PSR             | Added <a href="#">Thermal Resistance</a> .<br>Updated to new template.<br>Completing Sunset Review.  |
| *J  | 5973872 | 11/22/2017 | AESATMP8        | Updated logo and Copyright.  |



## Sales, Solutions, and Legal Information

### Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at [Cypress Locations](#).

### Products

|                               |  |
|-------------------------------|--|
| ARM® Cortex® Microcontrollers | <a href="http://cypress.com/arm">cypress.com/arm</a>               |
| Automotive                    | <a href="http://cypress.com/automotive">cypress.com/automotive</a> |
| Clocks & Buffers              | <a href="http://cypress.com/clocks">cypress.com/clocks</a>         |
| Interface                     | <a href="http://cypress.com/interface">cypress.com/interface</a>   |
| Internet of Things            | <a href="http://cypress.com/iot">cypress.com/iot</a>               |
| Memory                        | <a href="http://cypress.com/memory">cypress.com/memory</a>         |
| Microcontrollers              | <a href="http://cypress.com/mcu">cypress.com/mcu</a>               |
| PSoC                          | <a href="http://cypress.com/psoc">cypress.com/psoc</a>             |
| Power Management ICs          | <a href="http://cypress.com/pmic">cypress.com/pmic</a>             |
| Touch Sensing                 | <a href="http://cypress.com/touch">cypress.com/touch</a>           |
| USB Controllers               | <a href="http://cypress.com/usb">cypress.com/usb</a>               |
| Wireless Connectivity         | <a href="http://cypress.com/wireless">cypress.com/wireless</a>     |

### PSoC® Solutions

[PSoC 1](#) | [PSoC 3](#) | [PSoC 4](#) | [PSoC 5LP](#) | [PSoC 6](#)

### Cypress Developer Community

[Forums](#) | [WICED IOT Forums](#) | [Projects](#) | [Video](#) | [Blogs](#) | [Training](#) | [Components](#)

### Technical Support

[cypress.com/support](http://cypress.com/support)

© Cypress Semiconductor Corporation, 2002-2017. This document is the property of Cypress Semiconductor Corporation and its subsidiaries, including Spansion LLC ("Cypress"). This document, including any software or firmware included or referenced in this document ("Software"), is owned by Cypress under the intellectual property laws and treaties of the United States and other countries worldwide. Cypress reserves all rights under such laws and treaties and does not, except as specifically stated in this paragraph, grant any license under its patents, copyrights, trademarks, or other intellectual property rights. If the Software is not accompanied by a license agreement and you do not otherwise have a written agreement with Cypress governing the use of the Software, then Cypress hereby grants you a personal, non-exclusive, nontransferable license (without the right to sublicense) (1) under its copyright rights in the Software (a) for Software provided in source code form, to modify and reproduce the Software solely for use with Cypress hardware products, only internally within your organization, and (b) to distribute the Software in binary code form externally to end users (either directly or indirectly through resellers and distributors), solely for use on Cypress hardware product units, and (2) under those claims of Cypress's patents that are infringed by the Software (as provided by Cypress, unmodified) to make, use, distribute, and import the Software solely for use with Cypress hardware products. Any other use, reproduction, modification, translation, or compilation of the Software is prohibited.

TO THE EXTENT PERMITTED BY APPLICABLE LAW, CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS DOCUMENT OR ANY SOFTWARE OR ACCOMPANYING HARDWARE, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. To the extent permitted by applicable law, Cypress reserves the right to make changes to this document without further notice. Cypress does not assume any liability arising out of the application or use of any product or circuit described in this document. Any information provided in this document, including any sample design information or programming code, is provided only for reference purposes. It is the responsibility of the user of this document to properly design, program, and test the functionality and safety of any application made of this information and any resulting product. Cypress products are not designed, intended, or authorized for use as critical components in systems designed or intended for the operation of weapons, weapons systems, nuclear installations, life-support devices or systems, other medical devices or systems (including resuscitation equipment and surgical implants), pollution control or hazardous substances management, or other uses where the failure of the device or system could cause personal injury, death, or property damage ("Unintended Uses"). A critical component is any component of a device or system whose failure to perform can be reasonably expected to cause the failure of the device or system, or to affect its safety or effectiveness. Cypress is not liable, in whole or in part, and you shall and hereby do release Cypress from any claim, damage, or other liability arising from or related to all Unintended Uses of Cypress products. You shall indemnify and hold Cypress harmless from and against all claims, costs, damages, and other liabilities, including claims for personal injury or death, arising from or related to any Unintended Uses of Cypress products.

Cypress, the Cypress logo, Spansion, the Spansion logo, and combinations thereof, WICED, PSoC, CapSense, EZ-USB, F-RAM, and Traveo are trademarks or registered trademarks of Cypress in the United States and other countries. For a more complete list of Cypress trademarks, visit [cypress.com](http://cypress.com). Other names and brands may be claimed as property of their respective owners.