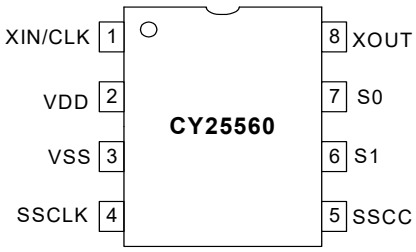
Contents

Pinouts

Figure 1. 8-pin SOIC pinout



Pin Description

Pin Number	Pin Name	Type	Pin Description
1	Xin/CLK	I	Clock or crystal connection input. See the Table on page 4 for input frequency range selection.
2	VDD	P	Positive power supply.
3	GND	P	Power supply ground.
4	SSCLK	O	Modulated clock output, that is the same frequency as the input clock or the crystal frequency.
5	SSCC	I	Spread spectrum clock control (enable/disable) function. SSCG function is enabled when input is high and disabled when input is low. This pin is pulled high internally.
6	S1	I	Tri-level logic input control pin used to select input frequency range and spread percent. See the Tri-Level Logic on page 4 for programming details. Pin 6 has an internal resistor divider network to V_{DD} and V_{SS}. See the Logic Block Diagram on page 1.
7	S0	I	Tri-level logic input control pin used to select input frequency range and spread percent. See the Tri-Level Logic on page 4 for programming details. Pin 7 has an internal resistor divider network to V_{DD} and V_{SS}. See the Logic Block Diagram on page 1.
8	Xout	O	Oscillator output pin connected to crystal. Leave this pin unconnected if an external clock is used to drive xin/clk input (Pin 1).

General Description

The Cypress CY25560 is a spread spectrum clock generator (SSCG) IC used to reduce the EMI found in today's high-speed digital electronic systems.

The CY25560 uses Cypress's proprietary phase-locked loop (PLL) and spread spectrum clock (SSC) technology to synthesize and frequency modulate the input frequency of the reference clock. By frequency modulating the clock, the measured EMI at the fundamental and harmonic frequencies of clock (SSCLK) is greatly reduced.

This reduction in radiated energy can significantly reduce the cost of complying with regulatory requirements and time to market without degrading system performance.

The CY25560 is a very simple and versatile device to use. The frequency and spread% range is selected by programming S0 and S1 digital inputs. These inputs use three (3) logic states including High (H), Low (L), and Middle (M) logic levels to select one of the nine available spread% ranges. See the Frequency and Spread% Selection (Center Spread) on page 4 for programming details.

CY25560 is optimized for SVGA (40 MHz) and XVGA (65 MHz) controller clocks and also suitable for applications where the frequency range is 25 MHz to 100 MHz.

A wide range of digitally selectable spread percentages is made possible by using three-level (High, Low, and Middle) logic at the S0 and S1 digital control inputs.

The output spread (frequency modulation) is symmetrically centered on the input frequency.

Spread spectrum clock control (SSCC) function enables or disables the frequency spread and is provided for easy comparison of system performance during EMI testing.

The CY25560 is available in an 8-pin SOIC package with 0 °C to 70 °C Commercial and –40 °C to 85 °C Industrial operating temperature ranges.

Frequency and Spread% Selection (Center Spread)

25 – 50 MHz (Low Range)

Input Frequency (MHz)	S1=M S0=M (%)	S1=M S0=0 (%)	S1=1 S0=0 (%)	S1=0 S0=0 (%)	S1=0 S0=M (%)
25 – 35	4.3	3.8	3.4	2.9	2.8
35 – 40	3.9	3.5	3.1	2.5	2.4
40 – 45	3.7	3.3	2.8	2.4	2.3
45 – 50	3.4	3.1	2.6	2.2	2.1

Select the Frequency and Center Spread % desired and then set S1, S0 as indicated.

50 – 100 MHz (High Range)

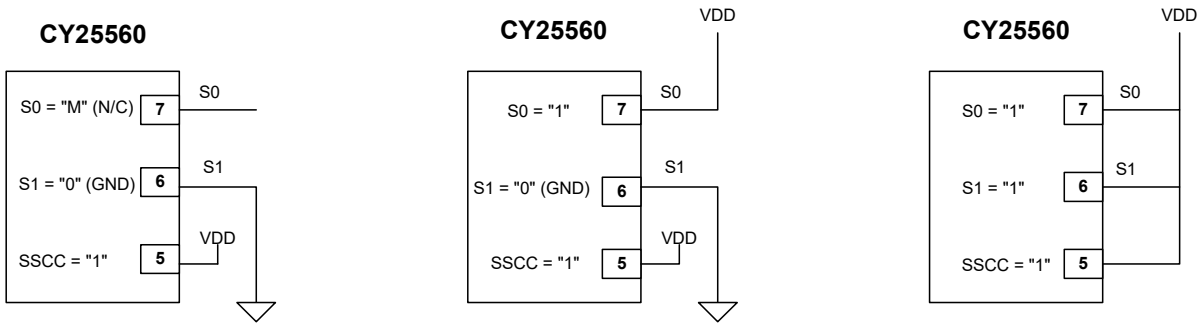
Input Frequency (MHz)	S1=1 S0=M (%)	S1=0 S0=1 (%)	S1=1 S0=1 (%)	S1=M S0=1 (%)
50 – 60	2.9	2.1	1.5	1.2
60 – 70	2.8	2.0	1.4	1.1
70 – 80	2.6	1.8	1.3	1.1
80 – 100	2.4	1.7	1.2	1.0

Select the Frequency and Center Spread % desired and then set S1, S0 as indicated.

Tri-Level Logic

With binary logic, four states can be programmed with two control lines, whereas three-level logic can program nine logic states using two control lines. Three-level logic in the CY25560 is implemented by defining a third logic state in addition to the standard logic ‘1’ and ‘0’. Pins 6 and 7 of the CY25560 recognize a logic state by the voltage applied to their respective pin. These states are defined as ‘0’ (Low), ‘M’ (Middle), and ‘1’ (One). Each of these states have a defined voltage range that is interpreted by the CY25560 as a ‘0’, ‘M’, or ‘1’ logic state. See the DC Electrical Characteristics on page 7 for voltage ranges for each logic state. The CY25560 has two equal value resistor dividers connected internally to Pins 6 and 7 that produce the default ‘M’ (Middle) state if these pins are left unconnected (NC). Pins 6 and/or 7 can be tied directly to ground or V_{DD} to program a logic ‘0’ or ‘1’ state, respectively.

Figure 2. Three-Level Logic Examples



SSCG Theory of Operation

The CY25560 is a PLL-type clock generator using a proprietary Cypress design. By precisely controlling the bandwidth of the output clock, the CY25560 becomes a low-EMI clock generator. The theory and detailed operation of the CY25560 is discussed in the following sections.

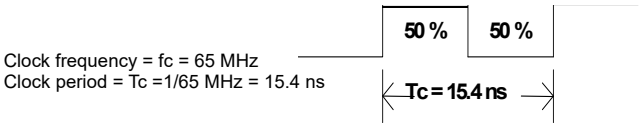
EMI

All digital clocks generate unwanted energy in their harmonics. Conventional digital clocks are square waves with a duty cycle that is very close to 50 percent. Because of this 50/50 duty cycle, digital clocks generate most of their harmonic energy in the odd harmonics, i.e., third, fifth, seventh, and so on. It is possible to reduce the amount of energy contained in the fundamental and odd harmonics by increasing the bandwidth of the fundamental clock frequency. Conventional digital clocks have a very high Q factor, that means that all of the energy at that frequency is

concentrated in a very narrow bandwidth, consequently, higher energy peaks. Regulatory agencies test electronic equipment by the amount of peak energy radiated from the equipment. By reducing the peak energy at the fundamental and harmonic frequencies, the equipment under test is able to satisfy agency requirements for EMI. Conventional methods of reducing EMI have been to use shielding, filtering, multilayer PCBs, and so on. The CY25560 uses the approach of reducing the peak energy in the clock by increasing the clock bandwidth, and lowering the Q factor.

SSCG

SSCG uses a patented technology of modulating the clock over a very narrow bandwidth and controlled rate of change, both peak and cycle-to-cycle. The CY25560 takes a narrow band digital reference clock in the range of 25 to 100 MHz and produces a clock that sweeps between a controlled start and stop frequency and precise rate of change. To understand what happens to a clock when SSCG is applied, consider a 65 MHz clock with a 50 percent duty cycle. From a 65 MHz clock we know the following:



If this clock is applied to the Xin/CLK pin of CY25560, the output clock at Pin 4 (SSCLK) sweeps back and forth between two frequencies. These two frequencies, F1 and F2, are used to calculate to total amount of spread or bandwidth applied to the reference clock at Pin 1. As the clock is making the transition from F1 to F2, the amount of time and sweep waveform play a very important role in the amount of EMI reduction realized from an SSCG clock.

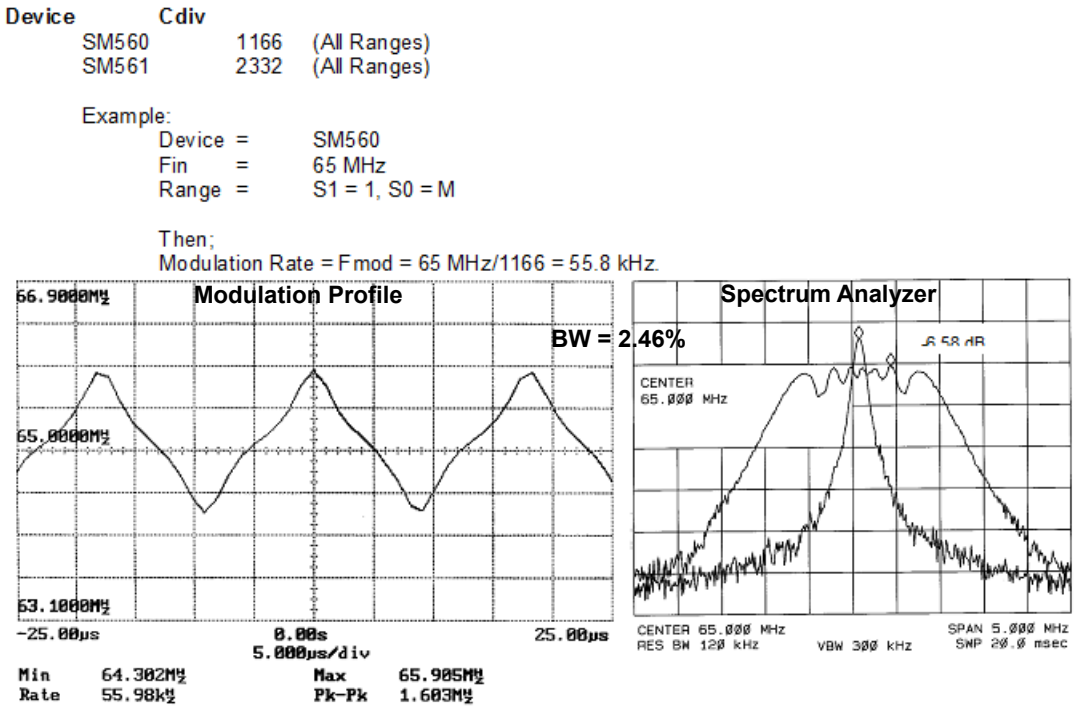
The modulation domain analyzer is used to visualize the sweep waveform and sweep period. Figure 3 shows the modulation profile of a 65 MHz SSCG clock. Notice that the actual sweep waveform is not a simple sine or sawtooth waveform. Figure 3 also shows a scan of the same SSCG clock using a spectrum analyzer. In this scan you can see a 6.48 dB reduction in the peak RF energy when using the SSCG clock.

Modulation Rate

SSCGs utilize frequency modulation (FM) to distribute energy over a specific band of frequencies. The maximum frequency of the clock (Fmax) and minimum frequency of the clock (Fmin) determine this band of frequencies. The time required to transition from Fmin to Fmax and back to Fmin is the period of the Modulation Rate, Tmod. Modulation Rates of SSCG clocks are generally referred to in terms of frequency or
Fmod = 1/Tmod.

The input clock frequency, Fin, and the internal divider count, Cdiv, determine the Modulation Rate. In some SSCG clock generators, the selected range determines the internal divider count. In other SSCG clocks, the internal divider count is fixed over the operating range of the device. The CY25560 has a fixed divider count of 1166.

Figure 3. SSCG Clock, CY25560, Fin = 65 MHz

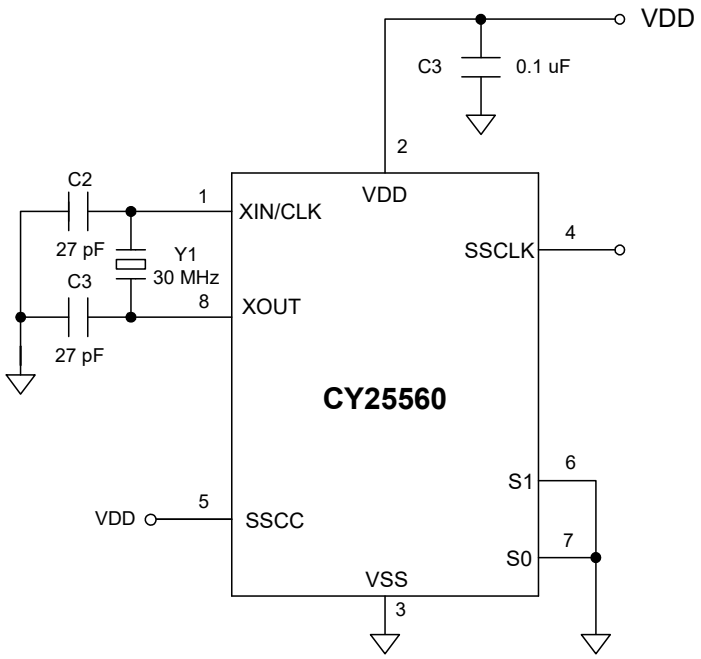


CY25560 Application Schematic

The schematic in Figure 4 demonstrates how the CY25560 is configured in a typical application. This application is shown as using a 30 MHz fundamental crystal. In most applications, an external reference clock is used. Apply the external clock signal at Xin (Pin 1) and leave Xout (Pin 8) unconnected (see Pin Description on page 3 for pin descriptions).

Contact Cypress if higher order crystal is to be used.

Figure 4. Application Schematic



Absolute Maximum Ratings

Commercial Grade [1, 2]

Supply Voltage (V_{DD}) .....–0.5 V to +6.0 V

DC Input Voltage .....–0.5 V to V_{DD} + 0.5 V

Junction Temperature ..... –40 °C to +140 °C

Operating Temperature ..... 0 °C to 70 °C

Storage Temperature ..... –65 °C to +150 °C

Static Discharge Voltage (ESD) ..... 2,000 V-Min

DC Electrical Characteristics

V_{DD} = 3.3 V ± 10%, T = 0 °C to 70 °C and C_L (Pin 4) = 15 pF, Unless Otherwise Noted

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{DD}	Power supply range	±10%	2.97	3.3	3.63	V
V_{IH}	Input high voltage	S0 and S1 only	0.85 × V_{DD}	V_{DD}	V_{DD}	V
V_{IM}	Input middle voltage	S0 and S1 only	0.40 × V_{DD}	0.50 × V_{DD}	0.60 × V_{DD}	V
V_{IL}	Input low voltage	S0 and S1 only	0.0	0.0	0.15 × V_{DD}	V
V_{OH}	Output high voltage	I_{OH} = 6 mA	2.4	–	–	V
V_{OL}	Output low voltage	I_{OH} = 6 mA	–	–	0.4	V
C_{in1}	Input capacitance	Xin/CLK (Pin 1)	3	4	5	pF
C_{in2}	Input capacitance	Xout (Pin 8)	6	8	10	pF
C_{in2}	Input capacitance	S0, S1, SSCC (Pins 7, 6, 5)	3	4	5	pF
I_{DD1}	Power supply current	FIN = 25 MHz, CL = 0	–	17	23	mA
I_{DD2}	Power supply current	FIN = 65 MHz, CL = 0	–	27	41	mA
I_{DD3}	Power supply current	FIN = 100 MHz, CL = 0	–	42	59	mA

X_{IN}/CLK DC Specifications

Parameter	Description	Conditions	Min	Max	Units
$V_{IH(X)}$	Input high voltage, X_{IN} Clock Input	F ≤ 100 MHz	80	–	% of V_{DD}
$V_{IL(X)}$	Input low voltage, X_{IN} Clock Input		–	15	% of V_{DD}

Electrical Timing Characteristics

V_{DD} = 3.3 V ± 10%, T = 0 °C to 70 °C and C_L (Pin 4) = 15 pF, Unless Otherwise Noted

Parameter	Description	Conditions	Min	Typ	Max	Unit
I_{CLKFR}	Input clock frequency range	V_{DD} = 3.30 V	25	–	100	MHz
t_F	Clock rise time (Pin 4)	SSCLK at 0.4 V–2.4 V	1.0	1.8	2.8	ns
t_R	Clock fall time (Pin 4)	SSCLK at 0.4 V–2.4 V	1.0	1.8	2.8	ns
D_{TYin}	Input clock duty cycle	XIN/CLK (Pin 1)	25	50	75	%
D_{TYout}	Output clock duty cycle	SSCLK (Pin 4)	45	50	55	%
J_{CC1}	Cycle-to-cycle jitter	Fin = 25 MHz–50 MHz, SSCC = 1	–	150	300	ps
J_{CC2}	Cycle-to-cycle jitter	Fin = 50 MHz–100 MHz, SSCC = 1	–	130	200	ps

Notes
1. Operation at any Absolute Maximum Rating is not implied.
2. Single Power Supply: The voltage on any input or I/O pin cannot exceed the power pin during power-up.

Absolute Maximum Conditions

Industrial Grade [3, 4]

Supply Voltage (V_{DD}) .....–0.5 V to +6.0 V

DC Input Voltage .....–0.5 V to V_{DD}+0.5 V

Junction Temperature ..... –40 °C to +140 °C

Operating Temperature ..... –40 °C to 85 °C

Storage Temperature ..... –65 °C to +150 °C

Static Discharge Voltage (ESD) ..... 2,000 V-Min

DC Electrical Characteristics

V_{DD} = 3.3 V ± 10%, T= –40 °C to 85 °C and C_L (Pin 4) = 15 pF, Unless Otherwise Noted

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{DD}	Power supply range	±10%	2.97	3.3	3.63	V
V_{IH}	Input high voltage	S0 and S1 only	0.85 × V_{DD}	V_{DD}	V_{DD}	V
V_{IM}	Input middle voltage	S0 and S1 only	0.40 × V_{DD}	0.50 × V_{DD}	0.60 × V_{DD}	V
V_{IL}	Input low voltage	S0 and S1 only	0.0	0.0	0.15 × V_{DD}	V
V_{OH}	Output high voltage	I_{OH} = 6 mA	2.2	–	–	V
V_{OL}	Output low voltage	I_{OH} = 6 mA	–	–	0.4	V
C_{in1}	Input capacitance	Xin/CLK (Pin 1)	3	4	5	pF
C_{in2}	Input capacitance	Xout (Pin 8)	6	8	10	pF
C_{in2}	Input capacitance	S0, S1, SSCC (Pins 7, 6, 5)	3	4	5	pF
I_{DD1}	Power supply current	FIN = 25 MHz, CL= 0	–	17	24	mA
I_{DD2}	Power supply current	FIN = 65 MHz, CL= 0	–	27	41	mA
I_{DD3}	Power supply current	FIN = 100 MHz, CL= 0	–	42	61	mA

Electrical Timing Characteristics

V_{DD} = 3.3 V ± 10%, T= –40 °C to 85 °C and C_L (Pin 4) = 15 pF, Unless Otherwise Noted

Parameter	Description	Conditions	Min	Typ	Max	Unit
I_{CLKFR}	Input clock frequency range	V_{DD} = 3.30 V	25	–	100	MHz
t_F	Clock rise time (Pin 4)	SSCLK at 0.4 V–2.4 V	1.0	1.8	3.0	ns
t_R	Clock fall time (Pin 4)	SSCLK at 0.4 V–2.4 V	1.0	1.8	3.0	ns
D_{TYin}	Input clock duty cycle	XIN/CLK (Pin 1)	25	50	75	%
D_{TYout}	Output clock duty cycle	SSCLK (Pin 4)	45	50	55	%
J_{CC1}	Cycle-to-cycle jitter	Fin = 25 MHz–50 MHz, SSCC = 1	–	150	300	ps
J_{CC2}	Cycle-to-cycle jitter	Fin = 50 MHz–100 MHz, SSCC = 1	–	130	200	ps

Thermal Resistance

Parameter [5]	Description	Test Conditions	8-pin SOIC	Unit
θ_{JA}	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, in accordance with EIA/JESD51.	131	°C/W
θ_{JC}	Thermal resistance (junction to case)		41	°C/W

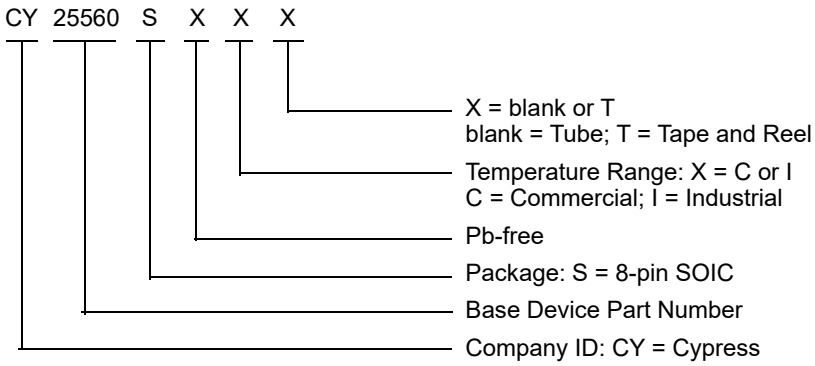
Notes

3. Operation at any Absolute Maximum Rating is not implied.
4. Single Power Supply: The voltage on any input or I/O pin cannot exceed the power pin during power-up.
5. These parameters are guaranteed by design and are not tested.

Ordering Information

Part Number	Package Type	Product Flow
Pb-free		
CY25560SXC	8-pin SOIC	Commercial, 0 °C to 70 °C
CY25560SXCT	8-pin SOIC – Tape and Reel	Commercial, 0 °C to 70 °C
CY25560SXI	8-pin SOIC	Industrial, –40 °C to 85 °C
CY25560SXIT	8-pin SOIC – Tape and Reel	Industrial, –40 °C to 85 °C

Ordering Code Definitions

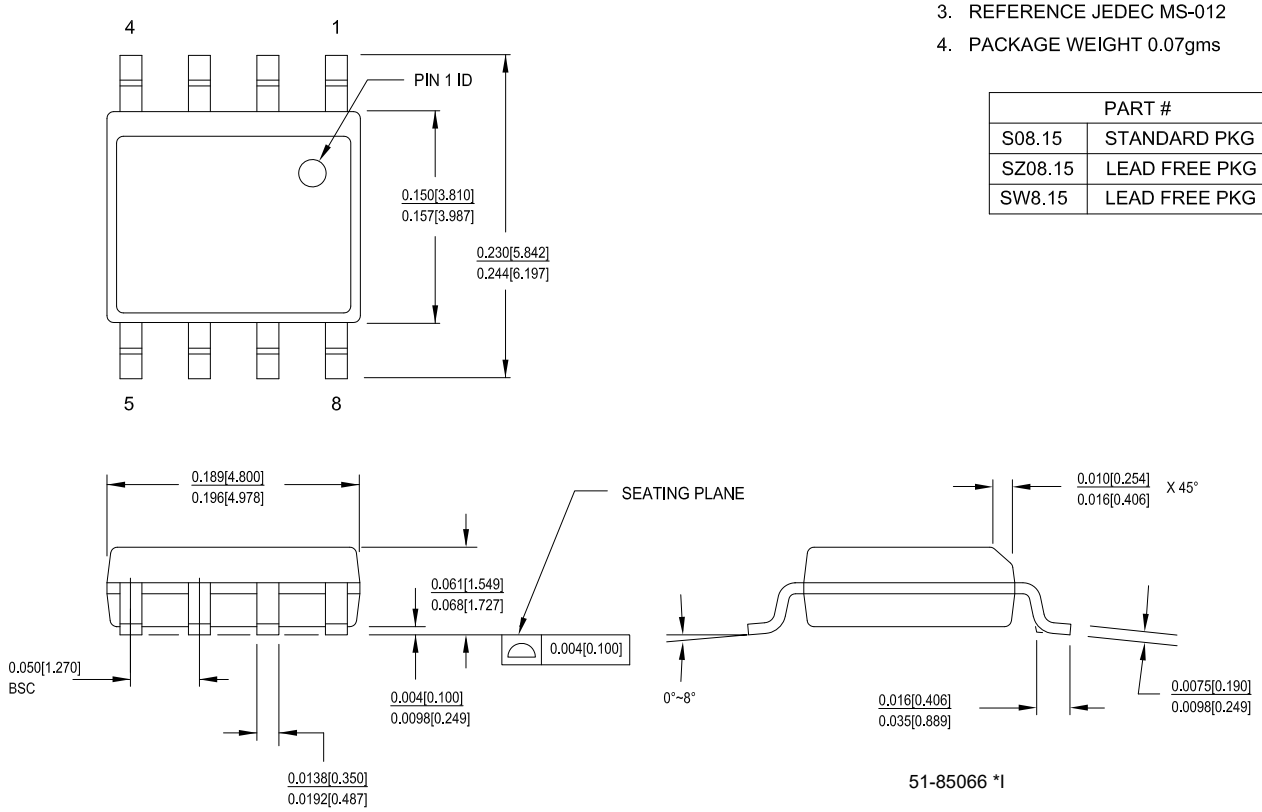


Package Drawing and Dimensions

Figure 5. 8-pin SOIC (150 Mils) S0815/SZ815/SW815 Package Outline, 51-85066

1. DIMENSIONS IN INCHES[MM] MIN.
   MAX.
2. PIN 1 ID IS OPTIONAL,
   ROUND ON SINGLE LEADFRAME
   RECTANGULAR ON MATRIX LEADFRAME
3. REFERENCE JEDEC MS-012
4. PACKAGE WEIGHT 0.07gms

PART #	
S08.15	STANDARD PKG
SZ08.15	LEAD FREE PKG
SW8.15	LEAD FREE PKG



Acronyms

Acronym	Description
EMI	Electromagnetic Interference
ESD	Electrostatic Discharge
PLL	Phase Locked Loop
SOIC	Small Outline Integrated Circuit
SSC	Spread Spectrum Clock
SSCG	Spread Spectrum Clock Generator
SVGA	Super Video Graphics Array
XVGA	Extended Video Graphics Array

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
mA	milliampere
ns	nanosecond
%	percent
pF	picofarad
ps	picosecond
W	watt

Document History Page

Document Title: CY25560, Spread Spectrum Clock Generator Document Number: 38-07425			
Revision	**ECN**	**Submission Date**	**Description of Change**
**	115261	06/12/02	New data sheet.
*A	119441	10/17/02	Corrected the values in the Absolute Maximum Ratings to match the device.
*B	122704	12/30/02	Added power up requirements to maximum ratings information.
*C	125549	05/15/03	Added Industrial Temperature Range to the device. Removed V_{OL2} and V_{OH2} spec in the DC specs table Changed IDD Values from 11/17/25 typ and 14/22/34max to 17/27/42 typ and 23/41/59 max Changed T_F/T_R values from 1.3/1.3 typ and 1.6/1.6 max to 1.8/1.8 typ and 2.8/2.8 max in the Electrical Char. table. Changed $J_{CC1/2}$ values from 200/250 typ and 250/300 max to 150/130 typ to 300/200 max in the Electrical Char. table. Changed the low power dissipation from 36/56/82mW to 56/89/139mW respectively. Changed the low cycle-to-cycle jitter from 195/175/100ps-typ to 450/225/150 ps-max
*D	314293	See ECN	Updated Ordering Information: Added Pb-free devices.
*E	2762435	09/11/09	Updated SSCG Theory of Operation: Updated SSCG: Fixed the frequency in figure. Updated Ordering Information: Removed Pb devices.
*F	2819309	12/01/09	Minor change - updated revision number and corrected the document number at the beginning of this table.
*G	3343531	08/12/2011	Added Ordering Code Definitions. Added Acronyms and Units of Measure. Updated Package Drawing and Dimensions.
*H	4511394	09/26/2014	Added XIN/CLK DC Specifications. Updated Package Drawing and Dimensions: spec 51-85066 – Changed revision from *E to *F. Updated to new template. Completing Sunset Review.
*I	4586478	03/12/2014	Updated Functional Description: Added “For a complete list of related documentation, click here.” at the end.
*J	5270202	05/13/2016	Updated SSCG Theory of Operation: Updated SSCG: Updated Figure 3. Added Thermal Resistance. Updated Package Drawing and Dimensions: spec 51-85066 – Changed revision from *F to *H. Updated to new template.
*K	6866984	04/24/2020	Updated Spec 51-85066 – Changed revision from *H to *I. Updated to template.

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