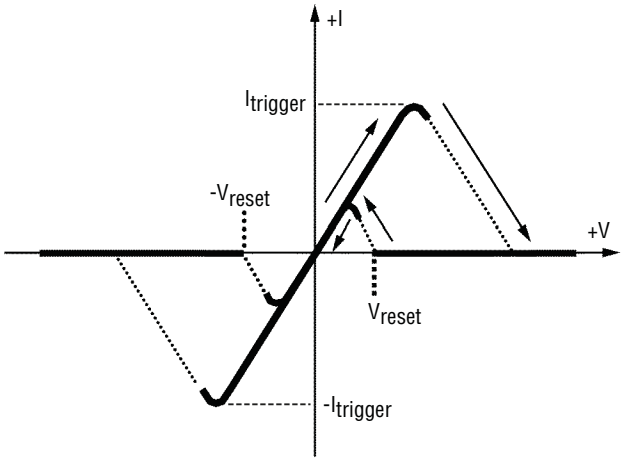
Applications

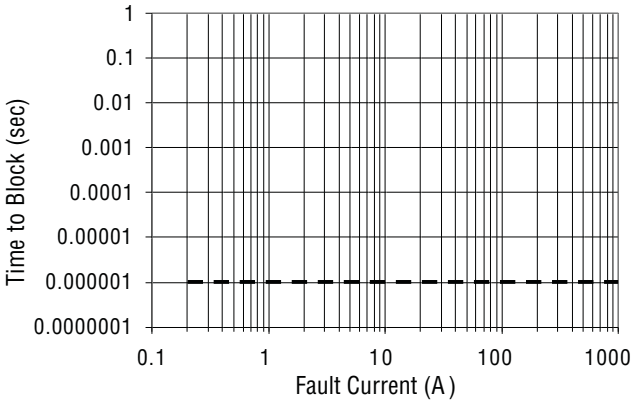
- Combo voice / xDSL linecards
- Voice linecards
- MDF, primary protection modules
- Process control equipment
- Test and measurement equipment
- General electronics

Typical Performance Characteristics

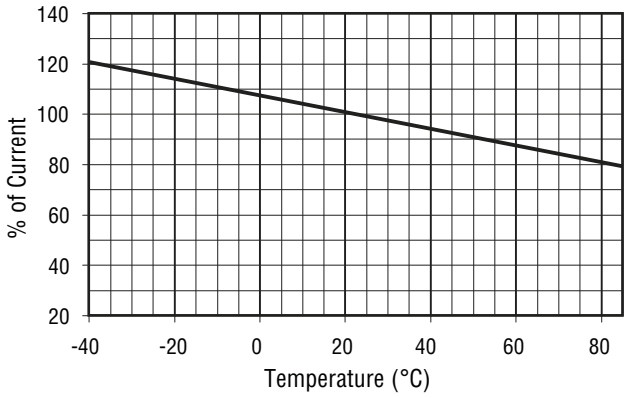
V-I Characteristics



Time to Block vs. Fault Current



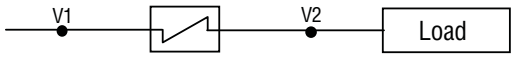
Current vs. Temperature



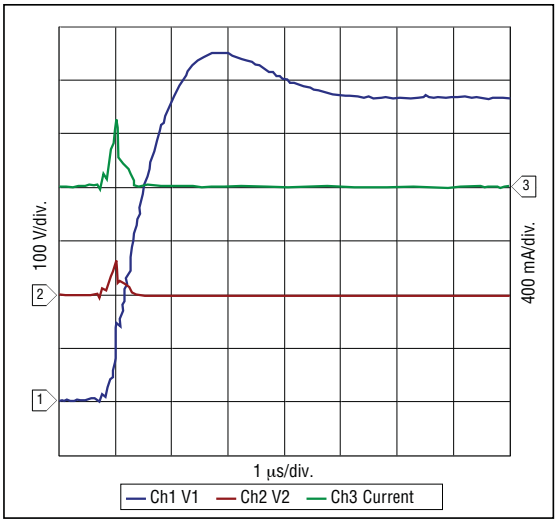
Operational Characteristics

The graphs below demonstrate the operational characteristics of the TBU® protector. For each graph the fault voltage, protected side voltage, and current is presented.

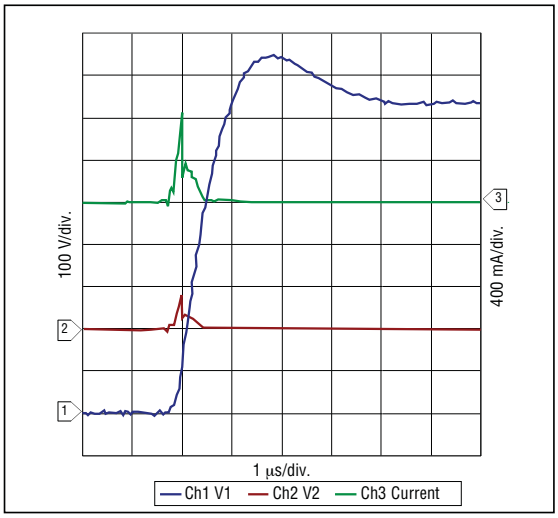
TEST CONFIGURATION DIAGRAM



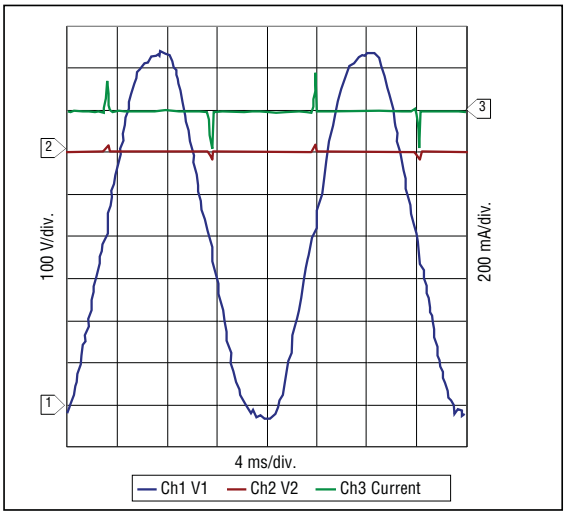
C650 Lightning, 650 V



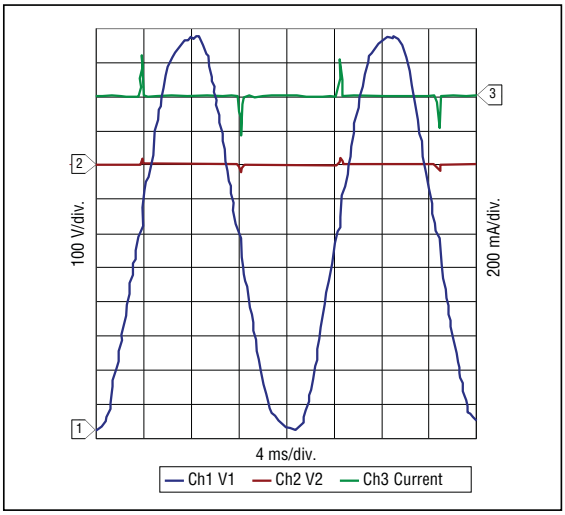
C850 Lightning, 850 V



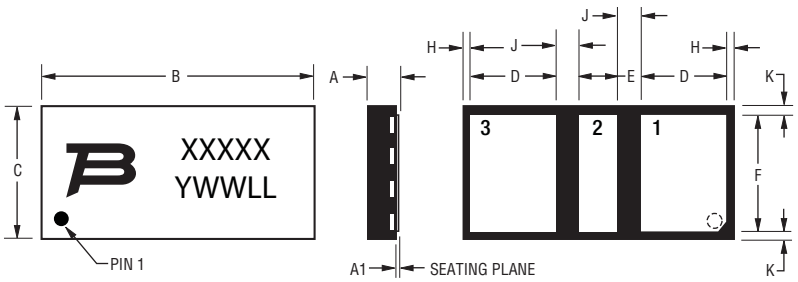
C650 Power Fault, 300 Vrms, 100 A



C850 Power Fault, 425 Vrms, 100 A



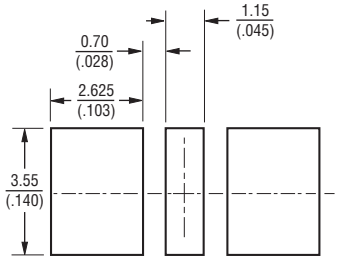
Product Dimensions



Dim.	Min.	Typ.	Max.
A	0.80 (.031)	0.90 (.035)	1.00 (.039)
A1	0.00 (.000)	0.025 (.001)	0.050 (.002)
B	8.15 (.321)	8.25 (.325)	8.35 (.329)
C	3.90 (.154)	4.00 (.157)	4.10 (.161)
D	2.55 (.100)	2.60 (.102)	2.65 (.104)
E	1.10 (.043)	1.15 (.045)	1.20 (.047)
F	3.45 (.136)	3.50 (.138)	3.55 (.140)
H	0.20 (.008)	0.25 (.010)	0.30 (.012)
J	0.65 (.026)	0.70 (.028)	0.75 (.030)
K	0.20 (.008)	0.25 (.010)	0.30 (.012)

DIMENSIONS: MM (INCHES)

Recommended Pad Layout



Pad Designation

Pad #	Apply
1	In/Out
2	NC
3	In/Out

NC = Solder to PCB; do not make electrical connection, do not connect to ground.

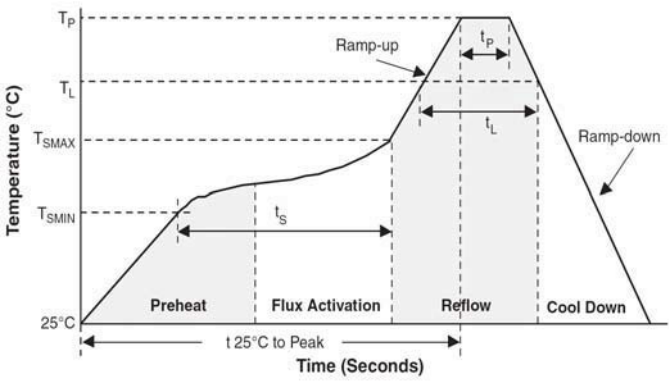
TBU® protectors have matte-tin termination finish. Suggested layout should use non-solder mask define (NSMD). Recommended stencil thickness is 0.10-0.12 mm (.004-.005 in.) with stencil opening size 0.025 mm (.0010 in.) less than the device pad size. As when heat sinking any power device, it is recommended that, wherever possible, extra PCB copper area is allowed. For minimum parasitic capacitance, do not allow any signal, ground or power signals beneath any of the pads of the device.

Thermal Resistances

Symbol	Parameter	Value	Unit
$R_{th(j-a)}$	Junction to leads (package)	116	°C/W

Reflow Profile

Profile Feature	Pb-Free Assembly
Average Ramp-Up Rate (Tsmax to Tp)	3 °C/sec. max.
Preheat - Temperature Min. (Tsmin) - Temperature Max. (Tsmax) - Time (tsmin to tsmax)	 150 °C 200 °C 60-180 sec.
Time maintained above: - Temperature (TL) - Time (tL)	 217 °C 60-150 sec.
Peak/Classification Temperature (Tp)	260 °C
Time within 5 °C of Actual Peak Temp. (tp)	20-40 sec.
Ramp-Down Rate	6 °C/sec. max.
Time 25 °C to Peak Temperature	8 min. max.



Specifications are subject to change without notice.
Users should verify actual device performance in their specific applications.
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C650 and C850 Series TBU® High-Speed Protectors

BOURNS®

How to Order

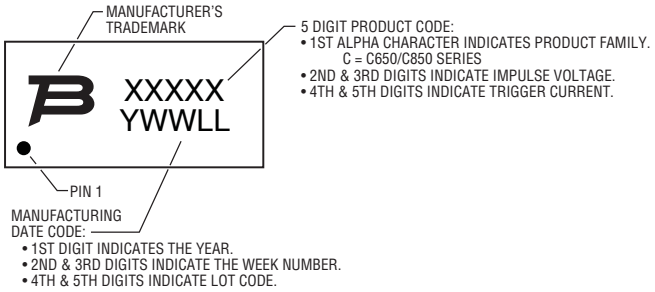
C 650 - 180 - WH

Form Factor
C = One TBU® protector in the device

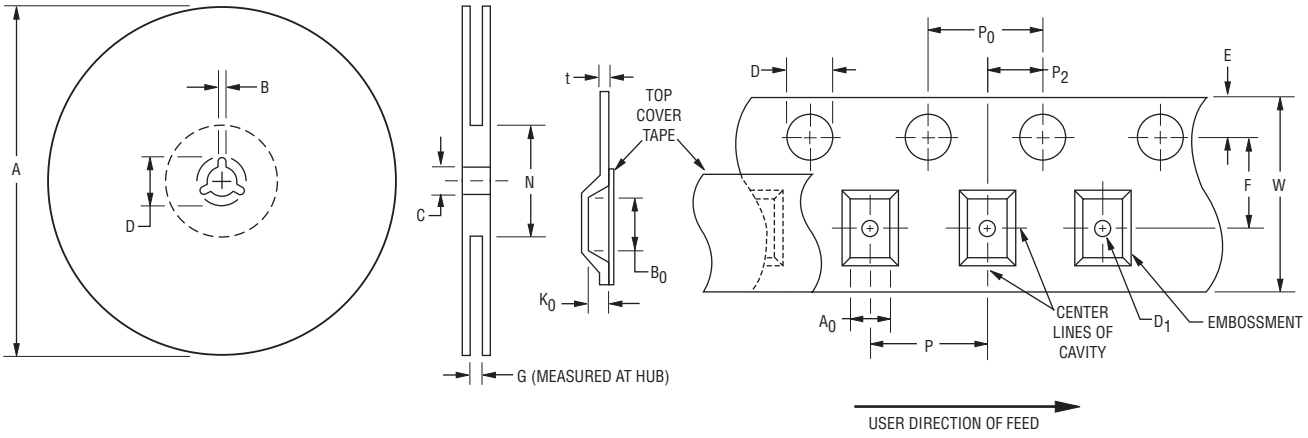
Impulse Voltage Rating
650 = 650 V
850 = 850 V

Iop Indicator
100 = 100 mA
180 = 180 mA
260 = 260 mA

Typical Part Marking



Packaging Specifications (per EIA468-B)



QUANTITY: 3000 PIECES PER REEL

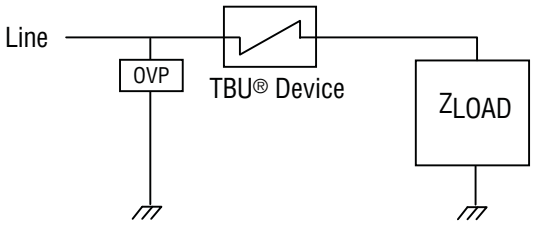
Device	A		B		C		D		G	N
	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Ref.	Ref.
C650, C850	326 (12.835)	330.25 (13.002)	1.5 (.059)	2.5 (.098)	12.8 (.504)	13.5 (.531)	20.2 (.795)	-	16.5 (.650)	102 (4.016)

Device	A_0		B_0		D		D_1		E		F	
	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	max.
C650, C850	4.2 (.165)	4.4 (.173)	8.45 (.333)	8.65 (.341)	1.5 (.059)	1.6 (.063)	1.5 (.059)	-	1.65 (.065)	1.85 (.073)	7.4 (.291)	7.6 (.299)
Device	K_0		P		P_0		P_2		t		W	
	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
C650, C850	1.1 (.043)	1.3 (.051)	7.9 (.311)	8.1 (.319)	3.9 (.159)	4.1 (.161)	1.9 (.075)	2.1 (.083)	0.25 (.010)	0.35 (.014)	15.7 (.618)	16.3 (.642)

DIMENSIONS: MM (INCHES)

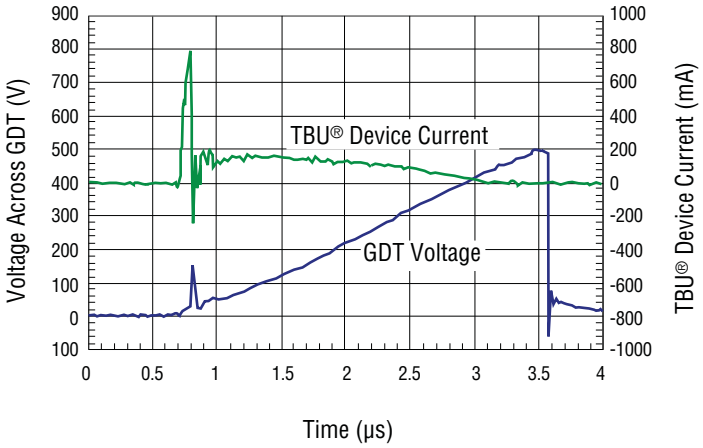
Reference Application

The C-series devices are general protectors that can be used in a variety of applications. The basic operation of the device will be demonstrated using the single line application shown in the figure below. The test circuit was subjected to a 1000 V, 10/700 μs surge waveform. The devices used were the TBU-C850-100-WH and a 2031-42T-SM-RPLF GDT (OVP) with a 10 ohm resistor for the load impedance.



General Application Circuit

The graph below shows the waveforms for the voltage across the overvoltage protector (GDT) and the current through the TBU® device. As the input line voltage increases, the current through the TBU® device increases rapidly until the trip current is reached. Due to finite reaction time for fast transients, the peak level may exceed the low frequency data sheet maximum for a very short period, typically ~100 ns. After this initial overshoot, the TBU® device will transition to the protected state, setting the current to the nominal current limiting level (~150 mA for this example). The TBU® device will then reduce the current down it to its very low quiescent level of 1 mA, typically. As the input line voltage increases to about 500 V, the GDT is triggered, reducing the input line voltage to a very low level which prevents the TBU® device from being subjected to a voltage level which exceeds its maximum rating (850 V in this example). The TBU® High-Speed Orotector and the GDT will remain in these states until the surge ends, which is about 700 μs later in this example. Only the first 4 μs of the surge are shown in the graph. For surges or AC voltages below the GDT breakover voltage, the GDT will not activate, and the TBU® device will stay in the protecting mode, blocking high voltages from the protected equipment.



TBU-C850-100-WH Response to a 1000 V, 10/700 μs Surge

REV. 09/15

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