

●Block Diagram

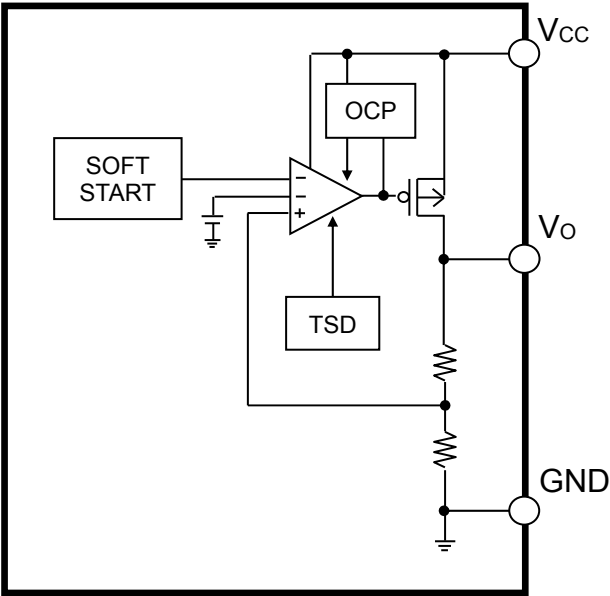
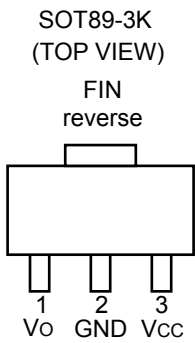


Figure. 1 Block Diagram

●Pin Configuration



●Pin Description

Pin No.	Pin name	Pin Function
1	Vo	Output pin
2	GND	GND pin
3	Vcc	Input pin
reverse	FIN	GND (Connected to 2pin)

●Absolute Maximum Ratings (Ta=25°C)

Parameter		Symbol	Limits	Unit
Power supply voltage		V _{CC}	-0.3 to +30.0 * ¹	V
Output voltage		V _O	-0.3 to +18	V
Power dissipation	SOT89-3K	P _D * ²	1.67 * ²	W
Operating temperature range		T _a	-25 to +85	°C
Storage temperature range		T _{stg}	-55 to +150	°C
Maximum junction temperature		T _{jmax}	+150	°C

*¹ Not to exceed P_D.

*² In case Ta ≥ 25°C (114.3mm × 76.2mm × 1.6mm when mounted on a 4-layer PCB based on JEDEC) is reduced by 13.4mW/°C

●Recommended Operating Conditions (Ta=25°C)

Parameter	Symbol	Min.	Max.	Unit
Input power supply voltage	V _{CC}	V _O +3.0	25.0	V
Output current	I _O	0.0	0.1	A

●Recommended Operating Condition

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Output Capacitor	C _{OUT}	0.3 * ³	1.0	-	μF	Ceramic capacitor recommended

*³ The minimum value of capacitor must met this specification over full operating conditions. (Ex: Temperature, DC bias)

●Electrical Characteristics (Unless otherwise specified, V_{CC}= V_O+5V, Ta=25°C)

Parameter	Symbol	Limits			Unit	Conditions
		Min.	Typ.	Max.		
Bias current	I _{CC}	-	300	450	μA	I _O =0A, V _O =3.3V
		-	300	450	μA	I _O =0A, V _O =5.0V
		-	300	450	μA	I _O =0A, V _O =5.4V
		-	400	600	μA	I _O =0A, V _O =12.0V
Line Regulation	Reg.I	-1	0.5	1	%	V _{CC} =(V _O +3V)→25.0V
Load Regulation	Reg I _O	-1.5	0.5	1.5	%	I _O =0→0.1A
Minimum dropout voltage	V _{CO}	-	1.0	3.0	V	I _O =0.1A
Output voltage	V _O	V _O × 0.99	V _O	V _O × 1.01	V	I _O =0A

●Performance Curve (Reference Data)

■ BD54FA1FP3

(Unless otherwise specified, Ta=25°C, Vcc=Vo+5V, C_{IN}=C_{OUT}=1μF)

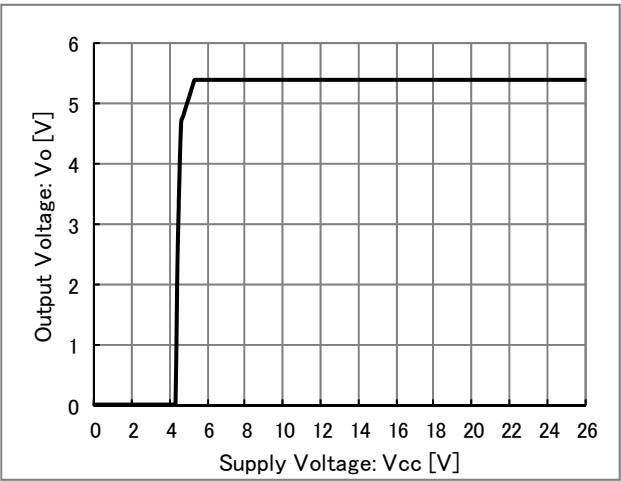


Figure 2. Vcc - Vo

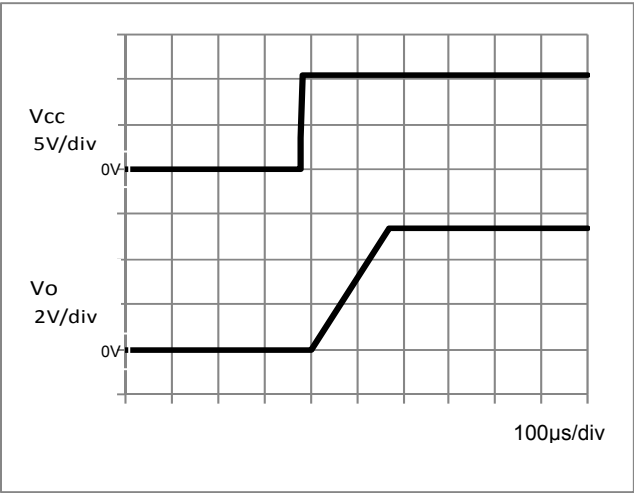


Figure 3. Input sequence
(C_{OUT} = 1μF)

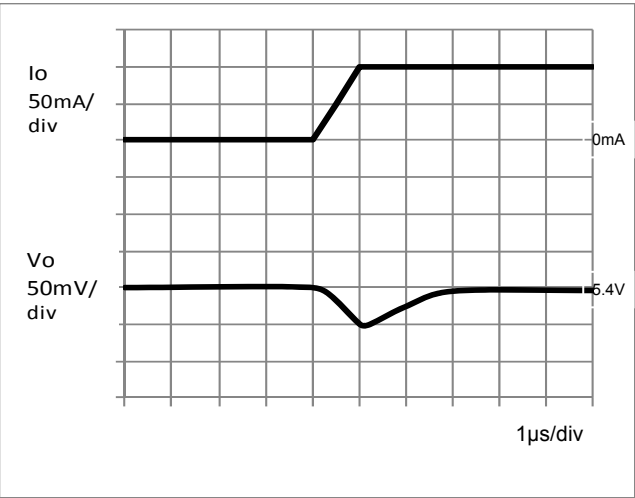


Figure 4. Transient Response
(I_O = 0A→0.1A)
(C_{OUT} = 1μF)

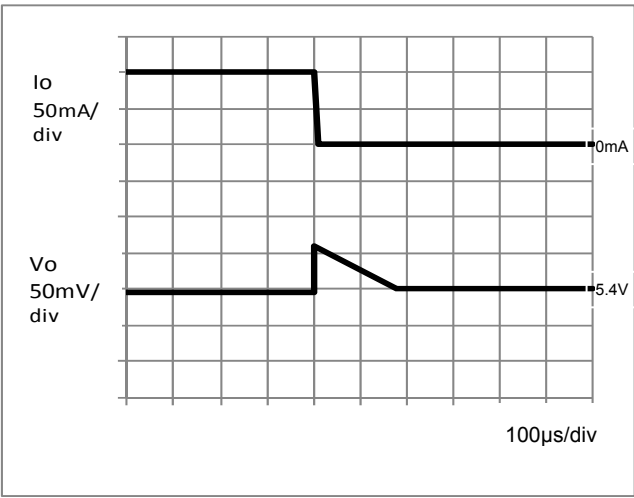


Figure 5. Transient Response
(I_O = 0.1A→0A)
(C_{OUT} = 1μF)

●Performance Curve (Reference Data)

■ BD54FA1FP3

(Unless otherwise specified, Ta=25°C, Vcc=Vo+5V, C_{IN}=C_{OUT}=1μF)

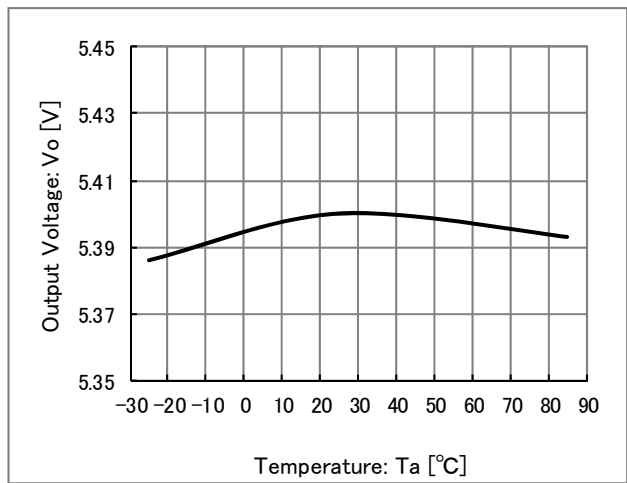


Figure 6. $T_a - V_o$
($I_o = 0\text{mA}$)

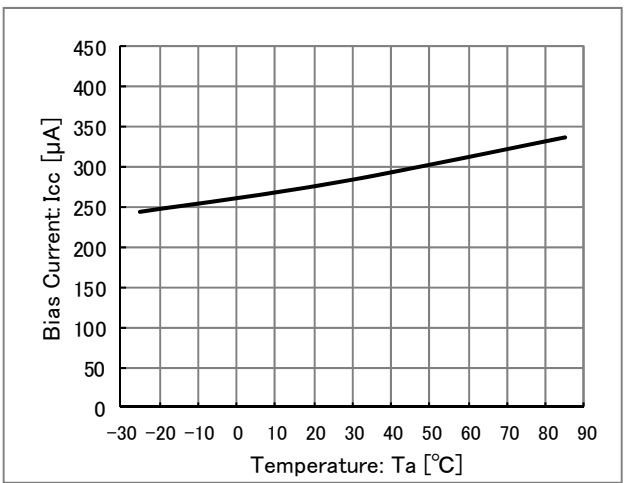


Figure 7. $T_a - I_{cc}$

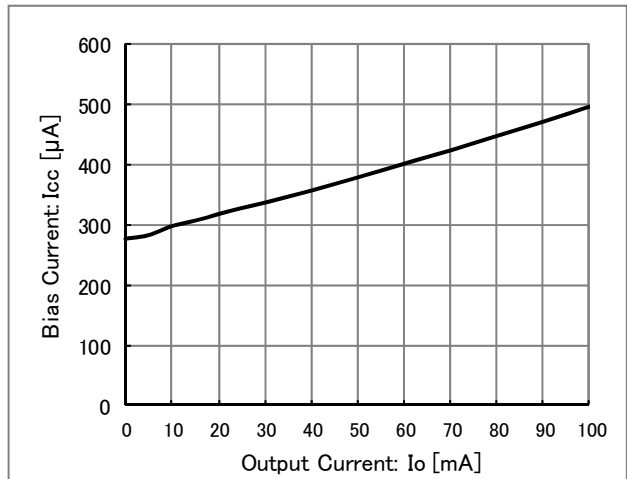


Figure 8. $I_o - I_{cc}$

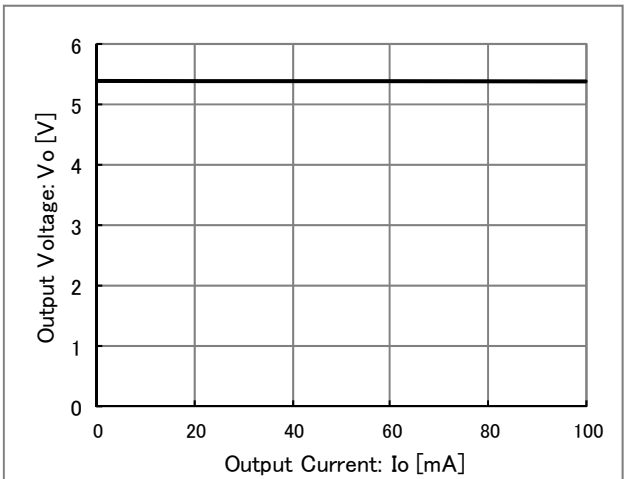


Figure 9. $I_o - V_o$

●Performance Curve (Reference Data)

■ BD54FA1FP3

(Unless otherwise specified, Ta=25°C, Vcc=Vo+5V, C_{IN}=C_{OUT}=1μF)

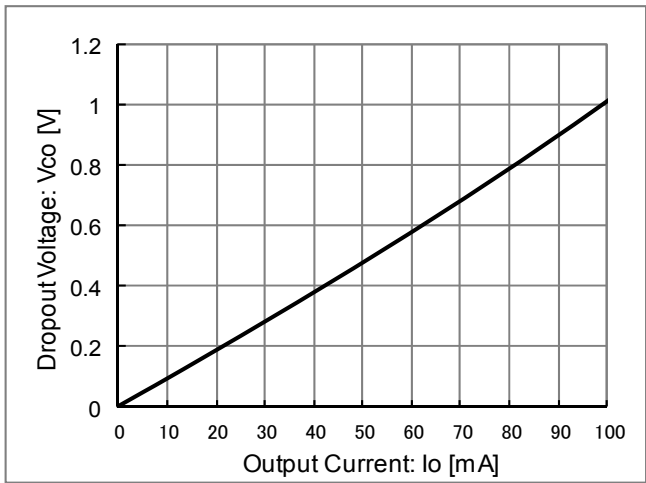


Figure 10. Minimum dropout Voltage

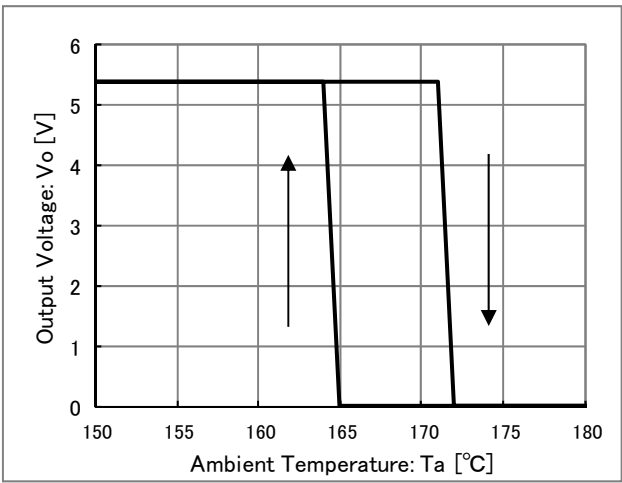


Figure 11. TSD
(Io = 0mA)

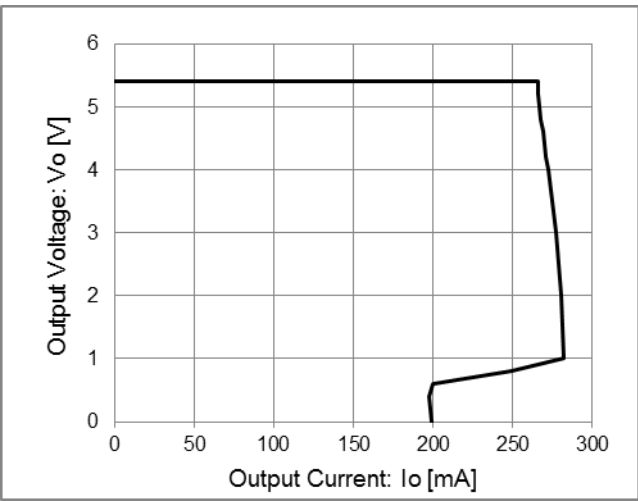


Figure 12. OCP

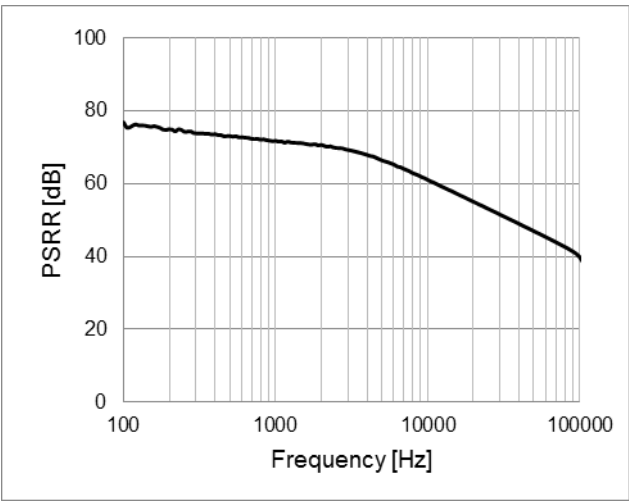


Figure 13. PSRR
(Io = 50mA)

●Performance Curve (Reference Data)

■ BD54FA1FP3

(Unless otherwise specified, Ta=25°C, Vcc=10.4V, CIN=COUT=1μF)

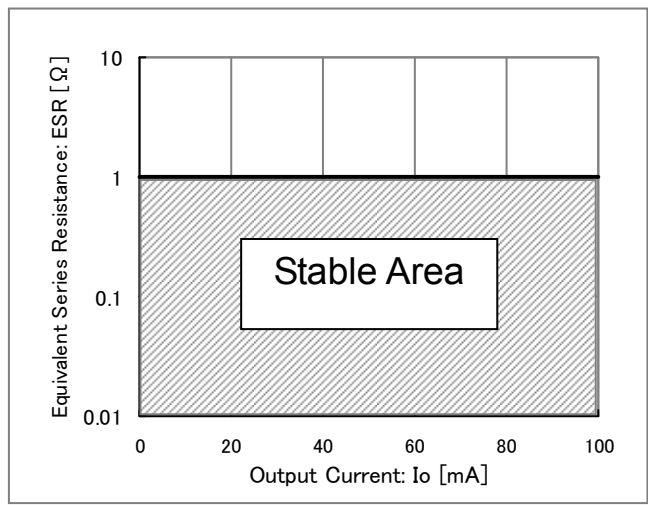
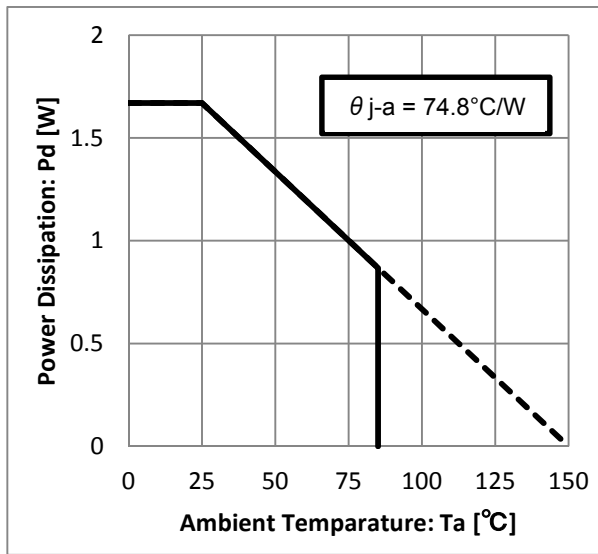


Figure 14. ESR Stable Region

●Power Dissipation

◎SOT89-3K



Measurement condition: mounted on 4-layer JEDEC standard board
Board size: 114.3mm × 76.2mm × 1.6mm

When considering thermal design, operation should be maintained within the following conditions.
(The temperature mentioned below is a guaranteed temperature, therefore, margins must be considered.)

1. Ambient temperature T_a is 85°C and below.
2. Junction temperature T_j is 150°C and below.

The junction temperature T_j can be determined as follows:

Calculation based on ambient temperature T_a

$$T_j = T_a + \theta_{j-a} \times W$$

<Reference Value>

- θ_{j-a} : SOT89-3K 74.8°C/W JEDEC standard 4 layers PCB
Board size: 114.3mm × 76.2mm × 1.6mm

Most of the heat loss that occurs in BDxxFA1FP3 is generated from the output Pch FET. Power loss is determined by the product of voltage drop across $V_{cc}-V_o$ and the output current. Check the conditions of output voltage and output current to be used between $V_{cc}-V_o$ and compare with the power dissipation characteristics.

In addition, power dissipation may change significantly due to board conditions because BDxxFA1FP3 uses power package. It is important to consider the board size to be used before proceeding with the design.

$$\text{Power consumption [W]} = \{ \text{Input voltage (Vcc)} - \text{Output voltage (Vo)} \} \times \text{Output current (Io: Ave)}$$

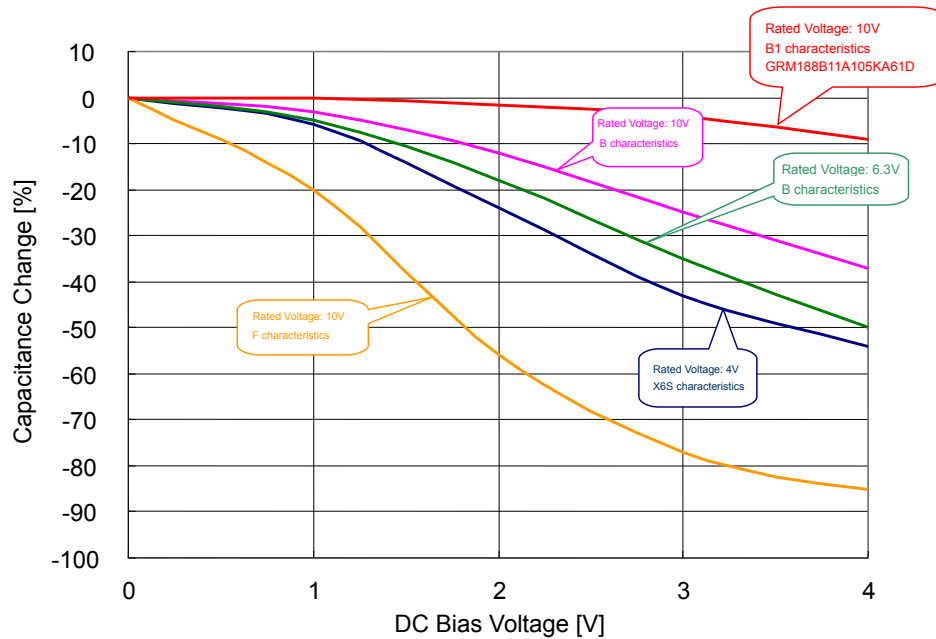
Example) $V_{cc} = 10.4\text{V}$, $V_o = 5.4\text{V}$, $I_o(\text{Average}) = 0.1\text{A}$

$$\begin{aligned} \text{Power consumption [W]} &= (10.4\text{V} - 5.4\text{V}) \times 0.1\text{A} \\ &= 0.5\text{W} \end{aligned}$$

●Input/Output Capacitor

It is recommended that a capacitor is placed close to pin between input pin and GND as well as output pin and GND. The input capacitor becomes more necessary when the power supply impedance is high or when the PCB trace has significant length. Moreover, the higher the capacitance of the output capacitor the more stable the output will be, even with load and line voltage variations. However, please check the actual functionality by mounting on a board for the actual application. Also, ceramic capacitors usually have different thermal and equivalent series resistance characteristics and may degrade gradually over continued use.

For additional details, please check with the manufacturer and select the best ceramic capacitor for your application.



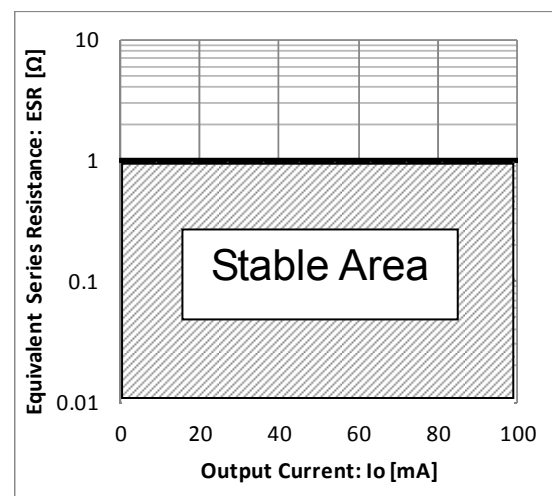
Ceramic Capacitor Capacitance Value - DC Bias Characteristics
(Characteristics Example)

●Output Capacitor Equivalent Series Resistance

To prevent oscillation, please attach a capacitor between V_O and GND. Generally, capacitor has ESR (Equivalent Series Resistance). Operation will be stable in ESR-I_o range*¹ shown in the right.

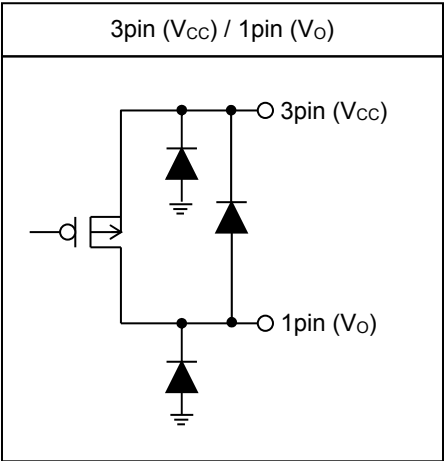
The 1.0 μ F ceramic capacitor and resistor at output in this characteristic data are connected in series and measured. Generally, ESR of ceramic capacitor, tantalum capacitor and electrolytic capacitor is different. Check the ESR of capacitor to be used and use it within the range of stable region.

However, please take note that for the same value of capacitance of different electrolytic capacitor, ESR are not always the same. In addition, ESR characteristics may also change due to wiring impedance of board, input power impedance and load impedance; therefore check the behavior in actual application.



*1 $T_a=25^\circ\text{C}$, $V_{CC}=6.3\text{V}$ to 25V , $I_o=0\text{A}$ to 0.1A

●Input/Output Equivalent Circuit



●Operational Notes

- (1) Absolute Maximum Value Rate
Operating the IC over the absolute maximum ratings may damage the IC. In addition, it is impossible to predict all destructive situations such as short-circuit modes, open circuit modes, etc. Therefore, it is important to consider circuit protection measures, like adding a fuse, in case the IC is operated in a special mode exceeding the absolute maximum ratings.
- (2) Reverse connection of power supply
Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply terminals.
- (3) Power supply line
Design the PCB layout pattern to provide low impedance ground and supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.
- (4) Ground voltage
The voltage of the ground pin must be the lowest voltage of all pins of the IC at all operating conditions. Ensure that no pins are at a voltage below the ground pin at any time, even during transient condition.
- (5) Thermal consideration
Use a thermal design that allows for a sufficient margin by taking into account the permissible power dissipation (Pd) in actual operating conditions.
- (6) Short between pins and mounting errors
Be careful when mounting the IC on printed circuit boards. The IC may be damaged if it is mounted in a wrong orientation or if pins are shorted together. Short circuit may be caused by conductive particles caught between the pins.
- (7) Operation under strong electromagnetic field
Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.
- (8) Thermal shutdown circuit
The IC incorporates a built-in thermal shutdown circuit, which is designed to turn off the IC when the internal temperature of the IC reaches a specified value. It is not designed to protect the IC from damage or guarantee its operation. Do not continue to operate the IC after this function is activated. Do not use the IC in conditions where this function will always be activated.

	TSD ON Temperature [°C] (Typ)	Hysteresis Temperature [°C] (Typ)
BDxxFA1FP3	173	8

- (9) Testing on application boards
When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from electro static discharge, ground the IC during assembly and use similar precautions during transport and storage.

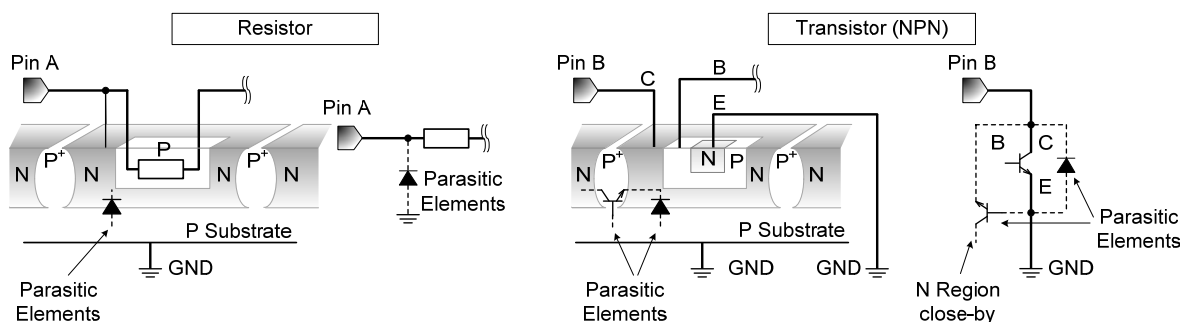
(10) Regarding input pins of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When $GND > Pin A$ and $GND > Pin B$, the P-N junction operates as a parasitic diode.

When $GND > Pin B$, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

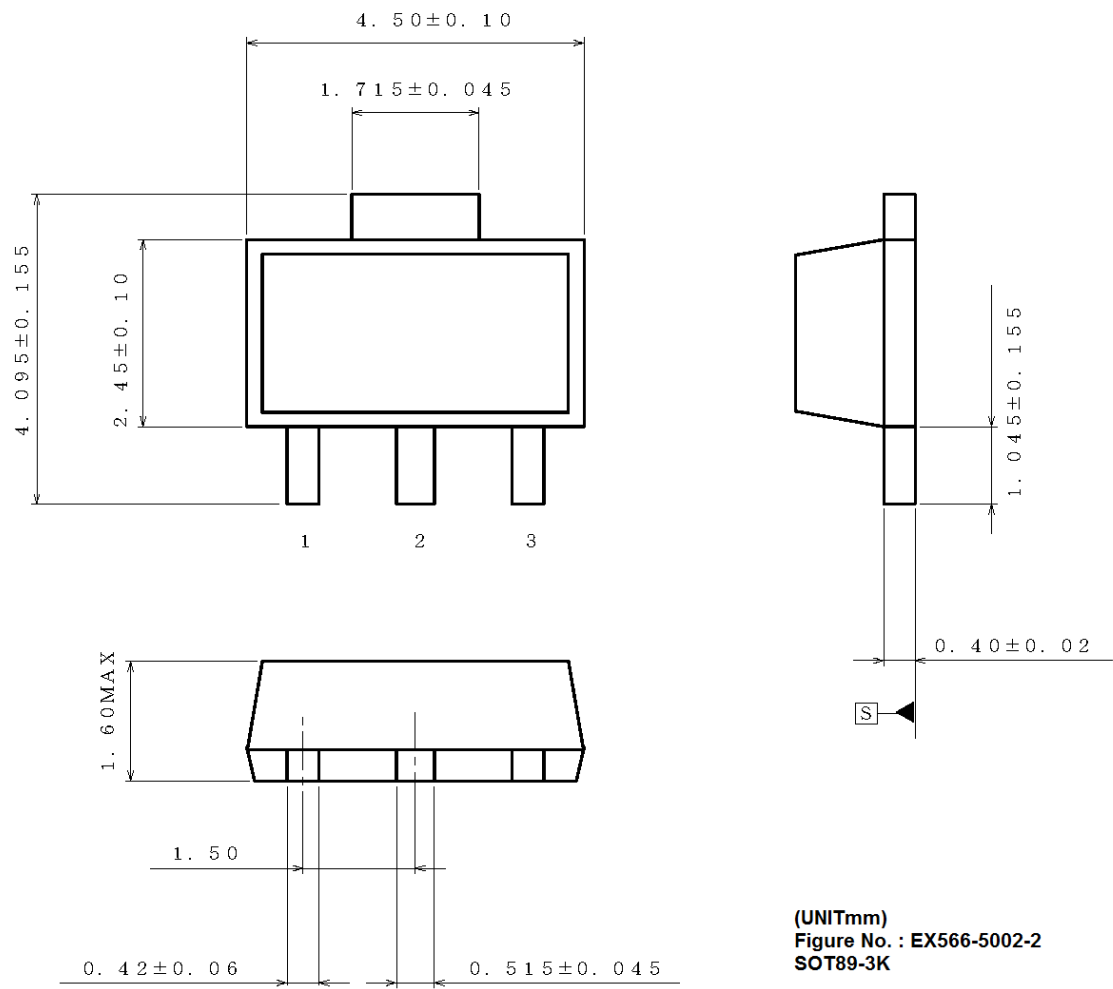


(11) Ground wiring pattern

When using both small-signal and large-current GND traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the GND traces of external components do not cause variations on the GND voltage. The power supply and ground lines must be as short and thick as possible to reduce line impedance.

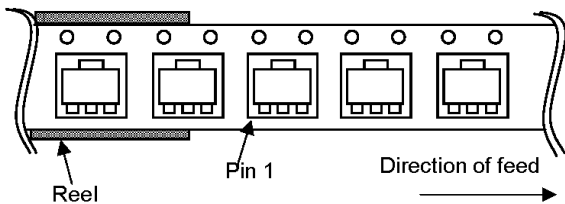
●External Measurement Drawing and Packing Forming Specification

Package Name	SOT89-3K
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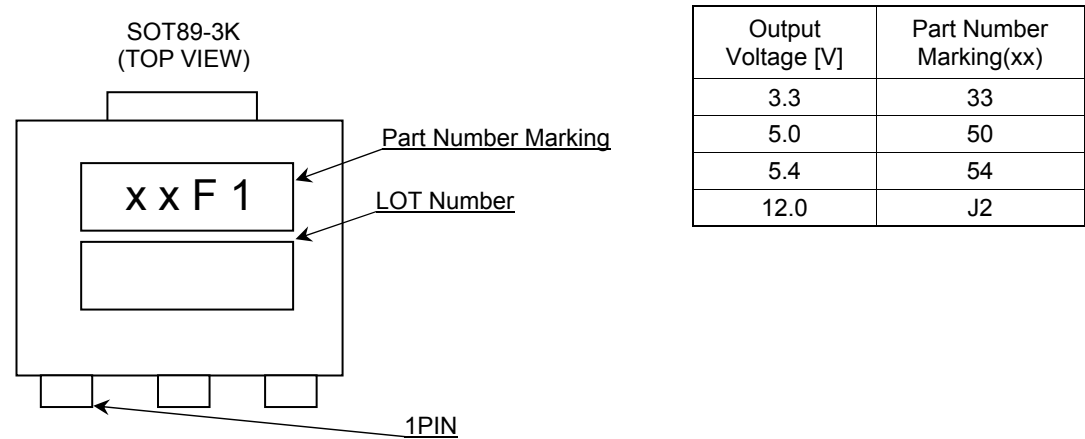


< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	1000pcs
Direction of feed	TL The direction is the pin 1 of product is at the lower left when you hold reel on the left hand and you pull out the tape on the right hand



●Marking Diagram



●Revision History

Date	Revision	Revision contents
2014.02.04	001	New release
2014.10.31	002	Added 5.0V and 12V to output voltage line-up.
2015.06.08	003	The document control number: TSZ02201-0R6R0A600600-1-2 →TSZ02201-0GAG0A600600-1-2. Modified the package name to SOT89-3K. Modified external measurement drawing.
2016.04.11	004	P.1 Ordering Information changed P.3 Electrical characteristics added P.6 Figure 13. PSRR modified from (I _o =0mA) to (I _o =50mA) The document control number: TSZ02201-0R6R0A600600-1-2 →TSZ02201-0G2G0A600060-1-2

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JAPAN	USA	EU	CHINA
CLASS III	CLASS III	CLASS II b	CLASS III
CLASS IV		CLASS III	

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- In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.
- De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.
- Confirm that operation temperature is within the specified range described in the product specification.
- ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

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- When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.
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 - [d] the Products are exposed to high Electrostatic
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