**Static @ $T_J$ = 25°C (unless otherwise specified)**

| | Parameter | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| $V_{(BR)DSS}$ | Drain-to-Source Breakdown Voltage | -150 | — | — | V | $V_{GS}$ = 0V, $I_D$ = -250µA |
| $\Delta V_{(BR)DSS}/\Delta T_J$ | Breakdown Voltage Temp. Coefficient | — | -0.20 | — | V/°C | Reference to 25°C, $I_D$ = -1mA ① |
| $R_{DS(on)}$ | Static Drain-to-Source On-Resistance | — | — | 0.295 | Ω | $V_{GS}$ = -10V, $I_D$ = -6.6A ④ |
| | | — | — | 0.58 | | $V_{GS}$ = -10V, $I_D$ = -6.6A ④$T_J$ =150°C |
| $V_{GS(th)}$ | Gate Threshold Voltage | -2.0 | — | -4.0 | V | $V_{DS}$ = $V_{GS}$, $I_D$ = -250µA |
| gfs | Forward Trans conductance | 3.6 | — | — | S | $V_{DS}$ = -50V, $I_D$ = -6.6A ⑥ |
| $I_{DSS}$ | Drain-to-Source Leakage Current | — | — | -25 | µA | $V_{DS}$ = -150 V, $V_{GS}$ = 0V |
| | | — | — | -250 | | $V_{DS}$ = -120V,$V_{GS}$ = 0V,$T_J$ =150°C |
| $I_{GSS}$ | Gate-to-Source Forward Leakage | — | — | -100 | nA | $V_{GS}$ = -20V |
| | Gate-to-Source Reverse Leakage | — | — | 100 | | $V_{GS}$ = 20V |

**Dynamic Electrical Characteristics @ $T_J$ = 25°C (unless otherwise specified)**

| | | | | | | |
|---|---|---|---|---|---|---|
| $Q_g$ | Total Gate Charge | — | — | 66 | nC | $I_D$ = -6.6A |
| $Q_{gs}$ | Gate-to-Source Charge | — | — | 8.1 | | $V_{DS}$ = -120V |
| $Q_{gd}$ | Gate-to-Drain Charge | — | — | 35 | | $V_{GS}$ = -10V, See Fig 6 and 13 ④ |
| $t_{d(on)}$ | Turn-On Delay Time | — | 14 | — | ns | $V_{DD}$ = -75V |
| $t_r$ | Rise Time | — | 36 | — | | $I_D$ = -6.6A |
| $t_{d(off)}$ | Turn-Off Delay Time | — | 53 | — | | $R_G$ = 6.8Ω |
| $t_f$ | Fall Time | — | 37 | — | | $R_D$ = 12Ω, See Fig 10 ④ |
| $L_D$ | Internal Drain Inductance | — | 4.5 | — | nH | Between lead, 6mm (0.25in.) from package ⑤ and center of die contact |
| $L_S$ | Internal Source Inductance | — | 7.5 | — | | |
| $C_{iss}$ | Input Capacitance | — | 860 | — | pF | $V_{GS}$ = 0V |
| $C_{oss}$ | Output Capacitance | — | 220 | — | | $V_{DS}$ = -25V |
| $C_{rss}$ | Reverse Transfer Capacitance | — | 130 | — | | $f$ = 1.0MHz, See Fig. 5 |

**Diode Characteristics**

| | Parameter | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| $I_S$ | Continuous Source Current (Body Diode) | — | — | -13 | A | MOSFET symbol showing the integral reverse p-n junction diode. |
| $I_{SM}$ | Pulsed Source Current (Body Diode) ① | — | — | -44 | | |
| $V_{SD}$ | Diode Forward Voltage | — | — | -1.6 | V | $T_J$ = 25°C,$I_S$ = -6.6A,$V_{GS}$ = 0V ④⑥ |
| $t_{rr}$ | Reverse Recovery Time | — | 160 | 240 | ns | $T_J$ = 25°C ,$I_F$ = -6.6A |
| $Q_{rr}$ | Reverse Recovery Charge | — | 1.2 | 1.7 | µC | di/dt = 100A/µs ④⑥ |
| $t_{on}$ | Forward Turn-On Time | Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD) | | | | |

**Notes:**

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)

② $V_{DD}$ = -25V, starting $T_J$ = 25°C, L = 14mH, $R_G$ = 25Ω, $I_{AS}$ = -6.6A. (See Fig.12)

③ $I_{SD}$ ≤ -6.6A, di/dt ≤ -620A/µs, $V_{DD}$ ≤ $V_{(BR)DSS}$, $T_J$ ≤ 175°C.

④ Pulse width ≤ 300µs; duty cycle ≤ 2%.

⑤ This is applied for I-PAK, $L_S$ of D-PAK is measured between lead and center of die contact .

⑥ Uses IRF6215 data and test conditions.

⑦ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994

⑧ $R_\theta$ is measured at $T_J$ approximately 90°C.

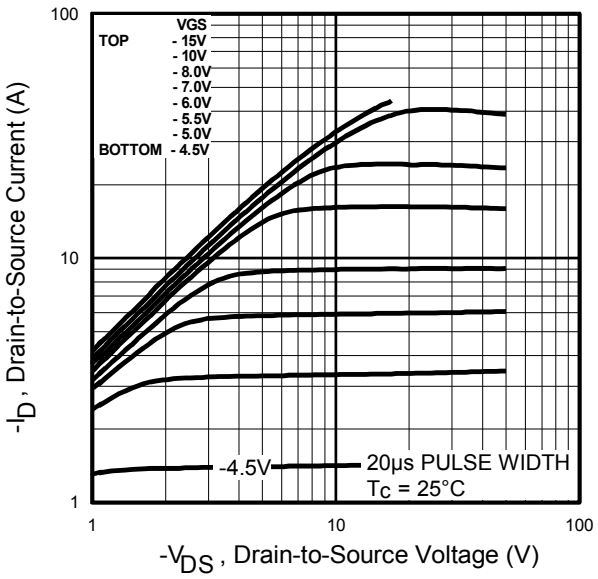



**Fig. 1** Typical Output Characteristics

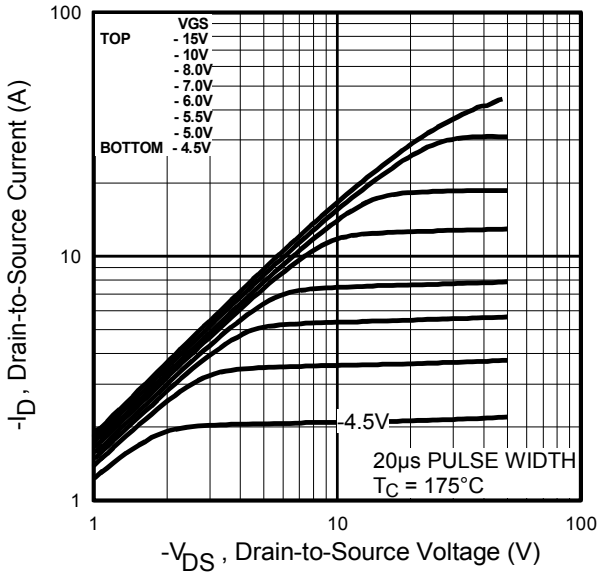



**Fig. 2** Typical Output Characteristics

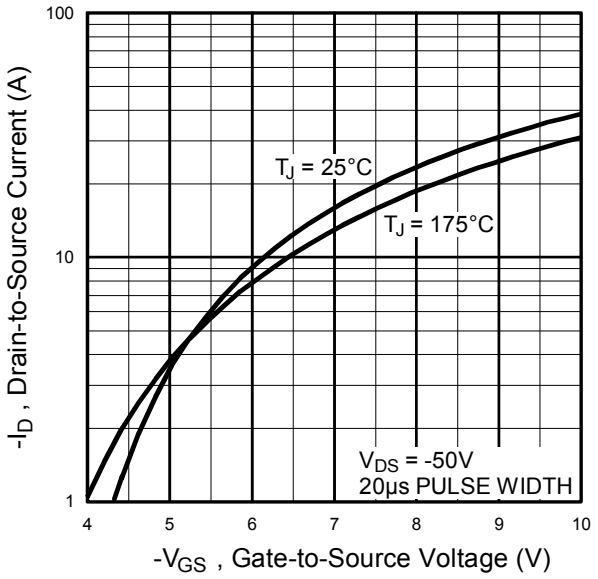



**Fig. 3** Typical Transfer Characteristics

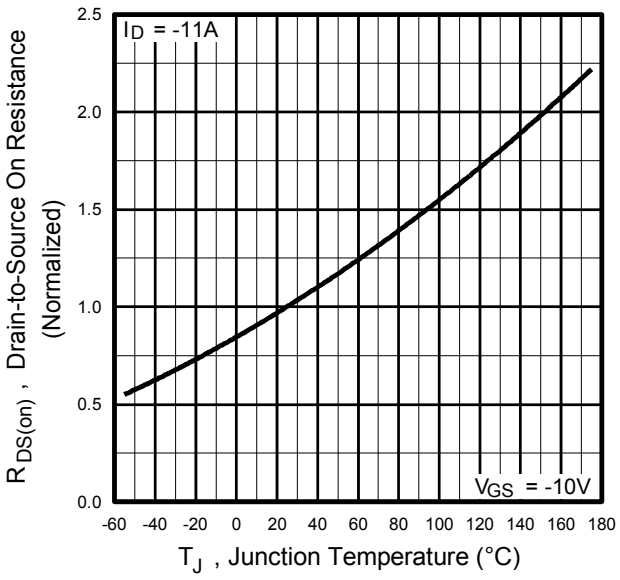



**Fig. 4** Normalized On-Resistance vs. Temperature

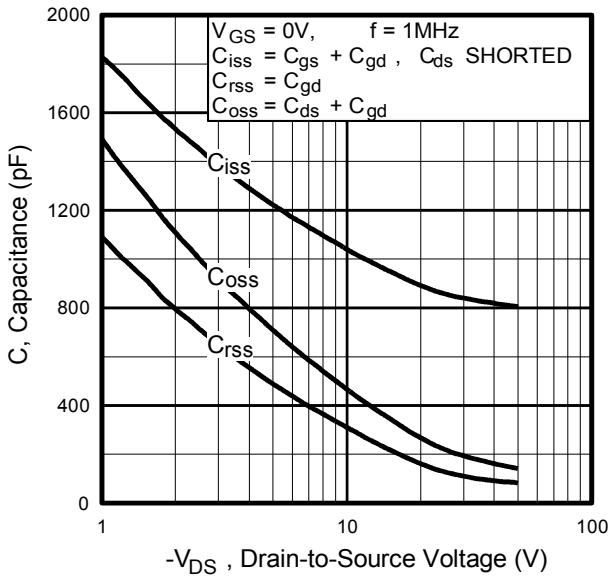



**Fig 5.** Typical Capacitance vs. Drain-to-Source Voltage

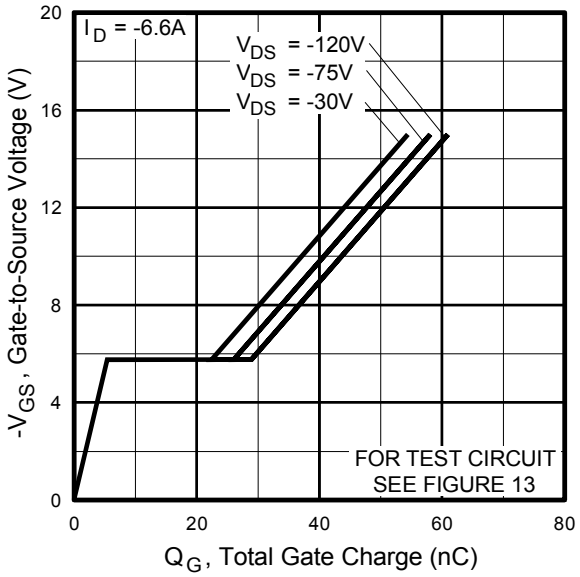



**Fig 6.** Typical Gate Charge vs. Gate-to-Source Voltage

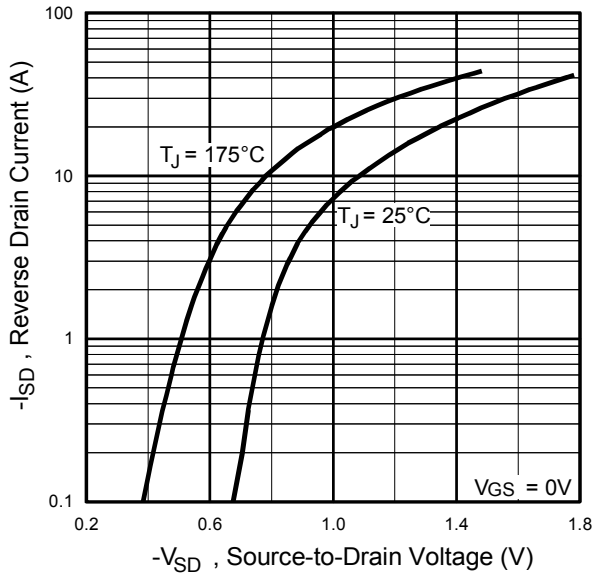



**Fig. 7** Typical Source-to-Drain Diode Forward Voltage

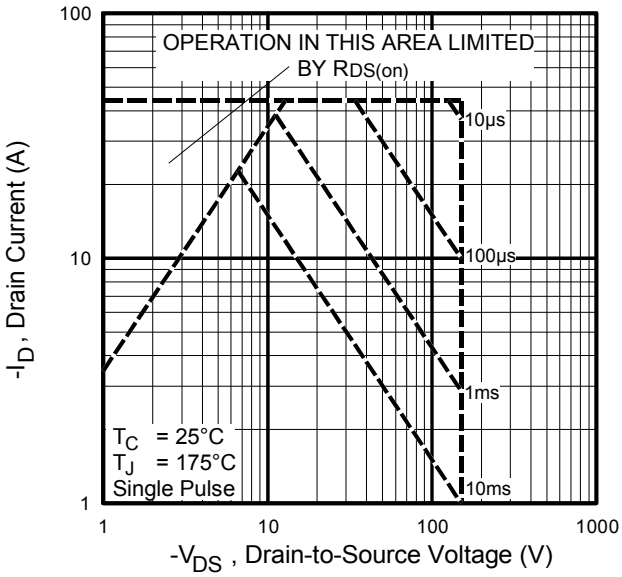



**Fig 8.** Maximum Safe Operating Area

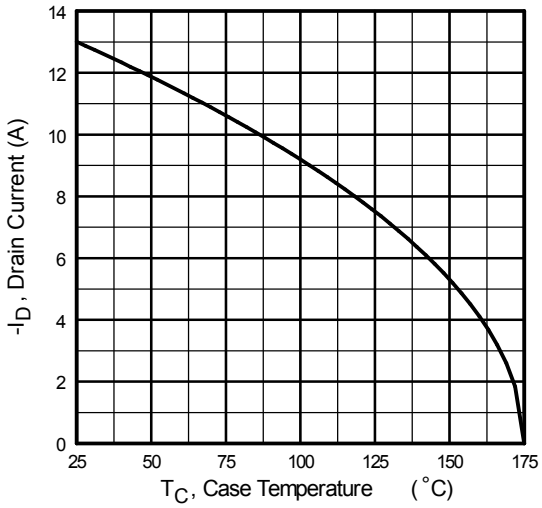



**Fig 9.** Maximum Drain Current vs. Case Temperature

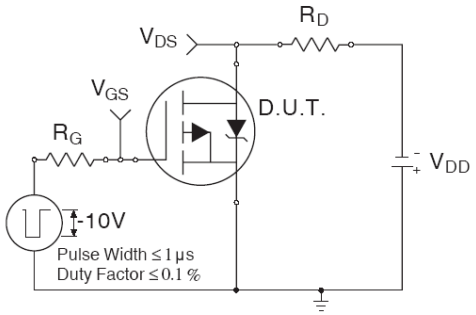



**Fig 10a.** Switching Time Test Circuit

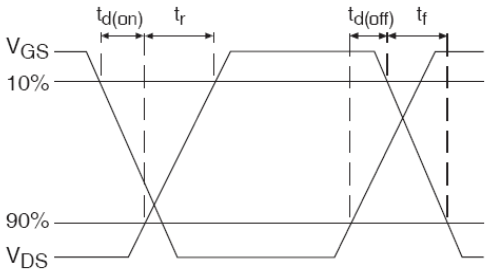



**Fig 10b.** Switching Time Waveforms

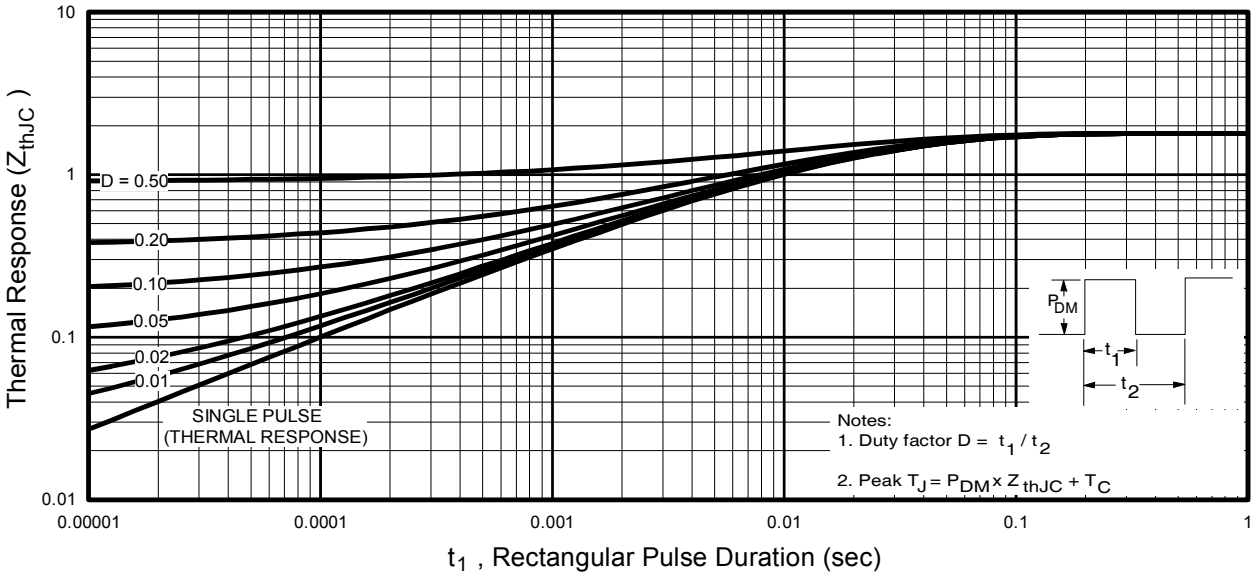



**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

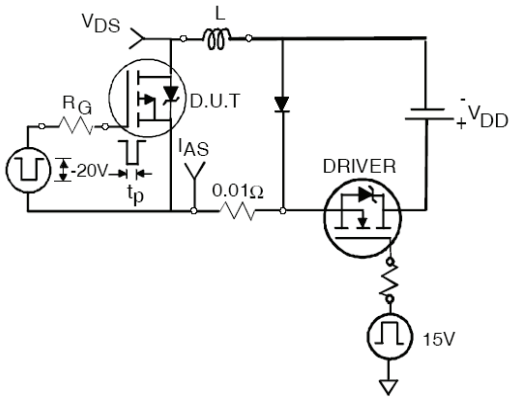



**Fig 12a.** Unclamped Inductive Test Circuit

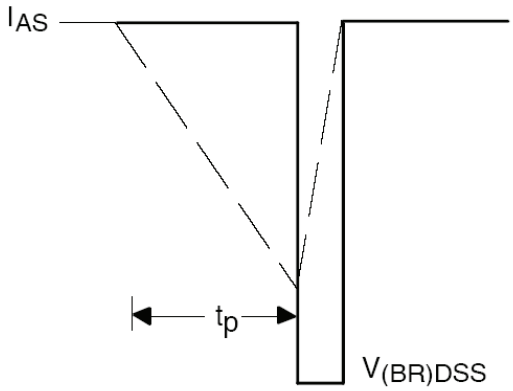



**Fig 12b.** Unclamped Inductive Waveforms

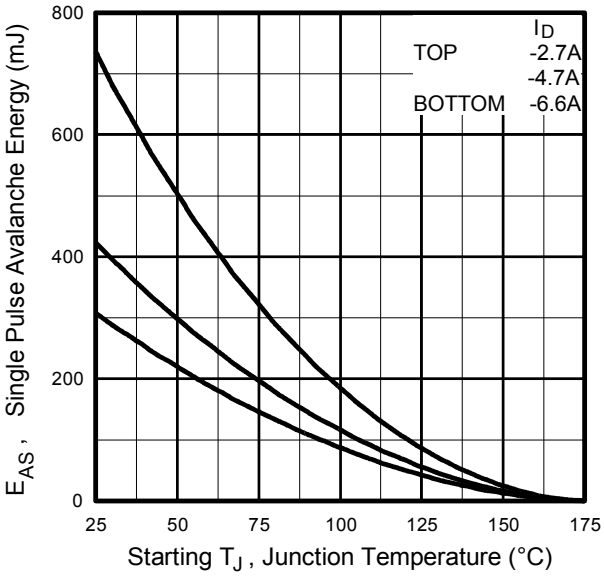



**Fig 12c.** Maximum Avalanche Energy vs. Drain Current

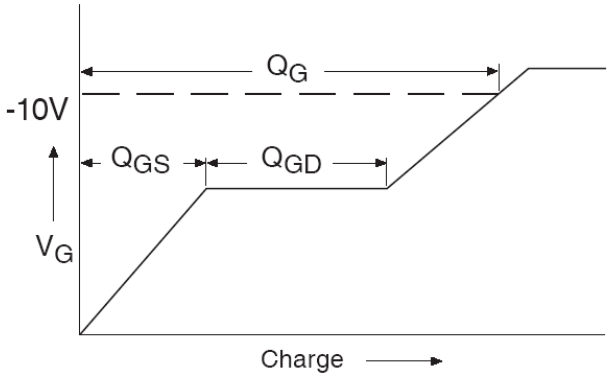



**Fig 13a.** Gate Charge Waveform

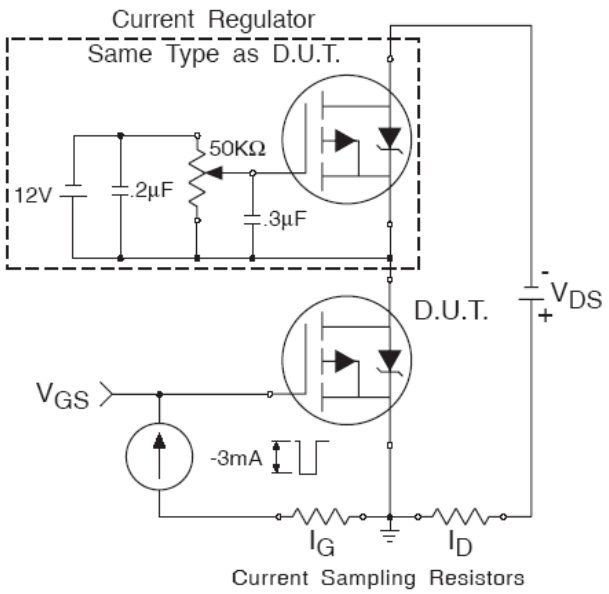
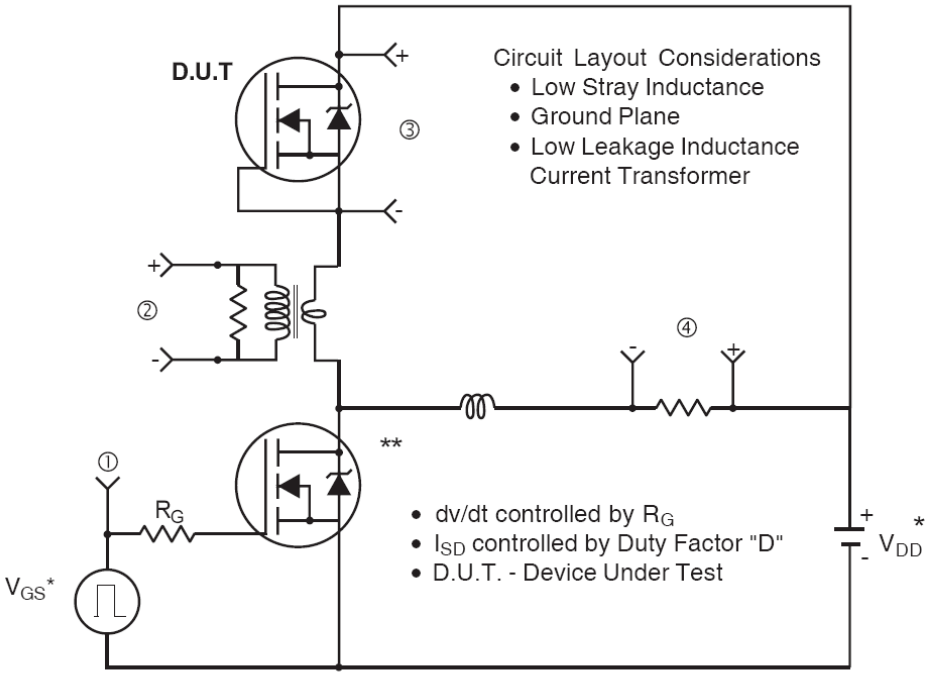
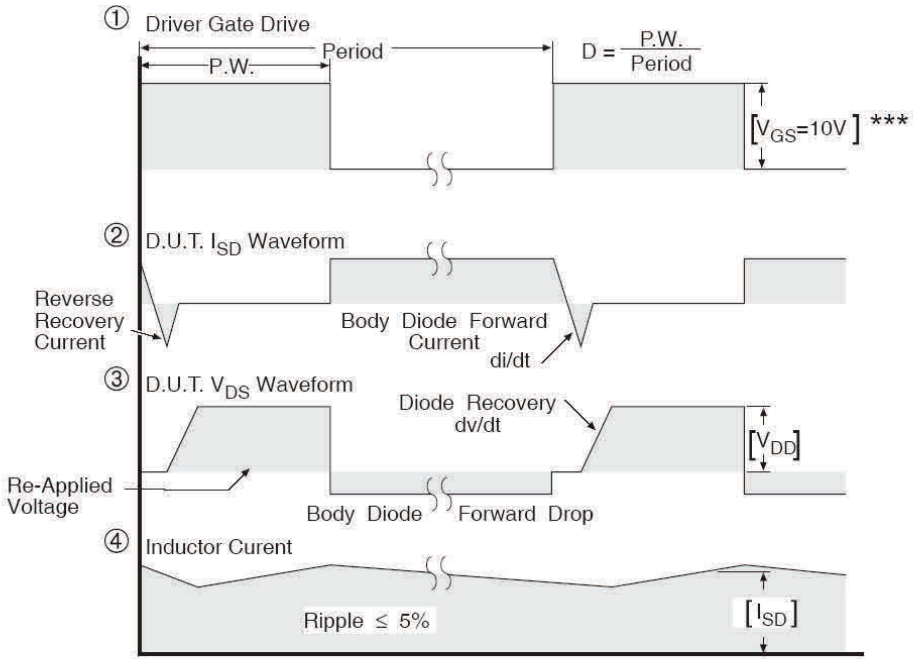



**Fig 13b.** Gate Charge Test Circuit

## Peak Diode Recovery dv/dt Test Circuit



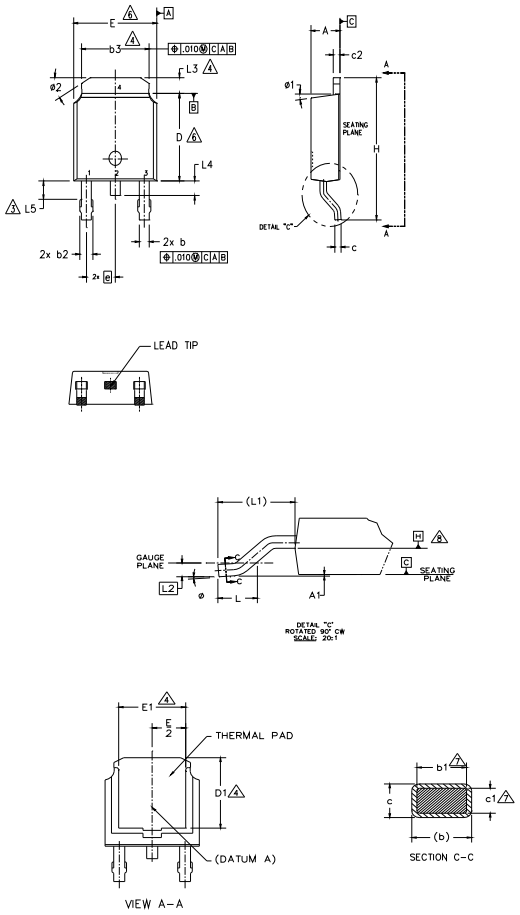

* Reverse Polarity for P-Channel
** Use P-Channel Driver for P-Channel Measurements




*** $V_{GS}$ = 5.0V for Logic Level and 3V Drive Devices

**Fig 14.** Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

## D-Pak (TO-252AA) Package Outline (Dimensions are shown in millimeters (inches))




NOTES:

1.– DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994

2.– DIMENSION ARE SHOWN IN INCHES [MILLIMETERS].

3 – LEAD DIMENSION UNCONTROLLED IN L5.

4 – DIMENSION D1, E1, L3 & b3 ESTABLISH A MINIMUM MOUNTING SURFACE FOR THERMAL PAD.

5.– SECTION C–C DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 AND 0.10 [0.13 AND 0.25] FROM THE LEAD TIP.

6 – DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005 [0.13] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.

7 – DIMENSION b1 & c1 APPLIED TO BASE METAL ONLY.

8 – DATUM A & B TO BE DETERMINED AT DATUM PLANE H.

9.– OUTLINE CONFORMS TO JEDEC OUTLINE TO–252AA.

| SYMBOL | DIMENSIONS | | | | NOTES |
|---|---|---|---|---|---|
| | MILLIMETERS | | INCHES | | |
| | MIN. | MAX. | MIN. | MAX. | |
| A | 2.18 | 2.39 | .086 | .094 | |
| A1 | – | 0.13 | – | .005 | |
| b | 0.64 | 0.89 | .025 | .035 | |
| b1 | 0.65 | 0.79 | .025 | .031 | 7 |
| b2 | 0.76 | 1.14 | .030 | .045 | |
| b3 | 4.95 | 5.46 | .195 | .215 | 4 |
| c | 0.46 | 0.61 | .018 | .024 | |
| c1 | 0.41 | 0.56 | .016 | .022 | 7 |
| c2 | 0.46 | 0.89 | .018 | .035 | |
| D | 5.97 | 6.22 | .235 | .245 | 6 |
| D1 | 5.21 | – | .205 | – | 4 |
| E | 6.35 | 6.73 | .250 | .265 | 6 |
| E1 | 4.32 | – | .170 | – | 4 |
| e | 2.29 BSC | | .090 BSC | | |
| H | 9.40 | 10.41 | .370 | .410 | |
| L | 1.40 | 1.78 | .055 | .070 | |
| L1 | 2.74 BSC | | .108 REF. | | |
| L2 | 0.51 BSC | | .020 BSC | | |
| L3 | 0.89 | 1.27 | .035 | .050 | 4 |
| L4 | – | 1.02 | – | .040 | |
| L5 | 1.14 | 1.52 | .045 | .060 | 3 |
| ø | 0° | 10° | 0° | 10° | |
| ø1 | 0° | 15° | 0° | 15° | |
| ø2 | 25° | 35° | 25° | 35° | |

LEAD ASSIGNMENTS

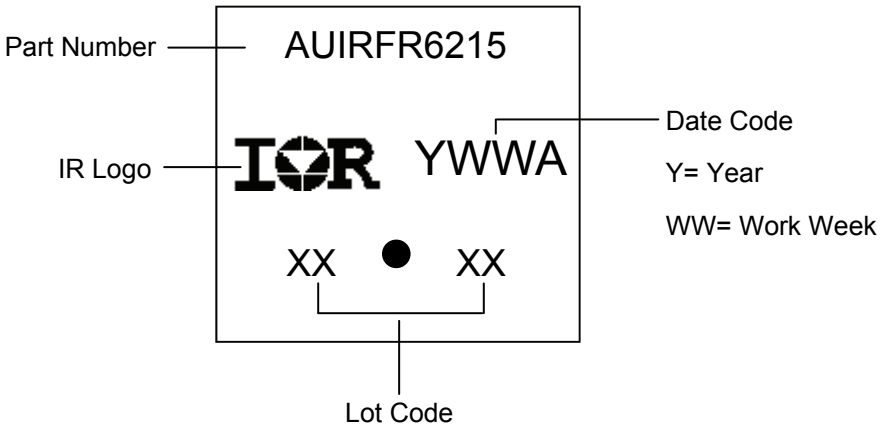
HEXFET

1.– GATE
2.– DRAIN
3.– SOURCE
4.– DRAIN

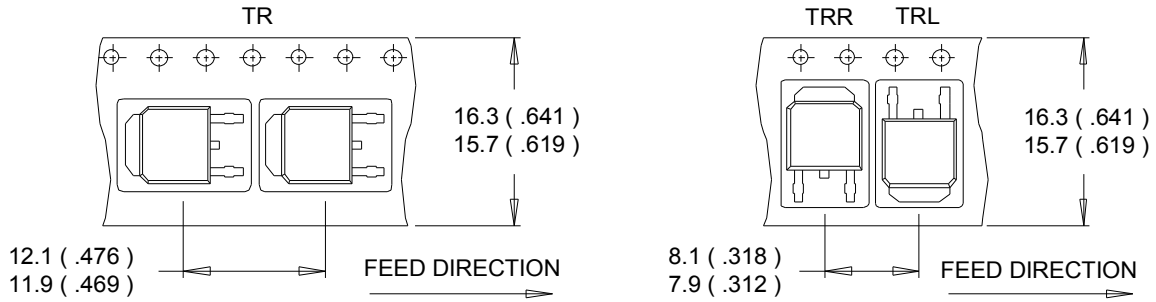
IGBT & CoPAK

1.– GATE
2.– COLLECTOR
3.– EMITTER
4.– COLLECTOR

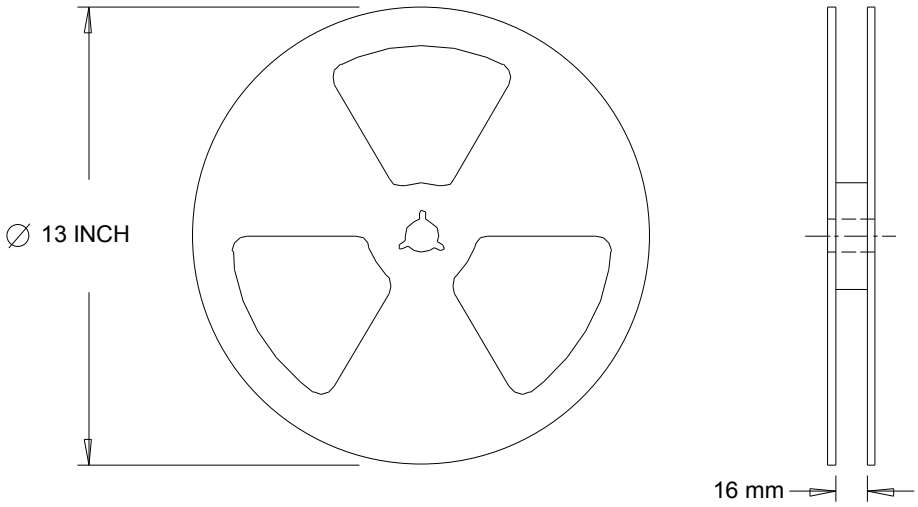
## D-Pak (TO-252AA) Part Marking Information



**D-Pak (TO-252AA) Tape & Reel Information** (Dimensions are shown in millimeters (inches))




NOTES :
1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS ( INCHES ).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.




NOTES :
1. OUTLINE CONFORMS TO EIA-481.

**Qualification Information**

| | | | |
|---|---|---|---|
| **Qualification Level** | | Automotive (per AEC-Q101) | |
| | | Comments: This part number(s) passed Automotive qualification. Infineon's Industrial and Consumer qualification level is granted by extension of the higher Automotive level. | |
| **Moisture Sensitivity Level** | | D-Pak | MSL1 |
| **ESD** | Machine Model | Class M4 † AEC-Q101-002 | |
| | Human Body Model | Class H3A † AEC-Q101-001 | |
| | Charged Device Model | Class C5 † AEC-Q101-005 | |
| **RoHS Compliant** | | Yes | |

† Highest passing voltage.

**Revision History**

| Date | Comments |
|---|---|
| 10/12/2015 | • Updated datasheet with corporate template<br>• Corrected ordering table on page 1. |
| 10/05/2017 | • Corrected typo error on part marking on page 8. |

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