Typical Applications Circuit

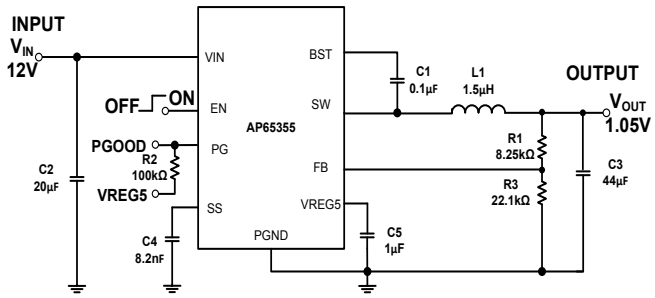
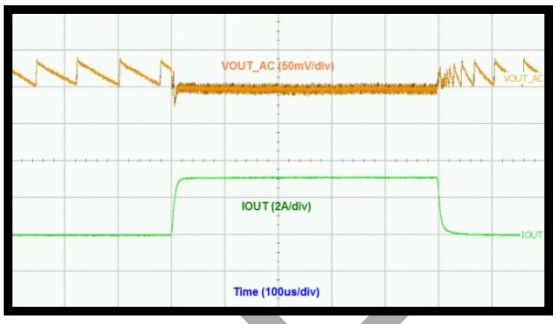


Figure 1 Typical Application Circuit



Pin Descriptions

Pin Name	Package	Function
	U-DFN3030-10	
EN	1	Enable input. EN is a digital input that turns the regulator on or off. Drive EN high to turn on the regulator, drive it low to turn off. EN can be safely connected to VIN directly for automatic startup.
FB	2	Feedback Input. FB senses the output voltage and regulates it. Drive FB with a resistive voltage divider connected to it from the output voltage.
VREG5	3	Internal power supply output pin to connect an additional capacitor. Connect a 1µF (typical) capacitor as close as possible to the VREG5 and PGND. This pin is not active when EN is low.
SS	4	Soft-start control input pin. SS controls the soft start period. Connect a capacitor from SS to PGND to set the soft-start period.
SW	6,7	Power Switching Output. SW is the switching node that supplies power to the output. Connect the output LC filter from SW to the output load. Note that a capacitor is required from SW to BST to power the high-side switch.
BST	8	Bootstrap pin. A bootstrap capacitor is connected between the BST pin and SW pin. The voltage across the bootstrap capacitor drives the internal high-side NMOS switch. A 0.1µF (typical) capacitor is required for proper operation.
VIN	9,10	Supply input. A capacitor should be connected between the VIN pin and PGND pin to keep the DC input voltage constant.
PG	5	Open drain power good output.
PGND	11 (Exposed Pad)	Power ground and GND. Exposed pad must be connected to as large of PGND plane as possible for maximum thermal performance.

Functional Block Diagram

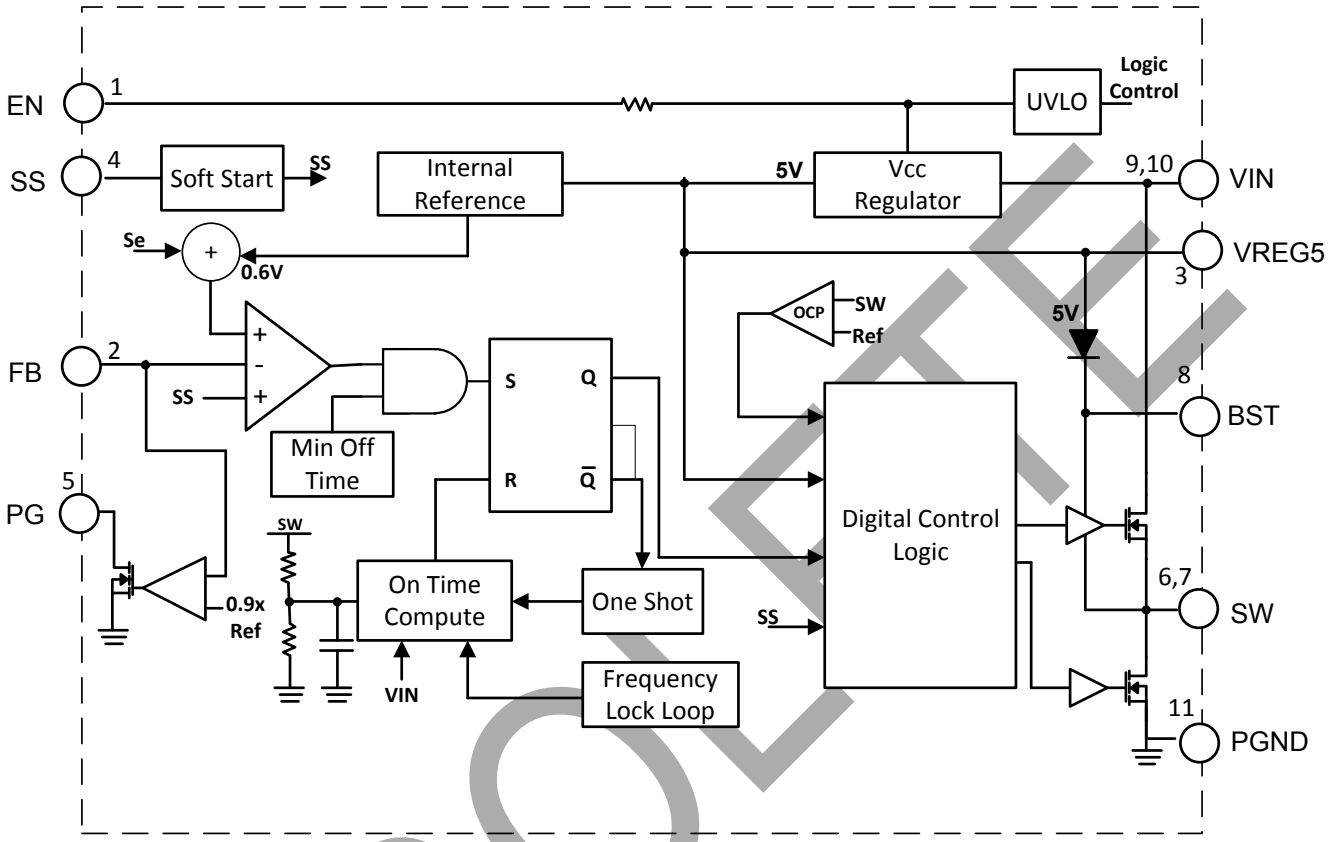


Figure 2 Functional Block Diagram

Absolute Maximum Ratings (Note 4) (@T_A = +25°C, unless otherwise specified.)

Symbol	Parameter	Rating	Unit
V_{IN}	Supply Voltage	-0.3 to 20	V
V_{VREG5}	VREG5 Pin Voltage	-0.3V to +6.0	V
V_{SW}	Switch Node Voltage	-1.0 to VIN +0.3	V
V_{BST}	Bootstrap Voltage	-0.3 to VSW +6.0	V
V_{FB}	Feedback Voltage	-0.3V to +6.0	V
V_{EN}	Enable/UVLO Voltage	-0.3V to VIN	V
V_{SS}	Soft-start PIN	-0.3V to +6.0	V
T_{ST}	Storage Temperature	-65 to +150	°C
T_J	Junction Temperature	+160	°C
T_L	Lead Temperature	+260	°C
ESD Susceptibility (Note 5)			
HBM	Human Body Model	2	kV
MM	Machine Model	200	V

Notes: 4. Stresses greater than the 'Absolute Maximum Ratings' specified above may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions exceeding those indicated in this specification is not implied. Device reliability may be affected by exposure to absolute maximum rating conditions for extended periods of time.
5. Semiconductor devices are ESD sensitive and may be damaged by exposure to ESD events. Suitable ESD precautions should be taken when handling and transporting these devices.

Thermal Resistance (Note 6)

Symbol	Parameter	Rating		Unit
θ_{JA}	Junction to Ambient	U-DFN3030-10	45.87	°C/W
θ_{JC}	Junction to Case	U-DFN3030-10	6.91	°C/W

Recommended Operating Conditions (Note 7) (@T_A = +25°C, unless otherwise specified.)

Symbol	Parameter	Min	Max	Unit
V_{IN}	Supply Voltage	4.5	18.0	V
T_J	Operating Junction Temperature Range	-40	+125	°C
T_A	Operating Ambient Temperature Range	-40	+85	°C

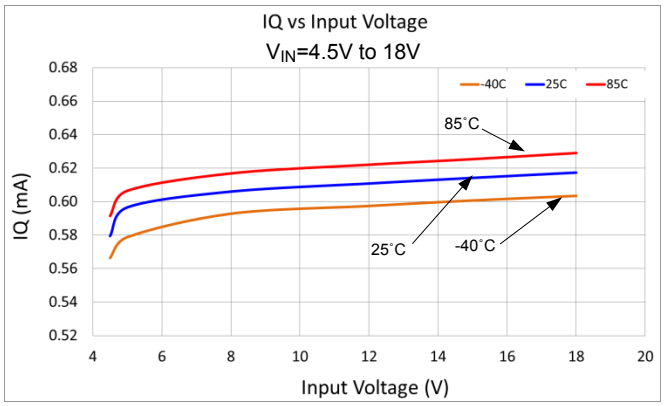
Notes: 6. Test condition: Device mounted on 1"x1" FR-4 substrate PCB, 2oz copper, with minimum recommended pad layout.
7. The device function is not guaranteed outside of the recommended operating conditions.

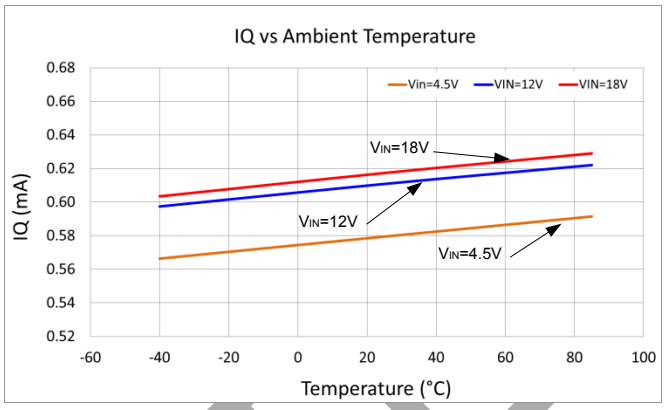
Electrical Characteristics (@T_A = +25°C, V_{IN} = 12V, unless otherwise specified.)

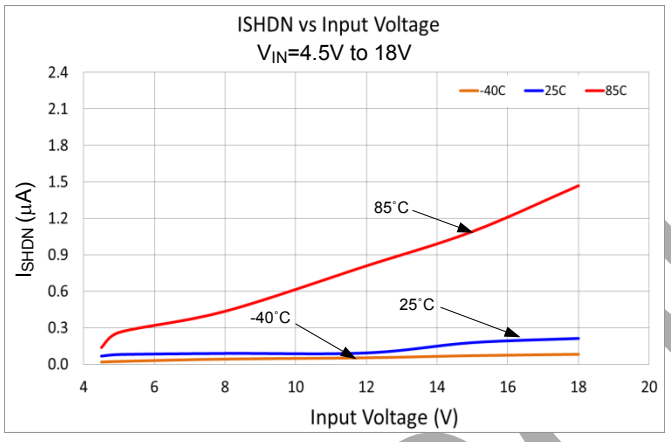
Symbol	Parameter	Condition	Min	Typ	Max	Unit
SUPPLY VOLTAGE (VIN PIN)						
V_{IN}	Input Voltage	—	4.5	—	18	V
I_Q	Quiescent Current	V_{FB} = 0.85V	—	0.6	0.75	mA
I_{SHDN}	Shutdown Supply Current	V_{EN} = 0V	—	0.1	1	μA
UNDER VOLTAGE LOCKOUT						
V_{UVLO}	UVLO Threshold	V_{IN} Rising Test VREG5 Voltage	3.6	3.85	4.1	V
V_{HYS}	UVLO Hysteresis	V_{IN} Falling Test VREG5 Voltage	0.16	0.35	0.47	V
ENABLE (EN PIN)						
V_{ENH}	EN High-level Input Voltage	—	1.25	—	18	V
V_{ENL}	EN Low-level Input Voltage	—	—	—	0.85	V
VOLTAGE REFERENCE (FB PIN)						
V_{FB}	Feedback Voltage (Note 8)	V_{OUT} = 1.05V, T_A = -40°C to +85°C, CCM	0.753	0.765	0.777	V
I_{FB}	Feedback Bias Current	V_{FB} = 0.8V	-0.1	0	0.1	μA
VREG5 OUTPUT						
V_{VREG5} VREG5 Output Voltage	VREG5 Output Voltage	6.0V<V_{IN}<18V 0<I_{VREG5}<5mA	4.8	5.1	5.4	V
—	Source Current Capability	V_{IN} = 6V, V_{VREG5} = 4V	—	100	—	mA
—	Load Regulation	0<I_{VREG5}<5mA	—	—	100	mV
—	Line Regulation	6.0V<V_{IN}<18V I_{VREG5} = 5mA	—	—	20	mV
MOSFET						
R_{DSONH}	High-side Switch On-resistance	—	—	90	—	mΩ
R_{DSONL}	Low-side Switch On-resistance	—	—	57	—	mΩ
CURRENT LIMIT						
I_{LIM-H}	Valley Current Limit (Note 8)	L = 1.5μH, T_A = -40°C to +85°C	3.3	4.5	5.5	A
ON-TIME TIMER						
t_{ON}	On Time	V_{IN} = 12V, V_{OUT} = 1.05V	—	150	—	ns
$t_{OFF-MIN}$	Minimum Off Time	V_{FB} = 0.7V	—	260	310	ns
THERMAL SHUTDOWN						
T_{OTSD}	Thermal Shutdown	—	—	150	—	°C
T_{HYS}	Thermal Shutdown Hysteresis	—	—	25	—	°C
SOFT START (SS PIN)						
$I_{SS-SOURCE}$	Soft-start Source Current	V_{SS}=1.0V	4.2	6.0	7.8	μA
$I_{SS-DISCHARGE}$	Soft-start Discharge Current	V_{SS}=0.5V	0.1	0.2	—	mA
POWER GOOD						
—	PG Threshold	V_{FB} Rising	85	90	95	%
—	PG Threshold	V_{FB} Falling	—	85	—	
—	PG Sink Current	PG = 0.5V	—	5	—	mA

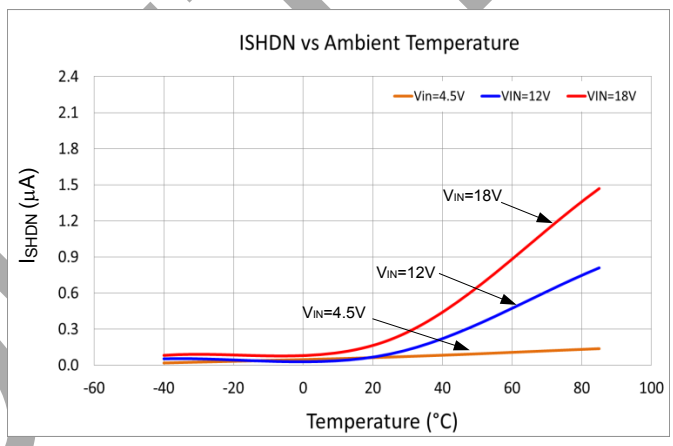
Note: 8. Compliance to the datasheet limits is assured by one or more methods: production test, characterization, and/or design.

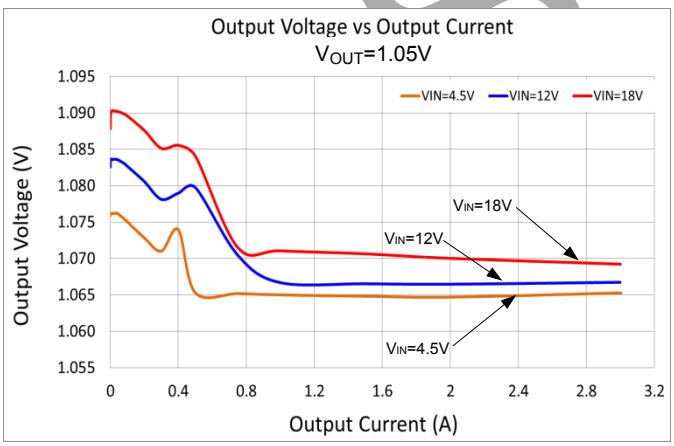
Typical Performance Characteristics (@T_A = +25°C, V_{IN} = 12V, V_{OUT} = 1.05V, unless otherwise specified.)

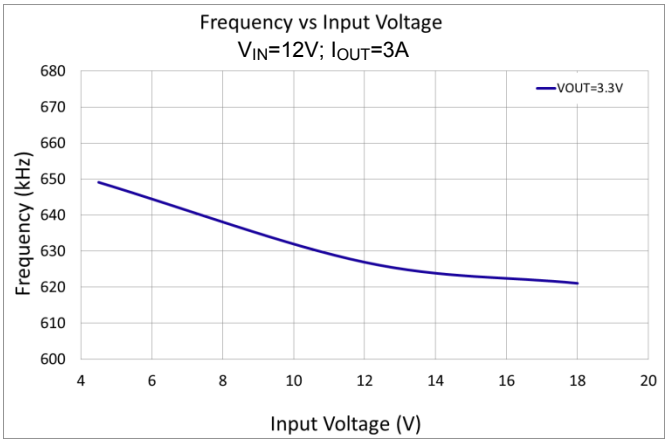




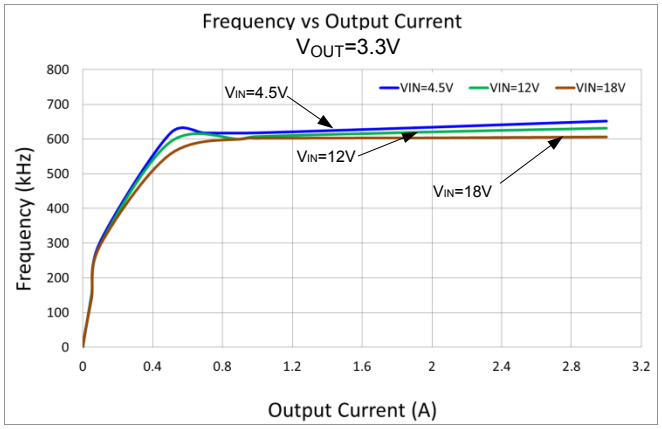


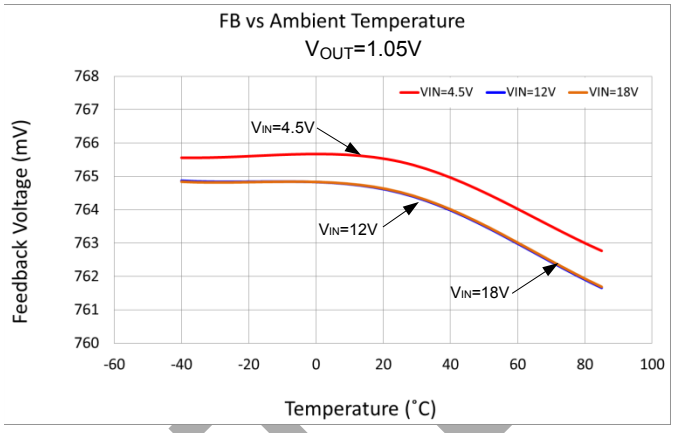


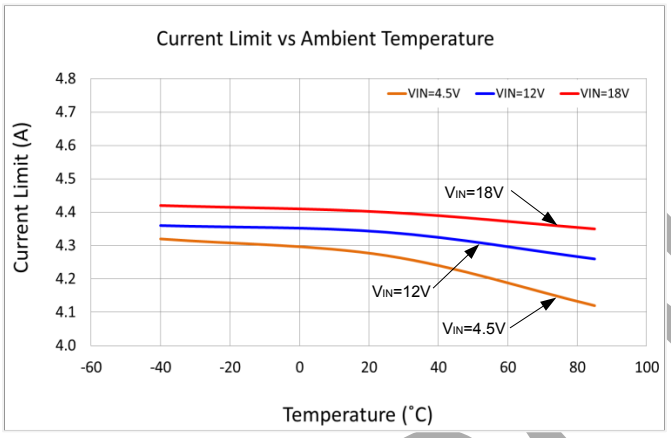


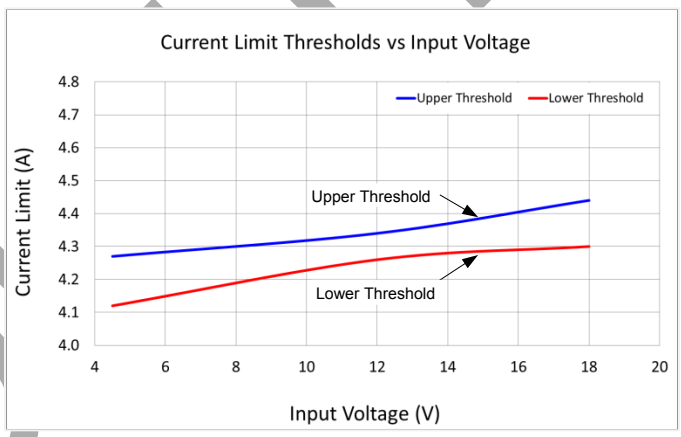


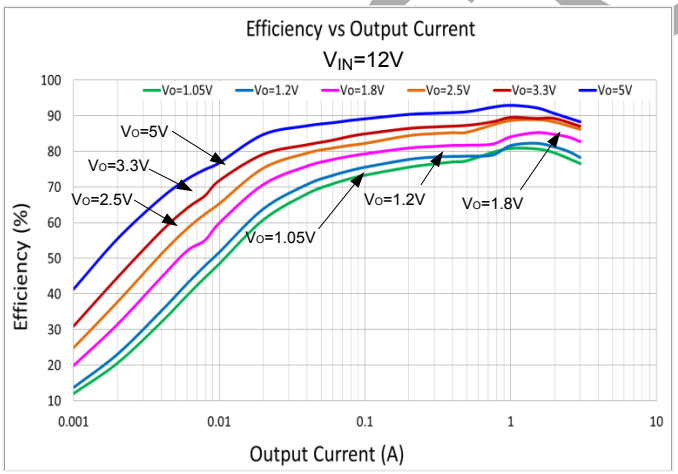
Typical Performance Characteristics (Cont.) (@T_A = +25°C, V_{IN} = 12V, V_{OUT} = 1.05V, unless otherwise specified.)

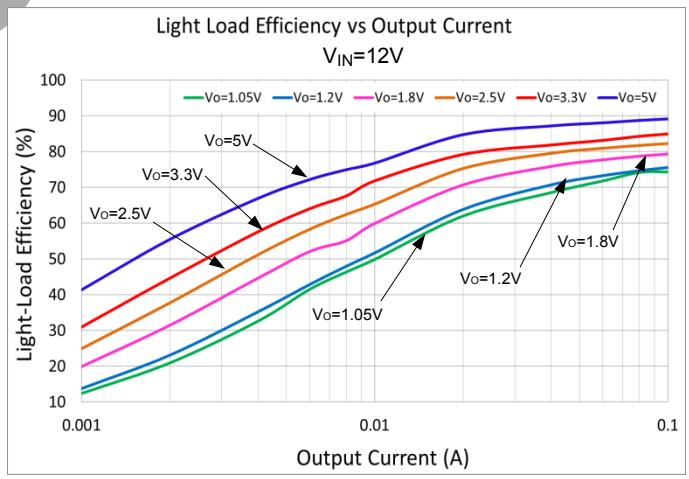








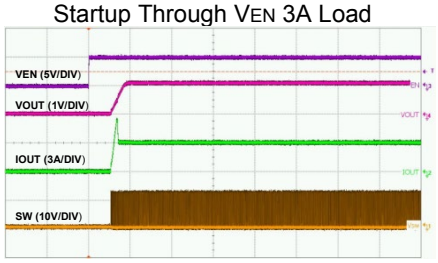




Typical Performance Characteristics (Cont.)

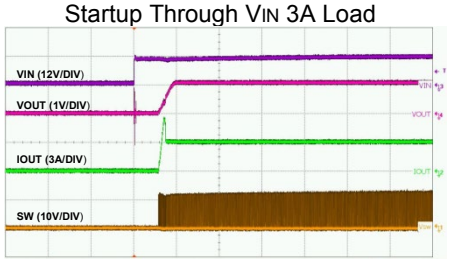
($@T_A$ = +25°C, V_{IN} = 12V, V_{OUT} = 1.05V, L = 1.5µH, C1 = 20µF, C2 = 44µF, unless otherwise specified.)

Startup Through VEN 3A Load



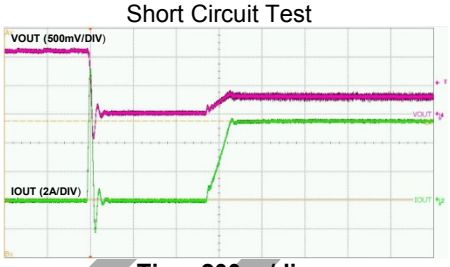
Time-1ms/div

Startup Through VIN 3A Load



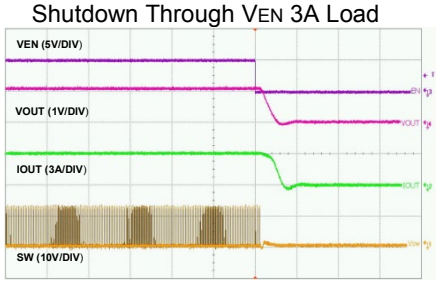
Time-1ms/div

Short Circuit Test



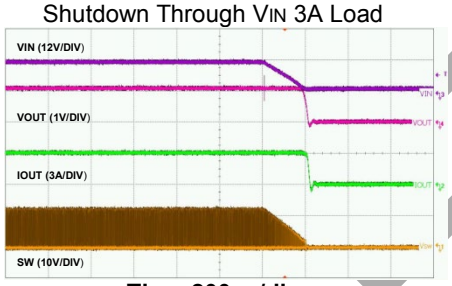
Time-200µs/div

Shutdown Through VEN 3A Load



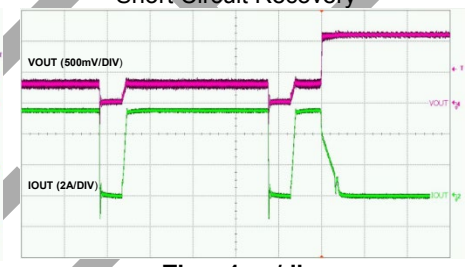
Time-50µs/div

Shutdown Through VIN 3A Load



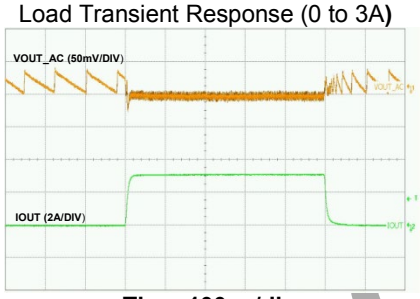
Time-200µs/div

Short Circuit Recovery



Time-1ms/div

Load Transient Response (0 to 3A)

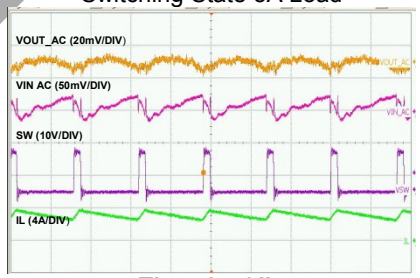


Time-100µs/div

Load Transient Response (1 to 3A)

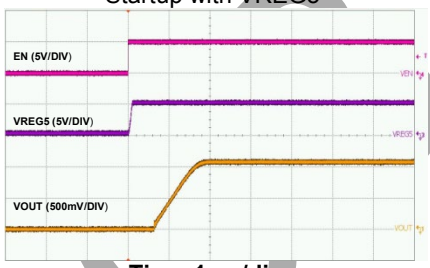
Time-100µs/div

Switching State 3A Load



Time-1µs/div

Startup with VREG5

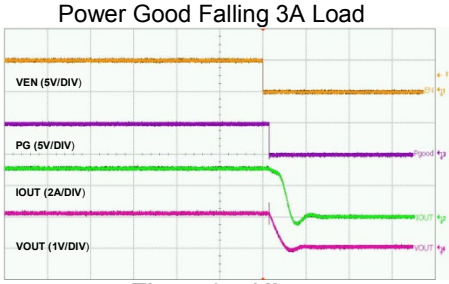


Time-1ms/div

Power Good Rising 3A Load

Time-500µs/div

Power Good Falling 3A Load



Time-50µs/div

Application Information

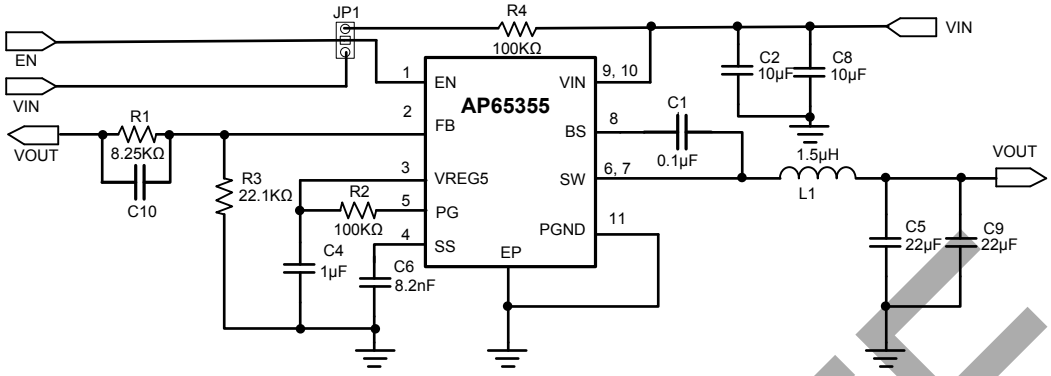


Figure 3 Typical Application of AP65355 evaluation board

PWM Operation and Adaptive On-time Control

The AP65355 is a synchronous step-down converter with internal power MOSFETs. Adaptive constant on-time (aCOT) control is employed to provide fast, transient response and easy loop stabilization. At the beginning of each cycle, the high-side MOSFET is turned on for a fixed one shot timer, ON-time period. This one shot is calculated by the converter's input voltage (V_{IN}) and the output voltage (V_{OUT}) cycle-by-cycle based to maintain a pseudo-fixed frequency over the input voltage range, hence it is called adaptive on-time control. The high-side MOSFET turned off after the fixed on time expire and turn on the low-side MOSFET. Once the output voltage dropped below the output regulation, the low-side turned off. The one-shot timer then reset and the high-side MOSFET is turned on again.

AP65355 uses an adaptive on-time control scheme and does not have a dedicated in-board oscillator. It runs with a pseudo-constant frequency of 650kHz by using the input voltage and output voltage to set the on-time one-shot timer. The on-time is inversely proportional to the input voltage and proportional to the output voltage. It can be calculated using the following equation:

$$t_{ON} = \frac{V_{OUT}}{V_{IN} \times f_S}$$

V_{OUT} is the output voltage
V_{IN} is the input voltage
f_S is the switching frequency

After an ON-time period, the AP65355 goes into the OFF-time period. The OFF-time period length depends on VFB in most cases. It will end when the FB voltage decreases below 0.76V, at which point the ON-time period is triggered. If the OFF-time period is less than the minimum OFF time, the minimum OFF time will be applied, which is about 260ns typical.

Power Save Mode

The AP65355 is designed with Power Save Mode (PSM) at light load conditions for high efficiency. The AP65355 automatically reduces the switching frequency and changes the Ton time to Tmin-on time during a light load condition to get high efficiency and low output ripple. As the output current decreases from heavy load condition, the inductor current decreases as well, and eventually comes close to zero current, which is the boundary between CCM and DCM. The low-side MOSFET is turned off when the inductor current reaches level zero. The load is provided only by the output capacitor. When FB voltage is lower than 0.76V, the next ON cycle begins. The on-time is the minimum on time that benefits for decreasing V_{OUT} ripple at light load conditions. When the output current increases from light to heavy load the switching frequency increases to sustain output voltage. The transition point to light load operation can be calculated using the following equation:

$$I_{LOAD} = \frac{V_{IN} - V_{OUT}}{2L} \times t_{ON}$$

t_{ON} is on-time

Enable

Above the 'EN high-level input voltage', the internal regulator is turned on and the quiescent current can be measured above this threshold. The enable (EN) input allows the user to control turning the regulator on or off. To enable the AP65355, EN must be pulled above the 'EN high-level input voltage.' To disable the AP65355, EN must be pulled below 'EN low-level input voltage.'

In Figure 3, EN is a high voltage input that can be safely connected to V_{IN} (up to 18V) directly or through a 100kΩ pull-up to V_{IN} for automatic start-up.

Application Information (Cont.)

Soft-Start

The soft-start time of the AP65355 is programmable by selecting different C_{SS} values. When the EN pin becomes high, the C_{SS} is charged by a current source, generating a ramp signal fed into non-inverting input of the error comparator. Reference voltage V_{REF}, or the internal soft-start voltage SS, (whichever is smaller), dominates the behavior of the non-inverting inputs of the error amplifier. Accordingly, the output voltage will follow the SS signal and ramp up smoothly to its target level. The capacitor value required for a given soft-start ramp time can be expressed as:

$$t_{SS} = 63 \times 10^3 \times C_{SS}$$

Where C_{SS} is the required capacitor between SS pin and PGND, t_{SS} is the desired soft-start time.

Over Current Protection (OCP)

Figure 4 shows the over current protection (OCP) scheme of AP65355. In each switching cycle, the inductor current is sensed by monitoring the low-side MOSFET during the OFF period. When the voltage between PGND pin and SW pin is lower than the over current trip level, V_{LIMIT}, the OCP will be triggered and the controller keeps the OFF state. A new switching cycle will begin when the measured voltage is higher than limit voltage. After 6μs, the internal OCL (Over Current Logic) threshold is set to a lower level and SS pin is discharged such that output is 0V. Then the switching action is blanked out for one t_{SS} before soft start re-initiated and OCP threshold is restored to higher value.

Because the $R_{DS(ON)}$ of MOSFET increases with temperature, V_{LIMIT} has 4ppm/°C temperature coefficient to compensate this temperature dependency of $R_{DS(ON)}$.

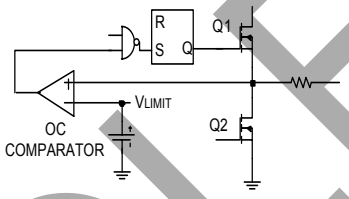


Figure 4 Overcurrent Protection Scheme

Under Voltage Lockout

The AP65355 provides an undervoltage lockout circuit to prevent it from undefined status during startup. The UVLO circuit shuts down the device when V_{IN} drops below 3.45V. The UVLO circuit has 320mV hysteresis, which means the device starts up again when V_{REG} rises to 3.75V (non-latch).

PG Comparator

PG is an open drain output controlled by a comparator connected to the feedback signal. If FB exceeds 90% of the internal reference voltage, PG will be high impedance. Otherwise, the PG output is connected to PGND.

Thermal shutdown

If the junction temperature of the device reaches the thermal shutdown limit of +150°C, the AP65355 shuts itself off, and both HMOS and LMOS will be turned off. The output is discharged with the internal transistor. When the junction cools to the required level (+130°C nominal), the device initiates soft-start as during a normal power-up cycle.

Power Derating Characteristics

To prevent the regulator from exceeding the maximum junction temperature, some thermal analysis is required. The temperature rise is given by:

$$T_{RISE} = PD \cdot (\theta_{JA})$$

Where PD is the power dissipated by the regulator and θ_{JA} is the thermal resistance from the junction of the die to the ambient temperature. The junction temperature, T_J, is given by:

$$T_J = T_A + T_{RISE}$$

T_A is the ambient temperature of the environment. For TSOT26 package, the θ_{JA} is +70°C/W. The actual junction temperature should not exceed the absolute maximum junction temperature of +125°C when considering the thermal design.

Setting the Output Voltage

The output voltage can be adjusted from 0.76 using an external resistor divider. Table 1 shows a list of resistor selection for common output voltages. Resistor R1 is selected based on a design tradeoff between efficiency and output voltage accuracy. For high values of R1 there is less current consumption in the feedback network. However, the tradeoff is output voltage accuracy due to the bias current in the error amplifier. R1 can be determined by the following equation:

$$R_1 = R_3 \cdot \left(\frac{V_{OUT}}{0.765} - 1 \right)$$

Application Information (Cont.)

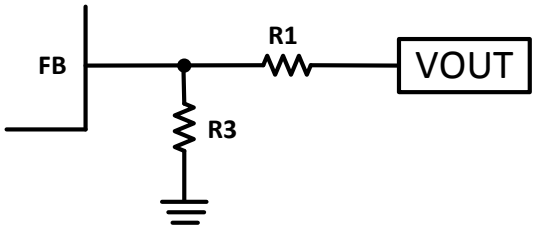


Figure 5 Feedback Divider Network

Output Voltage (V)	R1 (kΩ)	R3 (kΩ)
1	6.81	22.1
1.05	8.25	22.1
1.2	12.7	22.1
1.5	21.5	22.1
1.8	30.1	22.1
2.5	49.9	22.1
3.3	73.2	22.1
5	124	22.1

Table 1 Resistor Selection for Common Output

Inductor

Calculating the inductor value is a critical factor in designing a buck converter. For most designs, the following equation can be used to calculate the inductor value:

$$L = \frac{V_{OUT} \cdot (V_{IN} - V_{OUT})}{V_{IN} \cdot \Delta I_L \cdot f_S}$$

Where ΔI_L is the inductor ripple current and f_S is the buck converter switching frequency.

Choose the inductor ripple current to be 30% of the maximum load current. The maximum inductor peak current is calculated from:

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2}$$

Peak current determines the required saturation current rating, which influences the size of the inductor. Saturating the inductor decreases the converter efficiency while increasing the temperatures of the inductor and the internal MOSFETs. Hence choosing an inductor with an appropriate saturation current rating is important.

A 1μH to 3.3μH inductor with a DC current rating of at least 25% higher than the maximum load current is recommended for most applications. For highest efficiency, the inductor's DC resistance should be less than 100mΩ. Use a larger inductance for improved efficiency under light load conditions.

The phase boost can be achieved by adding an additional feed forward capacitor (C10) in parallel with R1.

Output Voltage (V)	C10(pF)	L1 (μH)	C5+C9 (μF)
1	—	1.0-1.5	22-68
1.05	—	1.0-1.5	22-68
1.2	—	1.0-1.5	22-68
1.5	—	1.5	22-68
1.8	5-22	1.5	22-68
2.5	5-22	2.2	22-68
3.3	5-22	2.2	22-68
5	5-22	3.3	22-68

Table 2 Recommended Component Selection

Input Capacitor

The input capacitor reduces the surge current drawn from the input supply and the switching noise from the device. The input capacitor has to sustain the ripple current produced during the on time on the upper MOSFET. It must have a low ESR to minimize the losses.

The RMS current rating of the input capacitor is a critical parameter that must be higher than the RMS input current. As a rule of thumb, select an input capacitor which has RMs rating greater than half of the maximum load current.

Due to large dI/dt through the input capacitors, electrolytic or ceramics should be used. If a tantalum must be used it must be surge protected, otherwise, capacitor failure could occur. For most applications greater than 10μF, ceramic capacitor is sufficient.

Application Information (Cont.)

Output Capacitor

The output capacitor keeps the output voltage ripple small, ensures feedback loop stability and reduces the overshoot of the output voltage. The output capacitor is a basic component for the fast response of the power supply. In fact, during load transient, for the first few microseconds, it supplies the current to the load. The converter recognizes the load transient and sets the duty cycle to maximum, but the current slope is limited by the inductor value.

Maximum capacitance required can be calculated from the following equation:
ESR of the output capacitor dominates the output voltage ripple. The amount of ripple can be calculated from the equation below:

$$V_{OUT\_RIPPLE} = \Delta I_{INDUCTOR} * ESR$$

An output capacitor with ample capacitance and low ESR is the best option. For most applications, a 22μF to 68μF ceramic capacitor will be sufficient.

$$C_O = \frac{L(I_{OUT} + \frac{\Delta I_{INDUCTOR}}{2})^2}{(\Delta V + V_{OUT})^2 - V_{OUT}^2}$$

Where ΔV is the maximum output voltage overshoot.

Bootstrap Capacitor

To ensure the proper operation, a ceramic capacitor must be connected between the VBST and SW pin. A 0.1μF ceramic capacitor is sufficient.

VREG5 Capacitor

To ensure the proper operation, a ceramic capacitor must be connected between the VREG5 and PGND pin. A 1μF ceramic capacitor is sufficient.

PC Board Layout

1. The AP65355 works at 3A load current, heat dissipation is a major concern in layout the PCB. A 2oz Copper in both top and bottom layer is recommended.
2. Provide sufficient vias in the thermal exposed pad for heat dissipate to the bottom layer.
3. Provide sufficient vias in the Output capacitor PGND side to dissipate heat to the bottom layer.
4. Make the bottom layer under the device as PGND layer for heat dissipation. The PGND layer should be as large as possible to provide better thermal effect.
5. Make the V_{IN} capacitors as close to the device as possible.
6. Make the V_{VREG5} capacitor as close to the device as possible.
7. The thermal pad of the device should be soldered directly to the PCB exposed copper plane to work as a heatsink. The thermal vias in the exposed copper plane increase the heat transfer to the bottom layer.

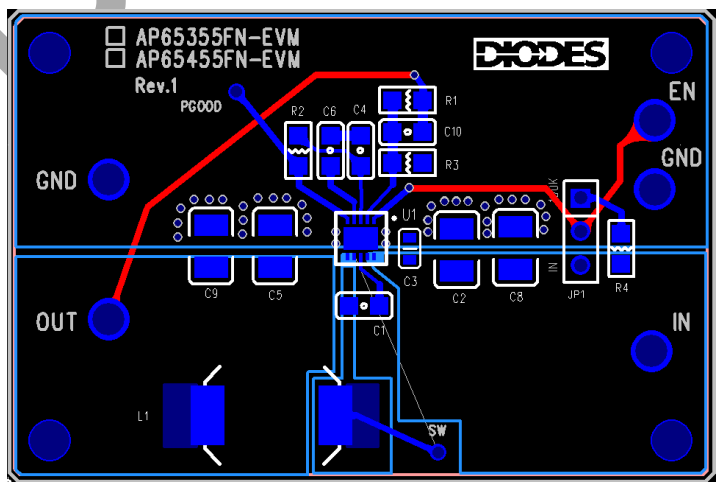
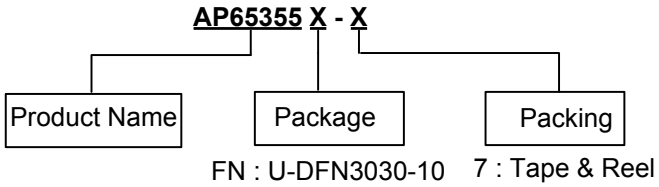


Figure 6 PC Board Layout

Ordering Information

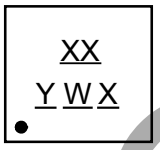


Part Number	Package Code	Package	Identification Code	Tape and Reel	
				Quantity	Part Number Suffix
AP65355FN-7	FN	U-DFN3030-10	UJ	3,000/Tape & Reel	-7

Marking Information

U-DFN3030-10

(Top View)



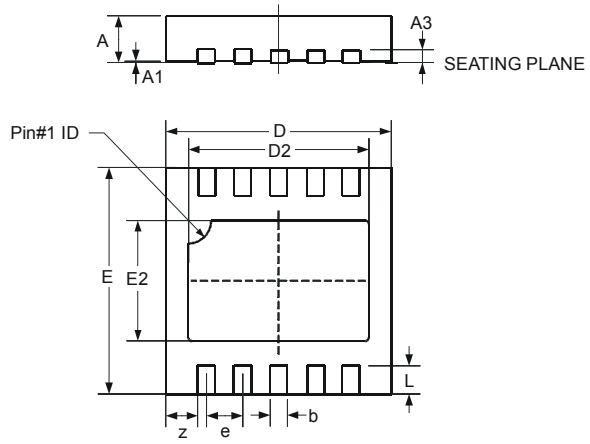
XX : Identification Code
Y : Year : 0~9
W : Week : A~Z : 1~26 week;
a~z : 27~52 week; z represents
52 and 53 week
X : Internal Code

Part Number	Package	Identification Code
AP65355FN-7	U-DFN3030-10	UJ

Package Outline Dimensions (All dimensions in mm.)

Please see http://www.diodes.com/package-outlines.html for the latest version.

U-DFN3030-10

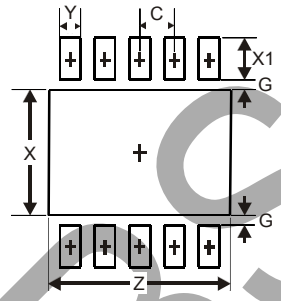


U-DFN3030-10			
Dim	Min	Max	Typ
A	0.57	0.63	0.60
A1	0	0.05	0.02
A3	—	—	0.15
b	0.20	0.30	0.25
D	2.90	3.10	3.00
D2	2.30	2.50	2.40
e	—	—	0.50
E	2.90	3.10	3.00
E2	1.50	1.70	1.60
L	0.25	0.55	0.40
z	—	—	0.375
All Dimensions in mm			

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

U-DFN3030-10



Dimensions	Value (in mm)
Z	2.60
G	0.15
X	1.80
X1	0.60
Y	0.30
C	0.50

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