Pin Configuration

MP Package
(PSOP-8)

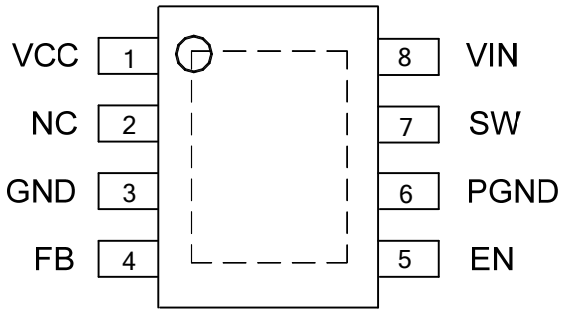


Figure 2. Pin Configuration of AP3435 (Top View)

Pin Description

Pin Number	Pin Name	Function
1	VCC	Supply input for the analog circuit
2	NC	No connection
3	GND	Ground pin
4	FB	Feedback pin. Receive the feedback voltage from a resistive divider connected across the output
5	EN	Chip enable pin. Active high, internal pull-high with 200kΩ resistor
6	PGND	Power switch ground pin
7	SW	Switch output pin
8	VIN	Power supply input for the MOSFET switch

1.0MHz, 3.5A, Synchronous Step Down DC-DC Converter AP3435

Functional Block Diagram

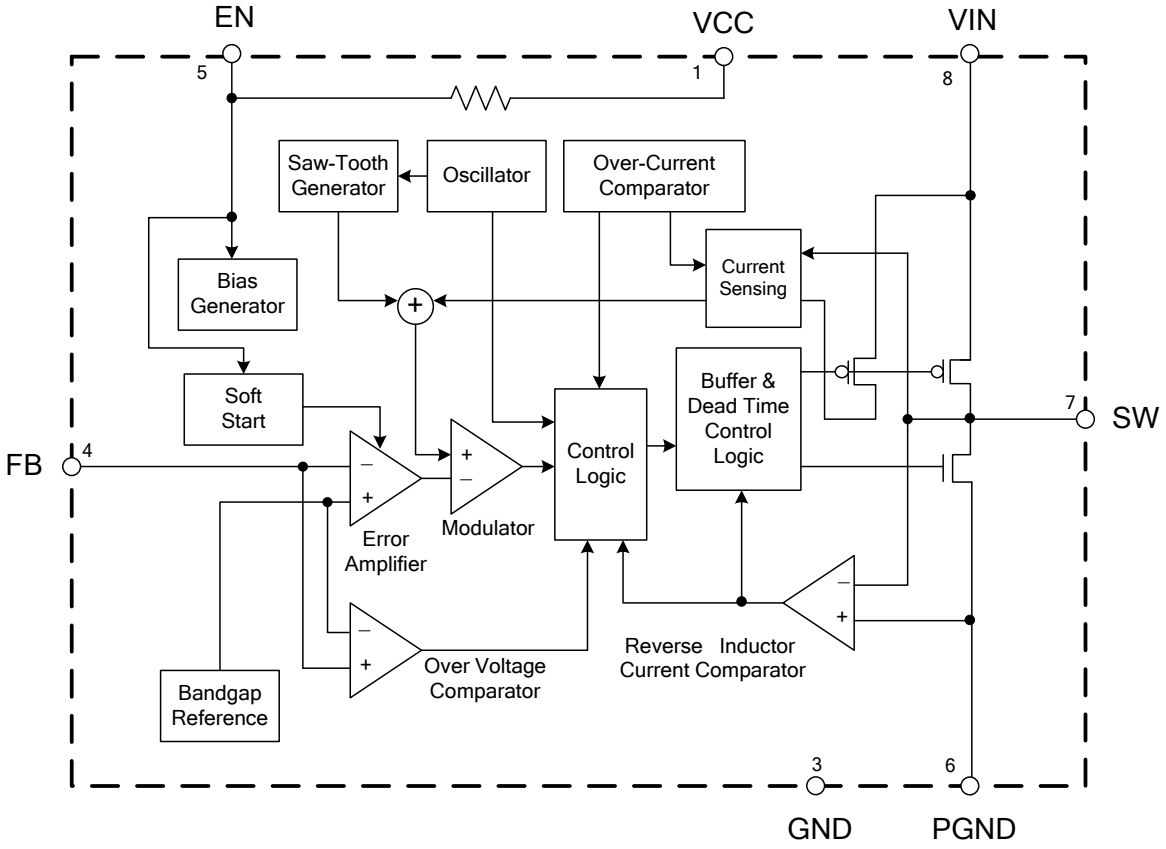
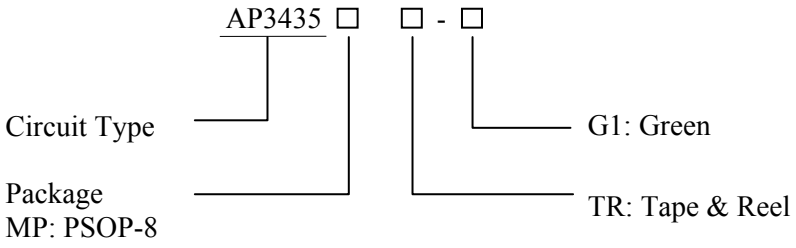


Figure 3. Functional Block Diagram of AP3435

Ordering Information



Package	Temperature Range	Part Number	Marking ID	Packing Type
PSOP-8	-40 to 80°C	AP3435MPTR-G1	3435MP-G1	Tape & Reel

BCD Semiconductor's Pb-free products, as designated with "G1" in the part number, are RoHS compliant and green.

Absolute Maximum Ratings (Note 1)

Parameter	Symbol	Value	Unit
Supply Input for the Analog Circuit	V_{CC}	0 to 6.0	V
Power Supply Input for the MOSFET Switch	V_{IN}	0 to 6.0	V
SW Pin Switch Voltage	V_{SW}	-0.3 to V_{IN}+0.3	V
Enable Input Voltage	V_{EN}	-0.3 to V_{IN}+0.3	V
SW Pin Switch Current	I_{SW}	4.5	A
Power Dissipation (on PCB, T_A=25°C)	P_D	2.47	W
Thermal Resistance (Junction to Ambient, Simulation)	θ_{JA}	40.43	°C/W
Operating Junction Temperature	T_J	160	°C
Operating Temperature	T_{OP}	-40 to 85	°C
Storage Temperature	T_{STG}	-55 to 150	°C
ESD (Human Body Model)	V_{HBM}	2000	V
ESD (Machine Model)	V_{MM}	200	V

Note 1: Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “Recommended Operating Conditions” is not implied. Exposure to “Absolute Maximum Ratings” for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit
Supply Input Voltage	V_{IN}	2.7	5.5	V
Junction Temperature Range	T_J	-40	125	°C
Ambient Temperature Range	T_A	-40	80	°C

Electrical Characteristics

V_{IN}=V_{CC}=V_{EN}=5V, V_{OUT}=1.2V, V_{FB}=0.8V, L=2.2μH, C_{IN}=10μF, C_{OUT}=22μF, T_A=25°C, unless otherwise specified.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		2.7		5.5	V
Shutdown Current	I_{OFF}	V_{EN}=0			1	μA
Active Current	I_{ON}	V_{FB}=0.95V		310		μA
Regulated Feedback Voltage	V_{FB}	For Adjustable Output Voltage	0.784	0.8	0.816	V
Regulated Output Voltage Accuracy	$\Delta V_{OUT}/V_{OUT}$	V_{IN}=2.7V to 5.5V, I_{OUT}=0 to 3.5A	-3		3	%
Peak Inductor Current	I_{PK}		4.5			A
Oscillator Frequency	f_{OSC}	V_{IN}=2.7V to 5.5V		1.0		MHz
PMOSFET RON	$R_{ON(P)}$	V_{IN}=5V		100		mΩ
NMOSFET RON	$R_{ON(N)}$	V_{IN}=5V		100		mΩ
EN High-level Input Voltage	V_{EN_H}		1.5			V
EN Low-level Input Voltage	V_{EN_L}				0.4	V
EN Input Current	I_{EN}			1		μA
Soft Start Time	t_{SS}			400		μs
Maximum Duty Cycle	D_{MAX}				100	%
Under Voltage Lock Out Threshold	V_{UVLO}	Rising		2.4		V
		Falling		2.3		
		Hysteresis		0.1		
Thermal Shutdown	T_{SD}	Hysteresis=30°C		150		°C
Input Over Voltage Protection (IOVP)	V_{IOVP}	Rising	5.8	5.9	6.0	V
		Hysteresis	0.3	0.4	0.5	V

Typical Performance Characteristics

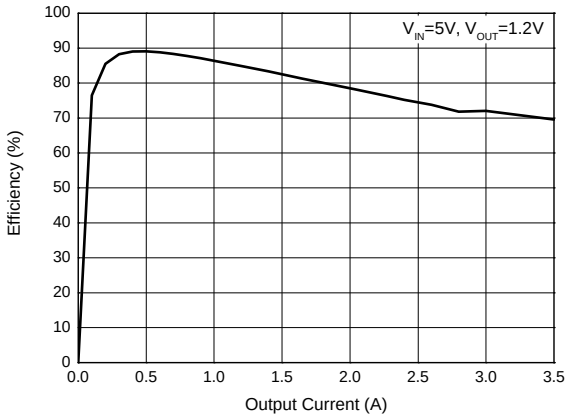


Figure 4. Efficiency vs. Output Current

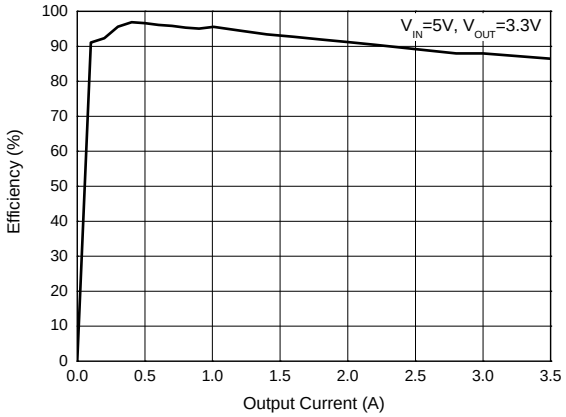


Figure 5. Efficiency vs. Output Current

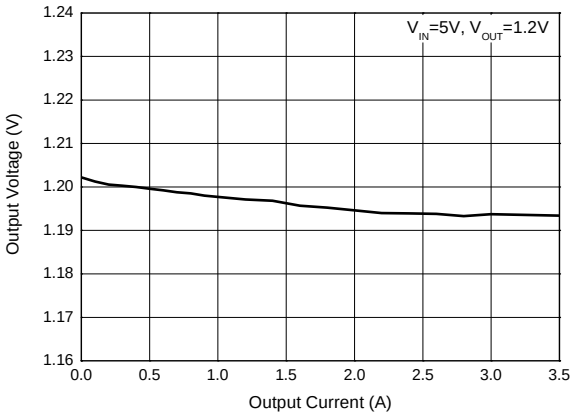


Figure 6. Load Regulation

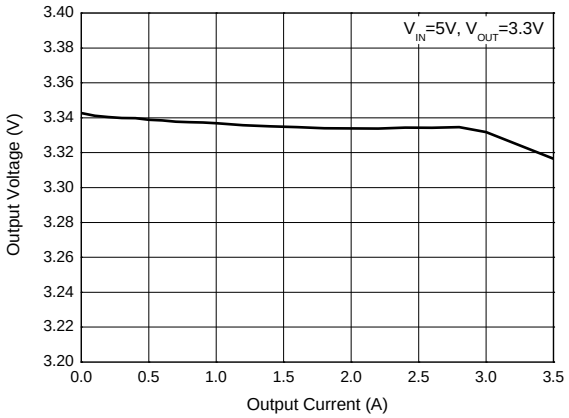


Figure 7. Load Regulation

Typical Performance Characteristics (Continued)

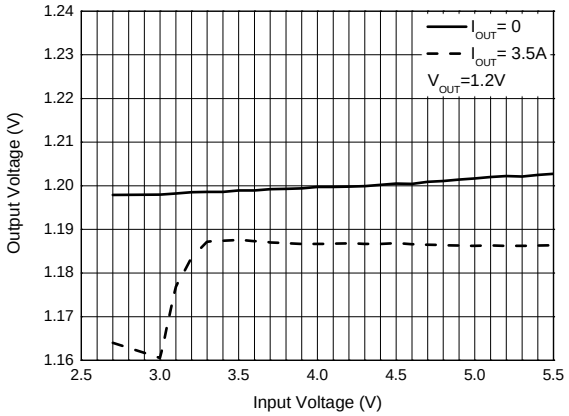


Figure 8. Line Regulation

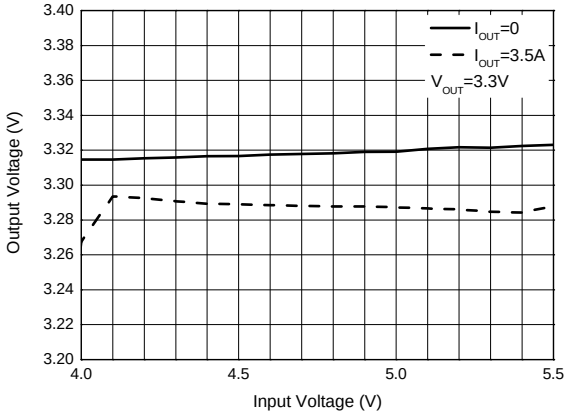


Figure 9. Line Regulation

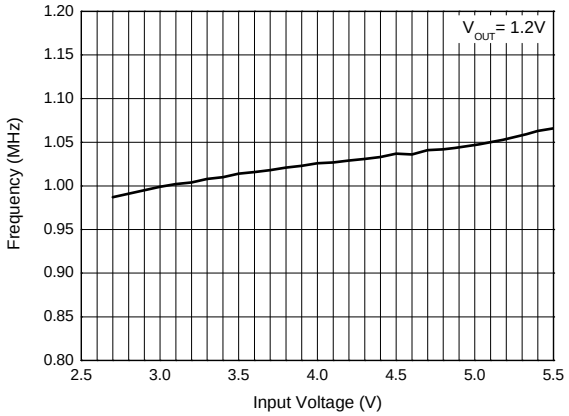


Figure 10. Frequency vs. Input Voltage

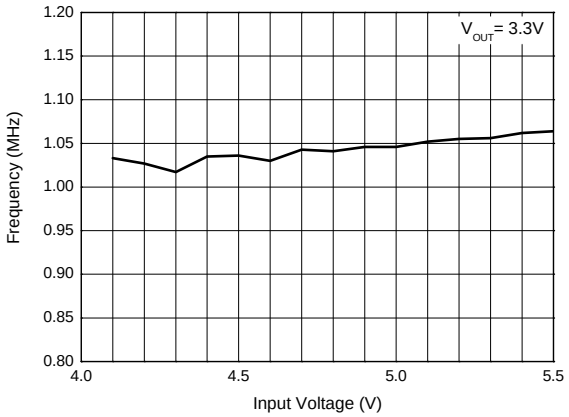


Figure 11. Frequency vs. Input Voltage

Typical Performance Characteristics (Continued)

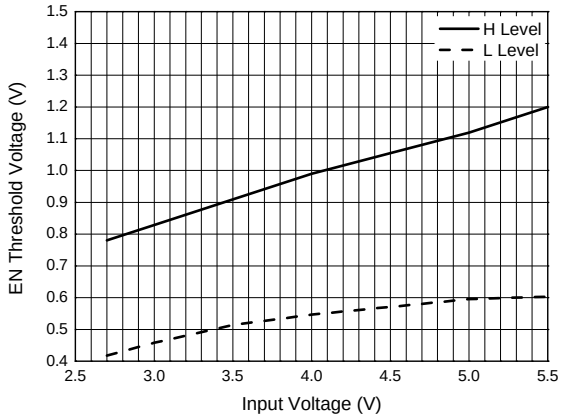


Figure 12. Enable Threshold Voltage vs. Input Voltage

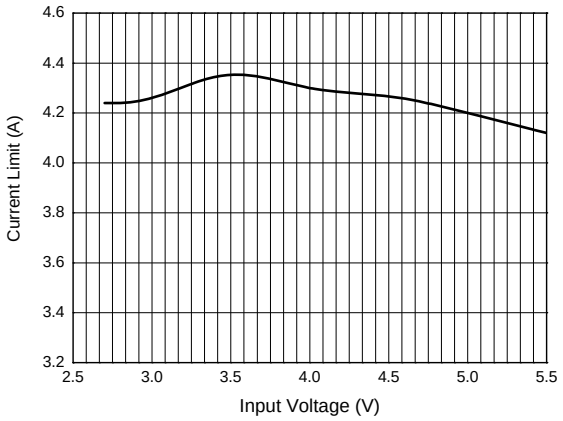


Figure 13. Current Limit vs. Input Voltage

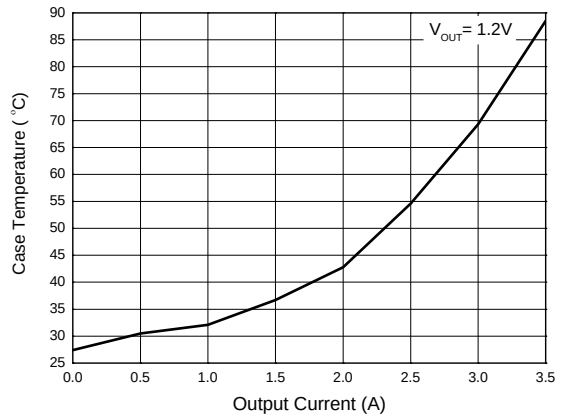
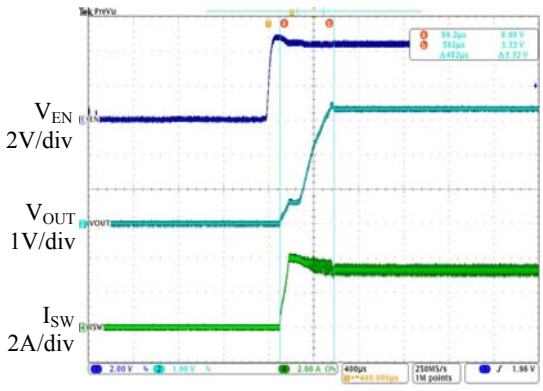


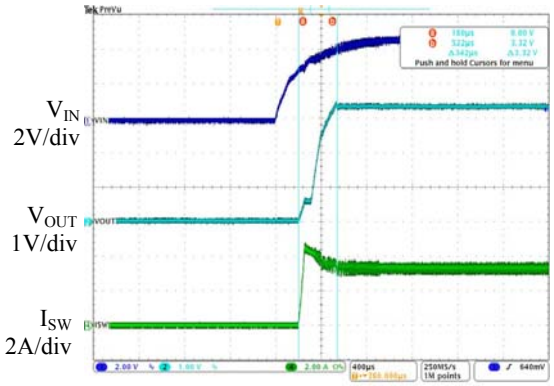
Figure 14. Case Temperature vs. Output Current



Time 400μs/div

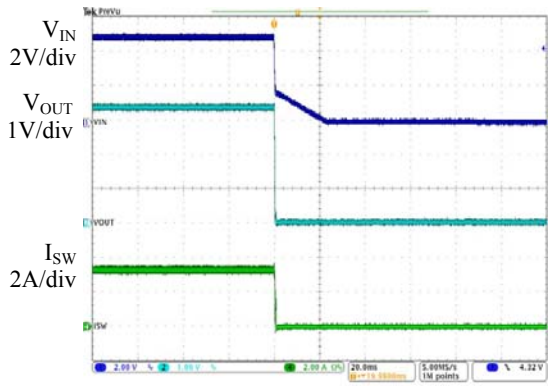
Figure 15. Enable Waveform
(V_{IN}=5V, V_{EN}=0V to 5V, V_{OUT}=3.3V, I_{OUT}=3.5A)

Typical Performance Characteristics (Continued)



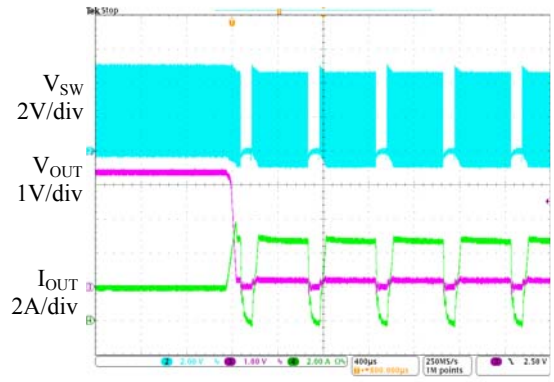
Time 400µs/div

Figure 16. Power-On
(V_{IN}=0V to 5V, V_{EN}=V_{IN}, V_{OUT}=3.3V, I_{OUT}=3.5A)



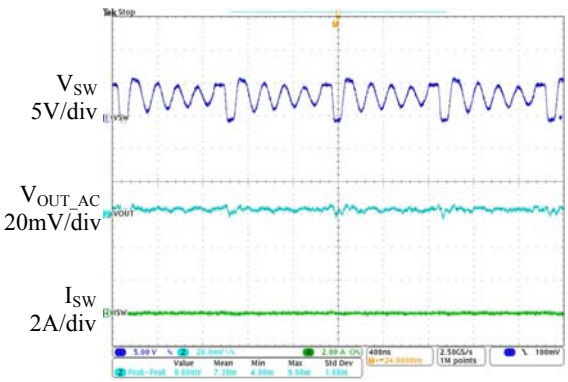
Time 20ms/div

Figure 17. Power-Off
(V_{IN}=5V to 0V, V_{EN}=V_{IN}, V_{OUT}=3.3V, I_{OUT}=3.5A)



Time 400µs/div

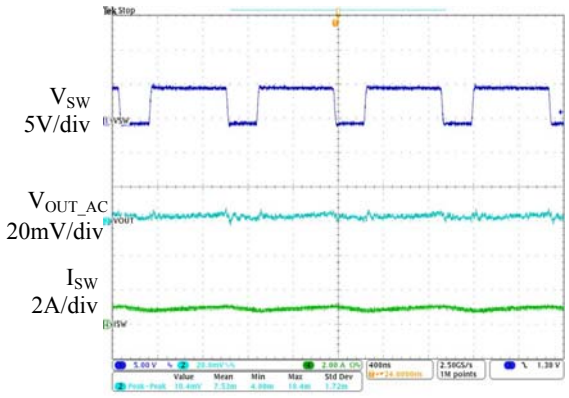
Figure 18. Short Circuit Protection
(V_{IN}=5V=V_{EN}, V_{OUT}=3.3V, I_{OUT}=2A to short)



Time 400ns/div

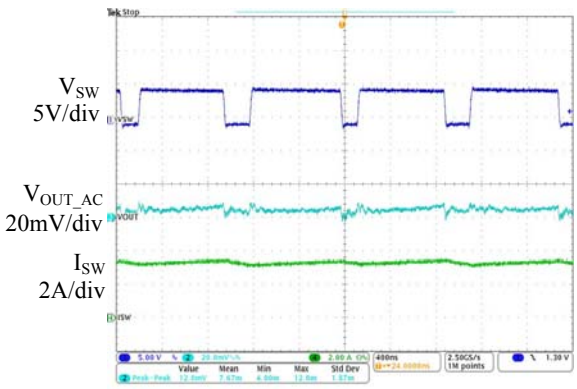
Figure 19. V_{OUT} Ripple
(V_{IN}=5V=V_{EN}, V_{OUT}=3.3V, I_{OUT}=0A)

Typical Performance Characteristics (Continued)



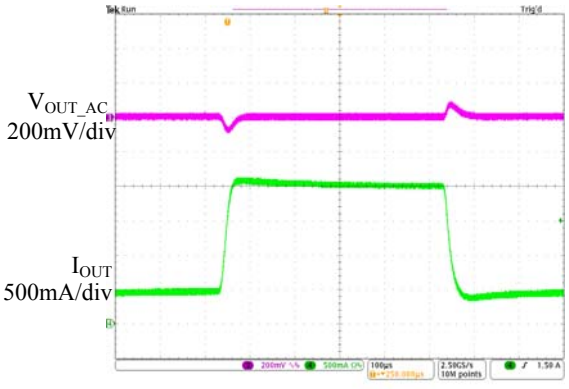
Time 400ns/div

Figure 20. V_{OUT} Ripple
(V_{IN}=5V=V_{EN}, V_{OUT}=3.3V, I_{OUT}=1A)



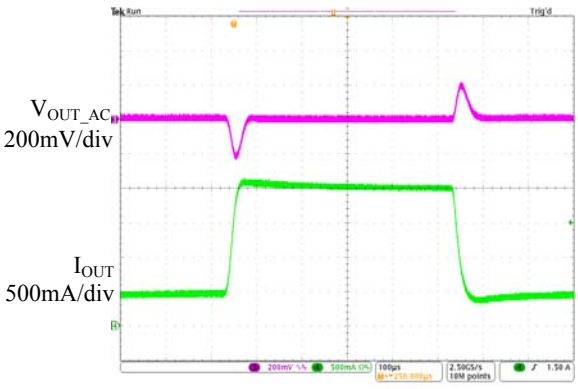
Time 400ns/div

Figure 21. V_{OUT} Ripple
(V_{IN}=5V=V_{EN}, V_{OUT}=3.3V, I_{OUT}=3.5A)



Time 100µs/div

Figure 22. Load Transient of 1.2V Output
(V_{IN}=5V=V_{EN}, V_{OUT}=1.2V, I_{OUT}=0.5A to 2A)



Time 100µs/div

Figure 23. Load Transient of 3.3V Output
(V_{IN}=5V=V_{EN}, V_{OUT}=3.3V, I_{OUT}=0.5A to 2A)

Typical Performance Characteristics (Continued)

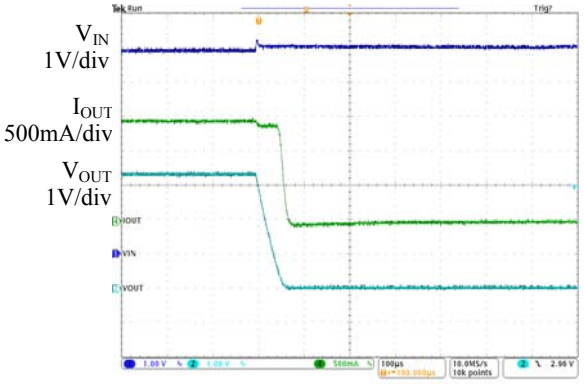


Figure 24. OVP Function (V_{IN}=5V to 6V)

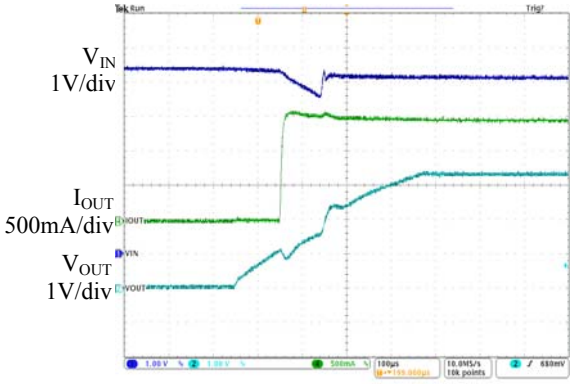


Figure 25. Leave OVP Function (V_{IN}=6V to 5V)

Application Information

The basic AP3435 application circuit is shown in Figure 27, external components selection is determined by the load current and is critical with the selection of inductor and capacitor values.

1. Inductor Selection

For most applications, the value of inductor is chosen based on the required ripple current with the range of 1μH to 6.8μH.

$$\Delta I_L = \frac{1}{f \times L} V_{OUT}(1 - \frac{V_{OUT}}{V_{IN}})$$

The largest ripple current occurs at the highest input voltage. Having a small ripple current reduces the ESR loss in the output capacitor and improves the efficiency. The highest efficiency is realized at low operating frequency with small ripple current. However, larger value inductors will be required. A reasonable starting point for ripple current setting is $\triangle I_L$=40%I_{MAX}. For a maximum ripple current stays below a specified value, the inductor should be chosen according to the following equation:

$$L = [\frac{V_{OUT}}{f \times \Delta I_L(MAX)}][1 - \frac{V_{OUT}}{V_{IN}(MAX)}]$$

The DC current rating of the inductor should be at least equal to the maximum output current plus half the highest ripple current to prevent inductor core saturation. For better efficiency, a lower DC-resistance inductor should be selected.

2. Capacitor Selection

The input capacitance, C_{IN}, is needed to filter the trapezoidal current at the source of the top MOSFET. To prevent large ripple voltage, a low ESR input capacitor sized for the maximum RMS current must be used. The maximum RMS capacitor current is given by:

$$I_{RMS} = I_{OMAX} \times \frac{[V_{OUT}(V_{IN} - V_{OUT})]^{\frac{1}{2}}}{V_{IN}}$$

It indicates a maximum value at V_{IN}=2V_{OUT}, where I_{RMS}=I_{OUT}/2. This simple worse-case condition is commonly used for design because even significant deviations do not much relieve. The selection of C_{OUT} is determined by the Effective Series Resistance (ESR) that is required to minimize output voltage ripple and load step transients, as well as the amount of bulk capacitor that is necessary to ensure that the control loop is stable. The output ripple, $\triangle V_{OUT}$, is determined by:

$$\Delta V_{OUT} \le \Delta I_L[ESR + \frac{1}{8 \times f \times C_{OUT}}]$$

The output ripple is the highest at the maximum input voltage since $\triangle I_L$ increases with input voltage.

3. Load Transient

A switching regulator typically takes several cycles to respond to the load current step. When a load step occurs, V_{OUT} immediately shifts by an amount equal to $\triangle I_{LOAD} \times$ ESR, where ESR is the effective series resistance of output capacitor. $\triangle I_{LOAD}$ also begins to charge or discharge C_{OUT} generating a feedback error signal used by the regulator to return V_{OUT} to its steady-state value. During the recovery time, V_{OUT} can be monitored for overshoot or ringing that would indicate a stability problem.

4. Output Voltage Setting

The output voltage of AP3435 can be adjusted by a resistive divider according to the following formula:

$$V_{OUT} = V_{REF} \times (1 + \frac{R_1}{R_2}) = 0.8V \times (1 + \frac{R_1}{R_2})$$

The resistive divider senses the fraction of the output voltage as shown in Figure 26.

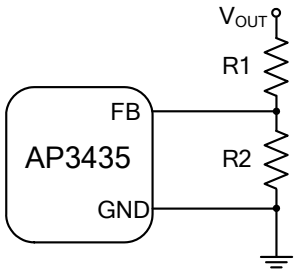


Figure 26. Setting the Output Voltage

Application Information (Continued)

5. Short Circuit Protection

When the AP3435 output node is shorted to GND, as V_{FB} drops under 0.4V, the chip will enter soft-start mode to protect itself, when short circuit is removed, and V_{FB} rises over 0.4V, the AP3435 recovers back to normal operation again. If the AP3435 reaches OCP threshold while short circuit, the AP3435 will enter soft-start cycle until the current under OCP threshold.

6. Efficiency Considerations

The efficiency of switching regulator is equal to the output power divided by the input power times 100%. It is usually useful to analyze the individual losses to determine what is limiting efficiency and which change could produce the largest improvement. Efficiency can be expressed as:

Efficiency=100%-L1-L2-…..

Where L1, L2, etc. are the individual losses as a percentage of input power.

Although all dissipative elements in the regulator produce losses, two major sources usually account for most of the power losses: V_{IN} quiescent current and I^2R losses. The V_{IN} quiescent current loss dominates the efficiency loss at very light load currents and the I^2R loss dominates the efficiency loss at medium to heavy load currents.

6.1 The V_{IN} quiescent current loss comprises two parts: the DC bias current as given in the electrical characteristics and the internal MOSFET switch gate charge currents. The gate charge current results from switching the gate capacitance of the internal power MOSFET switches. Each cycle the gate is switched from high to low, then to high again, and the packet of charge, dQ moves from V_{IN} to ground. The resulting dQ/dt is the current out of V_{IN} that is typically larger than the internal DC bias current. In continuous mode,

$$I_{GATE} = f \times (Q_P + Q_N)$$

Where Q_P and Q_N are the gate charge of power PMOSFET and NMOSFET switches. Both the DC bias current and gate charge losses are proportional to the V_{IN} and this effect will be more serious at higher input voltages.

6.2 I^2R losses are calculated from internal switch resistance, R_{SW} and external inductor resistance R_L. In continuous mode, the average output current flowing through the inductor is chopped between power PMOSFET switch and NMOSFET switch. Then, the series resistance looking into the SW pin is a function of both PMOSFET $R_{DS(ON)}$ and NMOSFET $R_{DS(ON)}$ resistance and the duty cycle (D):

$$R_{SW} = R_{DS(ON)P} \times D + R_{DS(ON)N} \times (1 - D)$$

Therefore, to obtain the I^2R losses, simply add R_{SW} to R_L and multiply the result by the square of the average output current.

Other losses including C_{IN} and C_{OUT} ESR dissipative losses and inductor core losses generally account for less than 2 % of total additional loss.

7. Thermal Characteristics

In most applications, the part does not dissipate much heat due to its high efficiency. However, in some conditions when the part is operating in high ambient temperature with high $R_{DS(ON)}$ resistance and high duty cycles, such as in LDO mode, the heat dissipated may exceed the maximum junction temperature. To avoid the part from exceeding maximum junction temperature, the user should do some thermal analysis. The maximum power dissipation depends on the layout of PCB, the thermal resistance of IC package, the rate of surrounding airflow and the temperature difference between junction and ambient.

8. Input Over Voltage Protection

When input voltage of AP3435 is near 6V, the IC will enter Input-Over-Voltage-Protection. It would be shut down and there will be no output voltage in this state. As the input voltage goes down below 5.5V, it will leave input OVP and recover the output voltage.

Application Information (Continued)

9. PCB Layout Considerations

When laying out the printed circuit board, the following checklist should be used to optimize the performance of AP3435.

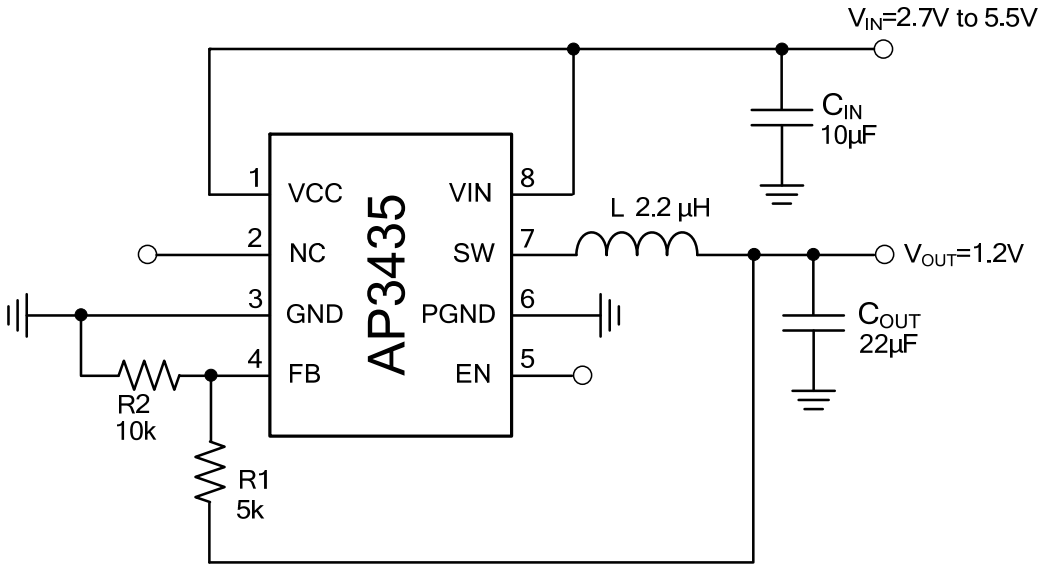
1) The power traces, including the GND trace, the SW trace and the VIN trace should be kept direct, short and wide.

2) Put the input capacitor as close as possible to the VIN and GND pins.

3) The FB pin should be connected directly to the feedback resistor divider.

4) Keep the switching node, SW, away from the sensitive FB pin and the node should be kept small area.

Typical Application



Note 2: $V_{OUT} = V_{REF} \times (1 + \frac{R_1}{R_2})$.

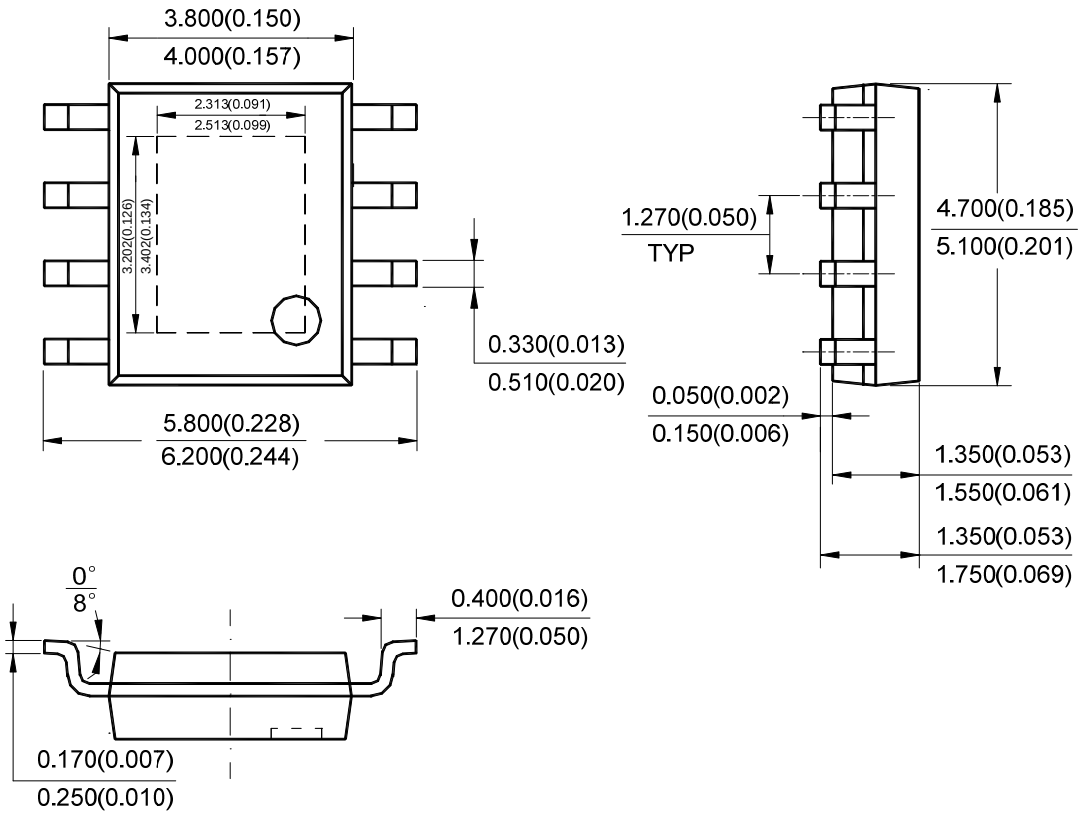
Figure 27. Typical Application Circuit of AP3435

V_{OUT}(V)	R1 (kΩ)	R2 (kΩ)	L (µH)
3.3	31.25	10	2.2
2.5	21.5	10	2.2
1.8	12.5	10	2.2
1.2	5	10	2.2
1.0	3	10	2.2

Table 1. Component Guide

Mechanical Dimensions

PSOP-8 **Unit:mm(inch)**



Note: Eject hole, oriented hole and mold mark is optional.

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