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11/2015—Rev. E to Rev. F

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3/2015—Rev. D to Rev. E

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3/2014—Rev. C to Rev. D

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3/2010—Rev. A to Rev. B

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3/2009—Rev. 0 to Rev. A

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5/2008—Revision 0: Initial Version

SPECIFICATIONS

All voltages are relative to their respective grounds, 3.0 V ≤ V_{DD1} ≤ 5.5 V and 3.0 V ≤ V_{DD2} ≤ 3.6 V, all minimum/maximum specifications apply over the entire recommended operation range, all typical specifications are at T_A = 25°C, V_{DD1} = 5 V, andV_{DD2} = 3.3 V, unless otherwise noted.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
SUPPLY CURRENT						
Power Supply Current, Logic Side						
TxD/RxD Data Rate = 500 kbps	I_{DD1}			2.0	mA	Unloaded
				2.0	mA	V_{DD2} = 3.6 V, half duplex configuration, $R_{TERMINATION}$ = 120 Ω, see Figure 20
Power Supply Current, Bus Side						
TxD/RxD Data Rate = 500 kbps	I_{DD2}			3.0	mA	Unloaded
				40	mA	V_{DD2} = 3.6 V, half duplex configuration, $R_{TERMINATION}$ = 120 Ω, see Figure 20
DRIVER						
Differential Outputs						
Differential Output Voltage	$\|V_{OD}\|$	2.0		3.6	V	Loaded, R_L = 100 Ω (RS-422), see Figure 14
		1.5		3.6	V	R_L = 54 Ω (RS-485), see Figure 14
		1.5		3.6	V	−7 V ≤ V_{TEST} ≤ 12 V, see Figure 15
$\Delta\|V_{OD}\|$ for Complementary Output States	$\Delta\|V_{OD}\|$			0.2	V	R_L = 54 Ω or 100 Ω, see Figure 14
Common-Mode Output Voltage	V_{OC}			3.0	V	R_L = 54 Ω or 100 Ω, see Figure 14
$\Delta\|V_{OC}\|$ for Complementary Output States	$\Delta\|V_{OC}\|$			0.2	V	R_L = 54 Ω or 100 Ω, see Figure 14
Output Leakage Current (Y, Z Pins)	I_O			30	µA	DE = 0 V, V_{DD2} = 0 V or 3.3 V, V_{IN} = 12 V
		−30			µA	DE = 0 V, V_{DD2} = 0 V or 3.3 V, V_{IN} = −7 V
Short-Circuit Output Current	I_{OS}			250	mA	
Logic Inputs (DE, $\overline{RE}$, TxD)						
Input Threshold Low	V_{IL}	0.25 × V_{DD1}			V	
Input Threshold High	V_{IH}			0.7 × V_{DD1}	V	
Input Current	I_I	−10	+0.01	+10	µA	
RECEIVER						
Differential Inputs						
Differential Input Threshold Voltage	V_{TH}	−200	−125	−30	mV	−7 V < V_{CM} < +12 V
Input Voltage Hysteresis	V_{HYS}		15		mV	V_{OC} = 0 V
Input Current (A, B)	I_I			125	µA	DE = 0 V, V_{DD} = 0 V or 3.6 V, V_{IN} = 12 V
		−100			µA	DE = 0 V, V_{DD} = 0 V or 3.6 V, V_{IN} = −7 V
Line Input Resistance	R_{IN}	96			kΩ	−7 V < V_{CM} < +12 V
Tristate Leakage Current	I_{OZR}			±1	µA	V_{DD1} = 5 V, 0 V < V_{OUT} < V_{DD1}
Logic Outputs						
Output Voltage Low	V_{OLRxD}		0.2	0.4	V	I_{ORxD} = 1.5 mA, V_A − V_B = −0.2 V
Output Voltage High	V_{OHRxD}	V_{DD1} − 0.3	V_{DD1} − 0.2		V	I_{ORxD} = −1.5 mA, V_A − V_B = +0.2 V
Short-Circuit Current				100	mA	
COMMON-MODE TRANSIENT IMMUNITY[1]		25			kV/µs	V_{CM} = 1 kV, transient magnitude = 800 V

[1] CM is the maximum common-mode voltage slew rate that can be sustained while maintaining specification-compliant operation. V_{CM} is the common-mode potential difference between the logic and bus sides. The transient magnitude is the range over which the common mode is slewed. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

TIMING SPECIFICATIONS

T_A = −40°C to +85°C.

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
DRIVER						
Propagation Delay	t_{DPLH}, t_{DPHL}	250		700	ns	R_L = 54 Ω, C_{L1} = C_{L2} = 100 pF, see Figure 16 and Figure 21
Differential Driver Output Skew ($t_{DPLH} - t_{DPHL}$)	t_{DSKEW}			100	ns	R_L = 54 Ω, C_{L1} = C_{L2} = 100 pF, see Figure 16 and Figure 21
Rise Time/Fall Time	t_{DR}, t_{DF}	200	450	1100	ns	R_L = 54 Ω, C_{L1} = C_{L2} = 100 pF, see Figure 16 and Figure 21
Enable Time	t_{ZL}, t_{ZH}			1.5	µs	R_L = 110 Ω, C_L = 50 pF, see Figure 18 and Figure 22
Disable Time	t_{LZ}, t_{HZ}			200	ns	R_L = 110 Ω, C_L = 50 pF, see Figure 18 and Figure 22
RECEIVER						
Propagation Delay	t_{PLH}, t_{PHL}			200	ns	C_L = 15 pF, see Figure 17 and Figure 23
Pulse Width Distortion, PWD = $\lvert t_{PLH} - t_{PHL} \rvert$	t_{PWD}			30	ns	C_L = 15 pF, see Figure 17 and Figure 23
Enable Time	t_{ZL}, t_{ZH}			13	ns	R_L = 1 kΩ, C_L = 15 pF, see Figure 19 and Figure 24
Disable Time	t_{LZ}, t_{HZ}			13	ns	R_L = 1 kΩ, C_L = 15 pF, see Figure 19 and Figure 24

PACKAGE CHARACTERISTICS

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
RESISTANCE						
Resistance (Input-to-Output)[1]	R_{I-O}		10^{12}		Ω	
CAPACITANCE						
Capacitance (Input-to-Output)[1]	C_{I-O}		3		pF	f = 1 MHz
Input Capacitance[2]	C_I		4		pF	
THERMAL RESISTANCE						
Input IC Junction-to-Case	θ_{JCI}		33		°C/W	Thermocouple located at center of package underside
Output IC Junction-to-Case	θ_{JCO}		28		°C/W	

[1] Device considered a 2-terminal device: Pin 1 to Pin 8 are shorted together and Pin 9 to Pin16 are shorted together.
[2] Input capacitance is from any input data pin to ground.

REGULATORY INFORMATION

Table 4.

UL[1]	CSA	VDE[2]
UL 1577 Component Recognition Program	Approved under CSA Component Acceptance Notice 5A, CSA 60950-1-07+A1+A2 and IEC 60950-1 second edition +A1+A2: Basic insulation at 780 V rms (1103 V peak) Reinforced insulation at 390 V rms (552 V peak) CSA 61010-1-12+A1 and IEC 61010-1 third edition: Basic 600 V rms, Overvoltage Category III Reinforced 300 V rms, Overvoltage Category III	Certified according to DIN V VDE V 0884-10 (VDE V 0884-10): 2006-12[2]
5000 V rms Isolation Voltage		Reinforced insulation, 849 V_{PEAK}

[1] In accordance with UL1577, each ADM2484E is proof tested by applying an insulation test voltage ≥ 6000 V rms for 1 second (current leakage detection limit = 10 µA).
[2] In accordance with DIN V VDE V 0884-10, each ADM2484E is proof tested by applying an insulation test voltage ≥ 1590 V_{PEAK} for 1 second (partial discharge detection limit = 5 pC).

INSULATION AND SAFETY-RELATED SPECIFICATIONS

Table 5.

Parameter	Symbol	Value	Unit	Conditions
Rated Dielectric Insulation Voltage		5000	V rms	1-minute duration
Minimum External Air Gap (Clearance)	L(I01)	7.7	mm min	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L(I02)	7.6	mm min	Measured from input terminals to output terminals, shortest distance along body
Minimum Internal Gap (Internal Clearance)		0.017	mm min	Insulation distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>400	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group		II		Material Group (DIN VDE 0110, 1/89, Table 1)

VDE 0884 INSULATION CHARACTERISTICS

This isolator is suitable for reinforced electrical isolation only within the safety limit data. Maintenance of the safety data must be ensured by means of protective circuits. An asterisk (*) on a package denotes VDE 0884 approval for 849 V_{PEAK} working voltage.

Table 6.

Description	Conditions	Symbol	Characteristic	Unit
CLASSIFICATIONS				
Installation Classification per DIN VDE 0110 for Rated Mains Voltage				
≤300 V rms			I to IV	
≤450 V rms			I to II	
≤600 V rms			I to II	
Climatic Classification			40/105/21	
Pollution Degree	DIN VDE 0110, see Table 1		2	
VOLTAGE				
Maximum Working Insulation Voltage		V_{IORM}	849	V_{PEAK}
Input-to-Output Test Voltage		V_{PR}		
Method b1	$V_{IORM} \times 1.875 = V_{PR}$, 100% production tested, t_m = 1 sec, partial discharge < 5 pC		1590	V_{PEAK}
Method a				
After Environmental Tests, Subgroup 1	$V_{IORM} \times 1.6 = V_{PR}$, t_m = 60 sec, partial discharge < 5 pC		1357	V_{PEAK}
After Input and/or Safety Test, Subgroup 2/Subgroup 3	$V_{IORM} \times 1.2 = V_{PR}$, t_m = 60 sec, partial discharge < 5 pC		1018	V_{PEAK}
Highest Allowable Overvoltage	(Transient overvoltage, t_{TR} = 10 sec)	V_{TR}	6000	V_{PEAK}
SAFETY-LIMITING VALUES	Maximum value allowed in the event of a failure, see Figure 9			
Case Temperature		T_S	150	°C
Input Current		$I_{S, INPUT}$	265	mA
Output Current		$I_{S, OUTPUT}$	335	mA
Insulation Resistance at T_S	V_{IO} = 500 V	R_S	$>10^9$	Ω

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted. Each voltage is relative to its respective ground.

Table 7.

Parameter	Rating
V_{DD1}	−0.5 V to +7 V
V_{DD2}	−0.5 V to +6 V
Logic Input Voltages	−0.5 V to V_{DD1} + 0.5 V
Bus Terminal Voltages	−9 V to +14 V
Logic Output Voltages	−0.5 V to V_{DD1} + 0.5 V
Average Output Current per Pin	±35 mA
ESD (Human Body Model) on A, B, Y, and Z Pins	±15 kV
Storage Temperature Range	−55°C to +150°C
Ambient Operating Temperature Range	−40°C to +85°C
θ_{JA} Thermal Impedance	73°C/W
T_J Junction Temperature	110°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Absolute maximum ratings apply individually only, not in combination.

Table 8. Maximum Continuous Working Voltage[1]

Parameter	Max	Unit	Reference Standard
AC Voltage			
Bipolar Waveform			
Basic Insulation	565	V_{PEAK}	50-year minimum lifetime
Reinforced Insulation	565	V_{PEAK}	50-year minimum lifetime
Unipolar Waveform			
Basic Insulation	1131	V_{PEAK}	50-year minimum lifetime
Reinforced Insulation	864	V_{PEAK}	Lifetime limited by package creepage maximum approved working voltage per IEC 60950-1
DC Voltage			
Basic Insulation	1066	V_{PEAK}	Lifetime limited by package creepage maximum approved working voltage per IEC 60950-1
Reinforced Insulation	529	V_{PEAK}	Lifetime limited by package creepage maximum approved working voltage per IEC 60950-1

[1] Refers to continuous voltage magnitude imposed across the isolation barrier.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

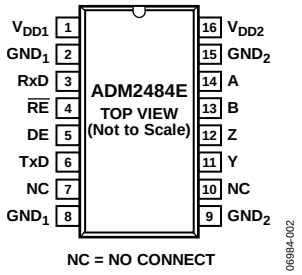

Figure 2. Pin Configuration

Table 9. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD1}	Power Supply (Logic Side). Decoupling capacitor to GND_1 required; capacitor value should be between 0.01 µF and 0.1 µF.
2	GND_1	Ground (Logic Side).
3	RxD	Receiver Output.
4	$\overline{RE}$	Receiver Enable Input. Active low logic input. When this pin is low, the receiver is enabled; when this pin is high, the receiver is disabled.
5	DE	Driver Enable Input. Active high logic input. When this pin is high, the driver (transmitter) is enabled; when this pin is low, the driver is disabled.
6	TxD	Transmit Data.
7	NC	No Connect. This pin must be left floating.
8	GND_1	Ground (Logic Side).
9	GND_2	Ground (Bus Side).
10	NC	No Connect. This pin must be left floating.
11	Y	Driver Noninverting Output.
12	Z	Driver Inverting Output.
13	B	Receiver Inverting Input.
14	A	Receiver Noninverting Input.
15	GND_2	Ground (Bus Side).
16	V_{DD2}	Power Supply (Bus Side). Decoupling capacitor to GND_2 required; capacitor value should be between 0.01 µF and 0.1 µF.

TYPICAL PERFORMANCE CHARACTERISTICS

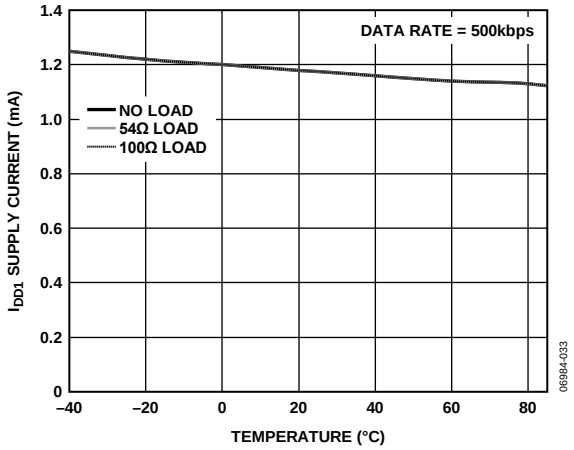

Figure 3. I_{DD1} Supply Current vs. Temperature (See Figure 20)

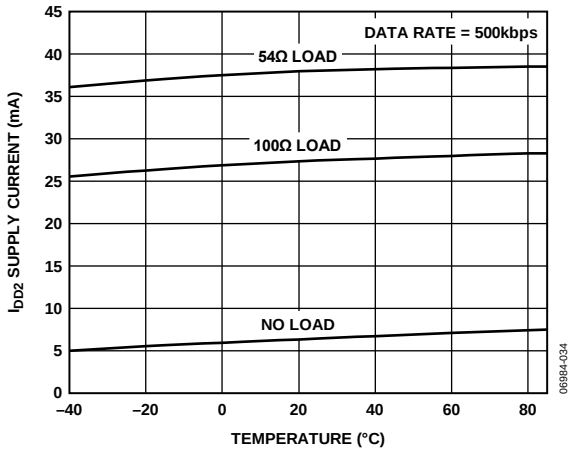

Figure 4. I_{DD2} Supply Current vs. Temperature (See Figure 20)

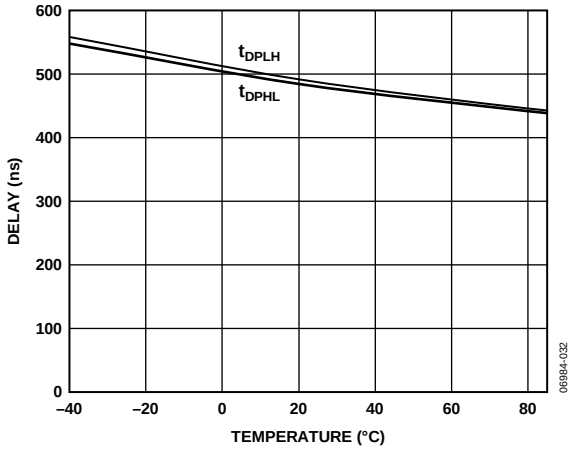

Figure 5. Driver Propagation Delay vs. Temperature

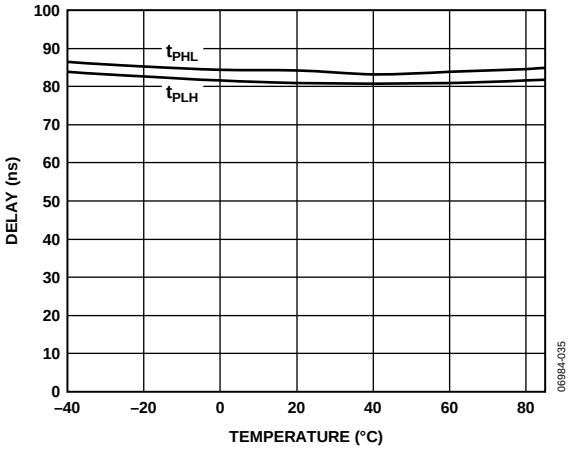

Figure 6. Receiver Propagation Delay vs. Temperature

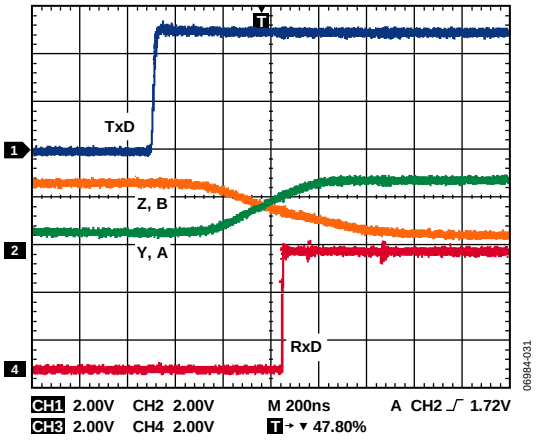

Figure 7. Driver/Receiver Propagation Delay, Low to High (R_L = 54 Ω, C_{L1} = C_{L2} = 100 pF)

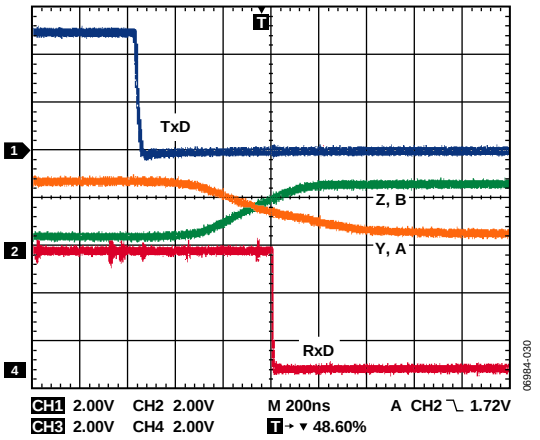

Figure 8. Driver/Receiver Propagation Delay, High to Low (R_L = 54 Ω, C_{L1} = C_{L2} = 100 pF)

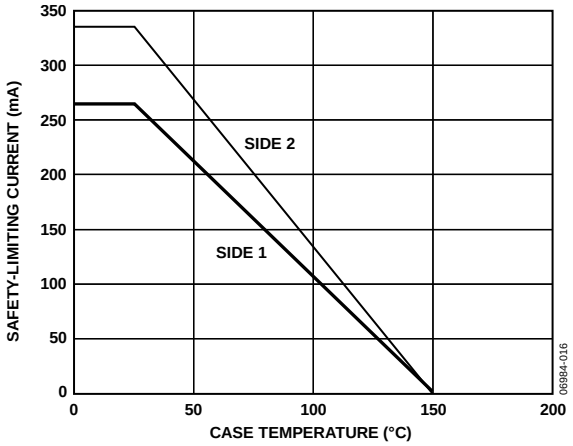

Figure 9. Thermal Derating Curve, Dependence of Safety-Limiting Values with Case Temperature per VDE 0884

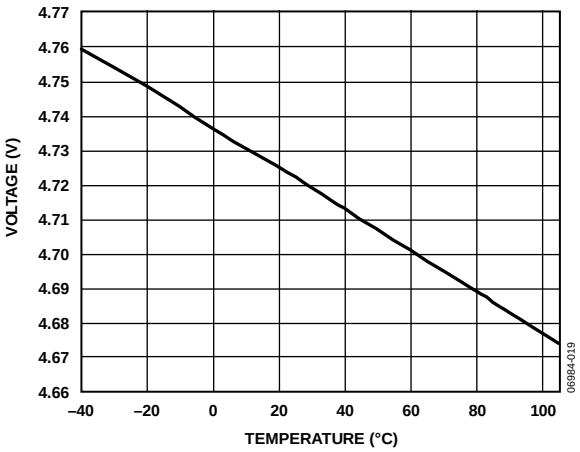

Figure 12. Receiver Output High Voltage vs. Temperature, I_{RxD} = −4 mA

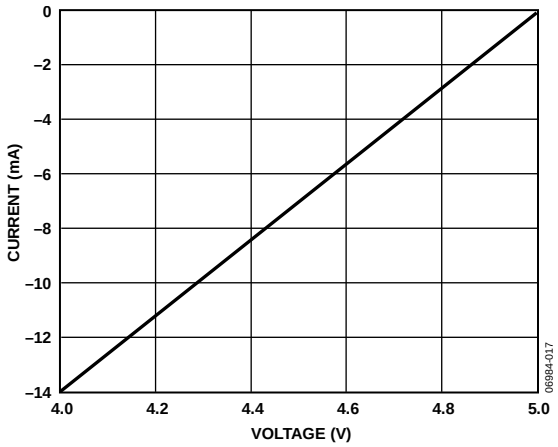

Figure 10. Output Current vs. Receiver Output High Voltage

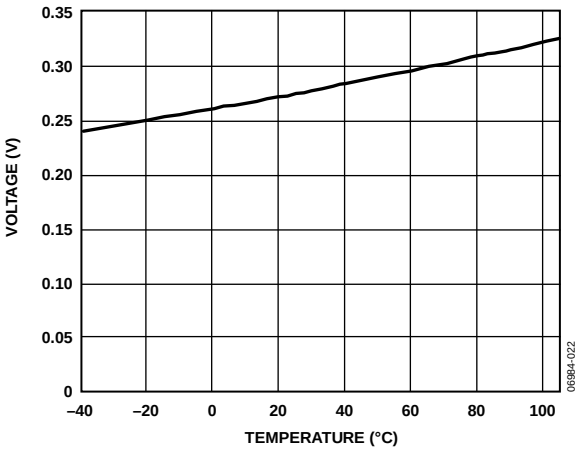

Figure 13. Receiver Output Low Voltage vs. Temperature, I_{RxD} = +4 mA

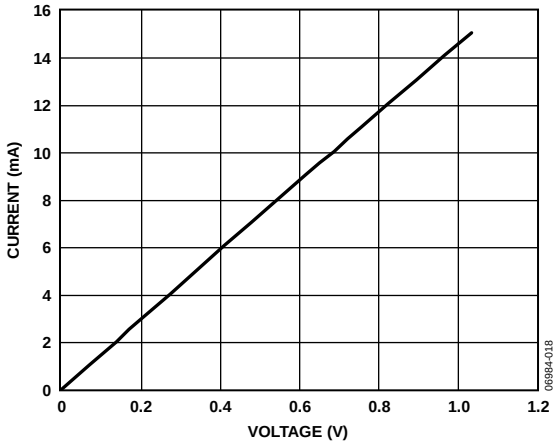

Figure 11. Output Current vs. Receiver Output Low Voltage

TEST CIRCUITS

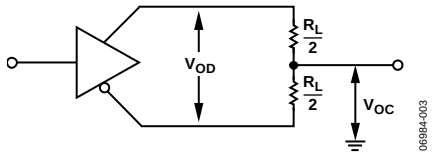

Figure 14. Driver Voltage Measurement

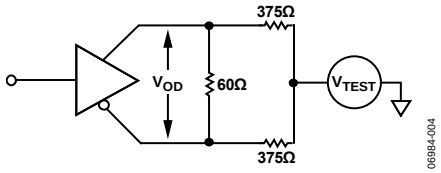

Figure 15. Driver Voltage Measurement

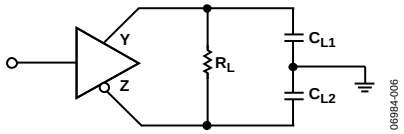

Figure 16. Driver Propagation Delay

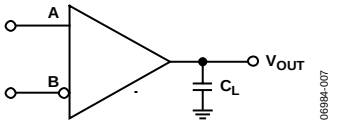

Figure 17. Receiver Propagation Delay

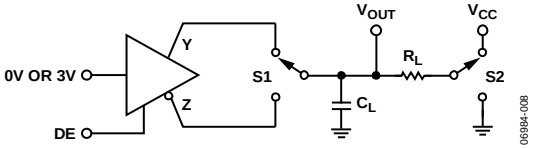

Figure 18. Driver Enable/Disable

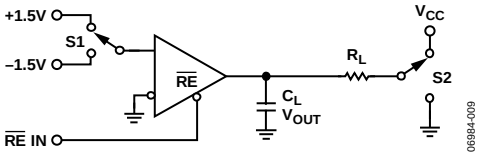

Figure 19. Receiver Enable/Disable

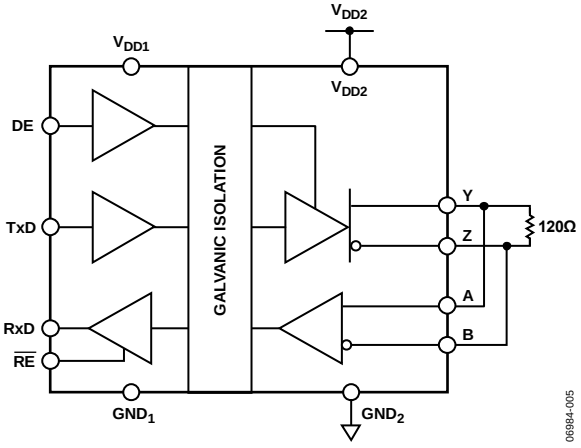

Figure 20. Supply Current Measurement Test Circuit

SWITCHING CHARACTERISTICS

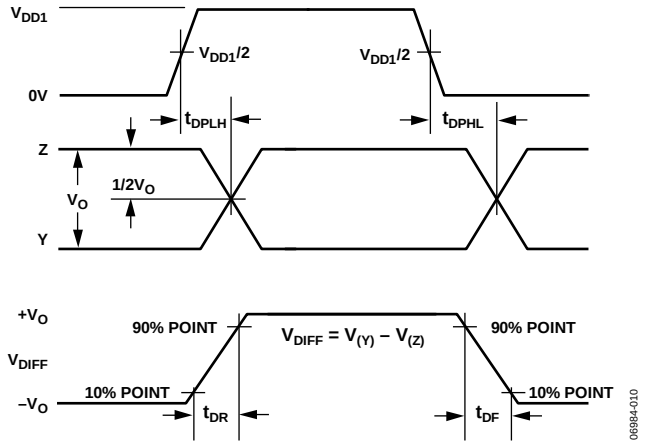

Figure 21. Driver Propagation Delay, Rise/Fall Timing

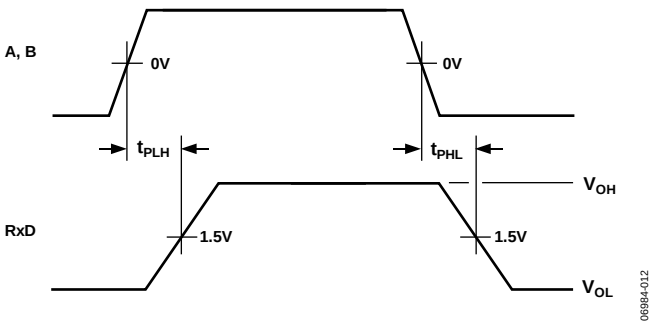

Figure 23. Receiver Propagation Delay

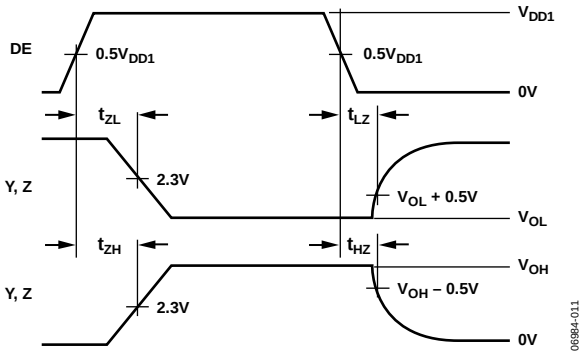

Figure 22. Driver Enable/Disable Delay

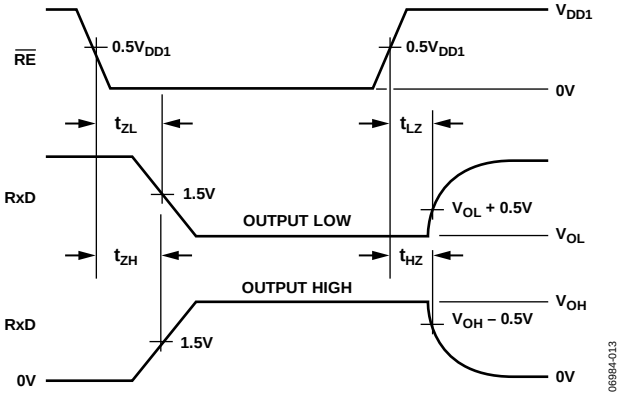

Figure 24. Receiver Enable/Disable Delay

CIRCUIT DESCRIPTION

ELECTRICAL ISOLATION

In the ADM2484E, electrical isolation is implemented on the logic side of the interface. Therefore, the part has two main sections: a digital isolation section and a transceiver section (see Figure 25). The driver input signal, which is applied to the TxD pin and referenced to the logic ground (GND_1), is coupled across an isolation barrier to appear at the transceiver section referenced to the isolated ground (GND_2). Similarly, the receiver input, which is referenced to the isolated ground in the transceiver section, is coupled across the isolation barrier to appear at the RxD pin referenced to the logic ground.

*i*Coupler *Technology*

The digital signals transmit across the isolation barrier using *i*Coupler technology. This technique uses chip scale transformer windings to couple the digital signals magnetically from one side of the barrier to the other. Digital inputs are encoded into waveforms that are capable of exciting the primary transformer winding. At the secondary winding, the induced waveforms are decoded into the binary value that was originally transmitted.

Positive and negative logic transitions at the input cause narrow (approximately 1 ns) pulses to be sent to the decoder via the transformer. The decoder is bistable and is, therefore, set or reset by the pulses, indicating input logic transitions. In the absence of logic transitions at the input for more than approximately 1 µs, a periodic set of refresh pulses, indicative of the correct input state, are sent to ensure dc correctness at the output. If the decoder receives no internal pulses for more than about 5 µs, then the input side is assumed to be unpowered or nonfunctional, in which case the output is forced to a default state (see Table 11).

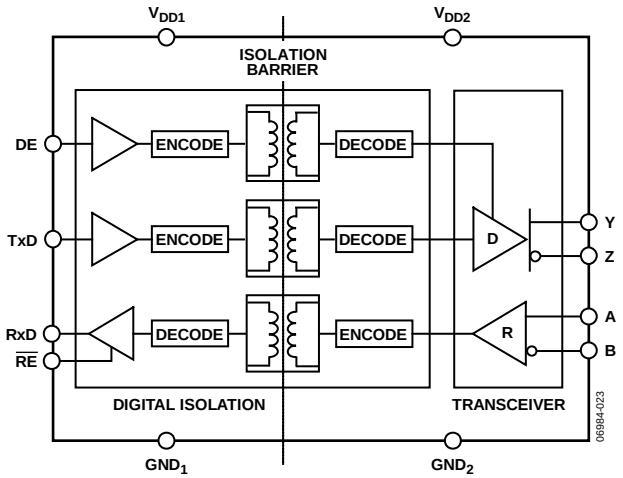

Figure 25. Digital Isolation and Transceiver Sections

TRUTH TABLES

The truth tables in this section use the abbreviations shown in Table 10.

Table 10. Truth Table Abbreviations

Letter	Description
H	High level
L	Low level
I	Indeterminate
X	Irrelevant
Z	High impedance (off)
NC	Disconnected

Table 11. Transmitting

Supply Status		Inputs		Outputs	
V_{DD1}	V_{DD2}	DE	TxD	Y	Z
On	On	H	H	H	L
On	On	H	L	L	H
On	On	L	X	Z	Z
On	Off	X	X	Z	Z
Off	On	L	X	Z	Z
Off	Off	X	X	Z	Z

Table 12. Receiving

Supply Status		Inputs		Output
V_{DD1}	V_{DD2}	A – B (V)	$\overline{RE}$	RxD
On	On	> –0.03	L or NC	H
On	On	< –0.2	L or NC	L
On	On	–0.2 < A – B < –0.03	L or NC	I
On	On	Inputs open	L or NC	H
On	On	X	H	Z
On	Off	X	L or NC	H
Off	Off	X	L or NC	L

THERMAL SHUTDOWN

The ADM2484E contains thermal shutdown circuitry that protects the part from excessive power dissipation during fault conditions. Shorting the driver outputs to a low impedance source can result in high driver currents. The thermal sensing circuitry detects the increase in die temperature under this condition and disables the driver outputs. This circuitry is designed to disable the driver outputs when a die temperature of 150°C is reached. As the device cools, the drivers re-enable at a temperature of 140°C.

TRUE FAIL-SAFE RECEIVER INPUTS

The receiver inputs have a true fail-safe feature ensuring that the receiver output is high when the inputs are open or shorted. During line-idle conditions, when no driver on the bus is enabled, the voltage across a terminating resistor at the receiver input decays to 0 V. With traditional transceivers, receiver input thresholds specified between −200 mV and +200 mV mean that external bias resistors are required on the A and B pins to ensure that the receiver outputs are in a known state. The true fail-safe receiver input feature eliminates the need for bias resistors by specifying the receiver input threshold between −30 mV and −200 mV. The guaranteed negative threshold means that when the voltage between A and B decays to 0 V; the receiver output is guaranteed to be high.

MAGNETIC FIELD IMMUNITY

The limitation on the magnetic field immunity of the *i*Coupler is set by the condition in which an induced voltage in the receiving coil of the transformer is large enough to either falsely set or reset the decoder. The following analysis defines the conditions under which this may occur. The 3 V operating condition of the ADM2484E is examined because it represents the most susceptible mode of operation.

The pulses at the transformer output have an amplitude greater then 1 V. The decoder has a sensing threshold of about 0.5 V, thus establishing a 0.5 V margin in which induced voltages can be tolerated.

The voltage induced across the receiving coil is given by

$$V = \left(\frac{-d\beta}{dt}\right)\sum \pi r_n^2 \; ; \; n = 1, 2, \ldots, N$$

where:
β is the magnetic flux density (gauss).
N is the number of turns in the receiving coil.
r_n is the radius of the nth turn in the receiving coil (cm).

Given the geometry of the receiving coil and an imposed requirement that the induced voltage is, at most, 50% of the 0.5 V margin at the decoder, a maximum allowable magnetic field can be determined using Figure 26.

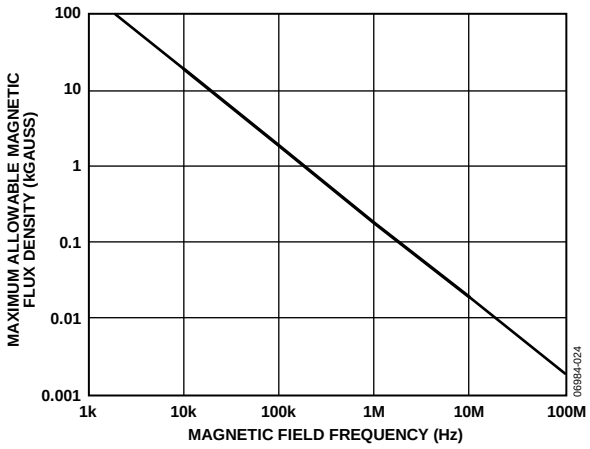

Figure 26. Maximum Allowable External Magnetic Flux Density

For example, at a magnetic field frequency of 1 MHz, the maximum allowable magnetic field of 0.2 kgauss induces a voltage of 0.25 V at the receiving coil. This is about 50% of the sensing threshold and does not cause a faulty output transition. Similarly, if such an event occurs during a transmitted pulse and is the worst-case polarity, it reduces the received pulse from >1.0 V to 0.75 V, still well above the 0.5 V sensing threshold of the decoder.

Figure 27 shows the magnetic flux density values in terms of more familiar quantities, such as maximum allowable current flow at given distances away from the ADM2484E transformers.

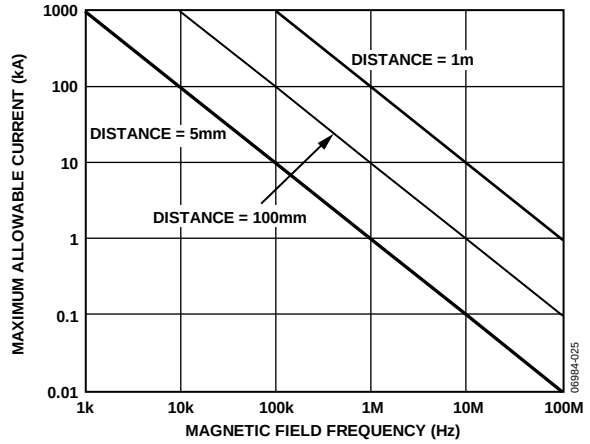

Figure 27. Maximum Allowable Current for Various Current-to-ADM2484E Spacings

With combinations of strong magnetic field and high frequency, any loops formed by PCB traces can induce error voltages large enough to trigger the thresholds of succeeding circuitry. Take care in the layout of such traces to avoid this possibility.

APPLICATIONS INFORMATION

ISOLATED POWER SUPPLY CIRCUIT

The ADM2484E requires isolated power capable of 3.3 V at up to approximately 75 mA (this current is dependent on the data rate and termination resistors used) to be supplied between the V_{DD2} and the GND_2 pins. A transformer driver circuit with a center tapped transformer and LDO can be used to generate the isolated 5 V supply, as shown in Figure 28. The center tapped transformer provides electrical isolation of the 5 V power supply. The primary winding of the transformer is excited with a pair of square waveforms that are 180° out of phase with each other. A pair of Schottky diodes and a smoothing capacitor are used to create a rectified signal from the secondary winding. The ADP3330 linear voltage regulator provides a regulated power supply to the bus-side circuitry (V_{DD2}) of the ADM2484E.

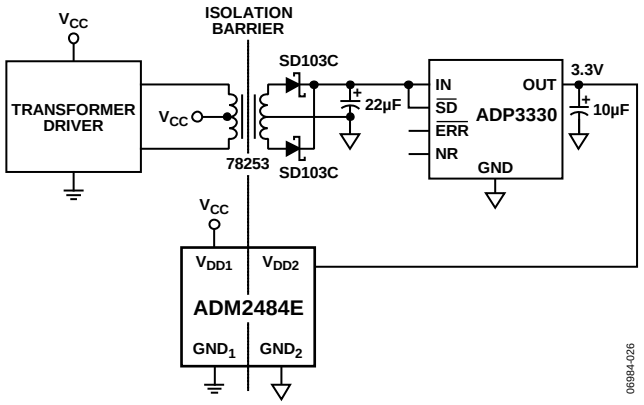

Figure 28. Isolated Power Supply Circuit

PC BOARD LAYOUT

The ADM2484E isolated RS-485 transceiver requires no external interface circuitry for the logic interfaces. Power supply bypassing is required at the input and output supply pins (see Figure 29). Bypass capacitors are conveniently connected between Pin 1 and Pin 2 for V_{DD1} and between Pin 15 and Pin 16 for V_{DD2}. Best practice suggests the following:

- A capacitor value between 0.01 µF and 0.1 µF.
- A total lead length between both ends of the capacitor and the input power supply pin that does not exceed 20 mm.
- Unless the ground pair on each package side is connected close to the package, consider bypassing between Pin 1 and Pin 8 and between Pin 9 and Pin 16.

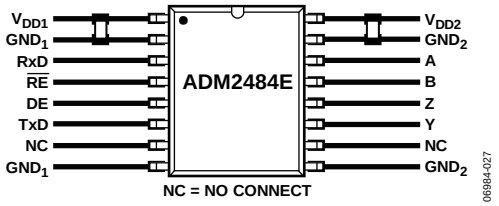

Figure 29. Recommended PCB Layout

In applications involving high common-mode transients, ensure that board coupling across the isolation barrier is minimized. Furthermore, design the board layout so that any coupling that does occur equally affects all pins on a given component side. Failure to ensure this could cause voltage differentials between pins exceeding the absolute maximum ratings of the device, thereby leading to latch-up or permanent damage.

TYPICAL APPLICATIONS

Figure 30 and Figure 31 show typical applications of the ADM2484E in half-duplex and full-duplex RS-485 network configurations. Up to 256 transceivers can be connected to the RS-485 bus. To minimize reflections, the line must be terminated at the receiving end in its characteristic impedance, and stub lengths off the main line must be kept as short as possible. For half-duplex operation, this means that both ends of the line must be terminated, because either end can be the receiving end.

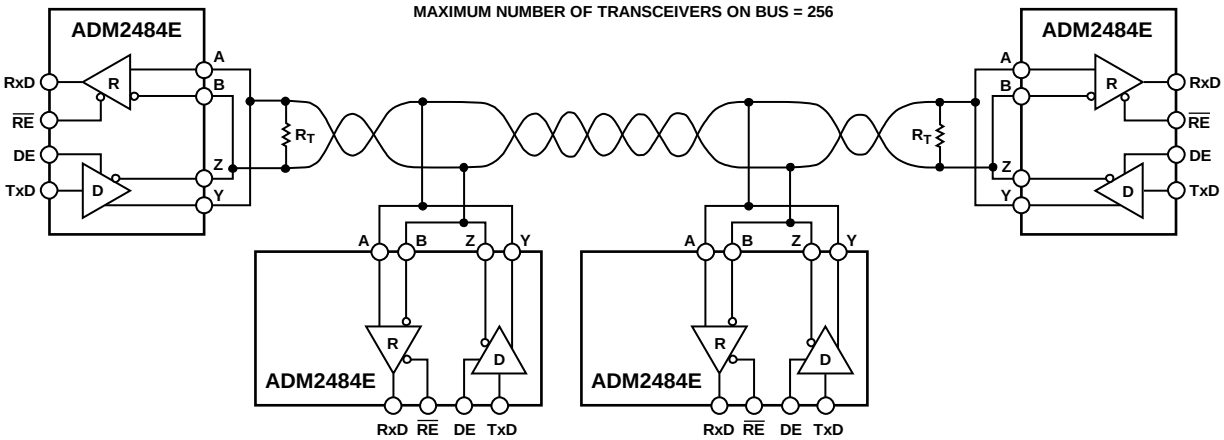

Figure 30. ADM2484E Typical Half-Duplex RS-485 Network

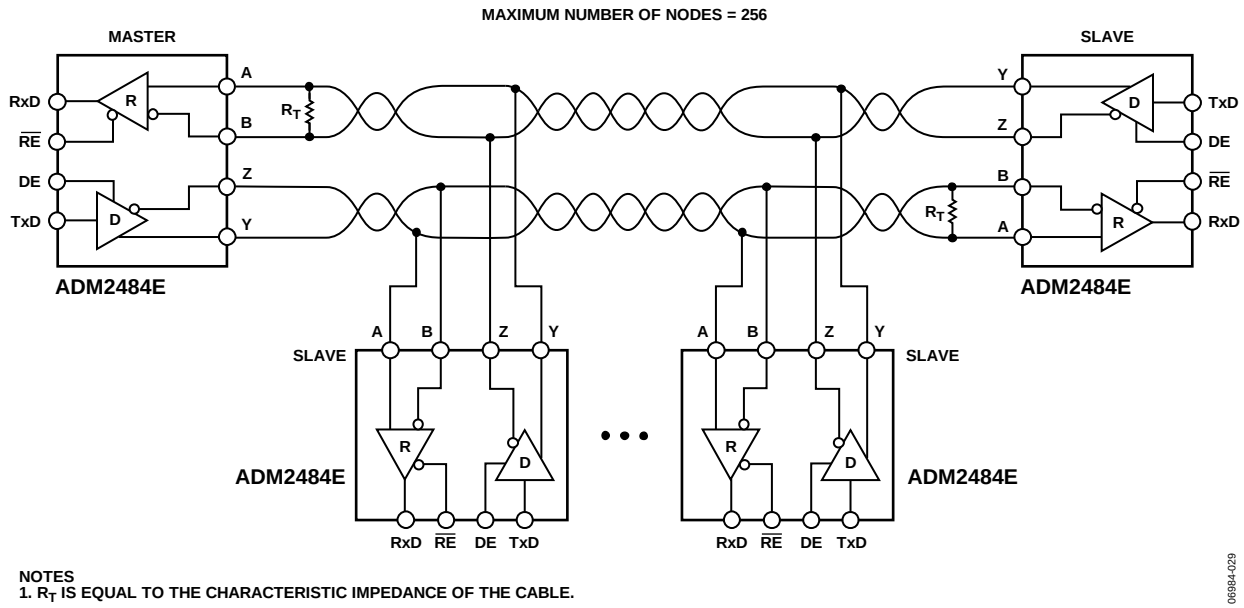

Figure 31. ADM2484E Typical Full Duplex RS-485 Network

OUTLINE DIMENSIONS

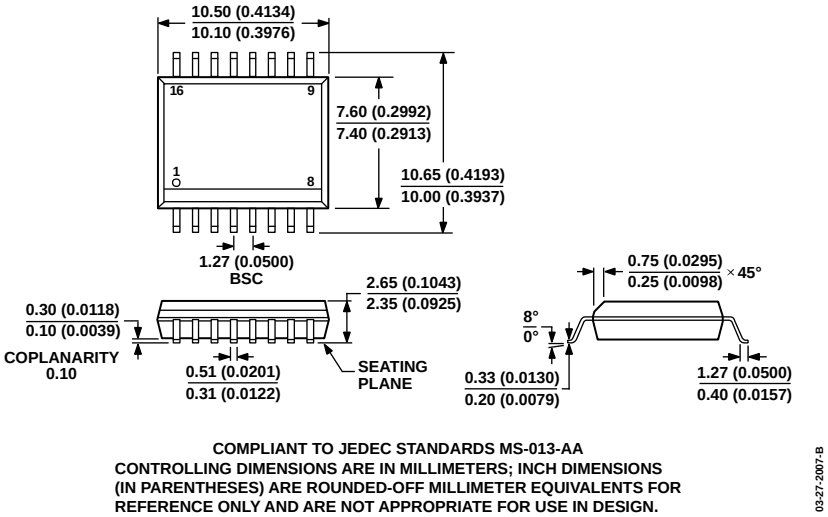

Figure 32. 16-Lead Standard Small Outline Package [SOIC_W]
Wide Body
(RW-16)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADM2484EBRWZ	−40°C to +85°C	16-Lead Standard Small Outline Package [SOIC_W]	RW-16
ADM2484EBRWZ-REEL7	−40°C to +85°C	16-Lead Standard Small Outline Package [SOIC_W]	RW-16
EVAL-ADM2484EEBZ		Evaluation Board	

[1] Z = RoHS Compliant Part.