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7/11—Revision 0: Initial Version

SPECIFICATIONS

All voltages are relative to their respective ground; 3.0 ≤ V_{CC} ≤ 5.5 V. All minimum/maximum specifications apply over the entire recommended operation range, unless otherwise noted. All typical specifications are at T_A = 25°C, V_{CC} = 5 V unless otherwise noted.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
ADM2687E SUPPLY CURRENT	I_{CC}					
Data Rate ≤ 500 kbps			90		mA	V_{CC} = 3.3 V, 100 Ω load between Y and Z
			72		mA	V_{CC} = 5 V, 100 Ω load between Y and Z
			125		mA	V_{CC} = 3.3 V, 54 Ω load between Y and Z
			98		mA	V_{CC} = 5 V, 54 Ω load between Y and Z
				140	mA	120 Ω load between Y and Z
ADM2682E SUPPLY CURRENT	I_{CC}					
Data Rate = 16 Mbps				175	mA	120 Ω load between Y and Z
				260	mA	54 Ω load between Y and Z
Data Rate = 16 Mbps, 4.5 ≤ V_{CC} ≤ 5.5 V				130	mA	120 Ω load between Y and Z
				200	mA	54 Ω load between Y and Z
ISOLATED SUPPLY VOLTAGE	V_{ISOOUT}		3.3		V	
DRIVER						
Differential Outputs						
Differential Output Voltage, Loaded	$\lvert V_{OD2}\rvert$	2.0		3.6	V	R_L = 100 Ω (RS-422), see Figure 29
		1.5		3.6	V	R_L = 54 Ω (RS-485), see Figure 29
	$\lvert V_{OD3}\rvert$	1.5		3.6	V	−7 V ≤ V_{TEST1} ≤ 12 V, see Figure 30
Δ$\lvert V_{OD}\rvert$ for Complementary Output States	Δ$\lvert V_{OD}\rvert$			0.2	V	R_L = 54 Ω or 100 Ω, see Figure 29
Common-Mode Output Voltage	V_{OC}			3.0	V	R_L = 54 Ω or 100 Ω, see Figure 29
Δ$\lvert V_{OC}\rvert$ for Complementary Output States	Δ$\lvert V_{OC}\rvert$			0.2	V	R_L = 54 Ω or 100 Ω, see Figure 29
Short-Circuit Output Current	I_{OS}			200	mA	
Output Leakage Current (Y, Z)	I_O			30	µA	DE = 0 V, $\overline{RE}$ = 0 V, V_{CC} = 0 V or 3.6 V, V_{IN} = 12 V
		−30			µA	DE = 0 V, $\overline{RE}$ = 0 V, V_{CC} = 0 V or 3.6 V, V_{IN} = −7 V
Logic Inputs DE, $\overline{RE}$, TxD						
Input Threshold Low	V_{IL}	0.27 V_{CC}			V	DE, $\overline{RE}$, TxD
Input Threshold High	V_{IH}			0.7 V_{CC}	V	DE, $\overline{RE}$, TxD
Input Current	I_I	−10	0.01	10	µA	DE, $\overline{RE}$, TxD
RECEIVER						
Differential Inputs						
Differential Input Threshold Voltage	V_{TH}	−200	−125	−30	mV	−7 V < V_{CM} < +12 V
Input Voltage Hysteresis	V_{HYS}		15		mV	V_{OC} = 0 V
Input Current (A, B)	I_I			125	µA	DE = 0 V, V_{CC} = 0 V or 3.6 V, V_{IN} = 12 V
		−100			µA	DE = 0 V, V_{CC} = 0 V or 3.6 V, V_{IN} = −7 V
Line Input Resistance	R_{IN}	96			kΩ	−7 V < V_{CM} < +12 V
Logic Outputs						
Output Voltage Low	V_{OL}		0.2	0.4	V	I_O = 1.5 mA, V_A − V_B = −0.2 V
Output Voltage High	V_{OH}	V_{CC} − 0.3	V_{CC} − 0.2		V	I_O = −1.5 mA, V_A − V_B = 0.2 V
Short-Circuit Current				100	mA	
COMMON-MODE TRANSIENT IMMUNITY[1]		25			kV/µs	V_{CM} = 1 kV, transient magnitude = 800 V

[1] CM is the maximum common-mode voltage slew rate that can be sustained while maintaining specification-compliant operation. V_{CM} is the common-mode potential difference between the logic and bus sides. The transient magnitude is the range over which the common-mode is slewed. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

ADM2682E TIMING SPECIFICATIONS

T_A = −40°C to +85°C.

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DRIVER						
Maximum Data Rate		16			Mbps	
Propagation Delay, Low to High	t_{DPLH}		63	100	ns	R_L = 54 Ω, C_{L1} = C_{L2} = 100 pF, see Figure 31 and Figure 35
Propagation Delay, High to Low	t_{DPHL}		64	100	ns	R_L = 54 Ω, C_{L1} = C_{L2} = 100 pF, see Figure 31 and Figure 35
Output Skew	t_{SKEW}		1	8	ns	R_L = 54 Ω, C_{L1} = C_{L2} = 100 pF, see Figure 31 and Figure 35
Rise Time/Fall Time	t_{DR}, t_{DF}			15	ns	R_L = 54 Ω, C_{L1} = C_{L2} = 100 pF, see Figure 31 and Figure 35
Enable Time	t_{ZL}, t_{ZH}			120	ns	R_L = 110 Ω, C_L = 50 pF, see Figure 32 and Figure 37
Disable Time	t_{LZ}, t_{HZ}			150	ns	R_L = 110 Ω, C_L = 50 pF, see Figure 32 and Figure 37
RECEIVER						
Propagation Delay, Low to High	t_{RPLH}		94	110	ns	C_L = 15 pF, see Figure 33 and Figure 36
Propagation Delay, High to Low	t_{RPHL}		95	110	ns	C_L = 15 pF, see Figure 33 and Figure 36
Output Skew[1]	t_{SKEW}		1	12	ns	C_L = 15 pF, see Figure 33 and Figure 36
Enable Time	t_{ZL}, t_{ZH}			15	ns	R_L = 1 kΩ, C_L = 15 pF, see Figure 34 and Figure 38
Disable Time	t_{LZ}, t_{HZ}			15	ns	R_L = 1 kΩ, C_L = 15 pF, see Figure 34 and Figure 38

[1] Guaranteed by design.

ADM2687E TIMING SPECIFICATIONS

T_A = −40°C to +85°C.

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DRIVER						
Maximum Data Rate		500			kbps	
Propagation Delay, Low to High	t_{DPLH}	250	503	700	ns	R_L = 54 Ω, C_{L1} = C_{L2} = 100 pF, see Figure 31 and Figure 35
Propagation Delay, High to Low	t_{DPHL}	250	510	700	ns	R_L = 54 Ω, C_{L1} = C_{L2} = 100 pF, see Figure 31 and Figure 35
Output Skew	t_{SKEW}		7	100	ns	R_L = 54 Ω, C_{L1} = C_{L2} = 100 pF, see Figure 31 and Figure 35
Rise Time/Fall Time	t_{DR}, t_{DF}	200		1100	ns	R_L = 54 Ω, C_{L1} = C_{L2} = 100 pF, see Figure 31 and Figure 35
Enable Time	t_{ZL}, t_{ZH}			2.5	µs	R_L = 110 Ω, C_L = 50 pF, see Figure 32 and Figure 37
Disable Time	t_{LZ}, t_{HZ}			200	ns	R_L = 110 Ω, C_L = 50 pF, see Figure 32 and Figure 37
RECEIVER						
Propagation Delay, Low to High	t_{RPLH}		91	200	ns	C_L = 15 pF, see Figure 33 and Figure 36
Propagation Delay, High to Low	t_{RPHL}		95	200	ns	C_L = 15 pF, see Figure 33 and Figure 36
Output Skew	t_{SKEW}		4	30	ns	C_L = 15 pF, see Figure 33 and Figure 36
Enable Time	t_{ZL}, t_{ZH}			15	ns	R_L = 1 kΩ, C_L = 15 pF, see Figure 34 and Figure 38
Disable Time	t_{LZ}, t_{HZ}			15	ns	R_L = 1 kΩ, C_L = 15 pF, see Figure 34 and Figure 38

PACKAGE CHARACTERISTICS

Table 4.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Resistance (Input-to-Output)[1]	R_{I-O}		10^{12}		Ω	
Capacitance (Input-to-Output)[1]	C_{I-O}		3		pF	f = 1 MHz
Input Capacitance[2]	C_I		4		pF	

[1] Device considered a 2-terminal device: short together Pin 1 to Pin 8 and short together Pin 9 to Pin 16.
[2] Input capacitance is from any input data pin to ground.

REGULATORY INFORMATION

Table 5. ADM2682E/ADM2687E Approvals

Organization	Approval Type
UL	To be recognized under the UL 1577 Component Recognition Program of Underwriters Laboratories, Inc. Single protection, 5000 V rms isolation voltage. In accordance with UL 1577, each ADM2682E/ADM2687E is proof tested by applying an insulation test voltage ≥ 6000 V rms for 1 second.
CSA (Pending)	To be approved under CSA Component Acceptance Notice #5A. Reinforced insulation per IEC 60601-1, 250 V rms (353 V peak) maximum working voltage. Basic insulation per IEC 60601-1, 400 V rms (566 V peak) maximum working voltage. Reinforced insulation per CSA 60950-1-07 and IEC 60950-1, 380 V rms (537 V peak) maximum working voltage. Basic insulation per CSA 60950-1-07 and IEC 60950-1, 600 V rms (848 V peak) maximum working voltage.
VDE	Certified according to DIN V VDE V 0884-10 (VDE 0884-10): 2006-12. In accordance with DIN EN 60747-5-2, each ADM2682E/ADM2687E is proof tested by applying an insulation test voltage ≥1590 V peak for 1 second.

INSULATION AND SAFETY-RELATED SPECIFICATIONS

Table 6.

Parameter	Symbol	Value	Unit	Test Conditions/Comments
Rated Dielectric Insulation Voltage		5000	V rms	1-minute duration
Minimum External Air Gap (Clearance)	L(I01)	>8.0	mm	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L(I02)	>8.0	mm	Measured from input terminals to output terminals, shortest distance along body
Minimum Internal Gap (Internal Clearance)		0.017 min	mm	Insulation distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>175	V	DIN IEC 112/VDE 0303-1
Isolation Group		IIIa		Material Group (DIN VDE 0110:1989-01, Table 1)

VDE 0884-10 INSULATION CHARACTERISTICS

This isolator is suitable for reinforced electrical isolation only within the safety limit data. Maintenance of the safety data must be ensured by means of protective circuits.

Table 7.

Description	Test Conditions/Comments	Symbol	Characteristic	Unit
CLASSIFICATIONS				
Installation Classification per DIN VDE 0110 for Rated Mains Voltage				
≤300 V rms			I to IV	
≤450 V rms			I to III	
≤600 V rms			I to II	
Climatic Classification			40/85/21	
Pollution Degree	Table 1 of DIN VDE 0110		2	
VOLTAGE				
Maximum Working Insulation Voltage		V_{IORM}	846	V peak
Input-to-Output Test Voltage		V_{PR}		
Method b1	$V_{IORM} \times 1.875 = V_{PR}$, 100% production tested, t_m = 1 sec, partial discharge < 5 pC		1590	V peak
Method a				
After Environmental Tests, Subgroup 1	$V_{IORM} \times 1.6 = V_{PR}$, t_m = 60 sec, partial discharge < 5 pC		1375	V peak
After Input and/or Safety Test, Subgroup 2/Subgroup 3	$V_{IORM} \times 1.2 = V_{PR}$, t_m = 60 sec, partial discharge < 5 pC		1018	V peak
Highest Allowable Overvoltage	Transient overvoltage, t_{TR} = 10 sec	V_{TR}	6000	V peak
SAFETY-LIMITING VALUES	Maximum value allowed in the event of a failure			
Case Temperature		T_S	150	°C
Input Current		$I_{S, INPUT}$	265	mA
Output Current		$I_{S, OUTPUT}$	335	mA
Insulation Resistance at T_S	V_{IO} = 500 V	R_S	$>10^9$	Ω

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted. All voltages are relative to their respective ground.

Table 8.

Parameter	Rating
V_{CC}	−0.5 V to +7 V
Digital Input Voltage (DE, $\overline{RE}$, TxD)	−0.5 V to V_{DD} + 0.5 V
Digital Output Voltage (RxD)	−0.5 V to V_{DD} + 0.5 V
Driver Output/Receiver Input Voltage	−9 V to +14 V
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−55°C to +150°C
ESD (Human Body Model) on A, B, Y, and Z pins	±15 kV
ESD (Human Body Model) on Other Pins	±2 kV
Thermal Resistance θ_{JA}	52°C/W
Lead Temperature	
Soldering (10 sec)	260°C
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Table 9. Maximum Continuous Working Voltage[1]

Parameter	Max	Unit	Reference Standard
AC Voltage			
Bipolar Waveform	424	V peak	All certifications, 50-year minimum lifetime
Unipolar Waveform			
Basic Insulation	600	V peak	
Reinforced Insulation	537	V peak	Maximum approved working voltage per IEC 60950-1
DC Voltage			
Basic Insulation	600	V peak	
Reinforced Insulation	537	V peak	Maximum approved working voltage per IEC 60950-1

[1] Refers to continuous voltage magnitude imposed across the isolation barrier. See the Insulation Lifetime section for more details.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

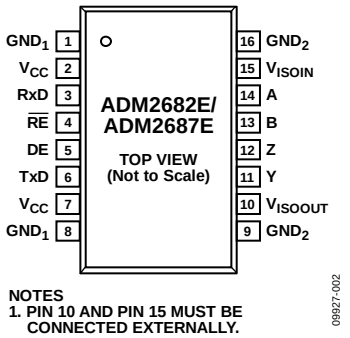


Figure 2. Pin Configuration

Table 10. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	GND_1	Ground, Logic Side.
2	V_{CC}	Logic Side Power Supply. It is recommended that a 0.1 µF and a 0.01 µF decoupling capacitor be fitted between Pin 2 and Pin 1.
3	RxD	Receiver Output Data. This output is high when (A − B) ≥ −30 mV and low when (A − B) ≤ −200 mV. The output is tristated when the receiver is disabled, that is, when $\overline{RE}$ is driven high.
4	$\overline{RE}$	Receiver Enable Input. This is an active-low input. Driving this input low enables the receiver, while driving it high disables the receiver.
5	DE	Driver Enable Input. Driving this input high enables the driver, while driving it low disables the driver.
6	TxD	Driver Input. Data to be transmitted by the driver is applied to this input.
7	V_{CC}	Logic Side Power Supply. It is recommended that a 0.1 µF and a 10 µF decoupling capacitor be fitted between Pin 7 and Pin 8.
8	GND_1	Ground, Logic Side.
9	GND_2	Ground, Bus Side.
10	V_{ISOOUT}	Isolated Power Supply Output. This pin must be connected externally to V_{ISOIN}. It is recommended that a reservoir capacitor of 10 µF and a decoupling capacitor of 0.1 µF be fitted between Pin 10 and Pin 9.
11	Y	Driver Noninverting Output
12	Z	Driver Inverting Output
13	B	Receiver Inverting Input.
14	A	Receiver Noninverting Input.
15	V_{ISOIN}	Isolated Power Supply Input. This pin must be connected externally to V_{ISOOUT}. It is recommended that a 0.1 µF and a 0.01 µF decoupling capacitor be fitted between Pin 15 and Pin 16.
16	GND_2	Ground, Bus Side.

TYPICAL PERFORMANCE CHARACTERISTICS

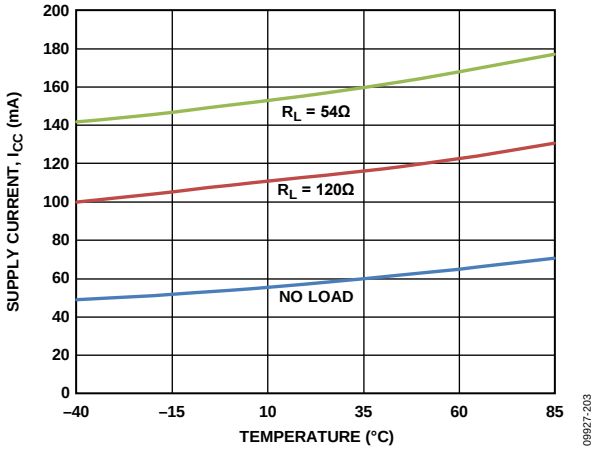


Figure 3. ADM2682E Supply Current (I_{CC}) vs. Temperature (Data Rate = 16 Mbps, DE = 3.3 V, V_{CC} = 3.3 V)

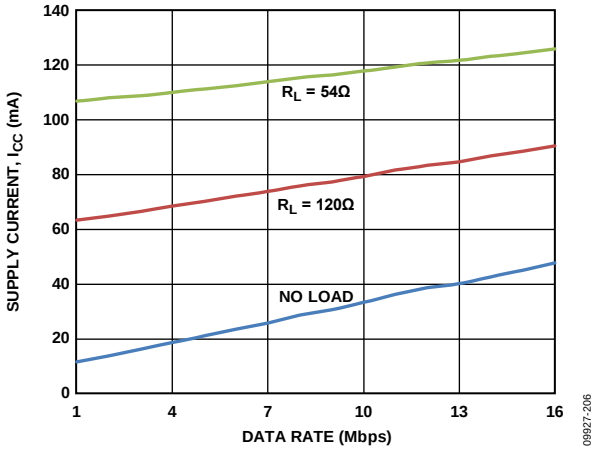


Figure 6. ADM2682E Supply Current (I_{CC}) vs. Data Rate (T_A = 25°C, DE = 5 V, V_{CC} = 5 V)

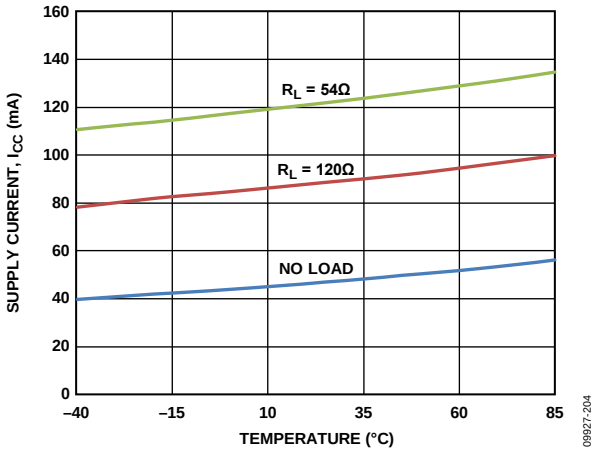


Figure 4. ADM2682E Supply Current (I_{CC}) vs. Temperature (Data Rate = 16 Mbps, DE = 5 V, V_{CC} = 5 V)

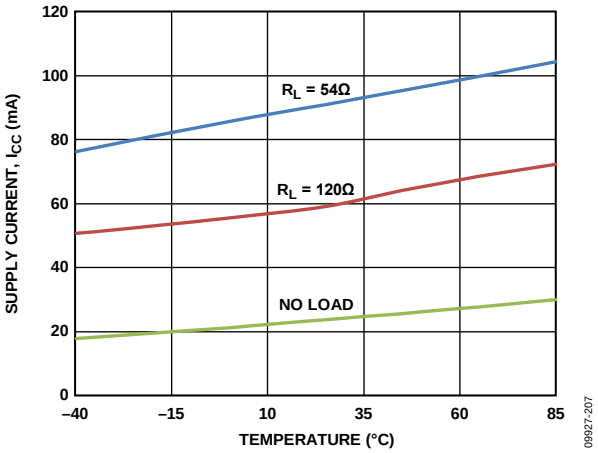


Figure 7. ADM2687E Supply Current (I_{CC}) vs. Temperature (Data Rate = 500 kbps, DE = 5 V, V_{CC} = 5 V)

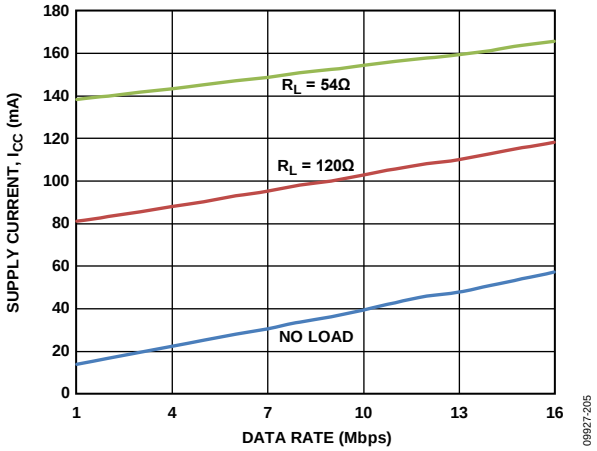


Figure 5. ADM2682E Supply Current (I_{CC}) vs. Data Rate (T_A = 25°C, DE = 3.3 V, V_{CC} = 3.3 V)

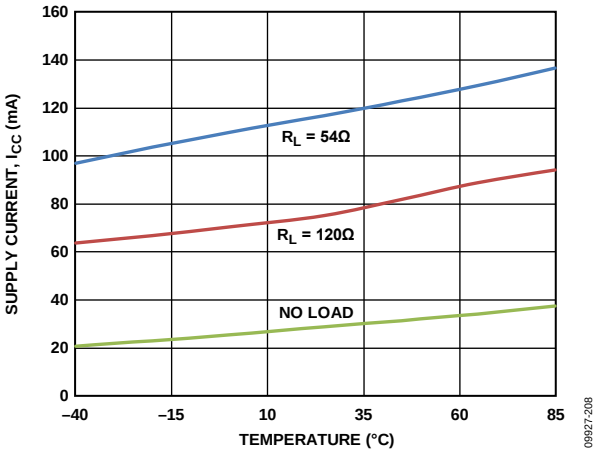


Figure 8. ADM2687E Supply Current (I_{CC}) vs. Temperature (Data Rate = 500 kbps, DE = 3.3 V, V_{CC} = 3.3 V)

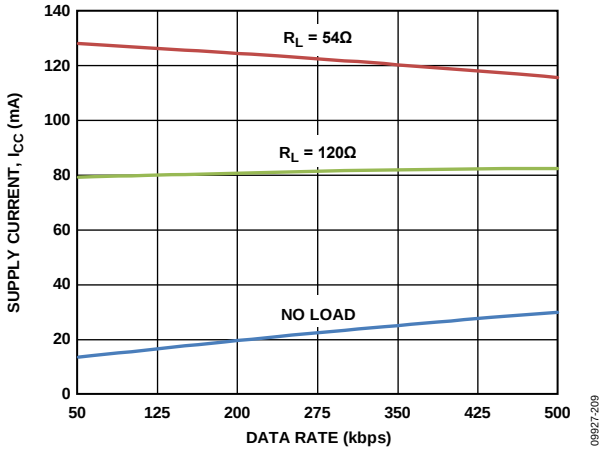


Figure 9. ADM2687E Supply Current (I_{CC}) vs. Data Rate (T_A = 25°C, DE = 3.3 V, V_{CC} = 3.3 V)

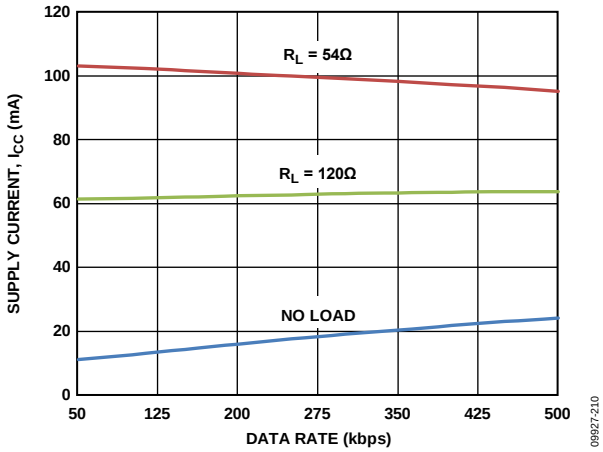


Figure 10. ADM2687E Supply Current (I_{CC}) vs. Data Rate (T_A = 25°C, DE = 5 V, V_{CC} = 5 V)

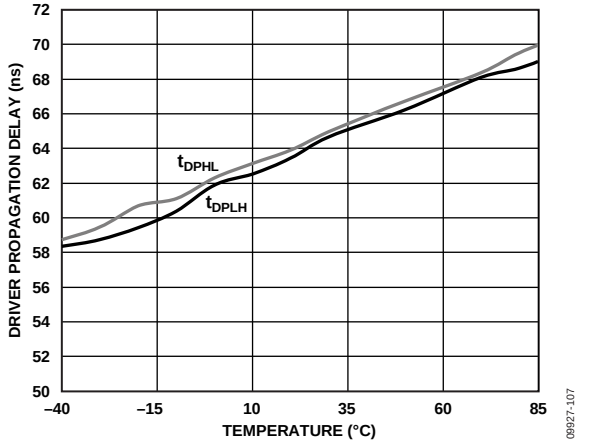


Figure 11. ADM2682E Differential Driver Propagation Delay vs. Temperature

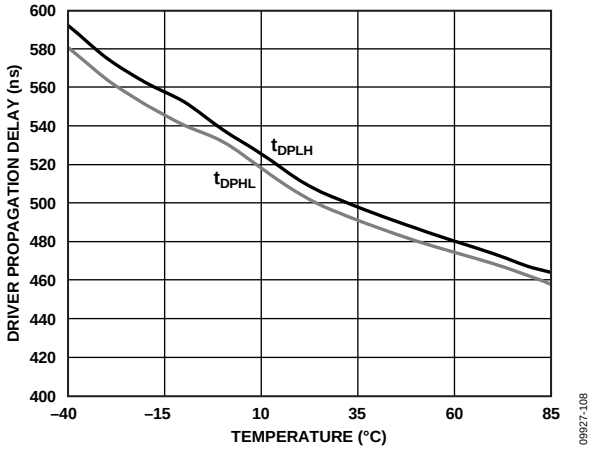


Figure 12. ADM2687E Differential Driver Propagation Delay vs. Temperature

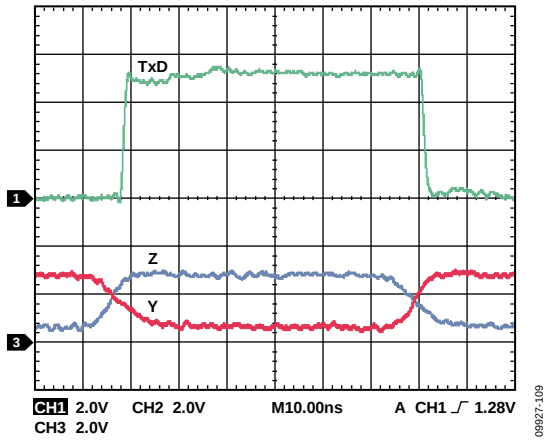


Figure 13. ADM2682E Driver Propagation Delay

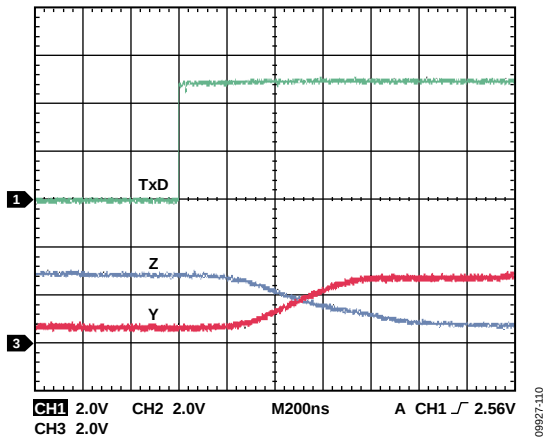


Figure 14. ADM2687E Driver Propagation Delay

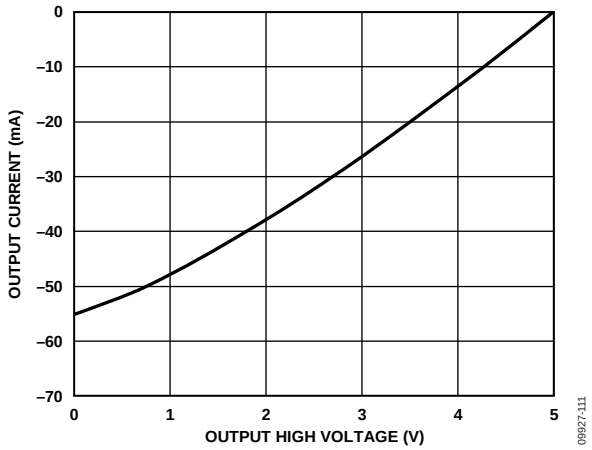


Figure 15. Receiver Output Current vs. Receiver Output High Voltage

Figure 16. Receiver Output Current vs. Receiver Output Low Voltage

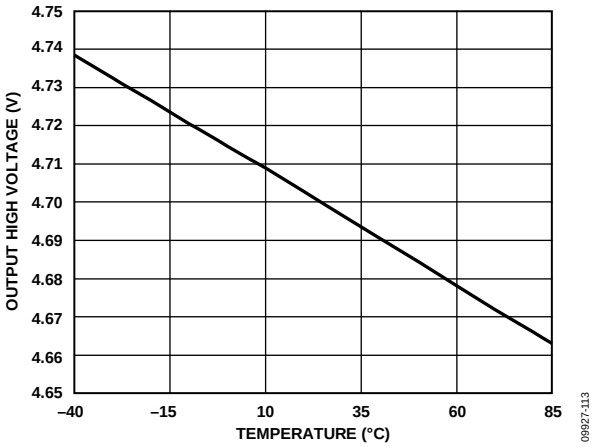


Figure 17. Receiver Output High Voltage vs. Temperature

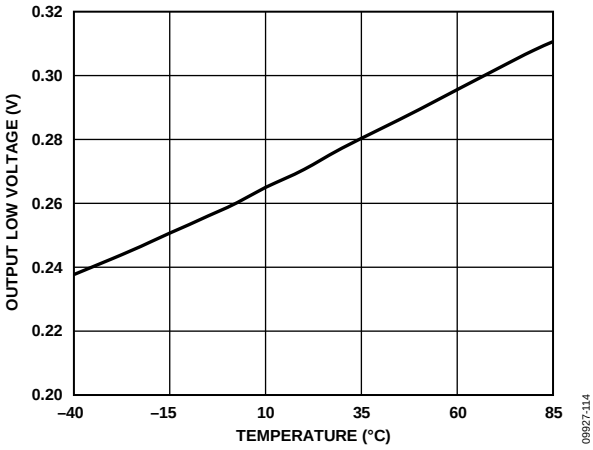


Figure 18. Receiver Output Low Voltage vs. Temperature

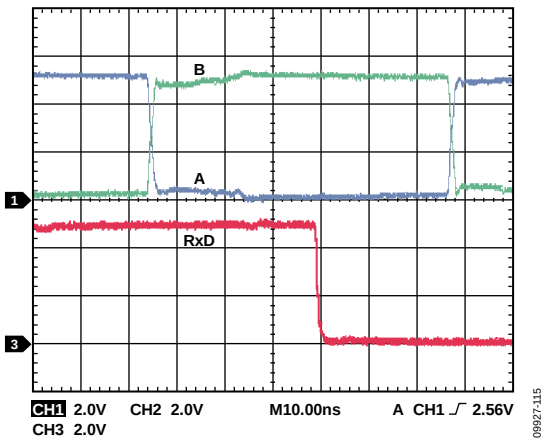


Figure 19. ADM2682E Receiver Propagation Delay

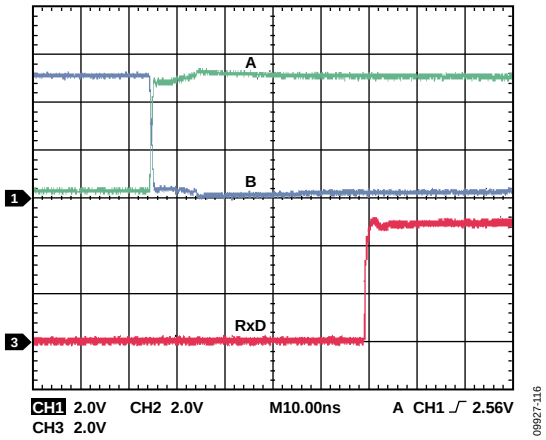


Figure 20. ADM2687E Receiver Propagation Delay

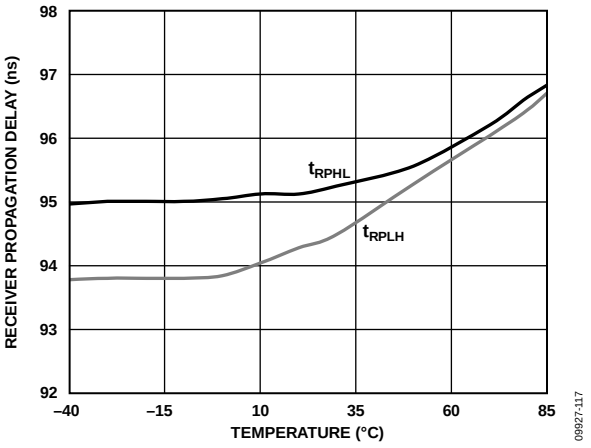


Figure 21. ADM2682E Receiver Propagation Delay vs. Temperature

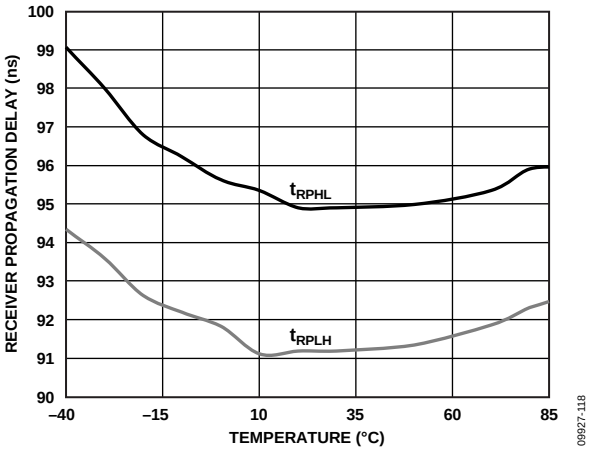


Figure 22. ADM2687E Receiver Propagation Delay vs. Temperature

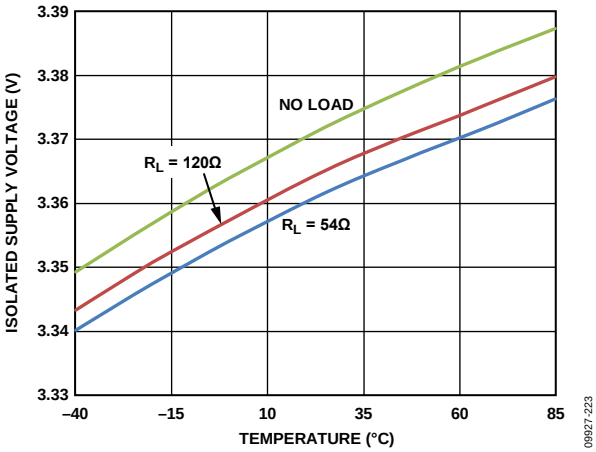


Figure 23. ADM2682E Isolated Supply Voltage vs. Temperature (V_{CC} = 3.3 V, Data Rate = 16 Mbps)

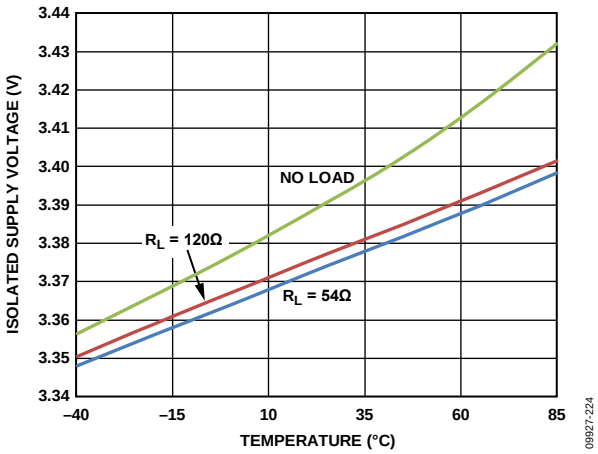


Figure 24. ADM2682E Isolated Supply Voltage vs. Temperature (V_{CC} = 5 V, Data Rate = 16 Mbps)

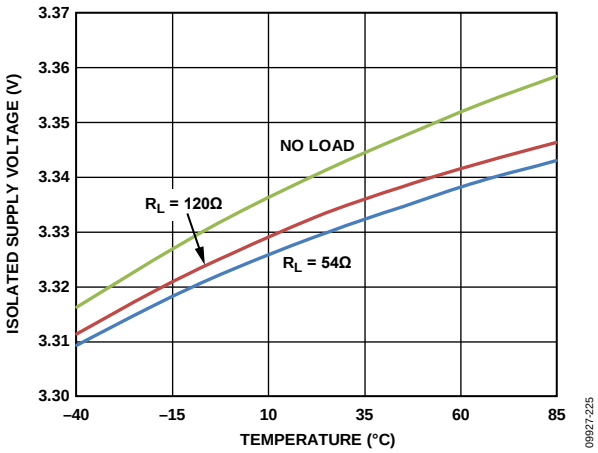


Figure 25. ADM2687E Isolated Supply Voltage vs. Temperature (V_{CC} = 3.3 V, Data Rate = 500 kbps)

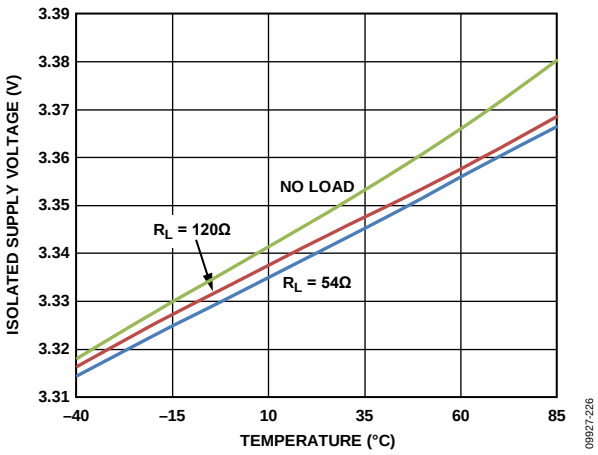


Figure 26. ADM2687E Isolated Supply Voltage vs. Temperature (V_{CC} = 5 V, Data Rate = 500 kbps)

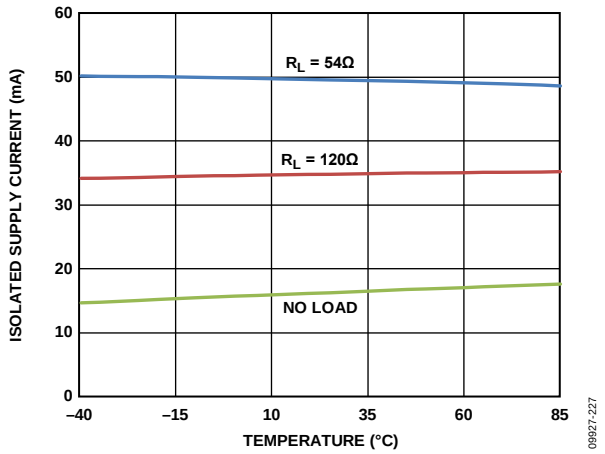


Figure 27. ADM2682E Isolated Supply Current vs. Temperature (V_{CC} = 3.3 V, Data Rate = 16 Mbps)

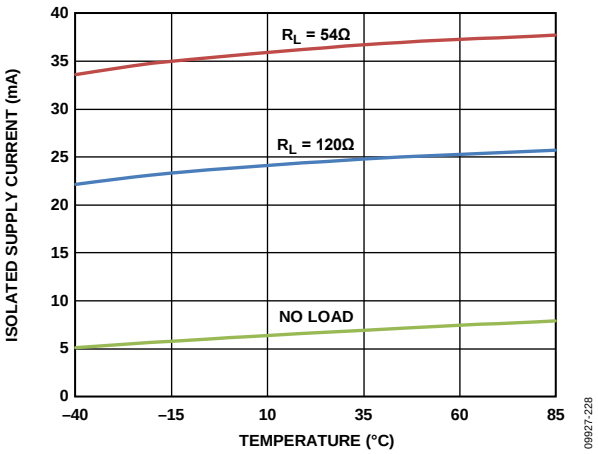


Figure 28. ADM2687E Isolated Supply Current vs. Temperature (V_{CC} = 3.3 V, Data Rate = 500 kbps)

TEST CIRCUITS

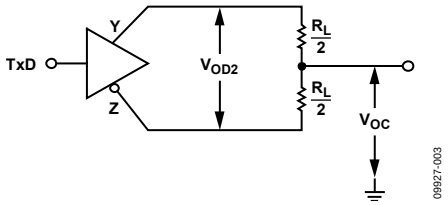


Figure 29. Driver Voltage Measurement

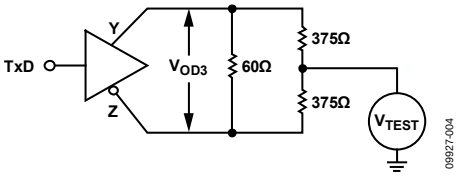


Figure 30. Driver Voltage Measurement over Common Mode

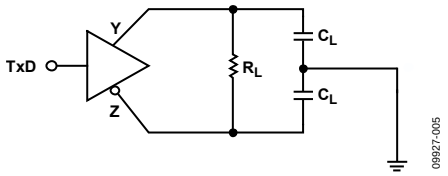


Figure 31. Driver Propagation Delay

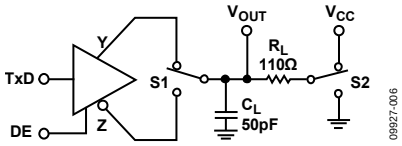


Figure 32. Driver Enable/Disable

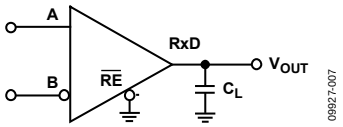


Figure 33. Receiver Propagation Delay

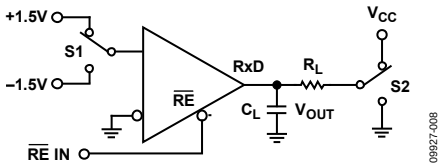


Figure 34. Receiver Enable/Disable

SWITCHING CHARACTERISTICS

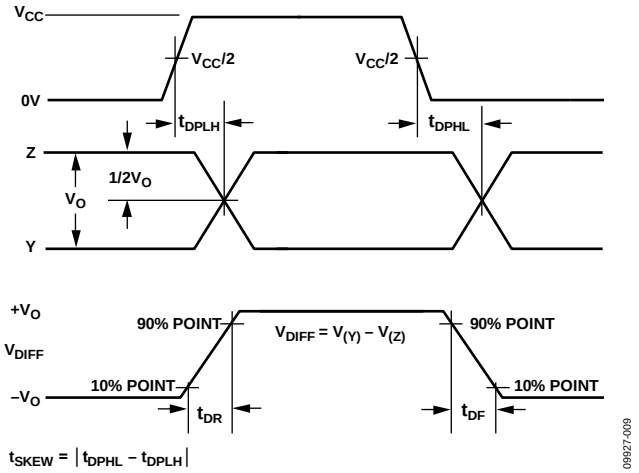


Figure 35. Driver Propagation Delay, Rise/Fall Timing

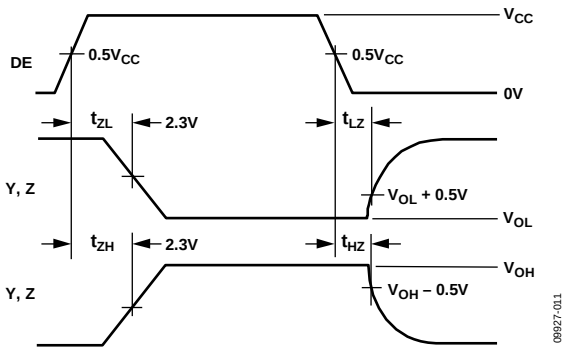


Figure 37. Driver Enable/Disable Timing

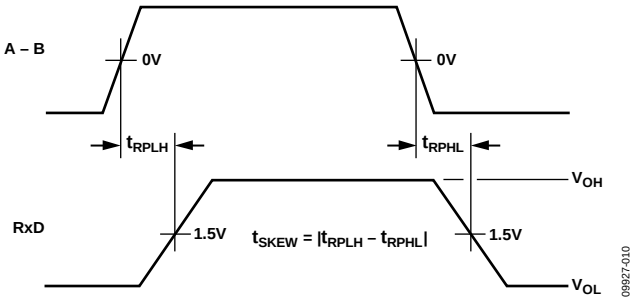


Figure 36. Receiver Propagation Delay

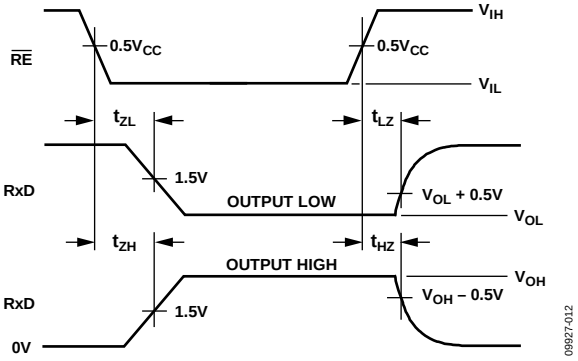


Figure 38. Receiver Enable/Disable Timing

CIRCUIT DESCRIPTION

SIGNAL ISOLATION

The ADM2682E/ADM2687E signal isolation of 5 kV rms is implemented on the logic side of the interface. The part achieves signal isolation by having a digital isolation section and a transceiver section (see Figure 1). Data applied to the TxD and DE pins and referenced to logic ground (GND_1) are coupled across an isolation barrier to appear at the transceiver section referenced to isolated ground (GND_2). Similarly, the single-ended receiver output signal, referenced to isolated ground in the transceiver section, is coupled across the isolation barrier to appear at the RxD pin referenced to logic ground.

POWER ISOLATION

The ADM2682E/ADM2687E power isolation of 5 kV rms is implemented using an *iso*Power integrated isolated dc-to-dc converter. The dc-to-dc converter section of the ADM2682E/ADM2687E works on principles that are common to most modern power supplies. It is a secondary side controller architecture with isolated pulse-width modulation (PWM) feedback. V_{CC} power is supplied to an oscillating circuit that switches current into a chip-scale air core transformer. Power transferred to the secondary side is rectified and regulated to 3.3 V. The secondary (V_{ISO}) side controller regulates the output by creating a PWM control signal that is sent to the primary (V_{CC}) side by a dedicated *i*Coupler (5 kV rms signal isolated) data channel. The PWM modulates the oscillator circuit to control the power being sent to the secondary side. Feedback allows for significantly higher power and efficiency.

TRUTH TABLES

The truth tables in this section use the abbreviations found in Table 11.

Table 11. Truth Table Abbreviations

Letter	Description
H	High level
L	Low level
X	Don't care
I	Indeterminate
Z	High impedance (off)
NC	Disconnected

Table 12. Transmitting (see Table 11 for Abbreviations)

Inputs		Outputs	
DE	**TxD**	**Y**	**Z**
H	H	H	L
H	L	L	H
L	X	Z	Z
X	X	Z	Z

Table 13. Receiving (see Table 11 for Abbreviations)

Inputs		Output
A – B	**$\overline{RE}$**	**RxD**
≥ −0.03 V	L or NC	H
≤ −0.2 V	L or NC	L
−0.2 V < A – B < −0.03 V	L or NC	I
Inputs open	L or NC	H
X	H	Z

THERMAL SHUTDOWN

The ADM2682E/ADM2687E contain thermal shutdown circuitry that protects the parts from excessive power dissipation during fault conditions. Shorting the driver outputs to a low impedance source can result in high driver currents. The thermal sensing circuitry detects the increase in die temperature under this condition and disables the driver outputs. This circuitry is designed to disable the driver outputs when a die temperature of 150°C is reached. As the device cools, the drivers are reenabled at a temperature of 140°C.

OPEN- AND SHORT-CIRCUIT, FAIL-SAFE RECEIVER INPUTS

The receiver inputs have open- and short-circuit, fail-safe features that ensure that the receiver output is high when the inputs are open or shorted. During line-idle conditions, when no driver on the bus is enabled, the voltage across a terminating resistance at the receiver input decays to 0 V. With traditional transceivers, receiver input thresholds specified between −200 mV and +200 mV mean that external bias resistors are required on the A and B pins to ensure that the receiver outputs are in a known state. The short-circuit, fail-safe receiver input feature eliminates the need for bias resistors by specifying the receiver input threshold between −30 mV and −200 mV. The guaranteed negative threshold means that when the voltage between A and B decays to 0 V, the receiver output is guaranteed to be high.

DC CORRECTNESS AND MAGNETIC FIELD IMMUNITY

The digital signals transmit across the isolation barrier using *i*Coupler technology. This technique uses chip-scale transformer windings to couple the digital signals magnetically from one side of the barrier to the other. Digital inputs are encoded into waveforms that are capable of exciting the primary transformer winding. At the secondary winding, the induced waveforms are decoded into the binary value that was originally transmitted.

Positive and negative logic transitions at the isolator input cause narrow (~1 ns) pulses to be sent to the decoder via the transformer. The decoder is bistable and is, therefore, either set or reset by the pulses, indicating input logic transitions. In the absence of logic transitions at the input for more than 1 µs, periodic sets of refresh pulses indicative of the correct input state are sent to ensure dc correctness at the output. If the decoder receives no internal pulses of more than approximately 5 µs, the input side

is assumed to be unpowered or nonfunctional, in which case, the isolator output is forced to a default state by the watchdog timer circuit.

This situation should occur in the ADM2682E/ADM2687E devices only during power-up and power-down operations. The limitation on the ADM2682E/ADM2687E magnetic field immunity is set by the condition in which induced voltage in the transformer receiving coil is sufficiently large to either falsely set or reset the decoder. The following analysis defines the conditions under which this can occur.

The 3.3 V operating condition of the ADM2682E/ADM2687E is examined because it represents the most susceptible mode of operation. The pulses at the transformer output have an amplitude of >1.0 V. The decoder has a sensing threshold of about 0.5 V, thus establishing a 0.5 V margin in which induced voltages can be tolerated. The voltage induced across the receiving coil is given by

$$V = (-d\beta/dt)\Sigma\pi r_n^2; n = 1, 2, \ldots, N$$

where:
β is magnetic flux density (gauss).
N is the number of turns in the receiving coil.
r_n is the radius of the nth turn in the receiving coil (cm).

Given the geometry of the receiving coil in the ADM2682E/ADM2687E and an imposed requirement that the induced voltage be, at most, 50% of the 0.5 V margin at the decoder, a maximum allowable magnetic field is calculated as shown in Figure 39.

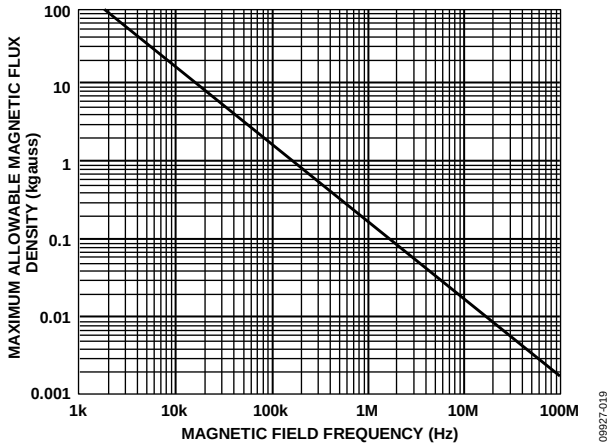


Figure 39. Maximum Allowable External Magnetic Flux Density

For example, at a magnetic field frequency of 1 MHz, the maximum allowable magnetic field of 0.2 kgauss induces a voltage of 0.25 V at the receiving coil. This is about 50% of the sensing threshold and does not cause a faulty output transition. Similarly, if such an event occurs during a transmitted pulse (and is of the worst-case polarity), it reduces the received pulse from >1.0 V to 0.75 V, which is still well above the 0.5 V sensing threshold of the decoder.

The preceding magnetic flux density values correspond to specific current magnitudes at given distances from the ADM2682E/ADM2687E transformers. Figure 40 expresses these allowable current magnitudes as a function of frequency for selected distances. As shown in Figure 40, the ADM2682E/ADM2687E are extremely immune and can be affected only by extremely large currents operated at high frequency very close to the component. For the 1 MHz example, a 0.5 kA current must be placed 5 mm away from the ADM2682E/ADM2687E to affect component operation.

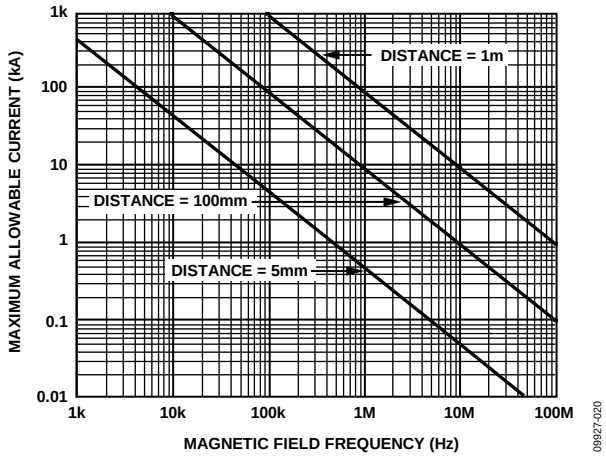


Figure 40. Maximum Allowable Current for Various Current-to-ADM2682E/ADM2687E Spacings

Note that in combinations of strong magnetic field and high frequency, any loops formed by PCB traces can induce error voltages sufficiently large to trigger the thresholds of succeeding circuitry. Take care in the layout of such traces to avoid this possibility.

APPLICATIONS INFORMATION

PCB LAYOUT

The ADM2682E/ADM2687E isolated RS-422/RS-485 transceiver contains an *iso*Power integrated dc-to-dc converter, requiring no external interface circuitry for the logic interfaces. Power supply bypassing is required at the input and output supply pins (see Figure 41). The power supply section of the ADM2682E/ADM2687E uses an 180 MHz oscillator frequency to pass power efficiently through its chip-scale transformers. In addition, the normal operation of the data section of the *i*Coupler introduces switching transients on the power supply pins.

Bypass capacitors are required for several operating frequencies. Noise suppression requires a low inductance, high frequency capacitor, whereas ripple suppression and proper regulation require a large value capacitor. These capacitors are connected between Pin 1 (GND_1) and Pin 2 (V_{CC}) and Pin 7 (V_{CC}) and Pin 8 (GND_1) for V_{CC}. The V_{ISOIN} and V_{ISOOUT} capacitors are connected between Pin 9 (GND_2) and Pin 10 (V_{ISOOUT}) and Pin 15 (V_{ISOIN}) and Pin 16 (GND_2). To suppress noise and reduce ripple, a parallel combination of at least two capacitors is required with the smaller of the two capacitors located closest to the device. The recommended capacitor values are 0.1 µF and 10 µF for V_{ISOOUT} at Pin 9 and Pin 10 and V_{CC} at Pin 7 and Pin 8. Capacitor values of 0.01 µF and 0.1 µF are recommended for V_{ISOIN} at Pin 15 and Pin 16 and V_{CC} at Pin 1 and Pin 2. The recommended best practice is to use a very low inductance ceramic capacitor, or its equivalent, for the smaller value capacitors. The total lead length between both ends of the capacitor and the input power supply pin should not exceed 10 mm.

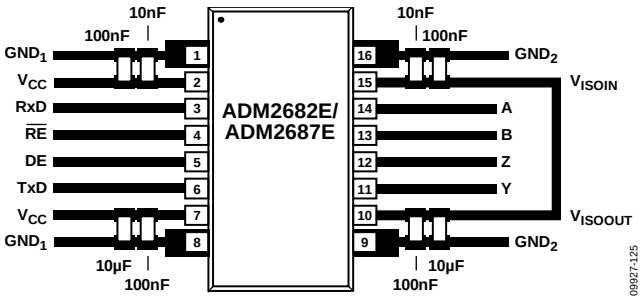


Figure 41. Recommended PCB Layout

In applications involving high common-mode transients, ensure that board coupling across the isolation barrier is minimized. Furthermore, design the board layout such that any coupling that does occur equally affects all pins on a given component side. Failure to ensure this can cause voltage differentials between pins exceeding the absolute maximum ratings for the device, thereby leading to latch-up and/or permanent damage.

The ADM2682E/ADM2687E dissipate approximately 675 mW of power when fully loaded. Because it is not possible to apply a heat sink to an isolation device, the devices primarily depend on heat dissipation into the PCB through the GND pins. If the devices are used at high ambient temperatures, provide a thermal path from the GND pins to the PCB ground plane. The board layout in Figure 41 shows enlarged pads for Pin 1, Pin 8, Pin 9, and Pin 16. Implement multiple vias from the pad to the ground plane to reduce the temperature inside the chip significantly. The dimensions of the expanded pads are at the discretion of the designer and dependent on the available board space.

EMI CONSIDERATIONS

The dc-to-dc converter section of the ADM2682E/ADM2687E components must, of necessity, operate at very high frequency to allow efficient power transfer through the small transformers. This creates high frequency currents that can propagate in circuit board ground and power planes, causing edge and dipole radiation. Grounded enclosures are recommended for applications that use these devices. If grounded enclosures are not possible, good RF design practices should be followed in the layout of the PCB. See the AN-0971 Application Note, *Recommendations for Control of Radiated Emissions with isoPower Devices*, for more information.

INSULATION LIFETIME

All insulation structures eventually break down when subjected to voltage stress over a sufficiently long period. The rate of insulation degradation is dependent on the characteristics of the voltage waveform applied across the insulation. Analog Devices conducts an extensive set of evaluations to determine the lifetime of the insulation structure within the ADM2682E/ADM2687E.

Accelerated life testing is performed using voltage levels higher than the rated continuous working voltage. Acceleration factors for several operating conditions are determined, allowing calculation of the time to failure at the working voltage of interest. The values shown in Table 9 summarize the peak voltages for 50 years of service life in several operating conditions. In many cases, the working voltage approved by agency testing is higher than the 50-year service life voltage. Operation at working voltages higher than the service life voltage listed leads to premature insulation failure.

The insulation lifetime of the ADM2682E/ADM2687E depends on the voltage waveform type imposed across the isolation barrier. The *i*Coupler insulation structure degrades at different rates, depending on whether the waveform is bipolar ac, unipolar ac, or dc. Figure 42, Figure 43, and Figure 44 illustrate these different isolation voltage waveforms.

Bipolar ac voltage is the most stringent environment. A 50-year operating lifetime under the bipolar ac condition determines the Analog Devices recommended maximum working voltage.

In the case of unipolar ac or dc voltage, the stress on the insulation is significantly lower. This allows operation at higher working voltages while still achieving a 50-year service life. The working voltages listed in Table 9 can be applied while maintaining the 50-year minimum lifetime, provided the voltage conforms to either the unipolar ac or dc voltage cases. Any cross-insulation voltage waveform that does not conform to Figure 43 or Figure 44 should be treated as a bipolar ac waveform, and its peak voltage should be limited to the 50-year lifetime voltage value listed in Table 9.

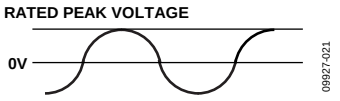


Figure 42. Bipolar AC Waveform

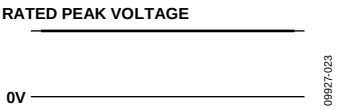
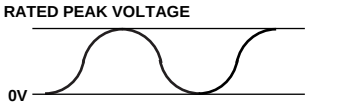


Figure 43. DC Waveform



NOTES
1. THE VOLTAGE IS SHOWN AS SINUSODIAL FOR ILLUSTRATION PURPOSES ONLY. IT IS MEANT TO REPRESENT ANY VOLTAGE WAVEFORM VARYING BETWEEN 0 AND SOME LIMITING VALUE. THE LIMITING VALUE CAN BE POSITIVE OR NEGATIVE, BUT THE VOLTAGE CANNOT CROSS 0V.

09927-022

Figure 44. Unipolar AC Waveform

ISOLATED SUPPLY CONSIDERATIONS

The typical output voltage of the integrated *iso*Power dc-to-dc isolated supply is 3.3 V. The isolated supply in the ADM2682E/ADM2687E is typically capable of supplying a current of 55 mA when the junction temperature of the device is kept below 130°C. This includes the current required by the internal RS-485 circuitry, and typically, no additional current is available on V_{ISOOUT} for external applications.

TYPICAL APPLICATIONS

An example application of the ADM2682E/ADM2687E for a full-duplex RS-485 node is shown in the circuit diagram of Figure 45. Refer to the PCB Layout section for the recommended placement of the capacitors shown in this circuit diagram. Placement of the R_T termination resistors depends on the location of the node and the network configuration. Refer to AN-960 Application Note, *RS-485/RS-422 Circuit Implementation Guide*, for guidance on termination.

Figure 46 and Figure 47 show typical applications of the ADM2682E/ADM2687E in half duplex and full duplex RS-485 network configurations. Up to 256 transceivers can be connected to the RS-485 bus. To minimize reflections, terminate the line at the receiving end in its characteristic impedance and keep stub lengths off the main line as short as possible. For half-duplex operation, this means that both ends of the line must be terminated because either end can be the receiving end.

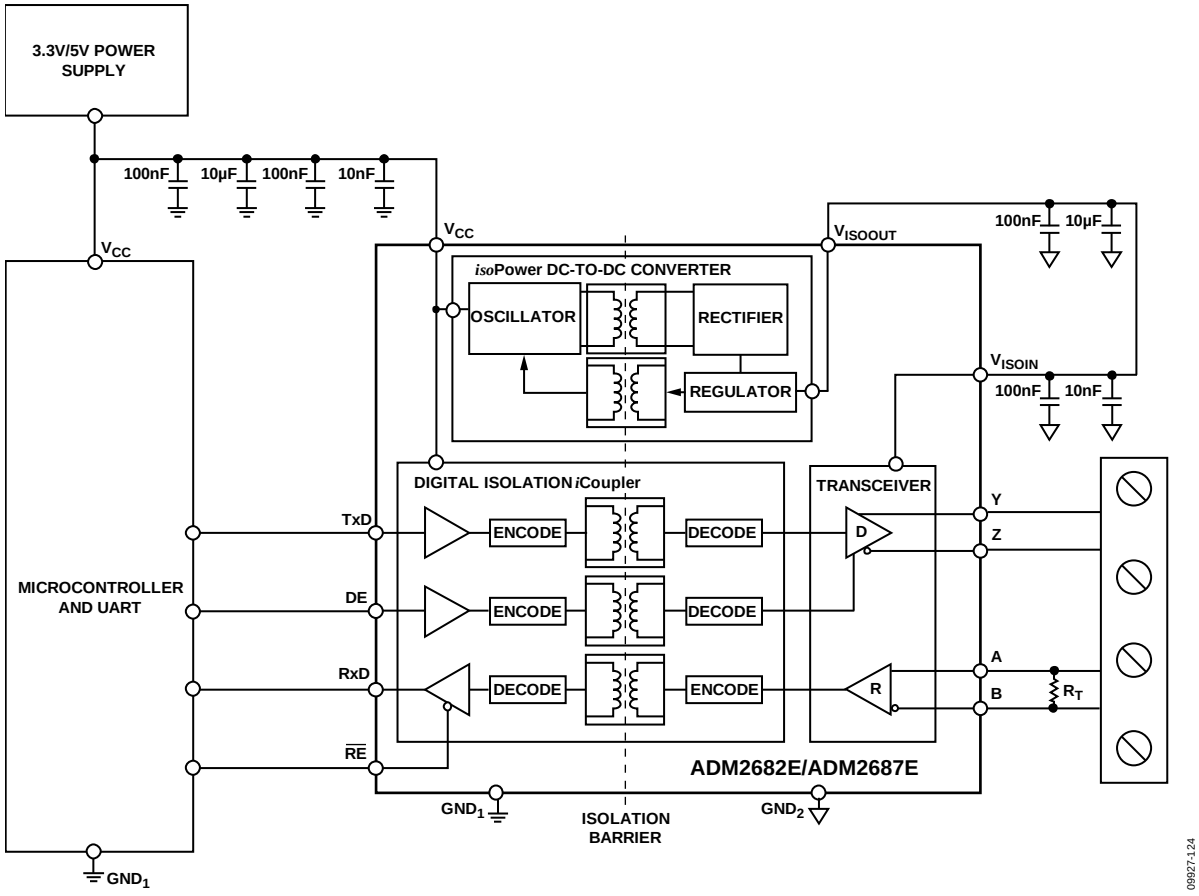


Figure 45. Example Circuit Diagram Using the ADM2682E/ADM2687E

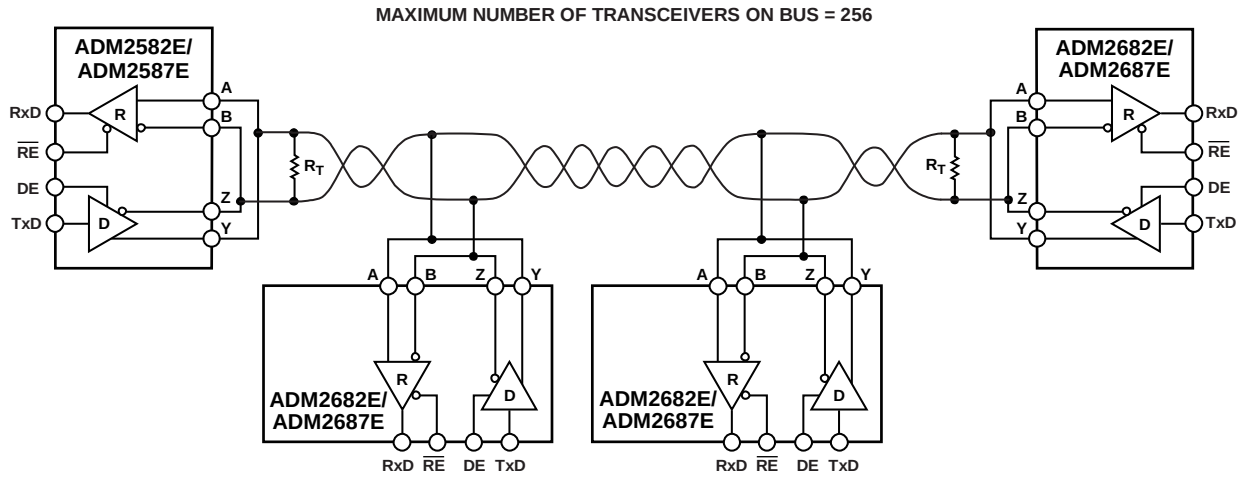


Figure 46. ADM2682E/ADM2687E Typical Half Duplex RS-485 Network

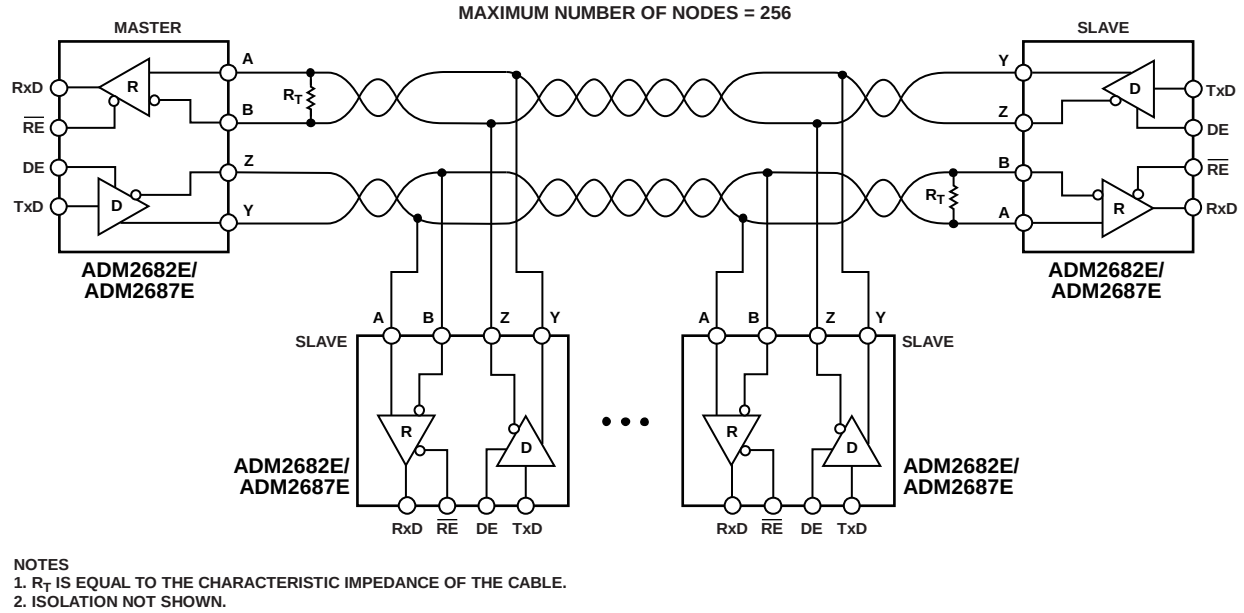
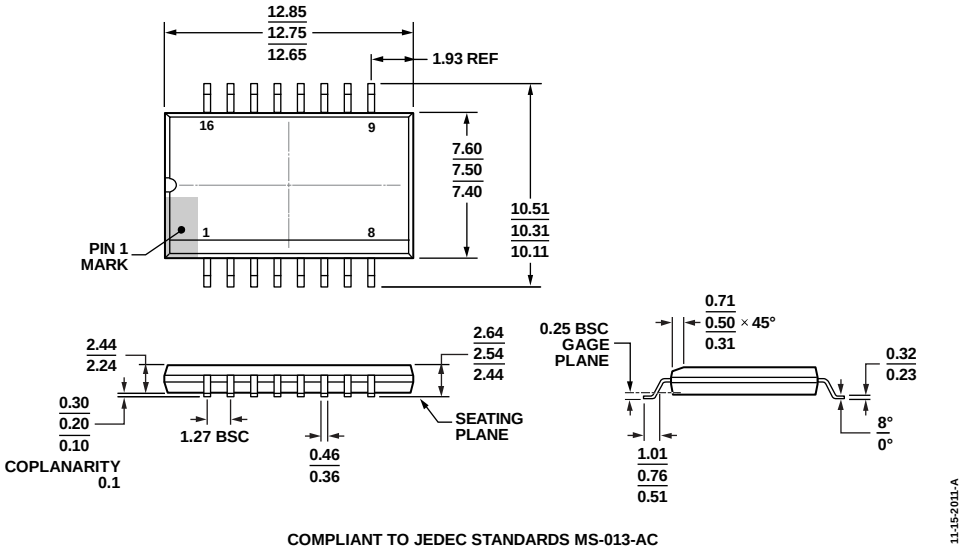


Figure 47. ADM2682E/ADM2687E Typical Full Duplex RS-485 Network

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-013-AC

Figure 48. 16-Lead Standard Small Outline Package with Increased Creepage [SOIC_IC]
Wide Body,
(RI-16-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Data Rate (Mbps)	Temperature Range	Package Description	Package Option
ADM2682EBRIZ	16	−40°C to +85°C	16-Lead SOIC_IC	RI-16-2
ADM2682EBRIZ-RL7	16	−40°C to +85°C	16-Lead SOIC_IC	RI-16-2
ADM2687EBRIZ	0.5	−40°C to +85°C	16-Lead SOIC_IC	RI-16-2
ADM2687EBRIZ-RL7	0.5	−40°C to +85°C	16-Lead SOIC_IC	RI-16-2
EVAL-ADM2682EEBZ			ADM2682E Evaluation Board	
EVAL-ADM2687EEBZ			ADM2687E Evaluation Board	

[1] Z = RoHS Compliant Part.

NOTES

NOTES