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## REVISION HISTORY

### 5/14—Rev. A to Rev. B

Removed ADM1088.....	Throughout
Changes to Capacitor-Adjustable Delay Circuit.....	9
Removed Figure 26; Renumbered Sequentially.....	12
Changes to Ordering Guide .....	15

### 4/06—Rev. 0 to Rev. A

Added Lead-Free Models .....	Universal
Update Outline Dimensions .....	15
Changes to Ordering Guide .....	15

### 7/04—Revision 0: Initial Version

## SPECIFICATIONS

$V_{CC}$  = full operating range,  $T_A$  =  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ , unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY					
$V_{CC}$ Operating Voltage Range	2.25		3.6	V	
$V_{IN}$ Operating Voltage Range	0		22	V	
Supply Current		10	15	$\mu\text{A}$	
$V_{IN}$ Rising Threshold, $V_{TH\_RISING}$	0.56	0.6	0.64	V	$V_{CC} = 3.3\text{ V}$
$V_{IN}$ Falling Threshold, $V_{TH\_FALLING}$	0.545	0.585	0.625	V	$V_{CC} = 3.3\text{ V}$
$V_{IN}$ Hysteresis		15		mV	
$V_{IN}$ to ENOUT/ $\overline{\text{ENOUT}}$ Delay					
$V_{IN}$ Rising		35		$\mu\text{s}$	CEXT floating, $C = 20\text{ pF}$
		2		ms	CEXT = 470 pF
$V_{IN}$ Falling		20		$\mu\text{s}$	$V_{IN} = V_{TH\_FALLING}$ to $(V_{TH\_FALLING} - 100\text{ mV})$
$V_{IN}$ Leakage Current		170		$\mu\text{A}$	$V_{IN} = 22\text{ V}$
CEXT Charge Current	125	250	375	nA	
Threshold Temperature Coefficient		30		ppm/ $^{\circ}\text{C}$	
ENIN/ $\overline{\text{ENIN}}$ to ENOUT/ $\overline{\text{ENOUT}}$ Propagation Delay		0.5		$\mu\text{s}$	$V_{IN} > V_{TH\_RISING}$
ENIN/ $\overline{\text{ENIN}}$ Voltage Low			$0.3 V_{CC} - 0.2$	V	
ENIN/ $\overline{\text{ENIN}}$ Voltage High	$0.3 V_{CC} + 0.2$			V	
ENIN/ $\overline{\text{ENIN}}$ Leakage Current		170		$\mu\text{A}$	ENIN/ $\overline{\text{ENIN}}$ = 22 V
ENOUT/ $\overline{\text{ENOUT}}$ Voltage Low			0.4	V	$V_{IN} < V_{TH\_FALLING}(\overline{\text{ENOUT}})$ , $V_{IN} > V_{TH\_RISING}(\overline{\text{ENOUT}})$ , $I_{SINK} = 1.2\text{ mA}$
ENOUT/ $\overline{\text{ENOUT}}$ Voltage High	$0.8 V_{CC}$			V	$V_{IN} > V_{TH\_RISING}(\overline{\text{ENOUT}})$ , $V_{IN} < V_{TH\_FALLING}(\overline{\text{ENOUT}})$ , $I_{SOURCE} = 500\text{ }\mu\text{A}$
ENOUT/ $\overline{\text{ENOUT}}$ Open-Drain Output Leakage Current (ADM1085/ADM1087)			0.4	$\mu\text{A}$	ENOUT/ $\overline{\text{ENOUT}}$ = 22 V

## ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ , unless otherwise noted.

**Table 3.**

Parameter	Rating
$V_{CC}$	–0.3 V to +6 V
$V_{IN}$	–0.3 V to +25 V
CEXT	–0.3 V to +6 V
ENIN, $\overline{\text{ENIN}}$	–0.3 V to +25 V
ENOUT, $\overline{\text{ENOUT}}$ (ADM1085, ADM1087)	–0.3 V to +25 V
ENOUT, $\overline{\text{ENOUT}}$ (ADM1086)	–0.3 V to +6 V
Operating Temperature Range	–40°C to +125°C
Storage Temperature Range	–65°C to +150°C
$\theta_{JA}$ Thermal Impedance, SC70	146°C/W
Lead Temperature	
Soldering (10 sec)	300°C
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

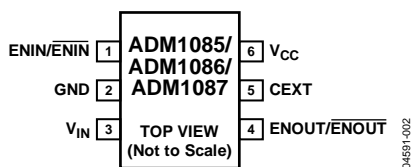


Figure 2. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	ENIN, $\overline{\text{ENIN}}$	Enable Input. Controls the status of the enable output. Active high for <a href="#">ADM1085/ADM1086</a> . Active low for <a href="#">ADM1087</a> .
2	GND	Ground.
3	V <sub>IN</sub>	Input for the Monitored Voltage Signal. Can be biased via a voltage divider resistor network to customize the effective input threshold. Can precisely monitor an analog power supply output signal and detect when it has powered up. The voltage applied at this pin is compared with a 0.6 V on-chip reference. With this reference, digital signals with various logic level thresholds can also be detected.
4	ENOUT, $\overline{\text{ENOUT}}$	Enable Output. Asserted when the voltage at V <sub>IN</sub> is above V <sub>TH_RISING</sub> and the time delay has elapsed, provided that the enable input is asserted. Active high for the <a href="#">ADM1085/ADM1086</a> . Active low for the <a href="#">ADM1087</a> .
5	CEXT	External Capacitor Pin. The capacitance on this pin determines the time delay on the enable output. The delay is seen only when the voltage at V <sub>IN</sub> rises past V <sub>TH_RISING</sub> , and not when it falls below V <sub>TH_FALLING</sub> .
6	V <sub>CC</sub>	Power Supply.

TYPICAL PERFORMANCE CHARACTERISTICS

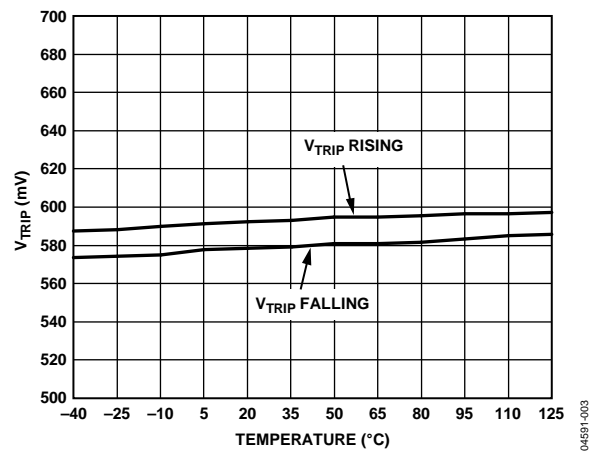


Figure 3.  $V_{IN}$  Threshold vs. Temperature

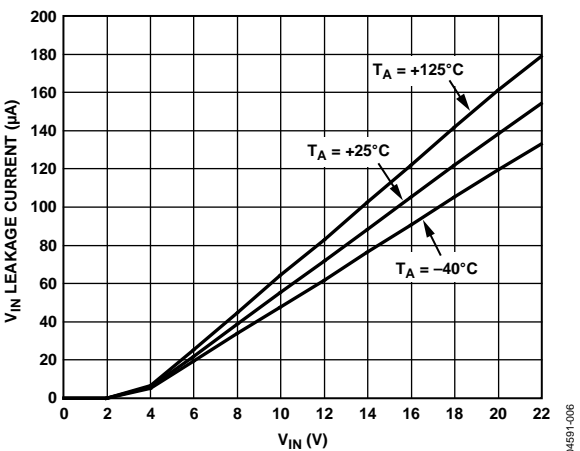


Figure 6.  $V_{IN}$  Leakage Current vs.  $V_{IN}$  Voltage

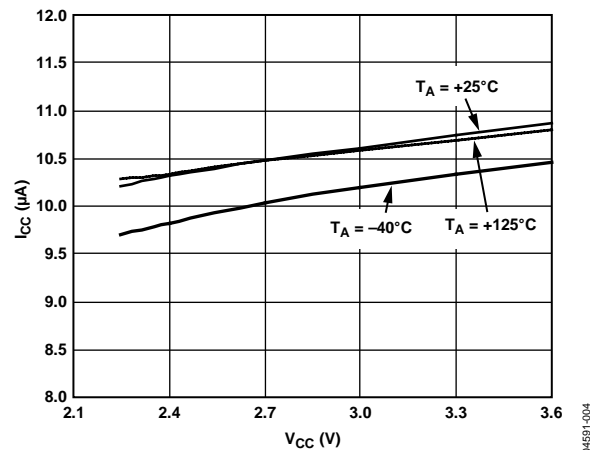


Figure 4. Supply Current vs. Supply Voltage

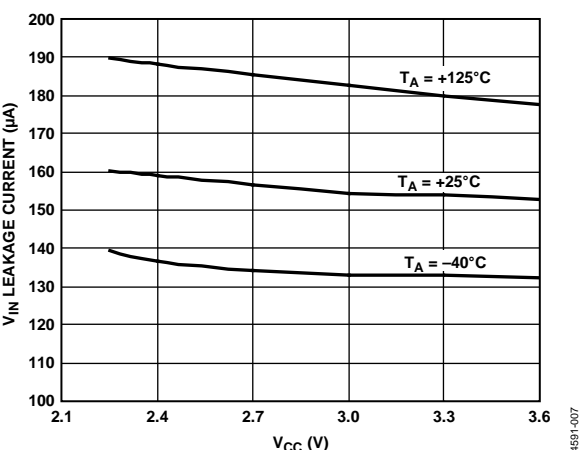


Figure 7.  $V_{IN}$  Leakage Current vs.  $V_{CC}$  Voltage

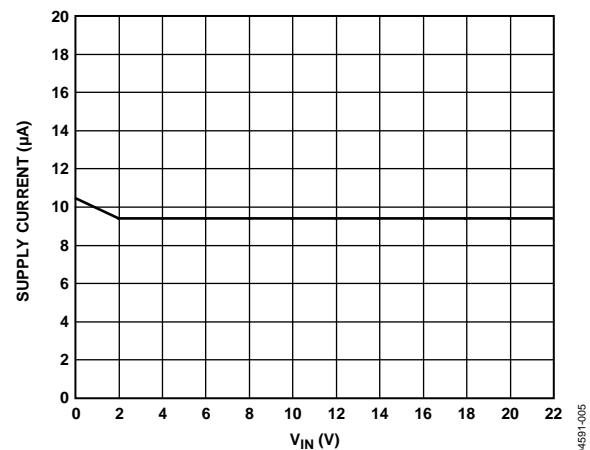


Figure 5. Supply Current vs.  $V_{IN}$  Voltage

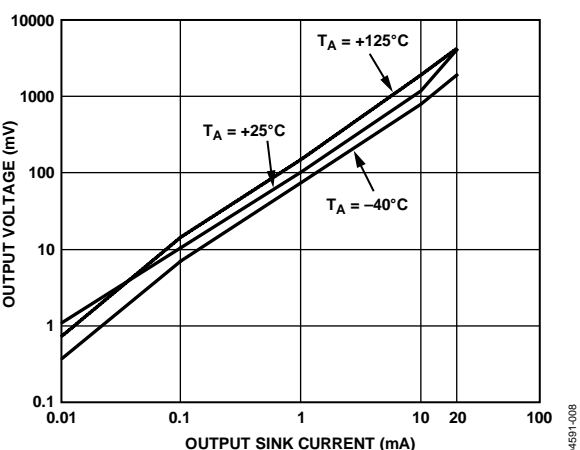


Figure 8. Output Voltage vs. Output Sink Current

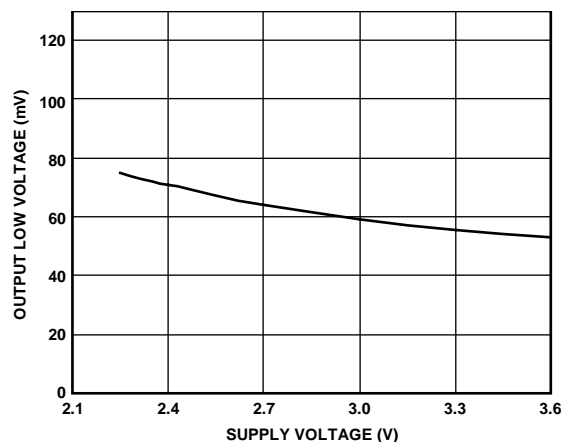


Figure 9. Output Low Voltage vs. Supply Voltage

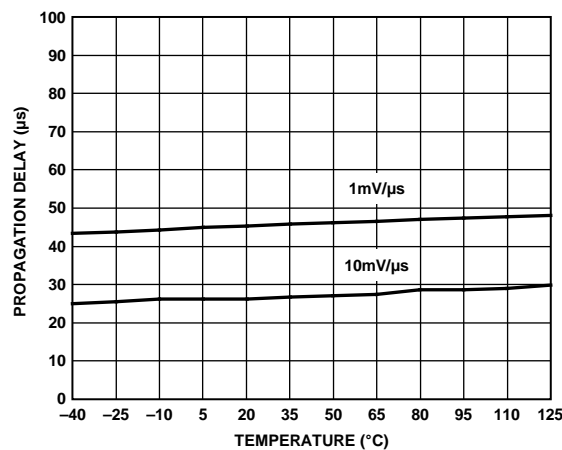
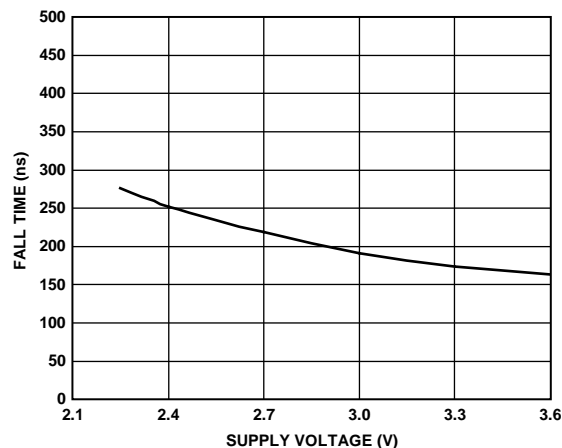
Figure 10. V<sub>CC</sub> Falling Propagation Delay vs. Temperature

Figure 11. Output Fall Time vs. Supply Voltage

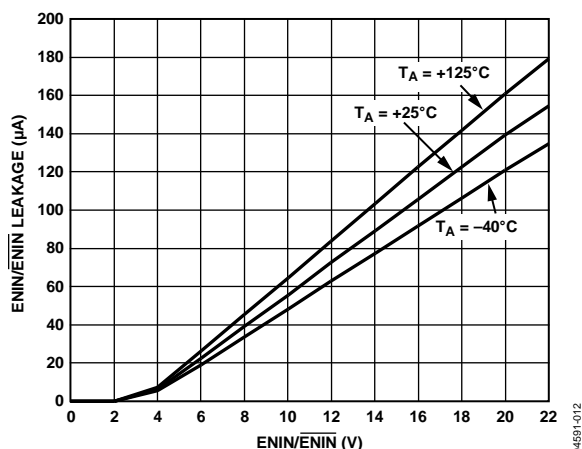


Figure 12. ENIN/ENIN Leakage Current vs. ENIN/ENIN Voltage

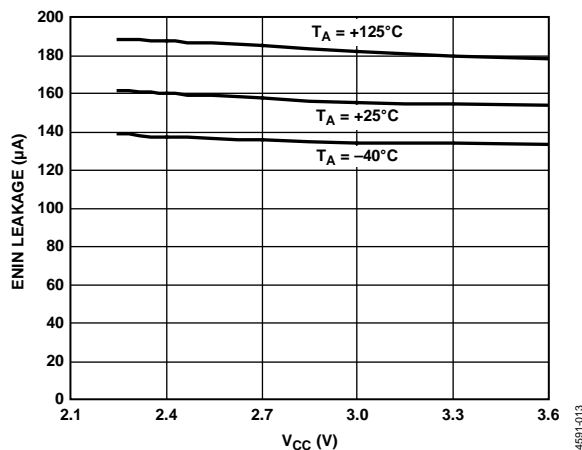
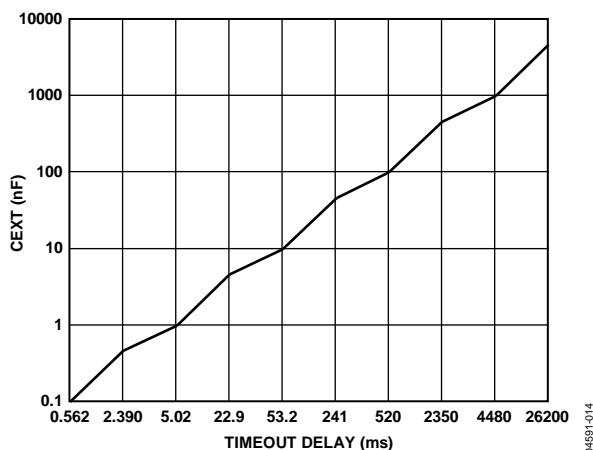
Figure 13. ENIN/ENIN Leakage Current vs. V<sub>CC</sub> Voltage

Figure 14. CEXT Capacitance vs. Timeout Delay

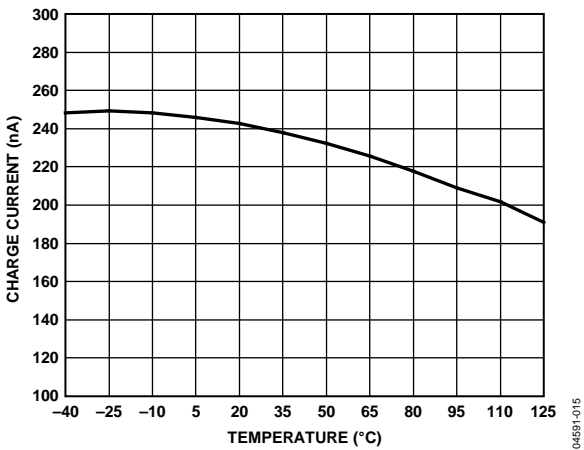


Figure 15. CEXT Charge Current vs. Temperature

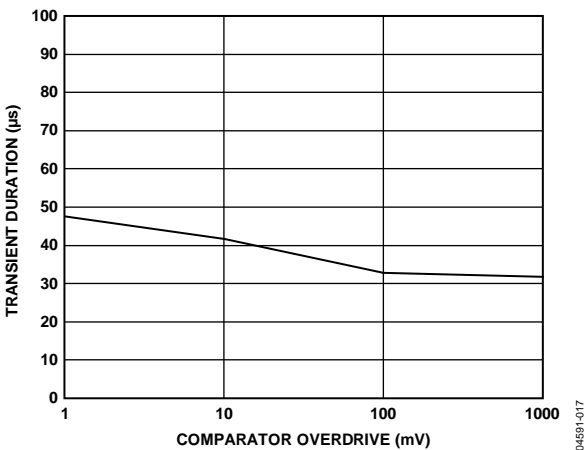


Figure 17. Maximum  $V_{IN}$  Transient Duration vs. Comparator Overdrive

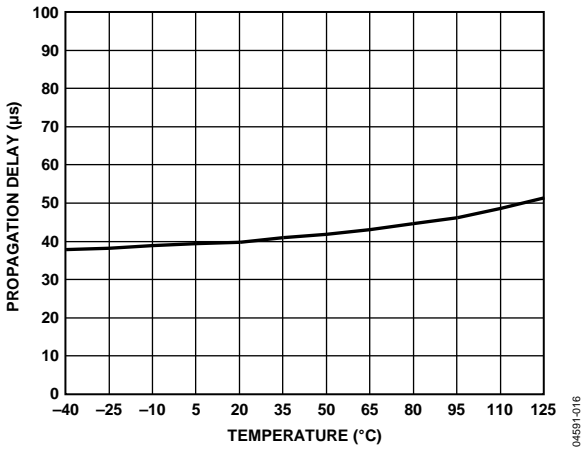


Figure 16.  $V_{IN}$  to  $ENOUT/\overline{ENOUT}$  Propagation Delay (CEXT Floating) vs. Temperature

## CIRCUIT INFORMATION

### TIMING CHARACTERISTICS AND TRUTH TABLES

The enable outputs of the ADM1085/ADM1086/ADM1087 are related to the  $V_{IN}$  and enable inputs by a simple AND function. The enable output is asserted only if the enable input is asserted and the voltage at  $V_{IN}$  is above  $V_{TH\_RISING}$ , with the time delay elapsed. Table 5 and Table 6 show the enable output logic states for different  $V_{IN}$ /enable input combinations when the capacitor delay has elapsed. The timing diagrams in Figure 18 and Figure 19 give a graphical representation of how the ADM1085/ADM1086/ADM1087 enable outputs respond to  $V_{IN}$  and enable input signals.

Table 5. ADM1085/ADM1086 Truth Table

$V_{IN}$	ENIN	ENOUT
$<V_{TH\_FALLING}$	0	0
$<V_{TH\_FALLING}$	1	0
$>V_{TH\_RISING}$	0	0
$>V_{TH\_RISING}$	1	1

Table 6. ADM1087 Truth Table

$V_{IN}$	ENIN	ENOUT
$<V_{TH\_FALLING}$	1	1
$<V_{TH\_FALLING}$	0	1
$>V_{TH\_RISING}$	1	1
$>V_{TH\_RISING}$	0	0

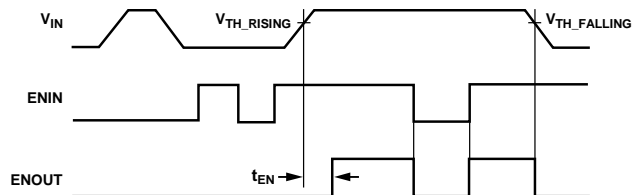


Figure 18. ADM1085/ADM1086 Timing Diagram

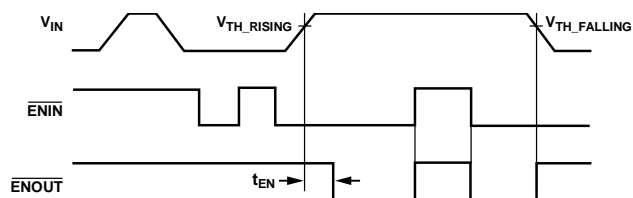


Figure 19. ADM1087 Timing Diagram

When  $V_{IN}$  reaches the upper threshold voltage ( $V_{TH\_RISING}$ ), an internal circuit generates a delay ( $t_{EN}$ ) before the enable output is asserted. If  $V_{IN}$  drops below the lower threshold voltage ( $V_{TH\_FALLING}$ ), the enable output is deasserted immediately.

Similarly, if the enable input is disabled while  $V_{IN}$  is above the threshold, the enable output deasserts immediately. Unlike  $V_{IN}$ , a low-to-high transition on ENIN (or high-to-low on  $\overline{ENIN}$ ) does not yield a time delay on ENOUT ( $\overline{ENOUT}$ ).

### CAPACITOR-ADJUSTABLE DELAY CIRCUIT

Figure 20 shows the internal circuitry used to generate the time delay on the enable output. A 250 nA current source charges a small internal parasitic capacitance ( $C_{INT}$ ). When the capacitor voltage reaches 1.2 V, the enable output is asserted. The time taken for the capacitor to reach 1.2 V, in addition to the propagation delay of the comparator, constitutes the enable timeout, which is typically 35  $\mu$ s.

To minimize the delay between  $V_{IN}$  falling below  $V_{TH\_FALLING}$  and the enable output deasserting, an NMOS transistor is connected in parallel with  $C_{INT}$ . The output of the voltage detector is connected to the gate of this transistor so that, when  $V_{IN}$  falls below  $V_{TH\_FALLING}$ , the transistor switches on and  $C_{INT}$  discharges quickly.

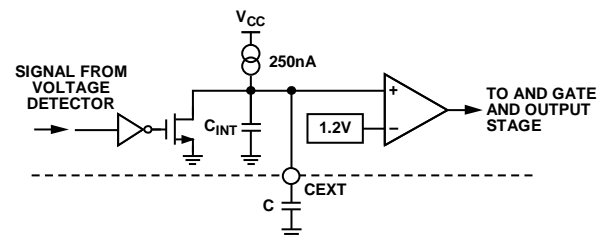


Figure 20. Capacitor-Adjustable Delay Circuit

Connecting an external capacitor to the CEXT pin delays the rise time—and therefore the enable timeout—further. The relationship between the value of the external capacitor and the resulting timeout is characterized by the following equation:

$$t_{EN} = (C \times 4.8 \times 10^6) + 35 \mu s$$

where:

$C$  is expressed in farads (F), and  
 $t_{EN}$  is expressed in seconds (sec).



**OPEN-DRAIN AND PUSH-PULL OUTPUTS**

The [ADM1085](#) and [ADM1087](#) have open-drain output stages that require an external pull-up resistor to provide a logic high voltage level. The geometry of the NMOS transistor enables the output to be pulled up to voltage levels as high as 22 V.

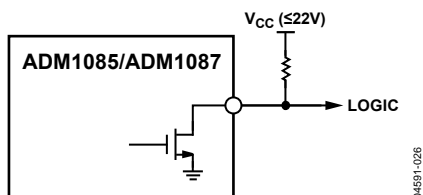


Figure 21. Open-Drain Output Stage

The [ADM1086](#) has a push-pull (CMOS) output stage that requires no external components to drive other logic circuits. An internal PMOS pull-up transistor provides the logic high voltage level.

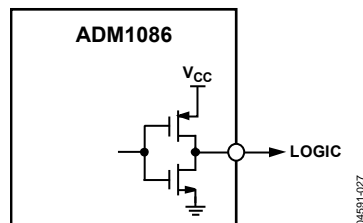


Figure 22. Push-Pull Output Stage



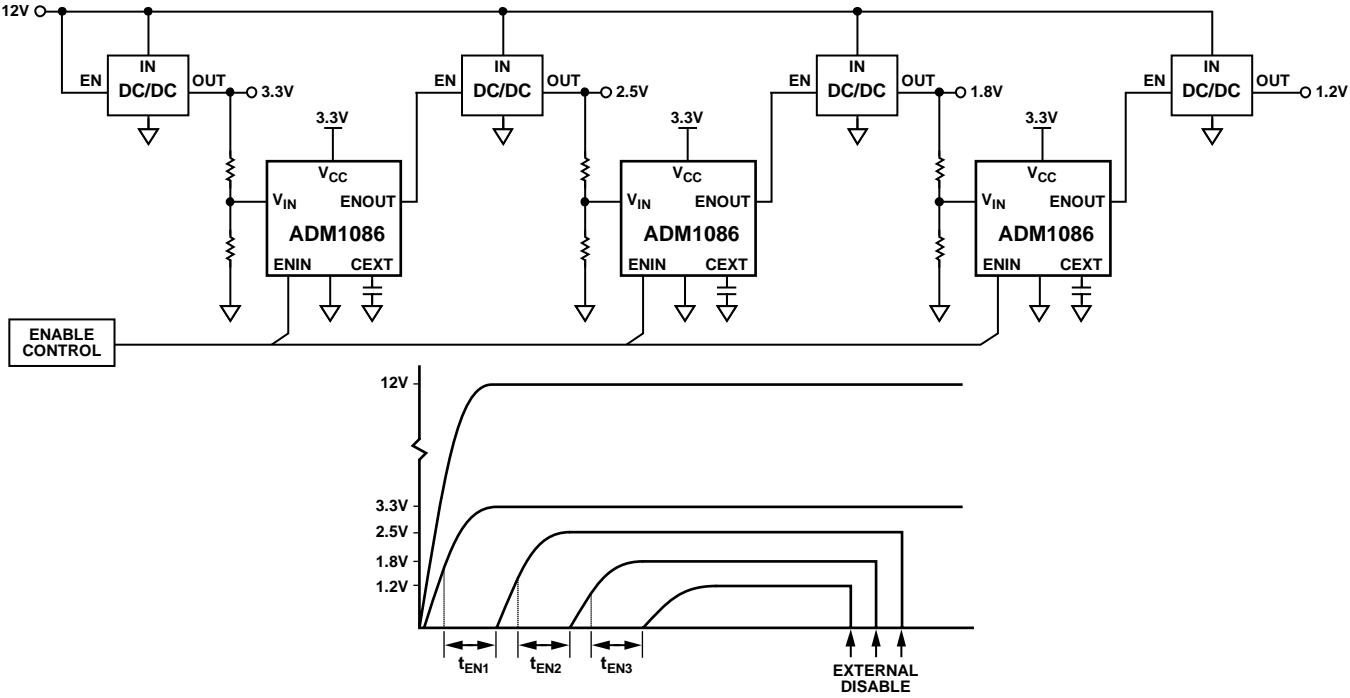


Figure 24. Typical ADM1086 Application Circuit

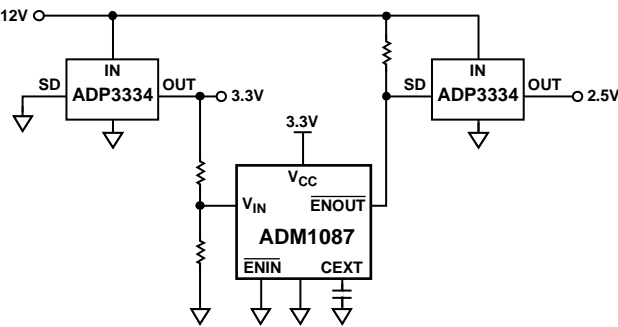


Figure 25. Typical ADM1087 Application Circuit Using ADP3334 Voltage Regulators

## DUAL LOFO SEQUENCING

A power sequencing solution for a portable device, such as a PDA, is shown in Figure 26. This solution requires that the microprocessor power supply turn on before the LCD display turns on, and that the LCD display power-down before the microprocessor powers down. In other words, the last power supply to turn on is the first one to turn off (LOFO).

An RC network connects the battery and the  $\overline{\text{SD}}$  input of the [ADP3333](#) voltage regulator. This causes power-up and power-down transients to appear at the  $\overline{\text{SD}}$  input when the battery is connected and disconnected. The 3.3 V microprocessor supply turns on quickly on power-up and turns off slowly on power-down. This is due to two factors: Capacitor C1 charges up to 9 V on power-up and charges down from 9 V on power-down, and the  $\overline{\text{SD}}$  pin has logic high and logic low input levels of 2 V and 0.4 V.

For the display power sequencing, the [ADM1085](#) is equipped with Capacitor C2 to create the delay between the microprocessor and display power turning on. When the system is powered down, the [ADM1085](#) turns off the display power immediately, while the 3.3 V regulator waits for C1 to discharge to 0.4 V before switching off.

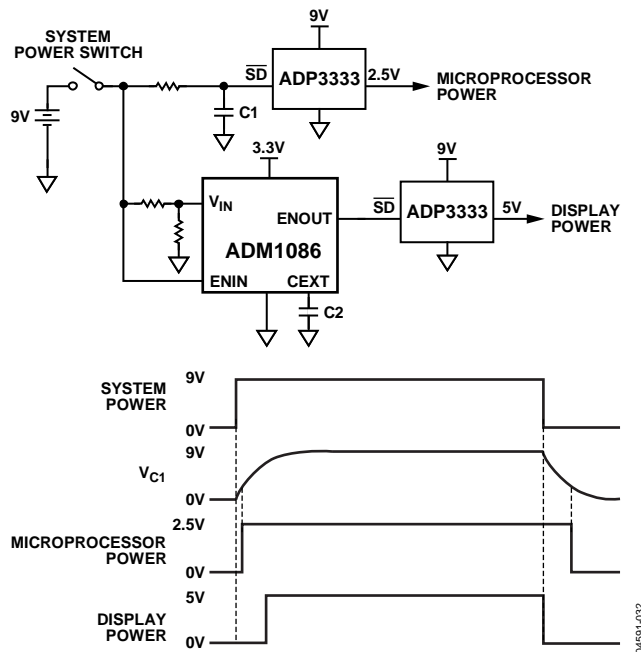


Figure 26. Dual LOFO Power-Supply Sequencing

## SIMULTANEOUS ENABLING

The enable output can drive multiple enable or shutdown regulator inputs simultaneously.

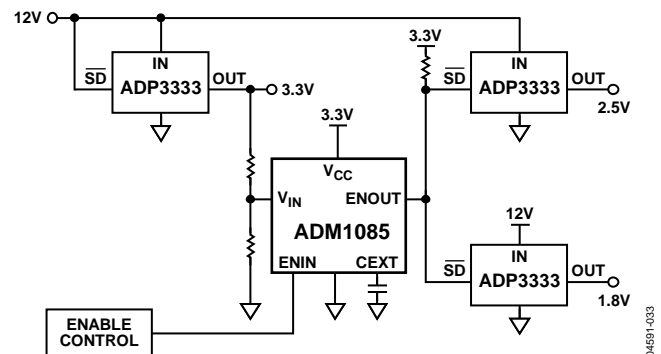


Figure 27. Enabling a Pair of Regulators from a Single [ADM1085](#)

## POWER GOOD SIGNAL DELAYS

Sometimes sequencing is performed by asserting power good signals when the voltage regulators are already on, rather than sequencing the power supplies directly. In these scenarios, a simple sequencer IC can provide variable delays so that enabling separate circuit blocks can be staggered in time.

For example, in a notebook PC application, a dedicated microcomputer asserts a power good signal for North Bridge™ and South Bridge™ ICs. The [ADM1086](#) delays the South Bridge signal, so that it is enabled after the North Bridge.

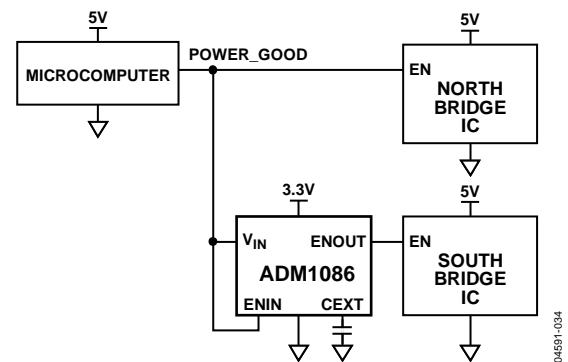


Figure 28. Power Good Delay

### QUAD-SUPPLY POWER GOOD INDICATOR

The enable output of the Simple Sequencers is equivalent to an AND function of  $V_{IN}$  and ENIN. ENOUT is high only when the voltage at  $V_{IN}$  is above the threshold and the enable input (ENIN) is high as well. Although ENIN is a digital input, it can tolerate voltages as high as 22 V and can detect if a supply is present. Therefore, a simple sequencer can monitor two supplies and assert what can be interpreted as a power good signal when both supplies are present. The outputs of two ADM1085s can be wire-AND'ed together to make a quad-supply power good indicator.

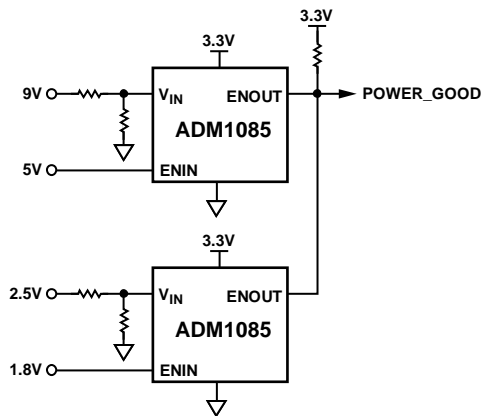


Figure 29. Quad-Supply Power Good Indicator

04591-035

### SEQUENCING WITH FET SWITCHES

The open-drain outputs of the ADM1085 and ADM1087 can drive external FET transistors that can switch on power supply rails. All that is needed is a pull-up resistor to a voltage source that is high enough to turn on the FET.

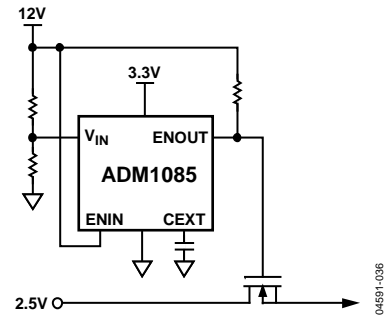


Figure 30. Sequencing with a FET Switch

04591-036

## OUTLINE DIMENSIONS

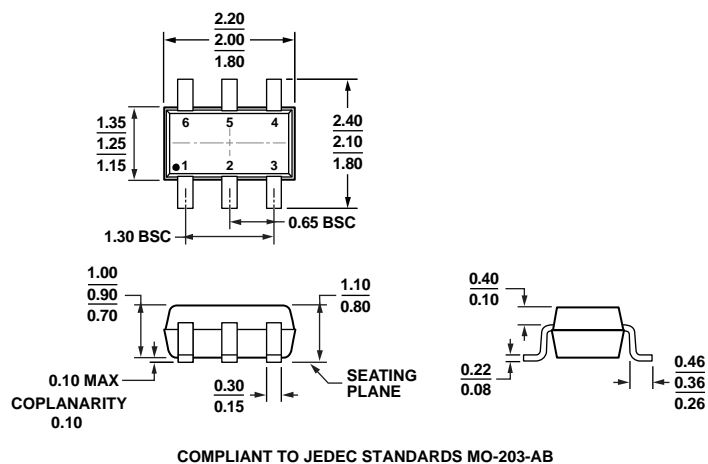


Figure 31. 6-Lead Thin Shrink Small Outline Transistor Package [SC70]  
(KS-6)  
Dimensions shown in millimeters

## ORDERING GUIDE

Model <sup>1</sup>	Temperature Range	Ordering Quantity	Package Description	Package Option	Branding
ADM1085AKSZ-REEL7	–40°C to +125°C	3k	6-Lead Thin Shrink Small Outline Transistor Package (SC70)	KS-6	M7R
ADM1086AKSZ-REEL7	–40°C to +125°C	3k	6-Lead Thin Shrink Small Outline Transistor Package (SC70)	KS-6	M8M
ADM1087AKSZ-REEL7	–40°C to +125°C	3k	6-Lead Thin Shrink Small Outline Transistor Package (SC70)	KS-6	M7S
EVAL-ADM1087EBZ			Evaluation Board for the <a href="#">ADM1087</a> device. This board can also be used to evaluate the other devices in the family. Sample can be ordered separately.		

<sup>1</sup> Z = RoHS Compliant Part.

## NOTES