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REVISION HISTORY

5/15—Rev. D to Rev. E

Deleted 0.1 Hz to 10 Hz Noise Section, Figure 45, and Figure 46; Renumbered Sequentially	14
Updated Outline Dimensions	17
Changes to Ordering Guide	17

5/12—Rev. C to Rev. D

Changes to Figure 2 Caption	1
Updated Outline Dimensions	17
Changes to Ordering Guide	17

2/10—Rev. B to Rev. C

Added ADA4898-2	Throughout
Changes to Features	1
Changes to Table 1	3
Changes to Table 2	4
Changes to Figure 38, Figure 40, Figure 41	14
Changes to Figure 46	15
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Changes to PCB Layout Section	17
Changes to Ordering Guide	20

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6/09—Rev. A to Rev. B

Changes to General Description Section	1
Changes to Specifications Section	3
Changes to Figure 29 and Figure 31	11
Added Figure 32	12
Added Figure 41	13
Changes to $\overline{\text{PD}}$ (Power-Down) Pin Section	14
Added Table 6	14
Changes to Figure 45	15

8/08—Rev. 0 to Rev. A

Changes to General Description Section	1
Changes to Table 5	6
Changes to Figure 17	9
Changes to Figure 28	10
Changes to Figure 29 and Figure 32	11
Added 0.1 Hz to 10 Hz Noise Section	14
Added Figure 42 and Figure 43; Renumbered Sequentially	14
Changes to Grounding Section	16
Updated Outline Dimensions	17

5/08—Revision 0: Initial Version

SPECIFICATIONS

±15 V SUPPLY

$T_A = 25^\circ\text{C}$, $G = +1$, $R_F = 0\ \Omega$, R_G open, $R_L = 1\ \text{k}\Omega$ to GND (for $G > 1$, $R_F = 100\ \Omega$), unless otherwise noted.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
–3 dB Bandwidth	$V_{OUT} = 100\ \text{mV p-p}$		65		MHz
	$V_{OUT} = 2\ \text{V p-p}$		14		MHz
Bandwidth for 0.1 dB Flatness	$G = +2$, $V_{OUT} = 2\ \text{V p-p}$		3.3		MHz
Slew Rate	$V_{OUT} = 5\ \text{V step}$		55		V/ μs
Settling Time to 0.1%	$V_{OUT} = 5\ \text{V step}$		85		ns
NOISE/DISTORTION PERFORMANCE					
Harmonic Distortion SFDR	$f = 100\ \text{kHz}$, $V_{OUT} = 2\ \text{V p-p}$		–116		dBc
	$f = 500\ \text{kHz}$, $V_{OUT} = 2\ \text{V p-p}$		–93		dBc
	$f = 1\ \text{MHz}$, $V_{OUT} = 2\ \text{V p-p}$		–79		dBc
Input Voltage Noise	$f = 1\ \text{kHz}$		0.9		nV/ $\sqrt{\text{Hz}}$
Input Current Noise	$f = 1\ \text{kHz}$		2.4		pA/ $\sqrt{\text{Hz}}$
DC PERFORMANCE					
Input Offset Voltage	$R_F = 1\ \text{k}\Omega$, see Figure 43		20	125	μV
Input Offset Voltage Drift	$R_F = 1\ \text{k}\Omega$, see Figure 43		1		$\mu\text{V}/^\circ\text{C}$
Input Bias Current	$R_F = 1\ \text{k}\Omega$, see Figure 43		–0.1	–0.4	μA
Input Bias Offset Current	$R_F = 1\ \text{k}\Omega$, see Figure 43		0.03	0.3	μA
Input Bias Current Drift	$R_F = 1\ \text{k}\Omega$, see Figure 43		2		nA/ $^\circ\text{C}$
Open-Loop Gain	$V_{OUT} = \pm 5\ \text{V}$	99	103		dB
INPUT CHARACTERISTICS					
Input Resistance	Differential mode		5		k Ω
	Common mode		30		M Ω
Input Capacitance	Differential mode		3.2		pF
	Common mode		2.5		pF
Input Common-Mode Voltage Range	See Figure 43		± 11		V
Common-Mode Rejection Ratio	$V_{CM} = \pm 2\ \text{V}$	–103	–126		dB
PD (POWER-DOWN) PIN (ADA4898-1)					
$\overline{\text{PD}}$ Input Voltages	Chip powered down		≤ -14		V
	Chip enabled		≥ -13		V
$\overline{\text{PD}}$ Turn On Time	$V_{OUT} = 100\ \text{mV p-p}$		100		ns
$\overline{\text{PD}}$ Turn Off Time	$V_{OUT} = 100\ \text{mV p-p}$		20		μs
Input Leakage Current	$\overline{\text{PD}} = +V_S$		0.1		μA
	$\overline{\text{PD}} = -V_S$		–0.2		μA
OUTPUT CHARACTERISTICS					
Output Voltage Swing	$R_L // (R_F + R_G) = 500\ \Omega$, see Figure 43	–11.0 to +11.8	–11.7 to +12.1		V
	$R_L // (R_F + R_G) = 1\ \text{k}\Omega$, see Figure 43	–12.5 to +12.5	–12.8 to +12.7		V
Linear Output Current	$f = 100\ \text{kHz}$, SFDR = –70 dBc, $R_L = 150\ \Omega$		40		mA
Short-Circuit Current	Sinking/sourcing		150		mA
Off Isolation	$f = 1\ \text{MHz}$, $\overline{\text{PD}} = -V_S$		80		dB
POWER SUPPLY					
Operating Range		± 4.5		± 16.5	V
Quiescent Current per Amplifier	$\overline{\text{PD}} = +V_S$		7.9	8.7	mA
	$\overline{\text{PD}} = -V_S$		0.1	0.3	mA
Positive Power Supply Rejection Ratio	$+V_S = 15\ \text{V}$ to $17\ \text{V}$, $-V_S = -15\ \text{V}$	–98	–107		dB
Negative Power Supply Rejection Ratio	$+V_S = 15\ \text{V}$, $-V_S = -15\ \text{V}$ to $-17\ \text{V}$	–100	–114		dB

±5 V SUPPLY

$T_A = 25^\circ\text{C}$, $G = +1$, $R_F = 0\ \Omega$, R_G open, $R_L = 1\ \text{k}\Omega$ to GND (for $G > 1$, $R_F = 100\ \Omega$), unless otherwise noted.

Table 2.

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
–3 dB Bandwidth	$V_{OUT} = 100\ \text{mV p-p}$		57		MHz
	$V_{OUT} = 2\ \text{V p-p}$		12		MHz
Bandwidth for 0.1 dB Flatness	$G = +2$, $V_{OUT} = 2\ \text{V p-p}$		3		MHz
Slew Rate	$V_{OUT} = 2\ \text{V step}$		50		V/ μs
Settling Time to 0.1%	$V_{OUT} = 2\ \text{V step}$		90		ns
NOISE/DISTORTION PERFORMANCE					
Harmonic Distortion SFDR	$f = 100\ \text{kHz}$, $V_{OUT} = 2\ \text{V p-p}$		–110		dBc
	$f = 500\ \text{kHz}$, $V_{OUT} = 2\ \text{V p-p}$		–95		dBc
	$f = 1\ \text{MHz}$, $V_{OUT} = 2\ \text{V p-p}$		–78		dBc
Input Voltage Noise	$f = 1\ \text{kHz}$		0.9		nV/ $\sqrt{\text{Hz}}$
Input Current Noise	$f = 1\ \text{kHz}$		2.4		pA/ $\sqrt{\text{Hz}}$
DC PERFORMANCE					
Input Offset Voltage	$R_F = 1\ \text{k}\Omega$, see Figure 43		30	160	μV
Input Offset Voltage Drift	$R_F = 1\ \text{k}\Omega$, see Figure 43		1		$\mu\text{V}/^\circ\text{C}$
Input Bias Current	$R_F = 1\ \text{k}\Omega$, see Figure 43		–0.1	–0.5	μA
Input Bias Offset Current	$R_F = 1\ \text{k}\Omega$, see Figure 43		0.05	0.3	μA
Input Bias Current Drift	$R_F = 1\ \text{k}\Omega$, see Figure 43		2		nA/ $^\circ\text{C}$
Open-Loop Gain	$V_{OUT} = \pm 1\ \text{V}$	87	94		dB
INPUT CHARACTERISTICS					
Input Resistance	Differential mode		5		k Ω
	Common mode		30		M Ω
Input Capacitance	Differential mode		3.2		pF
	Common mode		2.5		pF
Input Common-Mode Voltage Range	See Figure 43		–3 to +2.5		V
Common-Mode Rejection Ratio	$\Delta V_{CM} = 1\ \text{V p-p}$	–102	–120		dB
PD (POWER-DOWN) PIN (ADA4898-1)					
$\overline{\text{PD}}$ Input Voltages	Chip powered down		≤ -4		V
	Chip enabled		≥ -3		V
$\overline{\text{PD}}$ Turn On Time	$V_{OUT} = 100\ \text{mV p-p}$		100		ns
$\overline{\text{PD}}$ Turn Off Time	$V_{OUT} = 100\ \text{mV p-p}$		20		μs
Input Leakage Current	$\overline{\text{PD}} = +V_S$		0.1		μA
	$\overline{\text{PD}} = -V_S$		–2		μA
OUTPUT CHARACTERISTICS					
Output Voltage Swing	$R_L // (R_F + R_G) = 500\ \Omega$, see Figure 43	± 3.1	± 3.2		V
	$R_L // (R_F + R_G) = 1\ \text{k}\Omega$, see Figure 43	± 3.3	± 3.4		V
Linear Output Current	$f = 100\ \text{kHz}$, SFDR = –70 dBc, $R_L = 150\ \Omega$		8		mA
Short-Circuit Current	Sinking/sourcing		150		mA
Off Isolation	$f = 1\ \text{MHz}$, $\overline{\text{PD}} = -V_S$		80		dB
POWER SUPPLY					
Operating Range		± 4.5		± 16.5	V
Quiescent Current Per Amplifier	$\overline{\text{PD}} = +V_S$		7.5	8.4	mA
	$\overline{\text{PD}} = -V_S$		0.1	0.2	mA
Positive Power Supply Rejection Ratio	$+V_S = 5\ \text{V}$ to $7\ \text{V}$, $-V_S = -5\ \text{V}$	–95	–100		dB
Negative Power Supply Rejection Ratio	$+V_S = 5\ \text{V}$, $-V_S = -5\ \text{V}$ to $-7\ \text{V}$	–97	–104		dB

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage	36 V
Power Dissipation	See Figure 4
Differential Mode Input Voltage	± 1.5 V
Common-Mode Input Voltage	± 11.4 V
Storage Temperature Range	-65°C to $+150^{\circ}\text{C}$
Operating Temperature Range	-40°C to $+105^{\circ}\text{C}$
Lead Temperature (Soldering, 10 sec)	300°C
Junction Temperature	150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions; that is, θ_{JA} is specified for a device soldered in the circuit board with its exposed paddle soldered to a pad on the PCB surface that is thermally connected to a copper plane, with zero airflow.

Table 4.

Package Type	θ_{JA}	θ_{JC}	Unit
Single 8-Lead SOIC_N_EP on a 4-Layer Board	47	29	$^{\circ}\text{C}/\text{W}$
Dual 8-Lead SOIC_N_EP on a 4-Layer Board	42	29	$^{\circ}\text{C}/\text{W}$

MAXIMUM POWER DISSIPATION

The maximum safe power dissipation in the [ADA4898-1/ADA4898-2](#) package is limited by the associated rise in junction temperature (T_J) on the die. At approximately 150°C , which is the glass transition temperature, the plastic changes its properties. Even temporarily exceeding this temperature limit can change the stresses that the package exerts on the die, permanently shifting the parametric performance of the [ADA4898-1/ADA4898-2](#). Exceeding a junction temperature of 150°C for an extended period can result in changes in the silicon devices, potentially causing failure.

The power dissipated in the package (P_D) is the sum of the quiescent power dissipation and the power dissipated in the package due to the output load drive. The quiescent power is the voltage between the supply pins (V_S) times the quiescent current (I_S). The power dissipated due to the load drive depends upon the particular application. For each output, the power due to load drive is calculated by multiplying the load current by the associated voltage drop across the device. RMS voltages and currents must be used in these calculations.

Airflow increases heat dissipation, effectively reducing θ_{JA} . In addition, more metal directly in contact with the package leads from metal traces, through holes, ground, and power planes reduces the θ_{JA} . The exposed paddle on the underside of the package must be soldered to a pad on the PCB surface that is thermally connected to a copper plane to achieve the specified θ_{JA} .

Figure 4 shows the maximum power dissipation vs. the ambient temperature for the single and dual 8-lead SOIC_N_EP on a JEDEC standard 4-layer board, with its underside paddle soldered to a pad that is thermally connected to a PCB plane. θ_{JA} values are approximations.

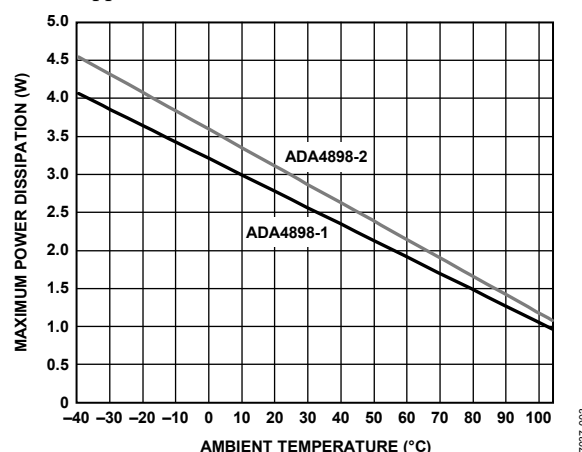


Figure 4. Maximum Power Dissipation vs. Ambient Temperature

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

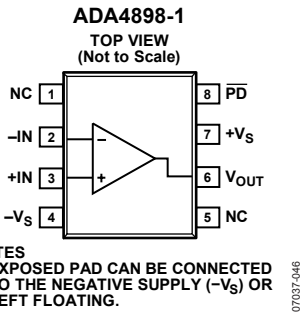


Figure 5. Single 8-Lead SOIC_N_EP Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	NC	No Connect.
2	-IN	Inverting Input.
3	+IN	Noninverting Input.
4	$-V_S$	Negative Supply.
5	NC	No Connect.
6	V_{OUT}	Output.
7	$+V_S$	Positive Supply.
8	PD	Power Down Not.
	EP	Exposed Pad. Can be connected to the negative supply ($-V_S$) or can be left floating.

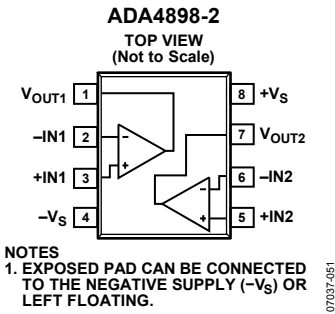


Figure 6. Dual 8-Lead SOIC_N_EP Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{OUT1}	Output 1.
2	-IN1	Inverting Input 1.
3	+IN1	Noninverting Input 1.
4	$-V_S$	Negative Supply.
5	+IN2	Noninverting Input 2.
6	-IN2	Inverting Input 2.
7	V_{OUT2}	Output 2.
8	$+V_S$	Positive Supply.
	EP	Exposed Pad. Can be connected to the negative supply ($-V_S$) or can be left floating.

TYPICAL PERFORMANCE CHARACTERISTICS

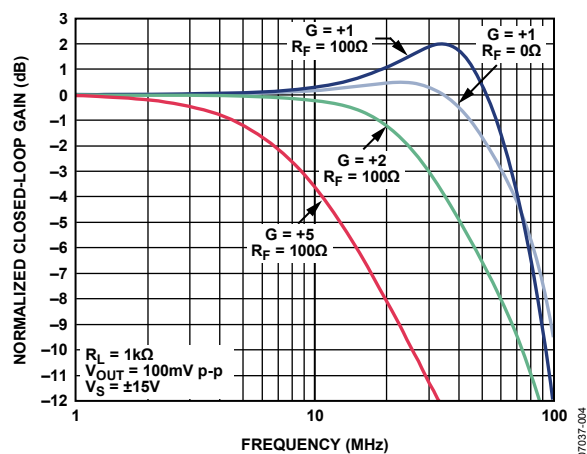


Figure 7. Small Signal Frequency Response for Various Gains

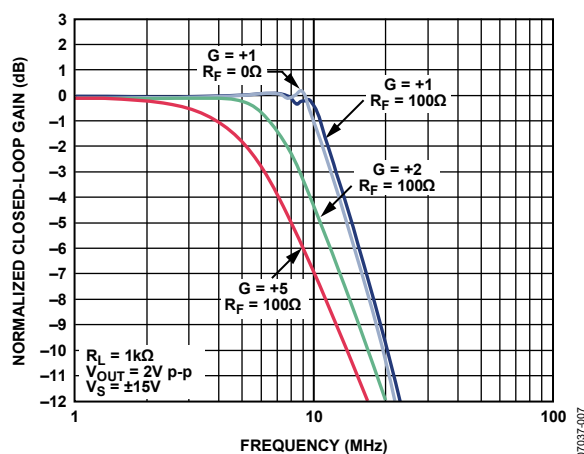


Figure 10. Large Signal Frequency Response for Various Gains

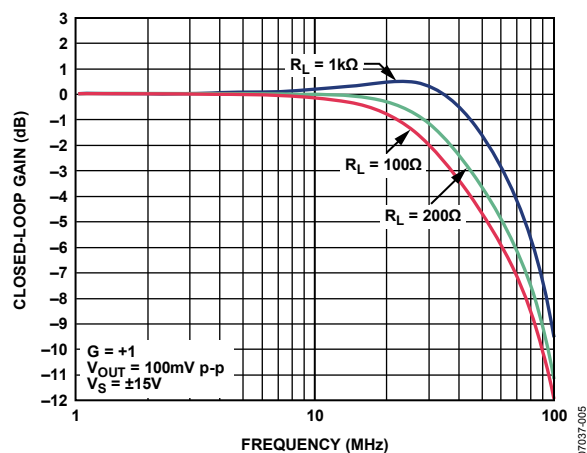


Figure 8. Small Signal Frequency Response for Various Loads

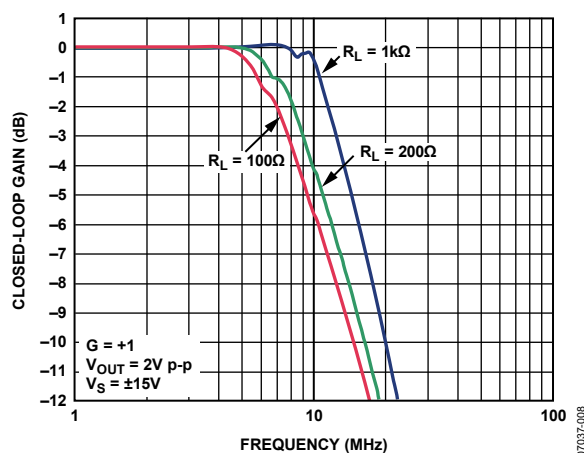


Figure 11. Large Signal Frequency Response for Various Loads

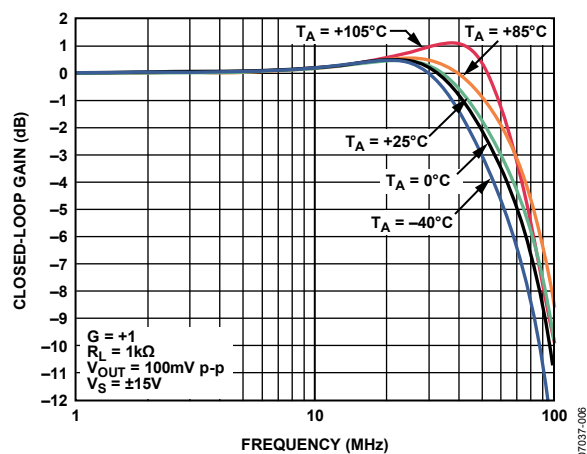


Figure 9. Small Signal Frequency Response for Various Temperatures

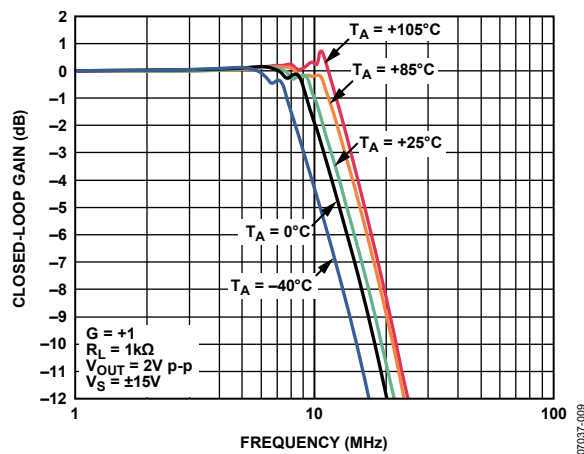


Figure 12. Large Signal Frequency Response for Various Temperatures

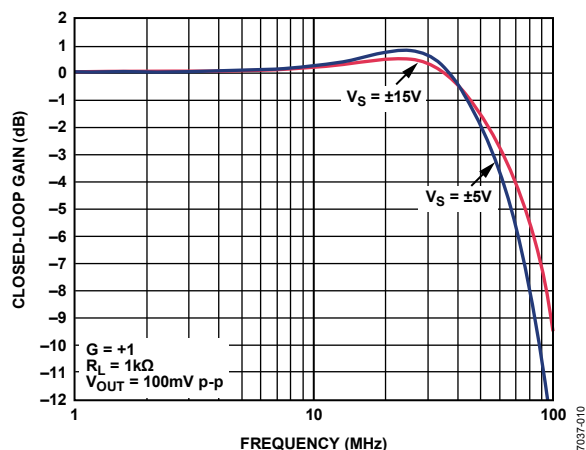


Figure 13. Small Signal Frequency Response for Various Supply Voltages

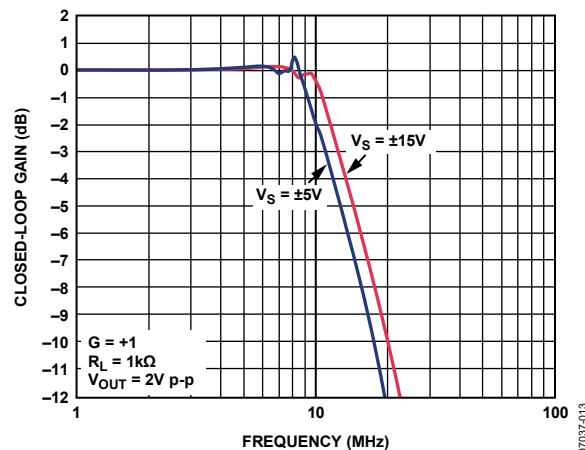


Figure 16. Large Signal Frequency Response for Various Supply Voltages

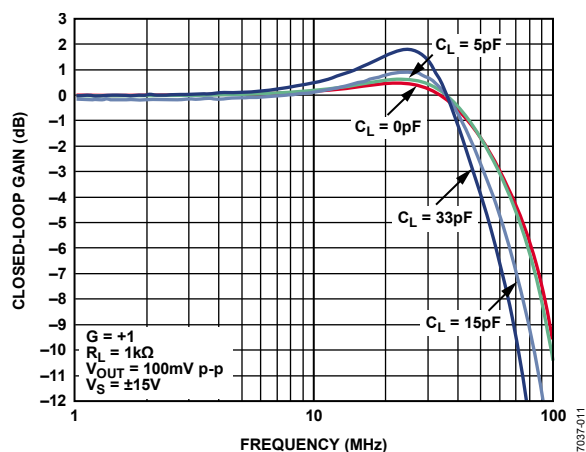


Figure 14. Small Signal Frequency Response for Various Capacitive Loads

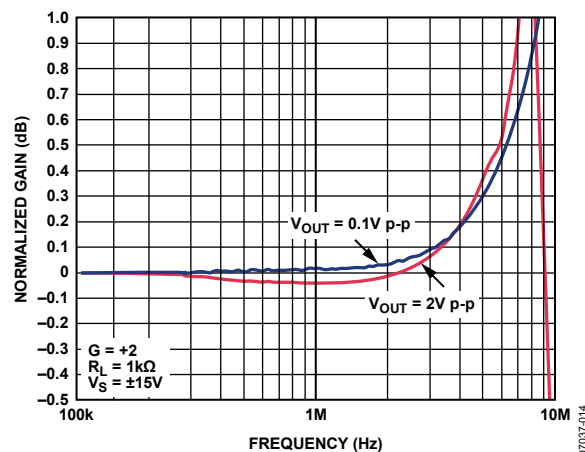


Figure 17. 0.1 dB Flatness for Various Output Voltages

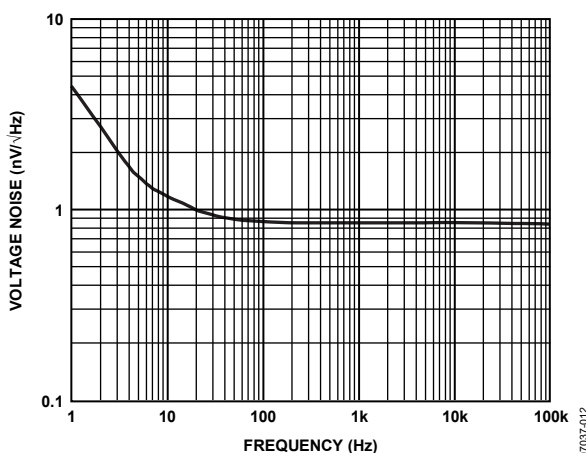


Figure 15. Voltage Noise vs. Frequency

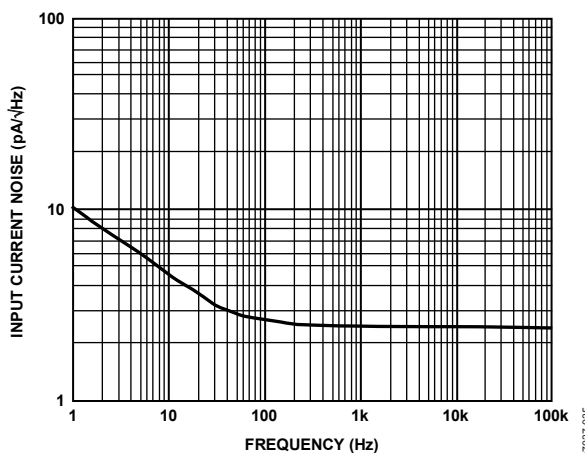


Figure 18. Input Current Noise vs. Frequency

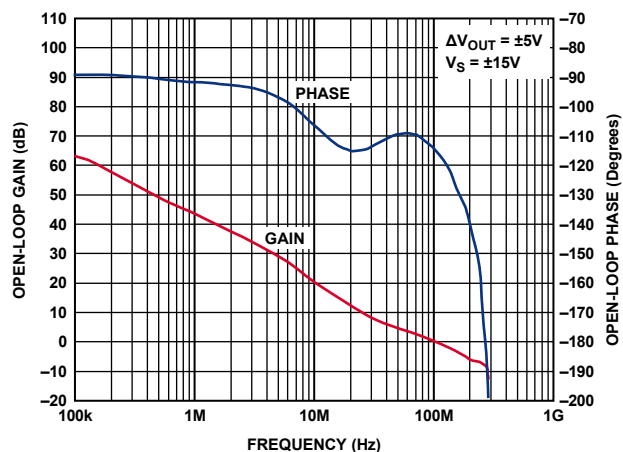


Figure 19. Open-Loop Gain and Phase vs. Frequency

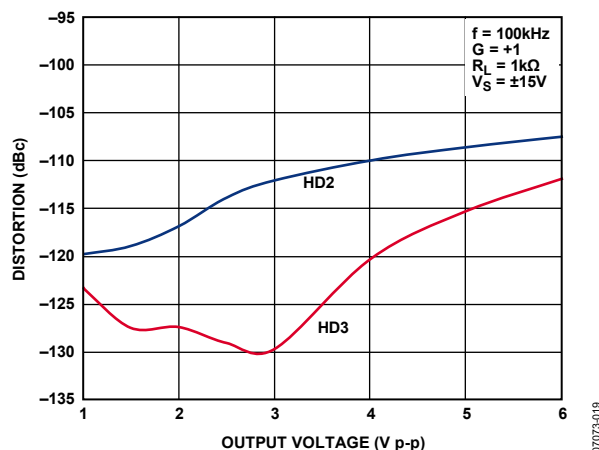


Figure 22. Harmonic Distortion vs. Output Amplitude

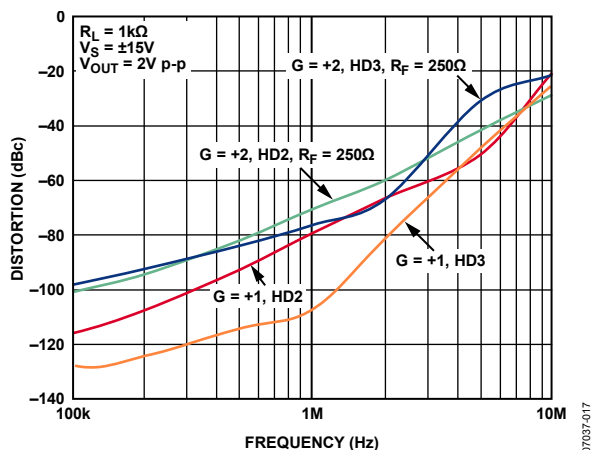


Figure 20. Harmonic Distortion vs. Frequency and Gain

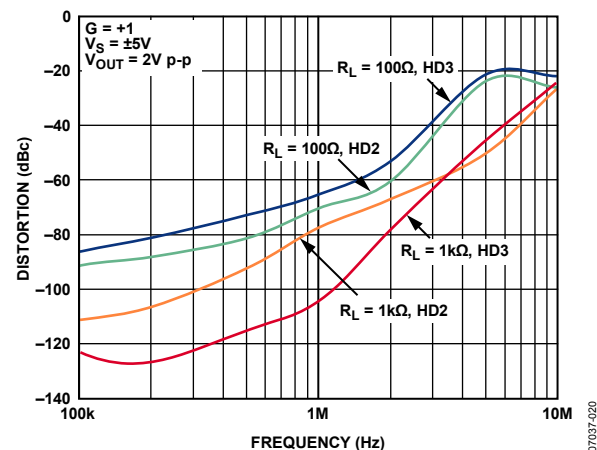


Figure 23. Harmonic Distortion vs. Frequency and Loads

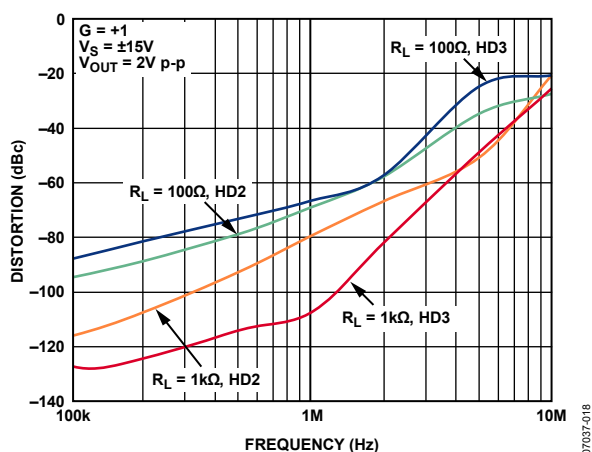


Figure 21. Harmonic Distortion vs. Frequency and Loads

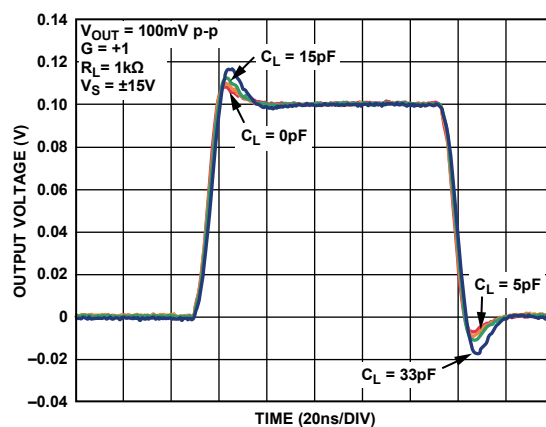


Figure 24. Small Signal Transient Response for Various Capacitive Loads

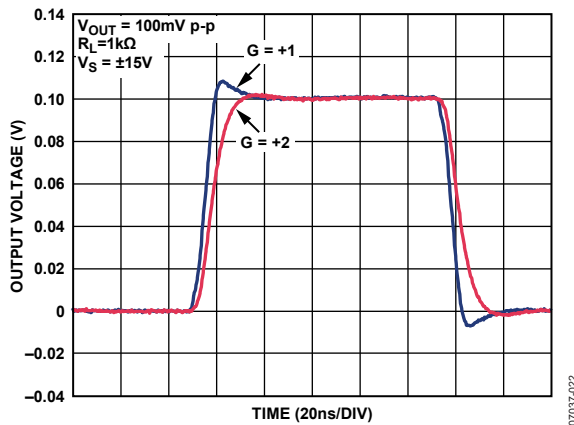


Figure 25. Small Signal Transient Response for Various Gains

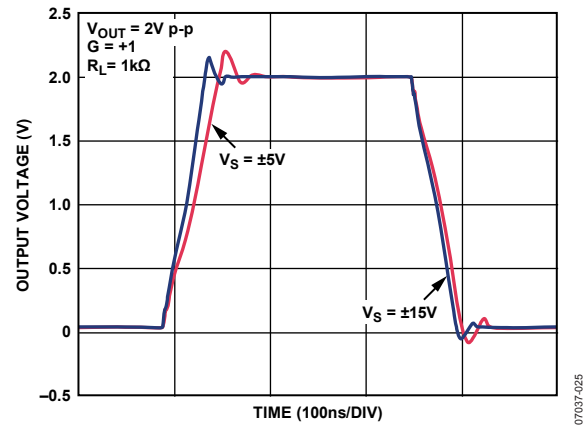


Figure 28. Large Signal Transient Response for Various Supply Voltages, $R_L = 1k\Omega$

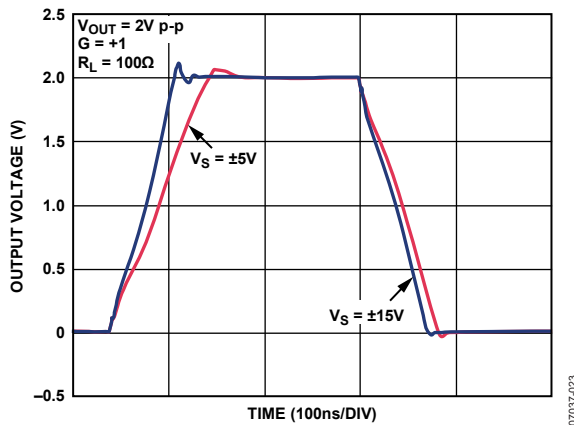


Figure 26. Large Signal Transient Response for Various Supply Voltages, $R_L = 100\Omega$

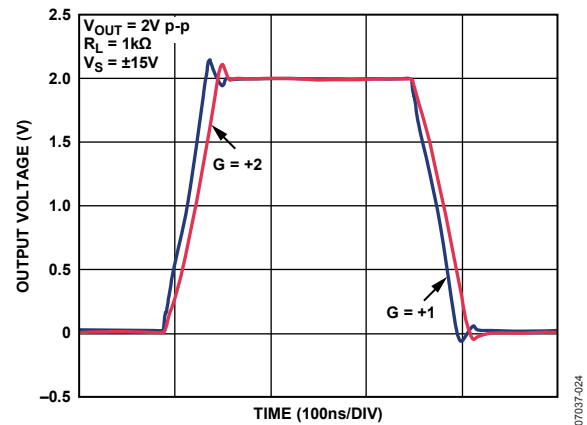


Figure 29. Large Signal Transient Response for Various Gains

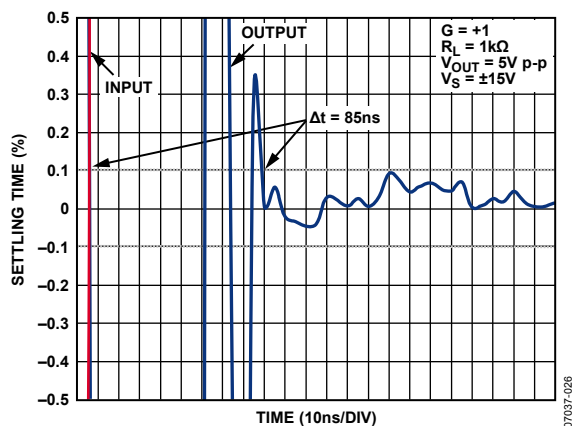


Figure 27. Settling Time

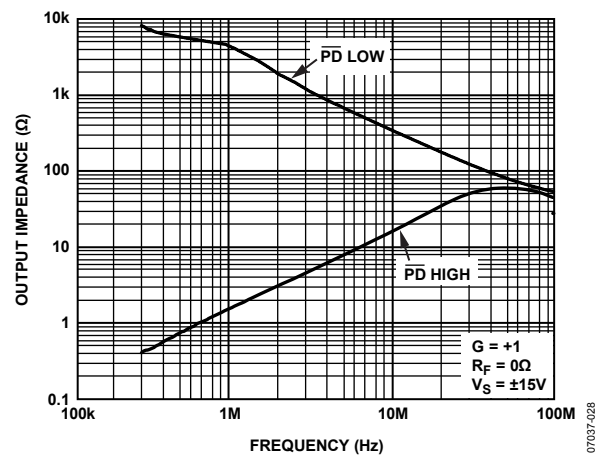


Figure 30. Output Impedance vs. Frequency

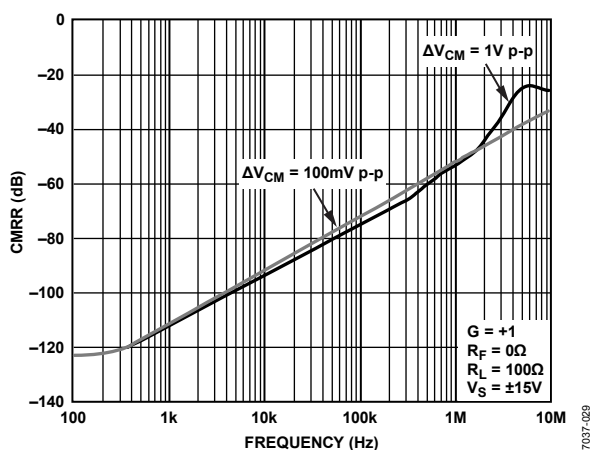


Figure 31. Common-Mode Rejection Ratio (CMRR) vs. Frequency

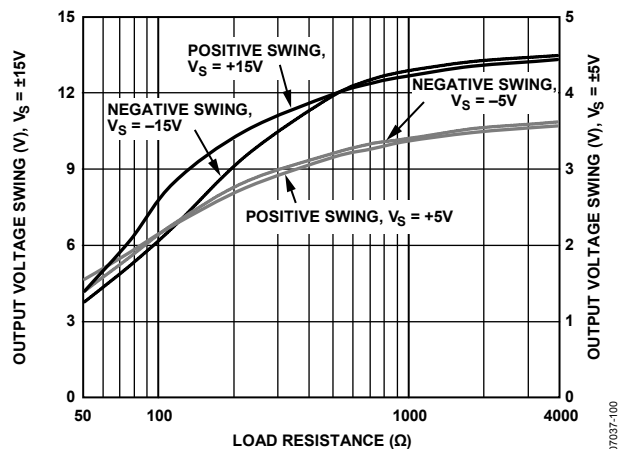
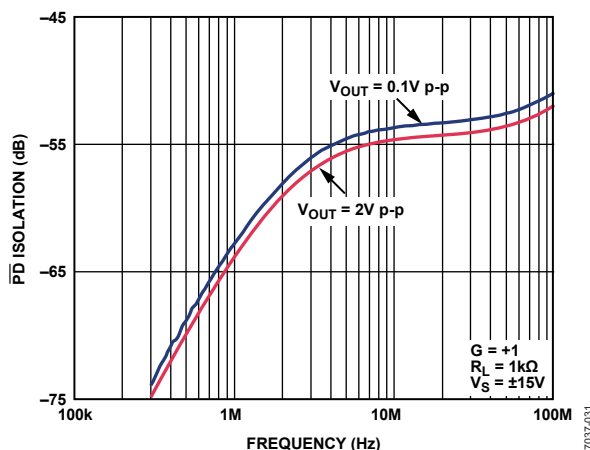
Figure 34. Output Swing vs. Load, $G = +2$, Load = $R_L // (R_F + R_G)$ 

Figure 32. PD Input to Output Isolation vs. Frequency

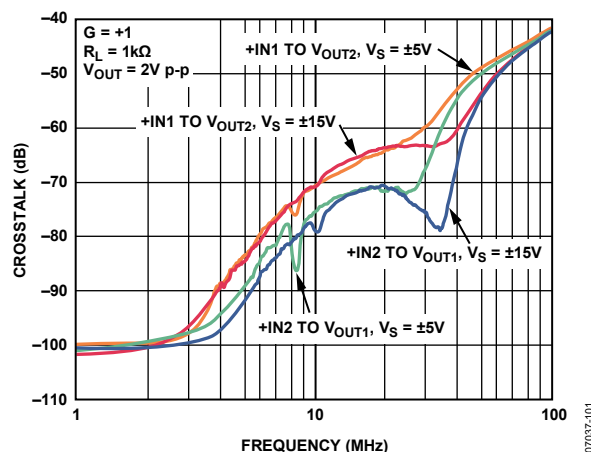


Figure 35. Crosstalk vs. Frequency

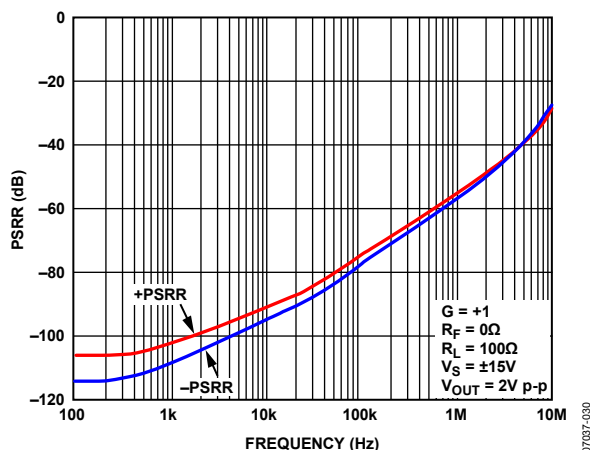


Figure 33. Power Supply Rejection Ratio (PSRR) vs. Frequency

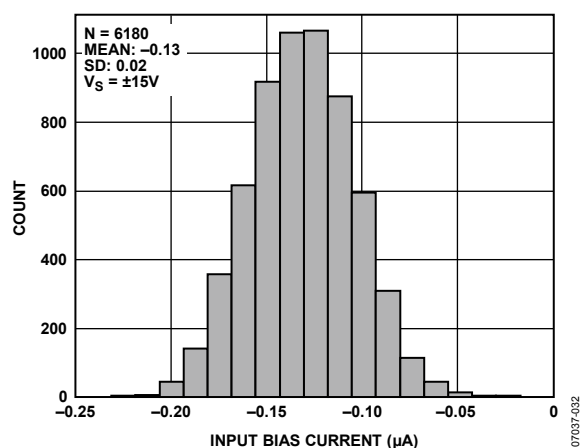


Figure 36. Input Bias Current Distribution

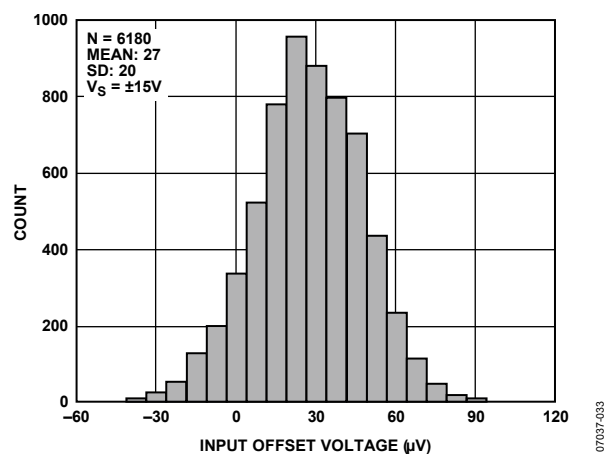


Figure 37. Input Offset Voltage Distribution, $V_S = \pm 15 V$

TEST CIRCUITS

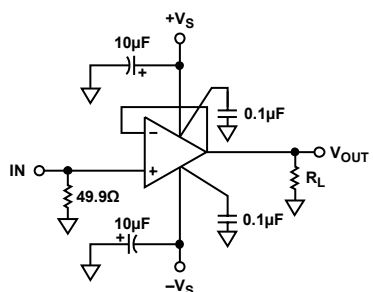


Figure 38. Typical Noninverting Load Configuration

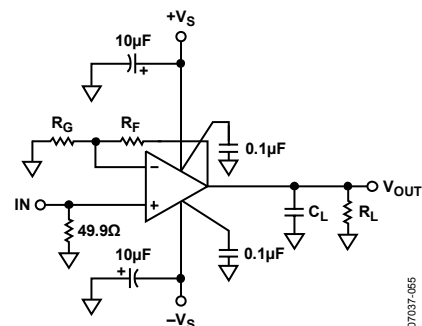


Figure 41. Typical Capacitive Load Configuration

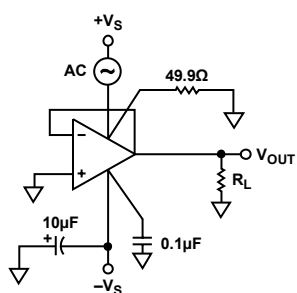


Figure 39. Positive Power Supply Rejection

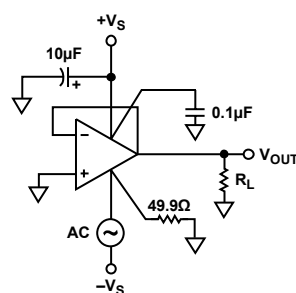


Figure 42. Negative Power Supply Rejection

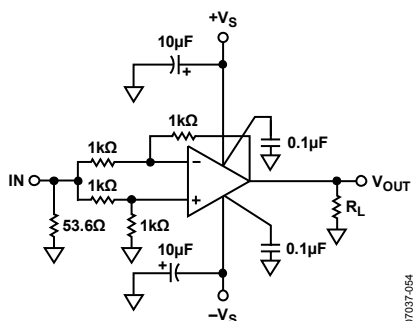


Figure 40. Common-Mode Rejection

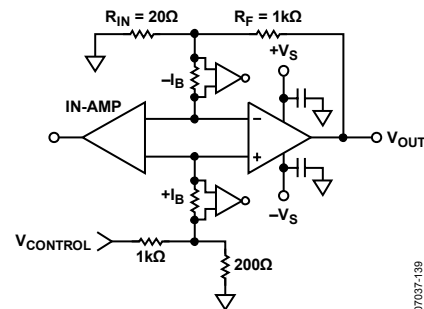


Figure 43. DC Test Circuit

THEORY OF OPERATION

The [ADA4898-1/ADA4898-2](#) are voltage feedback op amps that combine unity gain stability with 0.9 nV/ $\sqrt{\text{Hz}}$ input noise. They employ a highly linear input stage that can maintain greater than -90 dBc (at 2 V p-p) distortion out to 600 kHz while in a unity-gain configuration. This rare combination of unity gain stability, low input-referred noise, and extremely low distortion is the result of Analog Devices, Inc., proprietary op amp architecture and high voltage bipolar processing technology.

The simplified [ADA4898-1/ADA4898-2](#) topology, shown in Figure 44, is a single gain stage with a unity-gain output buffer. It has over 100 dB of open-loop gain and maintains precision specifications, such as CMRR, PSRR, and offset, to levels that are normally associated with topologies having two or more gain stages.

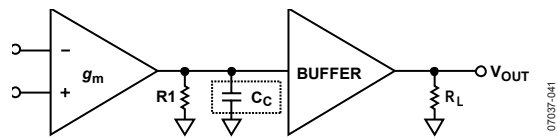


Figure 44. Topology

PD (POWER-DOWN) PIN FOR THE [ADA4898-1](#)

The $\overline{\text{PD}}$ pin saves power by decreasing the quiescent power dissipated in the device. It is very useful when power is an issue and the device does not need to be turned on at all times. The response of the device is rapid when going from power-down mode to full power operation mode. Note that $\overline{\text{PD}}$ does not put the output in a high-Z state, which means that the [ADA4898-1/ADA4898-2](#) are not recommended for use as multiplexers. Leaving the $\overline{\text{PD}}$ pin floating keeps the amplifier in full power operation mode.

Table 7. Power-Down Voltage Control

PD Pin	$\pm 15\text{ V}$	$\pm 10\text{ V}$	$\pm 5\text{ V}$
Power-Down Mode	$\leq -14\text{ V}$	$\leq -9\text{ V}$	$\leq -4\text{ V}$

APPLICATIONS INFORMATION

HIGHER FEEDBACK RESISTOR GAIN OPERATION

The ADA4898-1/ADA4898-2 schematic for the noninverting gain configuration shown in Figure 45 is nearly a textbook example. The only exception is the feedback capacitor in parallel with the feedback resistor, R_F , but this capacitor is recommended only when using a large R_F value ($>300\ \Omega$). Figure 46 shows the difference between using a $100\ \Omega$ resistor and a $1\ \text{k}\Omega$ feedback resistor. Due to the high input capacitance in the ADA4898-1/ADA4898-2 when using a higher feedback resistor, more peaking appears in the closed-loop gain. Using the lower feedback resistor resolves this issue; however, when running at higher supplies ($\pm 15\ \text{V}$) with an R_F of $100\ \Omega$, the system draws a lot of extra current into the feedback network. To avoid this problem, a higher feedback resistor can be used with a feedback capacitor in parallel. Figure 46 shows the effect of placing a feedback capacitor in parallel with a larger R_F . In this gain-of-2 configuration, $R_F = R_G = 1\ \text{k}\Omega$ and $C_F = 2.7\ \text{pF}$. When using C_F , the peaking drops from 6 dB to less than 2 dB.

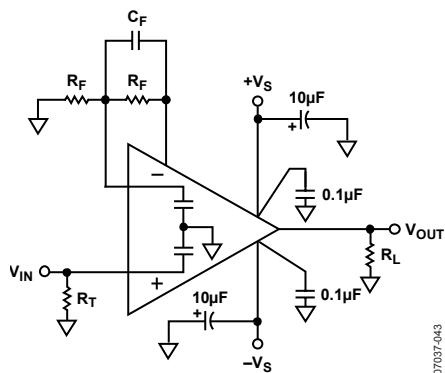


Figure 45. Noninverting Gain Schematic

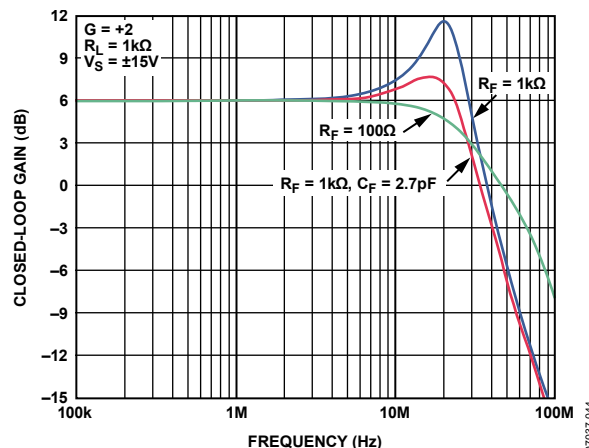


Figure 46. Small Signal Frequency Response for Various Feedback Impedances

RECOMMENDED VALUES FOR VARIOUS GAINS

Table 8 provides a useful reference for determining various gains and associated performance. R_F is set to $100\ \Omega$ for gains greater than 1. A low feedback R_F resistor value reduces peaking and minimizes the contribution to the overall noise performance of the amplifier.

Table 8. Gains and Recommended Resistor Values Associated with Them (Conditions: $V_S = \pm 5\ \text{V}$, $T_A = 25^\circ\text{C}$, $R_L = 1\ \text{k}\Omega$, $R_T = 49.9\ \Omega$)

Gain	$R_F\ (\Omega)$	$R_G\ (\Omega)$	-3 dB SS BW (MHz), $V_{OUT} = 100\ \text{mV p-p}$	Slew Rate (V/ μs), $V_{OUT} = 2\ \text{V Step}$	ADA4898-1/ADA4898-2 Voltage Noise (nV/ $\sqrt{\text{Hz}}$), RTO	Total System Noise (nV/ $\sqrt{\text{Hz}}$), RTO
+1	0	Not applicable	65	55	0.9	1.29
+2	100	100	30	50	1.8	3.16
+5	100	24.9	9	45	4.5	7.07

NOISE

To analyze the noise performance of an amplifier circuit, identify the noise sources, and then determine if each source has a significant contribution to the overall noise performance of the amplifier. To simplify the noise calculations, noise spectral densities were used rather than actual voltages to leave bandwidth out of the expressions. Noise spectral density, which is generally expressed in $\text{nV}/\sqrt{\text{Hz}}$, is equivalent to the noise in a 1 Hz bandwidth.

The noise model shown in Figure 47 has six individual noise sources: the Johnson noise of the three resistors, the op amp voltage noise, and the current noise in each input of the amplifier. Each noise source has its own contribution to the noise at the output. Noise is generally specified as referring to input (RTI), but it is often simpler to calculate the noise referred to the output (RTO) and then divide by the noise gain to obtain the RTI noise.

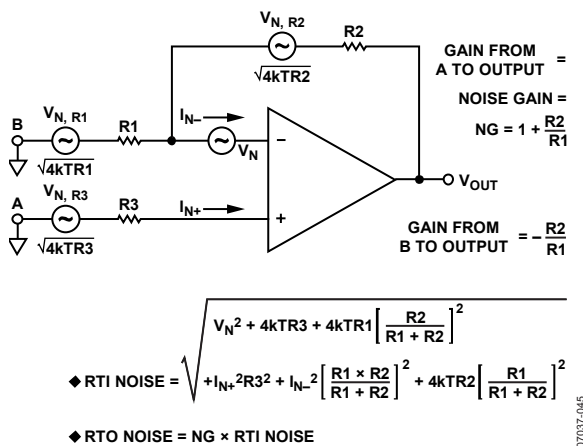


Figure 47. Op Amp Noise Analysis Model

All resistors have a Johnson noise that is calculated by

$$\sqrt{(4kBT R)}$$

where:

k is Boltzmann's constant ($1.38 \times 10^{-23} \text{ J/K}$).

B is the bandwidth in Hertz.

T is the absolute temperature in Kelvin.

R is the resistance in ohms.

A simple relationship that is easy to remember is that a 50Ω resistor generates a Johnson noise of $1 \text{ nV}/\sqrt{\text{Hz}}$ at 25°C .

In applications where noise sensitivity is critical, care must be taken not to introduce other significant noise sources to the amplifier. Each resistor is a noise source. Attention to the following areas is critical to maintain low noise performance: design, layout, and component selection. A summary of noise performance for the amplifier and associated resistors is shown in Table 8.

CIRCUIT CONSIDERATIONS

Careful and deliberate attention to detail when laying out the ADA4898-1/ADA4898-2 boards yields optimal performance. Power supply bypassing, parasitic capacitance, and component selection all contribute to the overall performance of the amplifier.

PCB LAYOUT

Because the ADA4898-1/ADA4898-2 have small signal bandwidths of 65 MHz, it is essential that high frequency board layout techniques be employed. All ground and power planes under the pins of the ADA4898-1/ADA4898-2 should be cleared of copper to prevent the formation of parasitic capacitance between the input pins to ground and the output pins to ground. A single mounting pad on a SOIC footprint can add as much as 0.2 pF of capacitance to ground if the ground plane is not cleared from under the mounting pads.

POWER SUPPLY BYPASSING

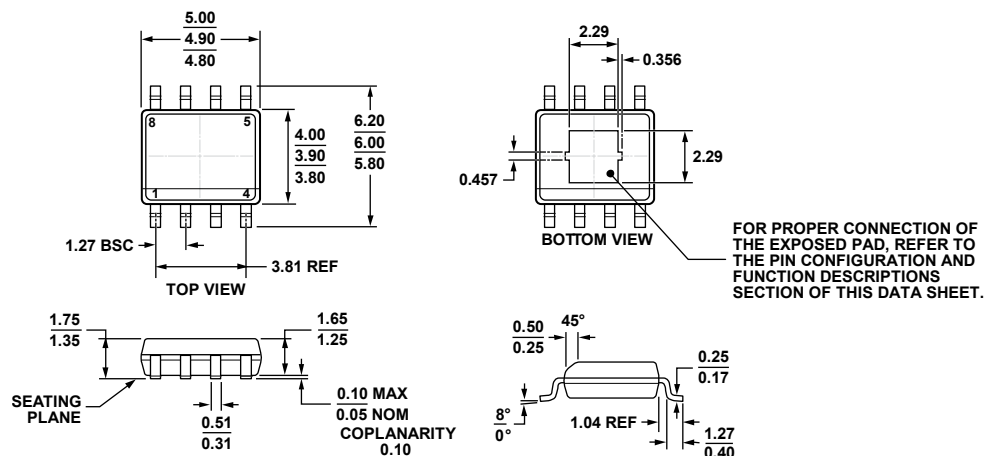
Power supply bypassing for the ADA4898-1/ADA4898-2 has been optimized for frequency response and distortion performance. Figure 45 shows the recommended values and location of the bypass capacitors. Power supply bypassing is critical for stability, frequency response, distortion, and PSR performance. The $0.1 \mu\text{F}$ capacitors shown in Figure 45 should be as close to the supply pins of the ADA4898-1/ADA4898-2 as possible. The $10 \mu\text{F}$ electrolytic capacitors should be adjacent to, but not necessarily close to, the $0.1 \mu\text{F}$ capacitors. The capacitor between the two supplies helps improve PSR and distortion performance. In some cases, additional paralleled capacitors can help improve frequency and transient response.

GROUNDING

Ground and power planes should be used where possible. Ground and power planes reduce the resistance and inductance of the power planes and ground returns. The returns for the input and output terminations, bypass capacitors, and R_G should all be kept as close to the ADA4898-1/ADA4898-2 as possible. The output load ground and the bypass capacitor grounds should be returned to the same point on the ground plane to minimize parasitic trace inductance, ringing, and overshoot and to improve distortion performance.

The ADA4898-1/ADA4898-2 package features an exposed paddle. For optimum electrical and thermal performance, solder this paddle to a negative supply plane.

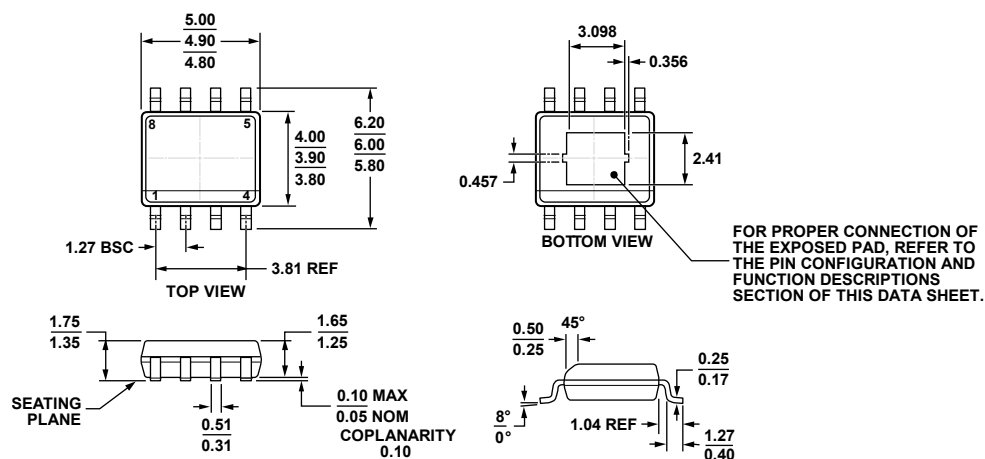
OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-012-AA

Figure 48. 8-Lead Standard Small Outline Package with Exposed Pad [SOIC_N_EP] (RD-8-1)

Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MS-012-AA

Figure 49. 8-Lead Standard Small Outline Package with Exposed Pad [SOIC_N_EP] (RD-8-2)

Dimensions shown in millimeters

ORDERING GUIDE

Model ¹	Temperature Range	Package Description	Package Option	Ordering Quantity
ADA4898-1YRDZ	-40°C to +105°C	8-Lead SOIC_N_EP	RD-8-1	98
ADA4898-1YRDZ-R7	-40°C to +105°C	8-Lead SOIC_N_EP	RD-8-1	1,000
ADA4898-1YRDZ-RL	-40°C to +105°C	8-Lead SOIC_N_EP	RD-8-1	2,500
ADA4898-2YRDZ	-40°C to +105°C	8-Lead SOIC_N_EP	RD-8-2	98
ADA4898-2YRDZ-R7	-40°C to +105°C	8-Lead SOIC_N_EP	RD-8-2	1,000
ADA4898-2YRD-EBZ		Evaluation Board		

¹ Z = RoHS Compliant Part.

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