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6/2016—Rev. A to Rev. B

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4/2013—Revision 0: Initial Version

SPECIFICATIONS

AC SPECIFICATIONS

VBAT = 3.0 V, T_A = 25°C, C_L = 2 pF on OUTP and OUTM, R_L = ∞, MODE pin high, R_{IN} = 2 × 500 Ω, V_{GAIN} = 0.6 V, differential operation, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT INTERFACE	INPD, INMD, INPR, and INMR pins				
Input Voltage Range			3		V p-p
−3 dB Bandwidth			18		MHz
Input Resistance	Standard configuration using the INPR and INMR inputs	0.8	1	1.2	kΩ
Input Capacitance			2		pF
OUTPUT INTERFACE	OUTP and OUTM pins				
Small Signal Bandwidth	V_{GAIN} = 0.6 V		18		MHz
Peak Slew Rate	V_{GAIN} = 0.6 V		50		V/µs
Peak-to-Peak Output Swing	Single-ended		0.7		V p-p
	Differential		1.4		V p-p
	Difference output swing		2.8		V p-p
Common-Mode Voltage			1.5		V
Input-Referred Voltage Noise					
Using Internal Resistors	V_{GAIN} = 1.1 V		4.5		nV/√Hz
	V_{GAIN} = 0.6 V		15		nV/√Hz
	V_{GAIN} = 0.1 V		150		nV/√Hz
Using External 47 Ω Resistors	V_{GAIN} = 1.1 V		1.5		nV/√Hz
Offset Voltage	RTO, V_{GAIN} = 0.1 V, offset null enabled	−10		+10	mV
	RTO, V_{GAIN} = 0.6 V, offset null enabled	−10		+10	mV
	RTO, V_{GAIN} = 0.1 V, offset null disabled	−50		+50	mV
	RTO, V_{GAIN} = 0.6 V, offset null disabled	−200		+200	mV
POWER SUPPLY					
VBAT		3.0		5.0	V
I_{VBAT}	Minimum gain, V_{GAIN} = 0.1 V		6.0	8.0	mA
	Mid gain, V_{GAIN} = 0.6 V		3.0	3.8	mA
	Maximum gain, V_{GAIN} = 1.1 V		4.5	6.0	mA
GAIN CONTROL					
Gain Range	Standard configuration using the INPR and INMR inputs	0		80	dB
Gain Span			80		dB
Gain Voltage (V_{GAIN})	V_{GAIN} relative to COMM	0.1		1.1	V
Gain Slope		77	80	83	dB/V
		12	12.5	13	mV/dB
Gain Accuracy	Standard configuration using the INPR and INMR inputs; 0.1 V < V_{GAIN} < 1.1 V	−2	+0.5	+2	dB
VREF REFERENCE OUTPUT					
Output Voltage			1.5		V
Output Current			5		mA
Accuracy			2		%
DETO OUTPUT CURRENT			±10		µA
MODE INPUT					
Logic High		2.5		VBAT	V
Logic Low		COMM		0.6	V
AGC CONTROL	MODE = 0 V				
Maximum Target Amplitude	Expected rms output value for target = VAGC − VREF = 1.0 V		1.0		V rms

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
VBAT to COMM	−0.3 V to +5.5 V
INPR, INPD, INMD, INMR, MODE, GAIN, FBKM, FBKP, OUTM, OUTP, VAGC, VREF, OFSN	COMM to VBAT
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Maximum Junction Temperature	150°C
Lead Temperature (Soldering, 10 sec)	300°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Table 3. Thermal Resistance

Package Type	θ_{JA}	Unit
16-Lead LFCSP	48.75	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

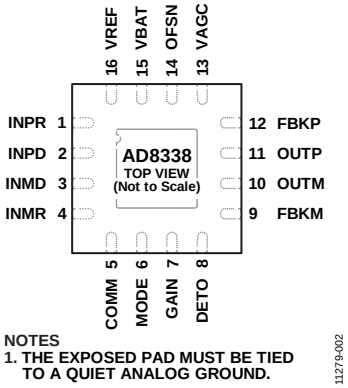

Figure 3. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
0	EPAD	Exposed Pad. The exposed pad must be tied to a quiet analog ground.
1	INPR	Positive 500 Ω Resistor Input for Voltage Input Applications.
2	INPD	Positive Input for Current Input Applications.
3	INMD	Negative Input for Current Input Applications.
4	INMR	Negative 500 Ω Resistor Input for Voltage Input Applications.
5	COMM	Ground.
6	MODE	Gain Mode. This pin selects positive or negative gain slope for gain control. When this pin is tied to VBAT, the gain of the AD8338 increases proportionally with an increase of the voltage on the GAIN pin. When this pin is tied to COMM, the gain decreases with an increase of the voltage on the GAIN pin.
7	GAIN	Gain Control Input, 12.5 mV/dB or 80 dB/V.
8	DETO	Detector Output Terminal, ±10 µA. If the AGC feature is not used, tie DETO to COMM.
9	FBKM	Negative Feedback Node. For more information, see the FBKP, FBKM, OUTP, and OUTM Pins section.
10	OUTM	Negative Output.
11	OUTP	Positive Output.
12	FBKP	Positive Feedback Node. For more information, see the FBKP, FBKM, OUTP, and OUTM Pins section.
13	VAGC	Voltage for Automatic Gain Control Circuit. This pin controls the target rms output voltage for the AGC circuit. For more information, see the AGC Circuit, VAGC Pin section. If the AGC feature is not used, tie VAGC to VREF.
14	OFSN	Offset Null Terminal. For more information, see the Offset Correction Circuit, OFSN Pin section. If the offset null feature is not used, tie OFSN to ground; otherwise, a capacitor to VREF is used to set the offset null high-pass corner.
15	VBAT	Positive Supply Voltage.
16	VREF	Internal 1.5 V Voltage Reference.

TYPICAL PERFORMANCE CHARACTERISTICS

VBAT = 3.0 V, T_A = 25°C, C_L = 2 pF on OUTP and OUTM, R_L = ∞, MODE pin high, R_{IN} = 2 × 500 Ω, V_{GAIN} = 0.6 V, differential operation; unless otherwise noted.

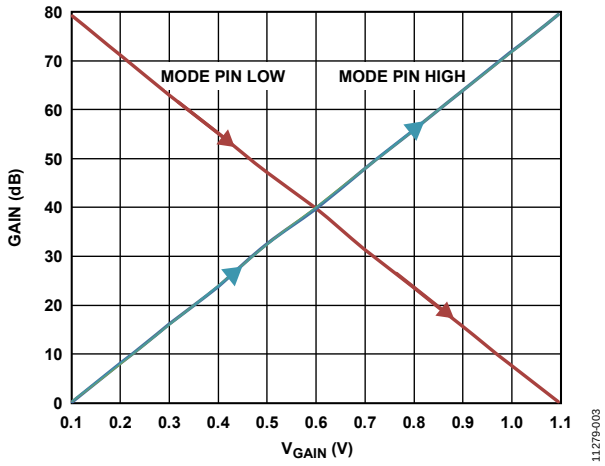

Figure 4. Gain vs. V_{GAIN}

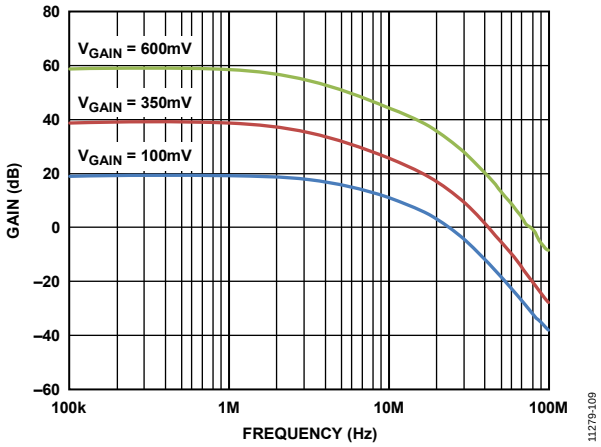

Figure 7. Gain vs. Frequency, R_{IN} = 2 × 50 Ω, 20 dB Steps

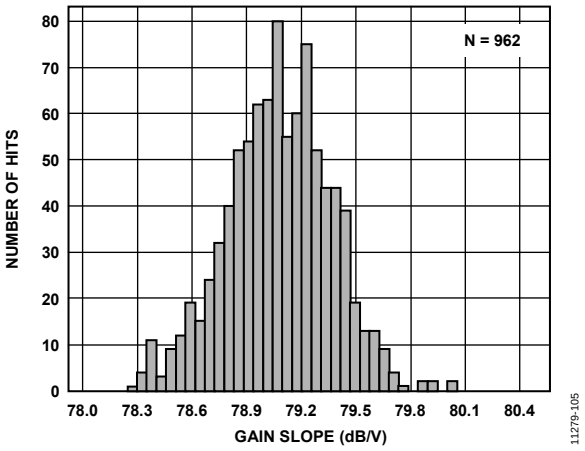

Figure 5. Gain Slope Histogram

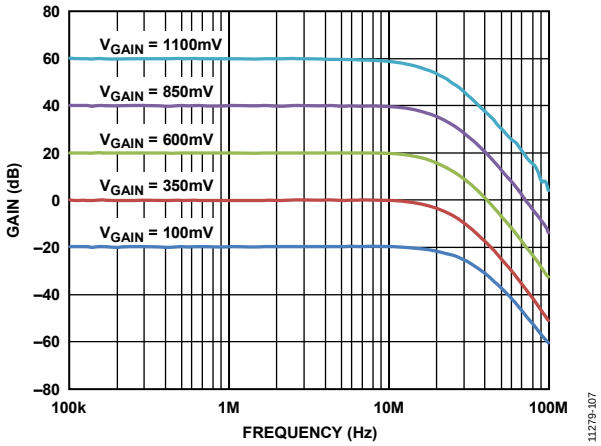

Figure 8. Gain vs. Frequency, R_{IN} = 2 × 5 kΩ, 20 dB Steps

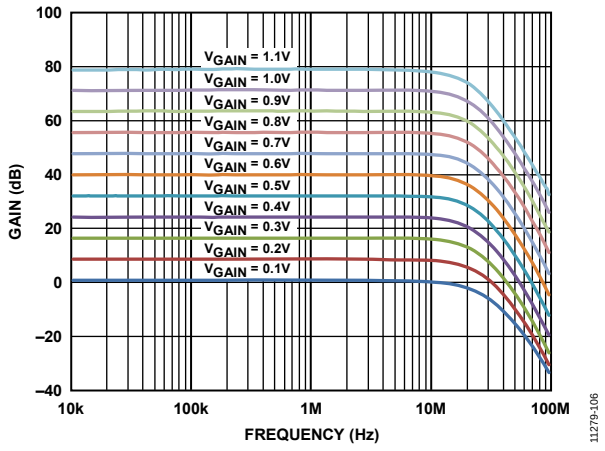

Figure 6. Gain vs. Frequency, 8 dB Steps

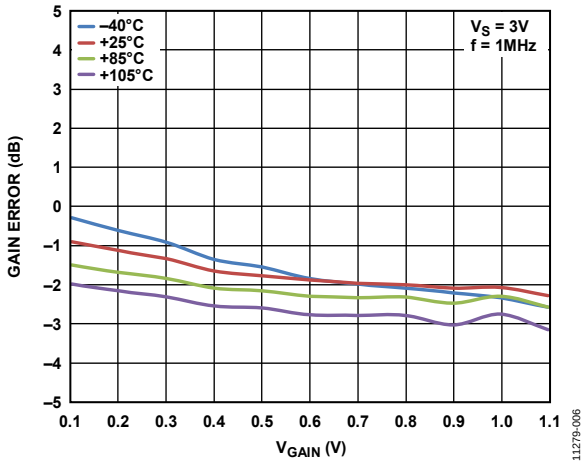

Figure 9. Gain Error vs. V_{GAIN} over Temperature

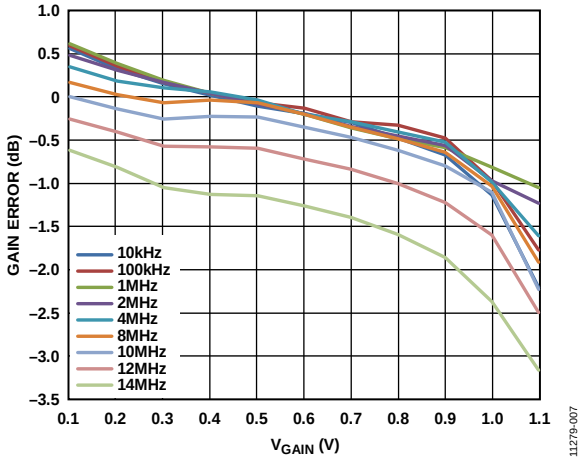

Figure 10. Gain Error vs. V_{GAIN} over Frequency

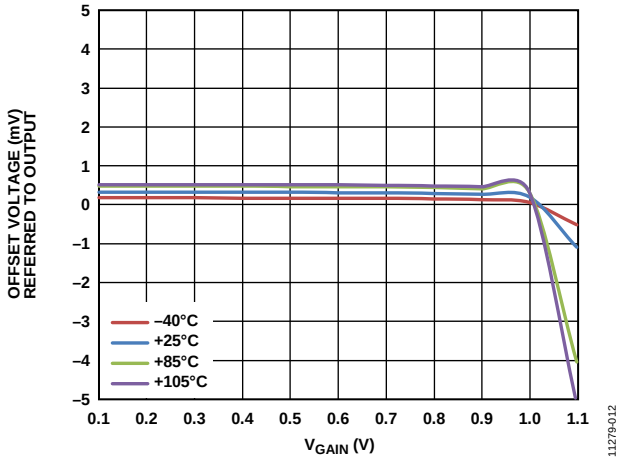

Figure 13. Differential Offset Voltage vs. V_{GAIN}, Offset Null On

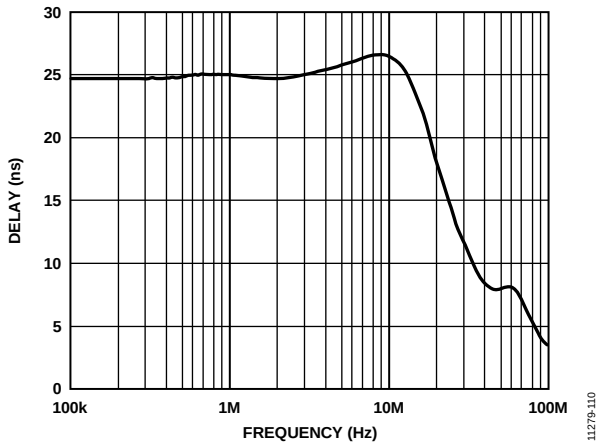

Figure 11. Group Delay vs. Frequency

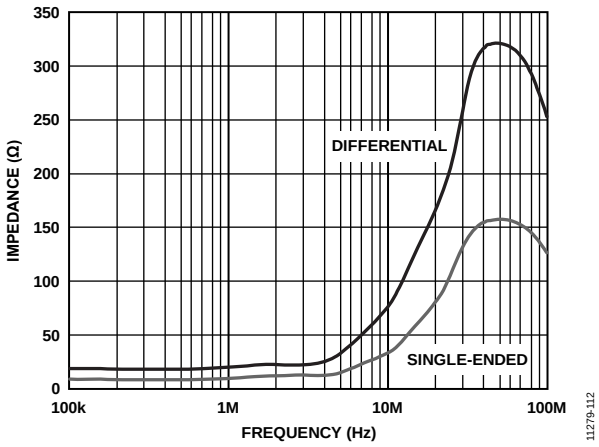

Figure 14. Output Impedance vs. Frequency

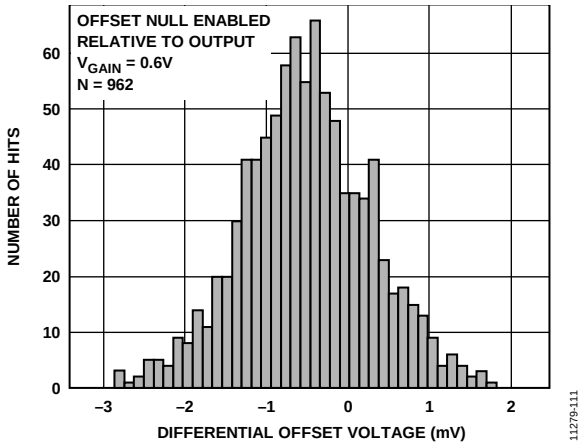

Figure 12. Differential Offset Voltage Histogram

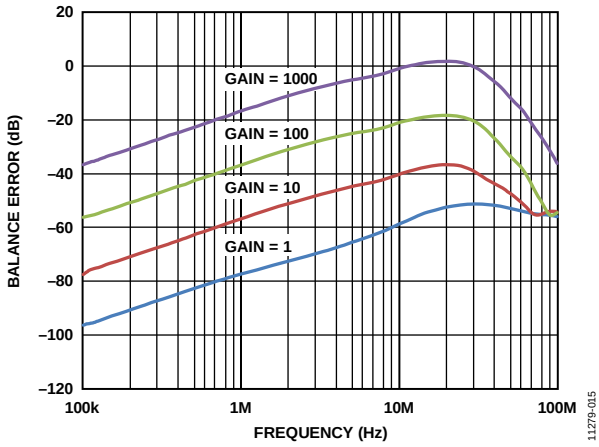

Figure 15. Output Balance Error vs. Frequency

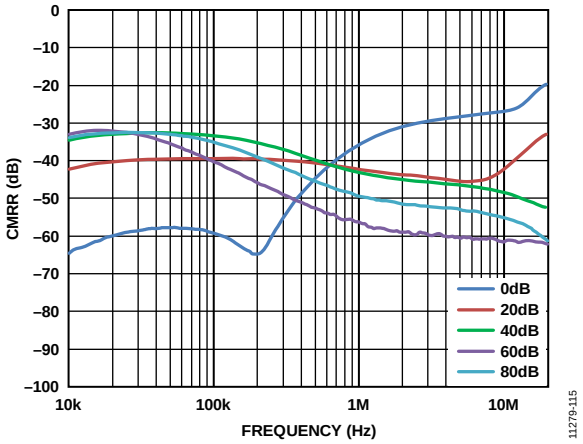

Figure 16. Common-Mode Rejection Ratio (CMRR) vs. Frequency over Gain, Offset Null On, Referred to Input

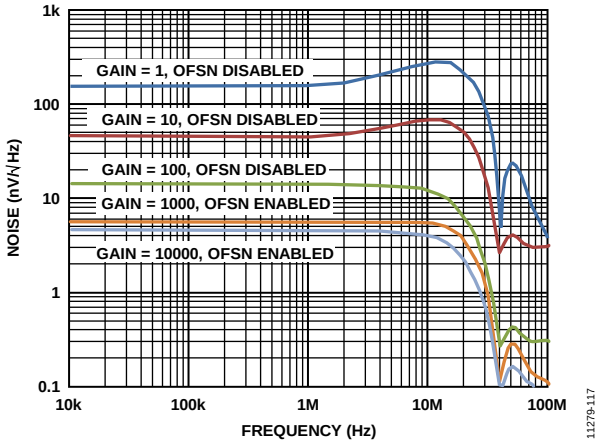

Figure 19. Input Referred Noise vs. Frequency

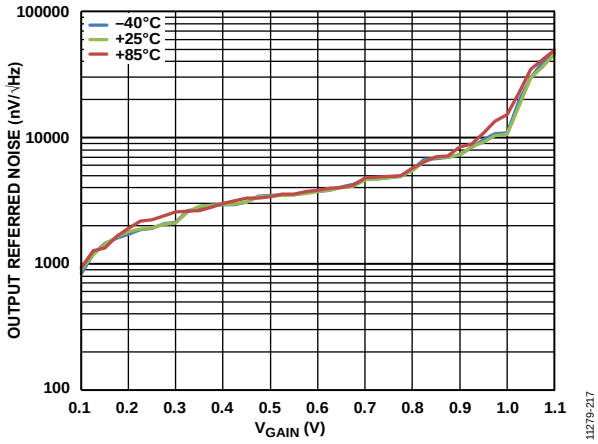

Figure 17. Output Referred Noise vs. V_{GAIN}

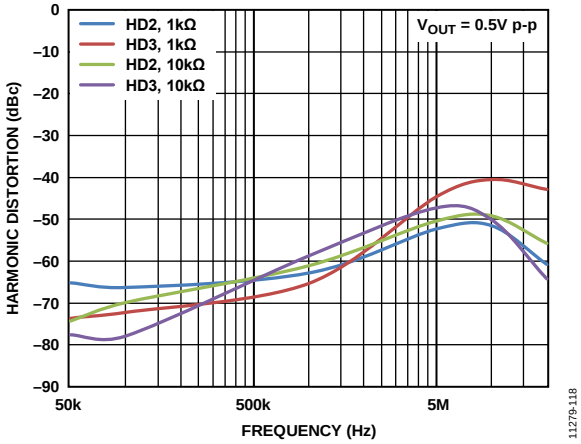

Figure 20. Harmonic Distortion vs. Frequency

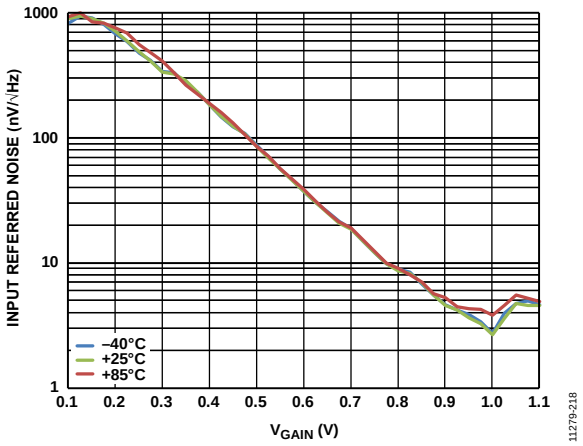

Figure 18. Input Referred Noise vs. V_{GAIN}

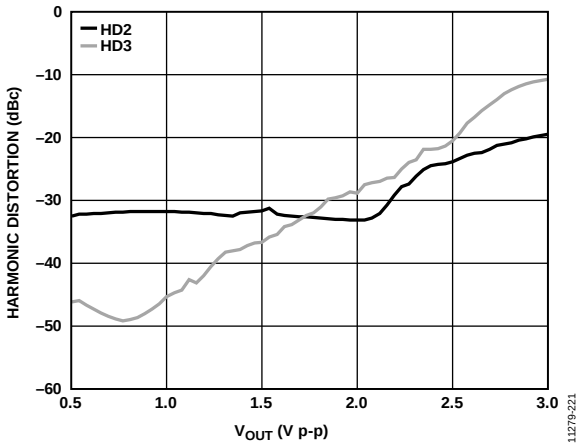

Figure 21. Harmonic Distortion vs. Output Amplitude

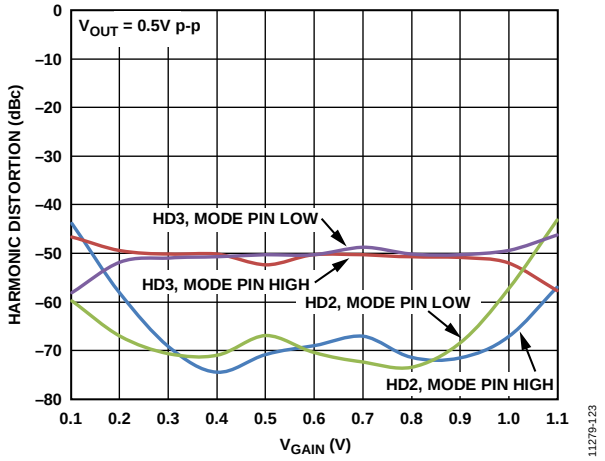

Figure 22. Harmonic Distortion vs. V_{GAIN}

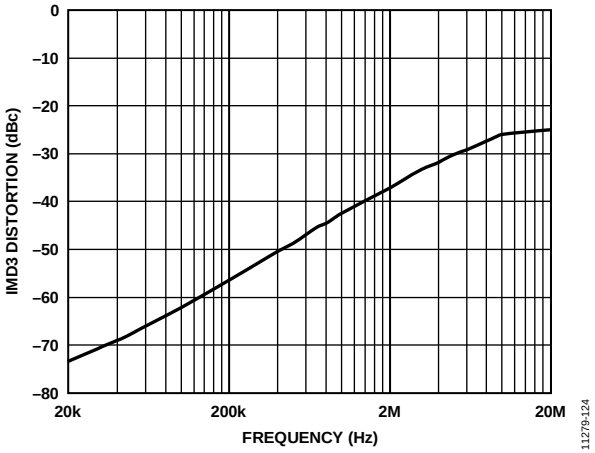

Figure 25. IMD3 Distortion vs. Frequency

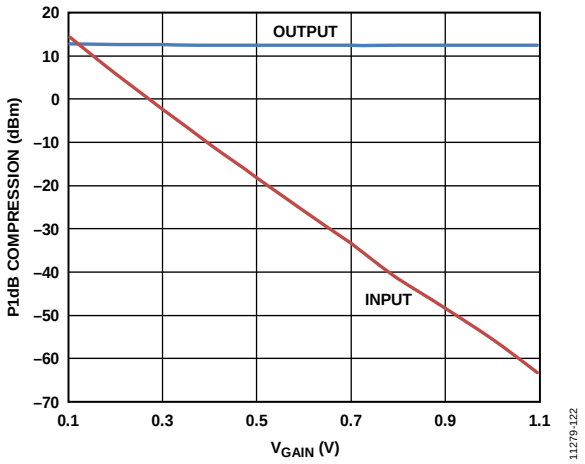

Figure 23. Input and Output 1 dB Compression vs. V_{GAIN}

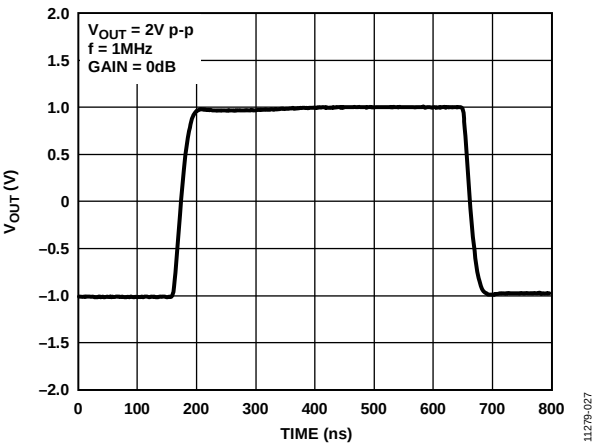

Figure 26. Large Signal Pulse Response vs. Time, V_{GAIN} = 0 V

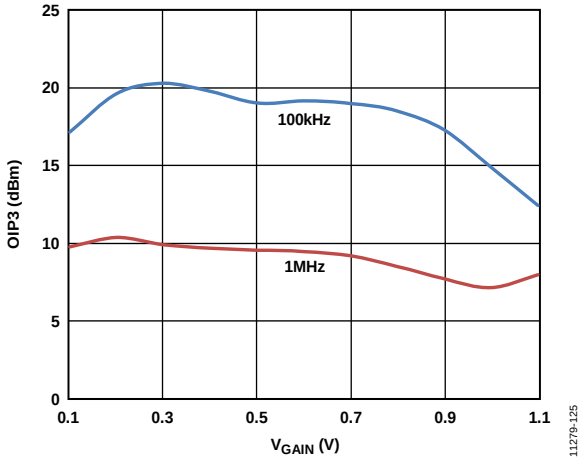

Figure 24. OIP3 vs. V_{GAIN}

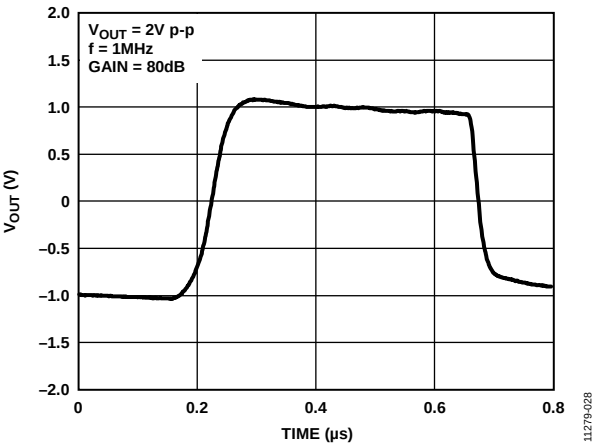

Figure 27. Large Signal Pulse Response vs. Time, V_{GAIN} = 1.0 V

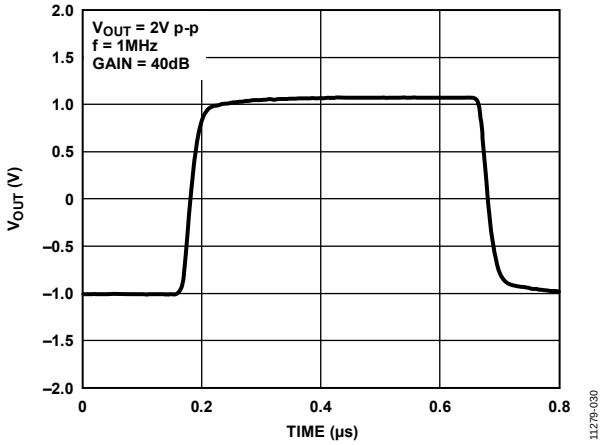

Figure 28. Large Signal Pulse Response vs. Time, V_{GAIN} = 0.6 V

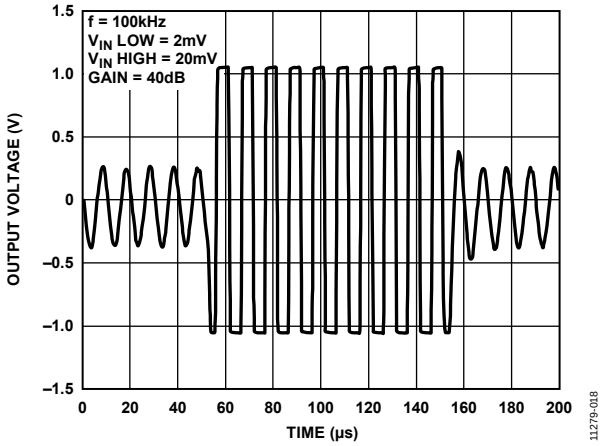

Figure 31. Overdrive Recovery vs. Time

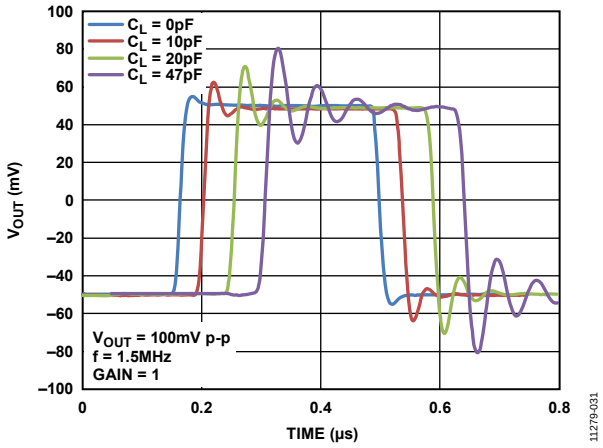

Figure 29. Small Signal Pulse Response vs. Time for Varying Capacitive Loads

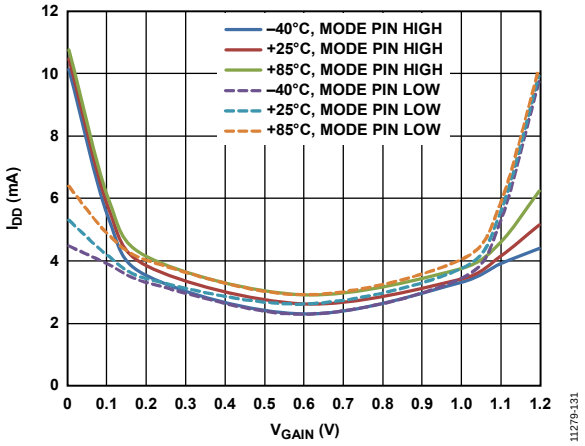

Figure 32. Supply Current vs. V_{GAIN}

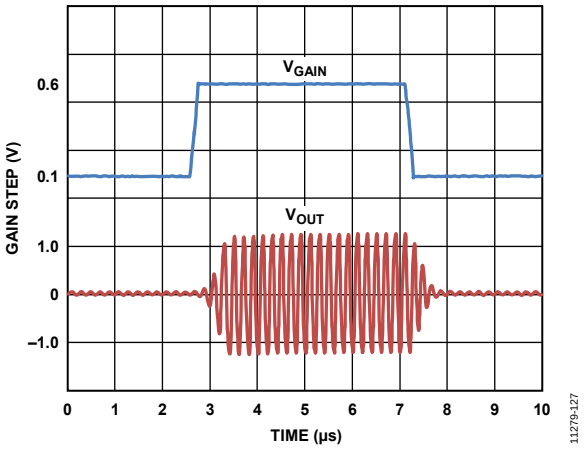

Figure 30. Gain Step Response vs. Time

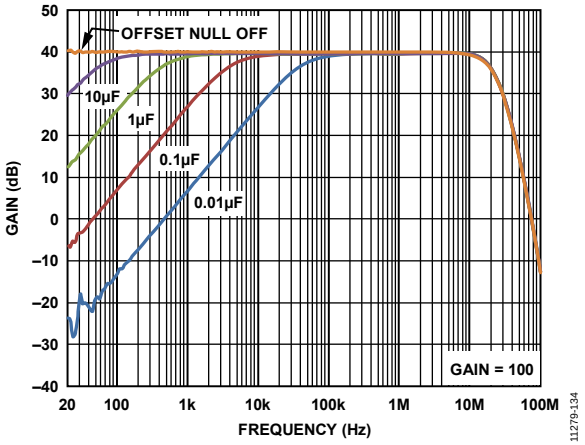

Figure 33. Offset Null Bandwidth vs. Offset Null Capacitor

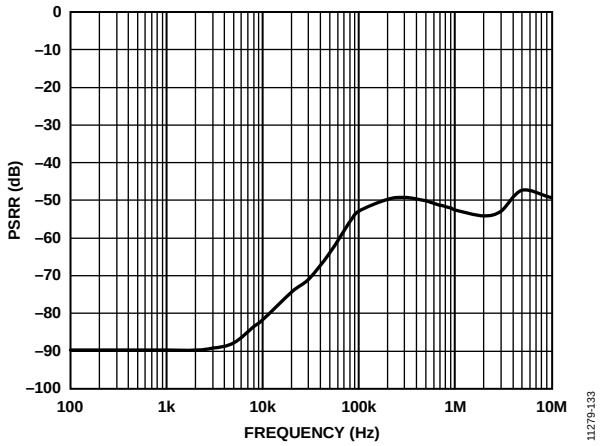

Figure 34. Power Supply Rejection Ratio (PSRR) vs. Frequency

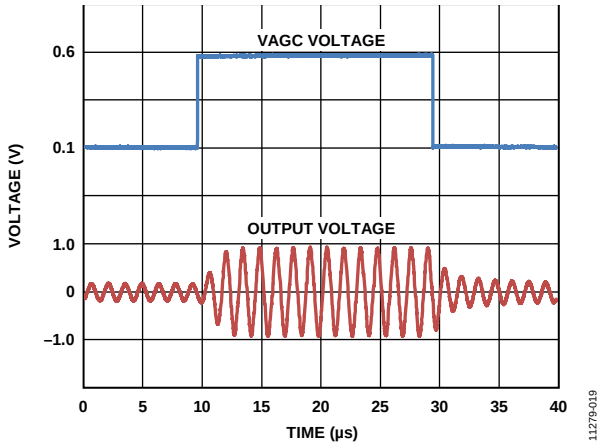

Figure 35. AGC Response vs. Time, No Load, Input 100 mV Differential

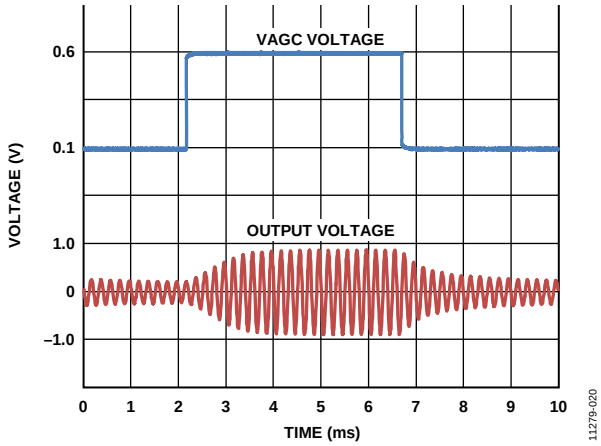

Figure 36. AGC Response vs. Time, C_L = 0.01 µF, Input 100 mV Differential

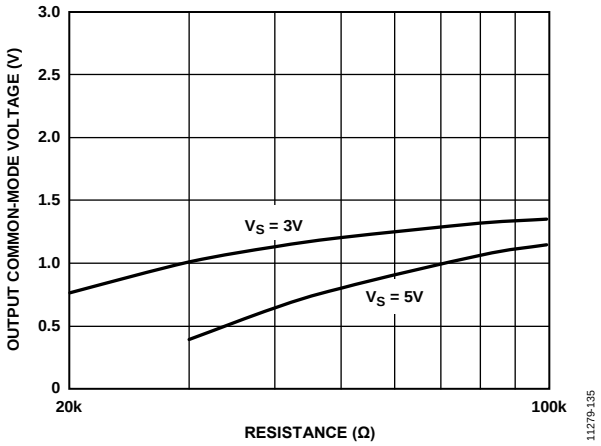

Figure 37. Output Common-Mode Voltage vs. Common-Mode Resistance (R_{CM}) to VBAT

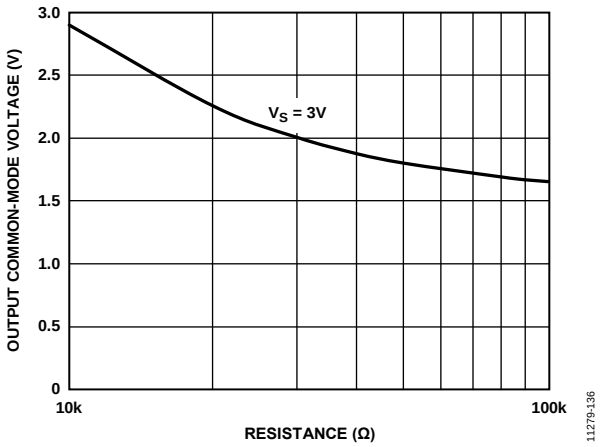

Figure 38. Output Common-Mode Voltage vs. R_{CM} to COMM

THEORY OF OPERATION

INTRODUCTION

The AD8338 is a single-supply variable gain amplifier (VGA) with an adjustable gain range of 80 dB. The AD8338 is an input variable gain amplifier (IVGA) that accepts a wide range of input amplitudes, and via its variable gain, compresses it to either a narrow range of output amplitudes or a constant output amplitude (for example, automatic gain control applications). Like other VGAs from Analog Devices, Inc., the AD8338 possesses a constant bandwidth over the entire gain range. Therefore, with a bandwidth of 18 MHz, the AD8338 achieves a gain-bandwidth product of 180 GHz at its highest gain setting (gain of 80 dB). Additionally, the differential output of the AD8338 allows the VGA to directly drive differential input ADCs without the need of a single-ended-to-differential converter.

OVERALL STRUCTURE OF THE AD8338

Figure 39 shows a block schematic of the AD8338 depicting the key sections of the VGA and a general overview of its features. The AD8338 signal path is comprised of the 500 Ω input resistors, the VGA core, and the transimpedance output amplifiers. The gain of the signal path is adjusted by the linear-in-dB gain interface and the voltage at Pin GAIN with respect to its local ground, Pin COMM. The automatic gain control (AGC) circuit block is a current output rms detector that can be used to drive the GAIN pin and configure the AD8338 as an AGC amplifier with constant rms output amplitude. This output amplitude is adjusted by the voltage at Pin VAGC with respect to the voltage at Pin VREF. The offset null circuit block allows the AD8338 to auto-zero any dc offset voltages. To enable the offset null functionality, connect a capacitor between the OFSN and VREF pins. To disable the offset null functionality, connect Pin OFSN to ground. The INPD, INMD, FBKP, and FBKM pins provide access to internal nodes in the VGA core of the AD8338 and output amplifiers, allowing the user to adjust the gain range, output common-mode voltage, and bandwidth of the device.

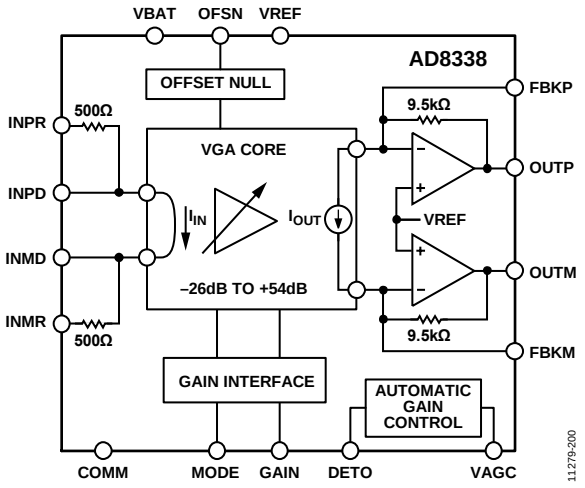

Figure 39. Block Schematic

VGA CORE

Figure 40 shows a simplified diagram of the VGA core at the heart of the AD8338. The key concepts regarding the operation of this VGA core are as follows. First, the ratio of the collector currents in the two differential pairs (Q1, Q2 and Q3, Q4) is identical given that the two differential pairs share the same base drive. This ratio is represented by the modulation factor, x, where values of x range from −1 to +1. Second, the input current signal is forced into the collectors of the input differential pair (Q1, Q2) by the loop amplifier to modulate the fixed tail current, I_D, and to set the modulation factor, x. The value of x in the input differential pair is replicated to the output differential pair (Q3, Q4) to modulate its fixed tail current, I_N, and to generate a differential output current. Third, the current gain of this cell is exactly $G = I_N/I_D$ over many decades of variable bias current.

By varying I_N, the overall function of the cell is that of a two-quadrant analog multiplier, exhibiting a linear relationship to both the signal modulation factor, x, and this numerator current. By varying I_D, the overall function is that of a two-quadrant analog divider, having a hyperbolic gain function with respect to the modulation factor, x, controlled by this denominator current. Because the AD8338 is an input VGA, it controls I_D to adjust the gain of the amplifier. However, because a hyperbolic gain function is generally of less value than one in which the decibel gain is a linear function of a control input, the AD8338 includes a special interface to provide either increasing or decreasing exponential control of I_D.

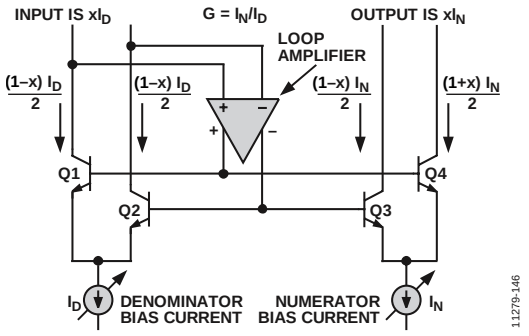

Figure 40. Simplified Diagram of the VGA Core

NORMAL OPERATING CONDITIONS

Normal operating conditions for the AD8338 are defined as follows:

- The input pins, INPR and INMR, are voltage driven (the source impedance is assumed to be zero).
- The output pins, OUTP and OUTM, are open circuited (the load impedance is assumed to be infinite).
- Pin COMM is grounded.
- Pin MODE is either tied to a logic high or left unconnected, to set the noninverted gain slope gain mode.

INPR, INMR, INPD, and INMD Pins

The input signal to the AD8338 is accepted at the INPR/INMR and the INPD/INMD differential input ports. These pins are internally biased to approximately 1.5 V, the voltage at the reference pin, VREF. The INPR and INMR pins are voltage input pins (see Figure 41) where the differential input voltage and the internal input resistors generate current, I_{IN}, the input current for the VGA core. While the voltage inputs can be driven in either a single-sided or a differential manner, operation using a differential drive is preferable and is assumed in all specifications, unless otherwise stated. The pin-to-pin input resistance between the voltage inputs is specified as 1000 Ω ± 20%. In most cases, the voltage input pins are ac-coupled via two capacitors chosen to provide adequate low frequency transmission. This results in the minimum input noise that increases when a common-mode voltage other than 1.5 V is forced onto these input pins. The short-circuit (INPR shorted to INMR) input-referred noise at maximum gain is approximately 4.5 nV/√Hz.

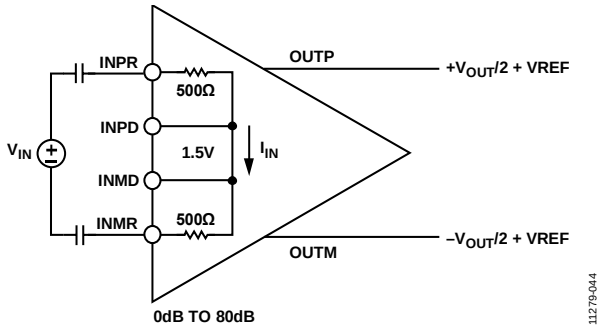

Figure 41. Input Voltage Applied to the INPR and INMR Pins

The INPD and INMD pins are current input pins (see Figure 42) where the differential input current is directly applied to the VGA core input. This input current can either be generated with an external current source like an unbiased photodiode, or with a voltage source and external coupling resistors (see Figure 43). The latter method allows the gain range of the AD8338 to be shifted as explained in the Explanation of the Gain Function section. When using the INPD and INMD inputs, the INPR and INMR pins must be shorted to one another to prevent stability issues.

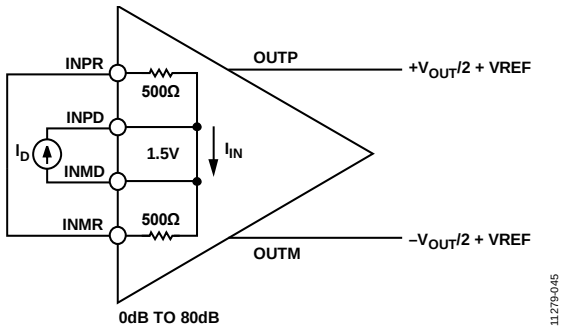

Figure 42. Input Current Applied to the INPD and INMD Pins

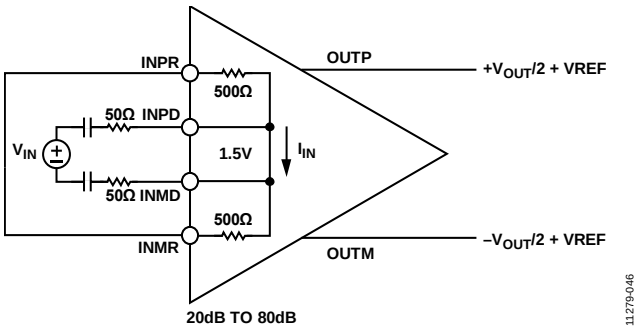

Figure 43. Using External Resistors at the INPD and INMD Pins

FBKP, FBKM, OUTP, and OUTM Pins

Output voltage pins, OUTP and OUTM, have a default common-mode voltage of 1.5 V, the voltage at the VREF reference pin. This output common-mode voltage can be adjusted by injecting common-mode currents into Pin FBKP and Pin FBKM, the summing nodes of the output amplifiers, which are also biased at 1.5 V. The output amplifiers of the AD8338 possess rail-to-rail output stages, which allow the output common mode of the VGA to be shifted from ground to the positive supply, though the use of such extreme values leaves only a small range for the differential output signal swing.

Adding feedback capacitors, C_{FBK}, across nodes (OUTP, FBKP and OUTM, FBKM) reduces the bandwidth of the output amplifiers of the AD8338 and the signal path of the VGA. These capacitors and the feedback resistors of the output amplifiers form a low-pass filter with a cut-off frequency of approximately

$$f_C = \frac{1}{2\pi \times R_{FBK} \times C_{FBK}} \quad (1)$$

where R_{FBK} are the internal feedback resistors of the output amplifiers; R_{FBK} is specified as 9,500 Ω ± 20%.

Reducing the bandwidth of the AD8338 minimizes output noise and simplifies the design of the antialiasing filter when using the VGA to drive an ADC.

Linear-in-dB Gain Control, GAIN Pin

To facilitate the use of an 80 dB gain range, the AD8338 has a linear-in-dB gain control. The gain is controlled by the voltage at Pin GAIN with respect to the local ground, COMM. In normal operating conditions, adjusting the voltage at Pin GAIN from 0.1 V to 1.1 V adjusts the gain from its lowest value of 0 dB to its highest value of 80 dB. The basic gain equation is

$$G(\text{dB}) = \frac{V_{GAIN}}{12.5\ \text{mV}} - 8\ \text{dB} \quad (2)$$

where V_{GAIN} is in volts.

Alternatively, the gain equation can be expressed as a numerical gain magnitude:

$$G_N = 0.398 \times 10^{\frac{V_{GAIN}}{250\ \text{mV}}} \quad (3)$$

where V_{GAIN} is in volts.

Inversion of the Gain Slope, MODE Pin

Pin MODE controls the polarity of the gain adjustment. That is, Pin MODE allows the slope of the gain function to be inverted. If Pin MODE is tied to VBAT, the gain of the AD8338 increases exponentially (or linear-in-dB) with an increase in the voltage at Pin GAIN. If Pin MODE is tied to COMM, the gain of the AD8338 decreases exponentially (or linear-in-dB) with an increase in the voltage at Pin GAIN. Figure 44 shows the two gain control modes when the AD8338 is configured in normal operating conditions.

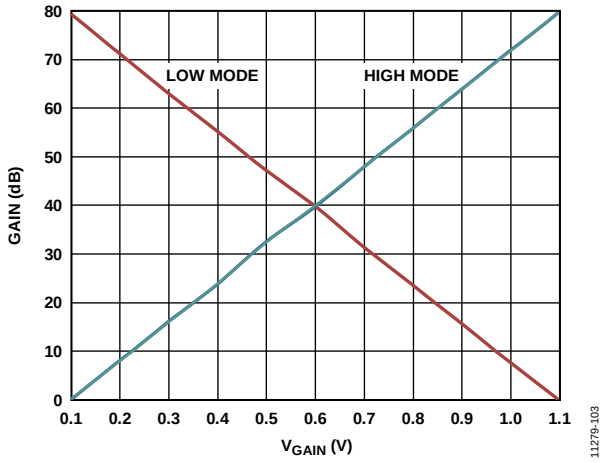

Figure 44. Two Gain Control Modes of the AD8338

Offset Correction Circuit, OFSN Pin

The AD8338 includes an internal offset correction circuit that cancels out any dc offsets present in the VGA. Connecting a capacitor, C_{OFSN}, between Pin OFSN and Pin VREF enables the offset correction circuit.

The offset correction circuit uses an internal auto-zero feedback loop, which introduces small signal, high-pass filter characteristics to the signal path. The −3 dB corner frequency is

$$f_{OFSN} = \frac{1}{2\pi \times 400\ \Omega \times C_{OFSN}} \quad (4)$$

Although the AD8338 exhibits a high-pass filter characteristic in its transfer function when the offset correction circuit is enabled, do not rely on the device as a high-pass filter. This is due to the narrow voltage range of dc input voltages that the circuit can reject. If signals at frequencies below the band of interest need to be rejected, for best performance, incorporate a high-pass filter preceding the AD8338 by ac coupling the inputs, as shown in Figure 41.

To provide a dc-coupled signal path, the offset correction circuit can be disabled by connecting Pin OFSN to Pin COMM. Exercise caution when operating the AD8338 with the offset correction circuit disabled, because at large gains, dc offsets cause large dc errors at the outputs of the VGA.

AGC Circuit, VAGC Pin

The AD8338 includes a current output rms detector that can be used to configure the AD8338 as an AGC amplifier (see Figure 46).

In this configuration, the AGC circuit compares the rms output amplitude of the VGA with the desired rms output amplitude (the voltage at Pin VAGC with respect to the voltage at Pin VREF), and drives Pin GAIN to minimize their difference. Therefore, in steady state conditions, the circuit forces the rms output amplitude of the AD8338 to be the voltage at Pin VAGC with respect to the voltage at Pin VREF. Because the AGC circuit uses negative feedback, the gain slope of the AD8338 needs to be set by connecting Pin MODE to ground.

The AGC attack time, or the time it takes for the AGC to respond to a change at the input, is set by the value of C_{DETO}. This time is approximately

$$T\ (\text{sec}) = 17{,}450\ \Omega \times (285\ \text{pF} + C_{DETO}) \quad (5)$$

Without C_{DETO}, the AGC response time is approximately 5 µs. With a 0.1 µF capacitor, the AGC response time is approximately 1.75 ms.

When using the AGC loop, the output voltage is set against an rms target, defined by the applied voltage at the VAGC pin. The output reflects the rms value of the absolute value difference between VAGC and VREF. The designer must be aware that for values of (VAGC − VREF) larger than 0.6 V, output limiting begins to greatly distort the signal.

$$V_{OUT\_RMS} = |V_{AGC} - V_{REF}| \quad (6)$$

$$V_{OUT\_RMS} = |V_{AGC} - 1.5| \quad (7)$$

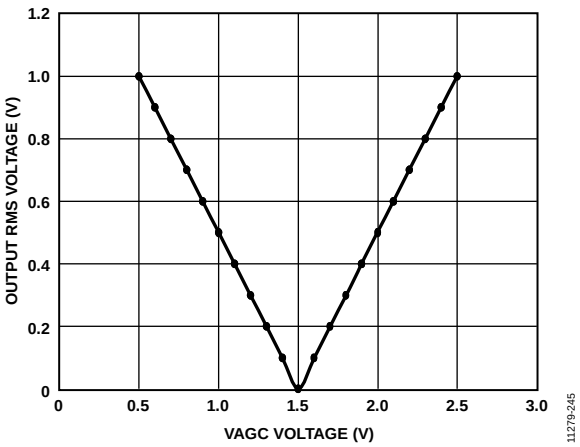

Figure 45. Output RMS Voltage vs. VAGC

Not all applications require the AGC circuit. Therefore, the AGC circuit can be disabled by connecting Pin DETO to ground, and connecting Pin VAGC to Pin VREF.

Internal Reference, Pin VREF

The AD8338 includes an internal 1.5 V voltage reference that is used to set the quiescent bias voltages of many key nodes in the VGA. These nodes include inputs pins (INPR, INMR, INPD, and INMD), output pins (OUTP and OUTM), and feedback pins (FBKP and FBKM). The output voltage of the internal reference, Pin VREF, can be bypassed with a 0.1 µF capacitor to Pin COMM; however, do not force VREF externally.

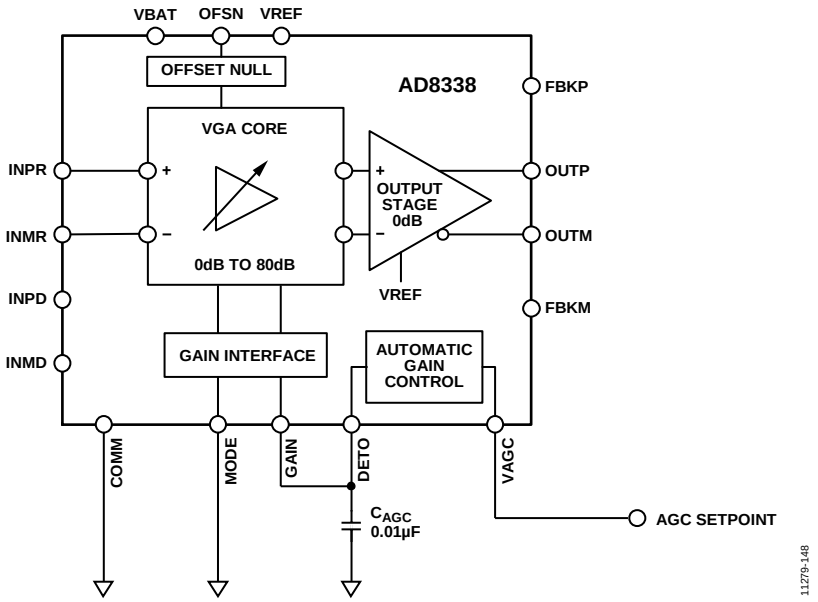

Figure 46. AD8338 Configured as an AGC Amplifier

EXPLANATION OF THE GAIN FUNCTION

The signal chain of the AD8338 can be broken down into three stages. The first stage is a differential, voltage to current converter comprised of the input resistors, R_P and R_N, of the VGA. These input resistors can either be the internal 500 Ω resistors coupled to Pin INPR and Pin INMR, or external resistors coupled to Pin INPD and Pin INMD. The transresistance of the voltage to current converter is $R_P + R_N$, such that the current flowing in the resistors is given by

$$I_{IN} = \frac{V_{INPx} - V_{INMx}}{R_P + R_N} \quad (8)$$

The current in the input resistors, I_{IN}, is fed to the second stage of the AD8338, the VGA core. The VGA core is a fully differential variable gain current amplifier with a gain range of 80 dB. In the noninverting gain slope setting (Pin MODE connected to Pin VBAT), the current gain of the VGA core spans from −26 dB (V_{GAIN} = 0.1 V) to +54 dB (V_{GAIN} = 1.1 V). In numerical gain magnitude, the gain of the VGA core is given by

$$I_{OUT\_VGA} = I_{IN} \times 10^{(80\,V_{GAIN} - 34)/20} \approx I_{IN} \times 0.02 \times 10^{\frac{V_{GAIN}}{250\text{ mV}}} \quad (9)$$

The differential output current of the VGA core is fed to the third stage of the AD8338, a fully differential, current to voltage converter comprised of the output amplifiers and their corresponding feedback resistors, R_{FBK} (9.5 kΩ). The overall transimpedance of the current to voltage converter is $2R_{FBK}$, such that the differential output voltage of the stage is given by

$$V_{OUT\_DIFF} = I_{OUT,VGA} \times 2 \times R_{FBK} \quad (10)$$

Therefore, the overall voltage gain of the AD8338 is

$$G(\text{dB}) = 80 \times (V_{GAIN}) + 20 \times \log\left(\frac{2 \times R_{FBK}}{R_P + R_N}\right) - 34 \quad (11)$$

Alternatively, the gain equation can be expressed as a numerical gain magnitude:

$$G_N = 0.02 \times \frac{2 \times R_{FBK}}{R_P + R_N} \times 10^{\frac{V_{GAIN}}{250\text{ mV}}} \quad (12)$$

Equation 11 and Equation 12 show that the gain range of the AD8338 can be shifted by using external input resistors, R_P and R_N. For example, driving the INPD and INMD pins with an R_P and R_N of 50 Ω shifts the gain range of the AD8338 up by 20 dB, to yield a range of 20 dB to 100 dB (see Figure 43). Similarly, driving the INPD and INMD pins with an R_P and R_N of 5 kΩ shifts the gain range down by 20 dB, to yield a range of −20 dB to +60 dB.

As shown in Figure 43, when using external resistors to drive the INPD and INMD pins, short the INPR and INMR pins to one another to prevent stability issues.

Effects of Using External Resistors

When the gain range is shifted through the use of external resistors, several trade-offs must be considered. External resistors connected to Pin INPD and Pin INMD load the current inputs of the VGA core, changing the dynamic behavior of the block and the −3 dB bandwidth of the AD8338. The −3 dB bandwidth of the AD8338 with external resistors is

$$f_{CL} = 18\text{ MHz} \times \left(\frac{500\,\Omega \times R_{EXT}}{500\,\Omega + R_{EXT}}\right) \times \frac{1}{500\,\Omega} \quad (13)$$

For example, with 50 Ω external resistors, the input-referred noise at maximum gain decreases to approximately 1 nV/√Hz, and the gain range shifts up by 20 dB. However, the −3 dB bandwidth is reduced from 18 MHz to approximately 1.8 MHz.

ADJUSTING THE OUTPUT COMMON-MODE VOLTAGE

The output common-mode voltage of the AD8338 differential outputs is nominally set to 1.5 V, the voltage at Pin VREF. This output common-mode voltage can be adjusted by connecting a resistor from each of the summing nodes of the output amplifier (Pin FBKP and Pin FBKM) to either Pin COMM or Pin VBAT. Connecting a resistor from Pin FBKP and Pin FBKM to Pin VBAT decreases the output common-mode voltage, whereas connecting a resistor from Pin FBKP and Pin FBKM to Pin COMM increases the output common-mode voltage (see Figure 47 and Figure 48).

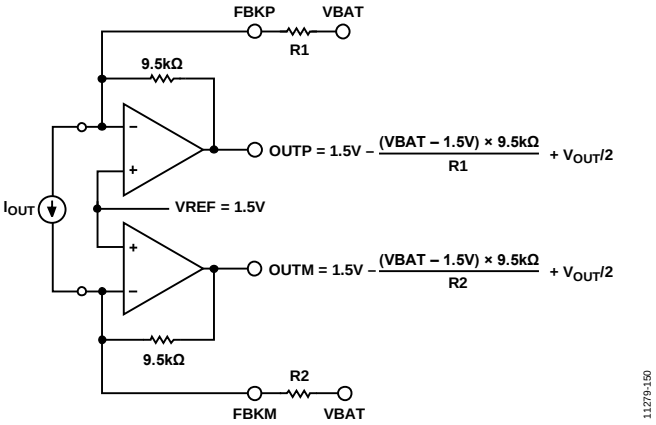

Figure 47. Decreasing the Output Common-Mode Voltage

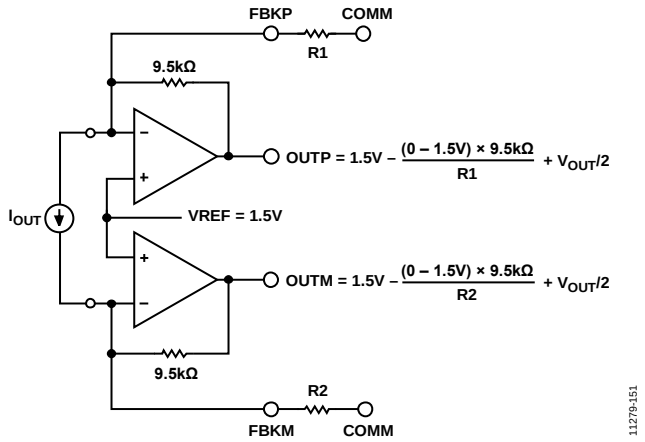

Figure 48. Increasing the Output Common-Mode Voltage

Table 5 and Table 6 show suggested values for the external resistors shown in Figure 47 and Figure 48, respectively.

Table 5. Resistor Values for Decreasing the Output Common-Mode Voltage

VBAT (V)	Target V_{OCM} (V)	Resistor Value (Ω)	Tied to
5.0	0.9	55,417	VBAT
3.3	0.9	28,500	VBAT
3.0	0.9	23,750	VBAT

Table 6. Resistor Values for Increasing the Output Common-Mode Voltage

VBAT (V)	Target V_{OCM} (V)	Resistor Value (Ω)	Tied to
Any	1.8	47,500	COMM
Any	2.0	28,500	COMM
Any	2.5	14,250	COMM

APPLICATIONS INFORMATION

The excellent performance of the AD8338 results in a flat response over various gains with rail-to-rail output signal swing, high drive capability, and a very high dynamic range at a low 20 mW of quiescent power at maximum gain. These features make the AD8338 an exceptional choice for use in battery-operated equipment, low frequency and baseband applications, and many other applications.

SIMPLE ON-OFF KEYED (OOK) RECEIVER

For low complexity, low power data communications, a simple link built using a modulating carrier tone in an on-off state provides a fast and cost-effective solution to the designer. Such designs are used in a variety of applications, including near-field communications among noninterference mechanical systems, low data rate sensors, RFID tags, and so on.

The schematic shown in Figure 49 demonstrates a complete inductive telemetry on-off keyed (OOK) front end. The crystal is cut for the target receive frequency of interest, creating a very narrow-band filter, typically around the 6.78 MHz ISM band.

The AD8338 amplifies the signal (the gain is set by an external controller) and drives a full-wave rectifier bridge. The output of this bridge is then low-pass filtered into 100 Ω terminations. This design provides excellent rejection of RF and excellent baseband information recovery for the decision stage that follows.

The reactive filter components (Capacitor C1 through Capacitor C4, Inductor L1, and Inductor L2) set the baseband recovery performance. A design trade-off exchanges baseband response for RF attenuation.

Table 7 provides typical values for these components at two data rates. Note that Capacitor C1 through Capacitor C4 are all of equal value, and Inductor L2 has the same value as Inductor L1.

Table 7. Typical Values for Components in Reactive Filter

Data Rate	C1 to C4	L1 and L2	Carrier Attenuation (f = 6.78 MHz)
19,200 bps	12 nF	240 µH	−101 dB
57,600 bps	3.9 nF	82 µH	−73 dB

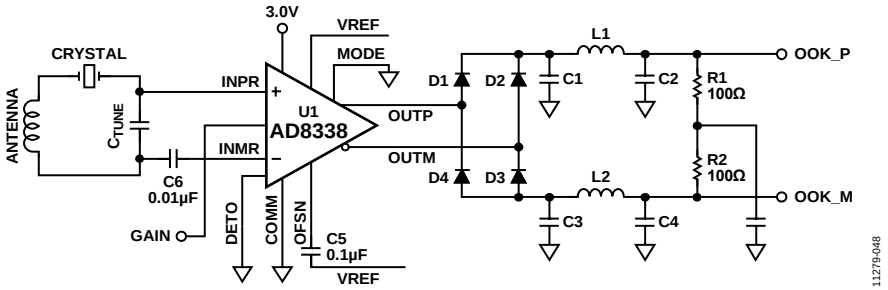

Figure 49. Complete, Low Power OOK Receiver

OUTLINE DIMENSIONS

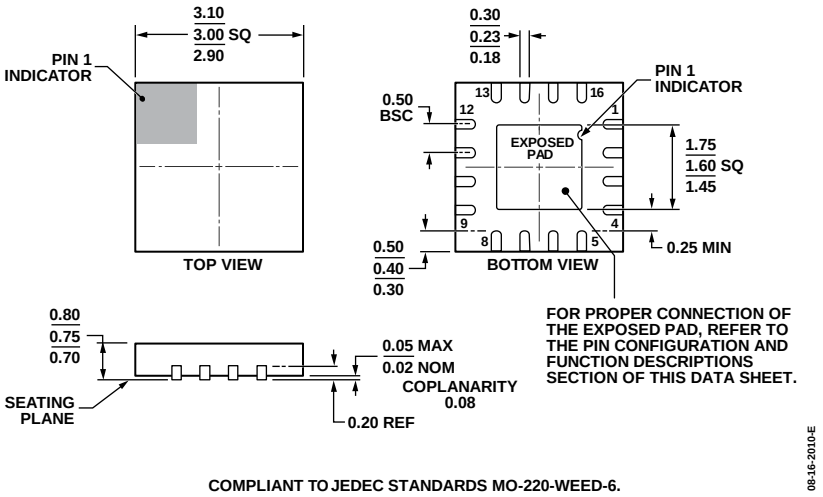

Figure 50. 16-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
3 mm × 3 mm Body, Very Very Thin Quad
(CP-16-22)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Branding
AD8338ACPZ-R7	−40°C to +85°C	16-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-16-22	Y4K
AD8338ACPZ-RL	−40°C to +85°C	16-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-16-22	Y4K
AD8338-EVALZ		AD8338 Evaluation Board		

[1] Z = RoHS Compliant Part.