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SPECIFICATIONS

V_{CC} = 2.7 V to 3.6 V, V_{REF} = 2.5 V internal or external, f_{DCLK} = 2 MHz; T_A = −40°C to +85°C, unless otherwise noted.

Table 1.

Parameter	AD7873A[1]	AD7873B[1]	Unit	Test Conditions/Comments
DC ACCURACY				
Resolution	12	12	Bits	
No Missing Codes	11	12	Bits min	
Integral Nonlinearity[2]	±2	± 1	LSB max	
Differential Nonlinearity[2]		−0.9/+1.5	LSB max	
Offset Error[2]	±6	±6	LSB max	$+V_{CC}$ = 2.7 V
Gain Error[2]	±4	±4	LSB max	External reference
Noise	70	70	µV rms typ	
Power Supply Rejection	70	70	dB typ	
SWITCH DRIVERS				
On Resistance[2]				
Y+, X+	5	5	Ω typ	
Y–, X–	6	6	Ω typ	
ANALOG INPUT				
Input Voltage Ranges	0 to V_{REF}	0 to V_{REF}	V	
DC Leakage Current	±0.1	±0.1	µA typ	
Input Capacitance	37	37	pF typ	
REFERENCE INPUT/OUTPUT				
Internal Reference Voltage	2.45/2.55	2.45/2.55	V min/max	
Internal Reference Tempco	±15	±15	ppm/°C typ	
V_{REF} Input Voltage Range	1/V_{CC}	1/V_{CC}	V min/max	
DC Leakage Current	±1	± 1	µA max	
V_{REF} Input Impedance	1	1	GΩ typ	$\overline{CS}$ = GND or $+V_{CC}$; typically 260 Ω when the on-board reference is enabled
TEMPERATURE MEASUREMENT				
Temperature Range	−40/+85	−40/+85	°C min/max	
Resolution				
Differential Method[3]	1.6	1.6	°C typ	
Single Conversion Method[4]	0.3	0.3	°C typ	
Accuracy				
Differential Method[3]	±2	±2	°C typ	
Single Conversion Method[4]	±2	±2	°C typ	
BATTERY MONITOR				
Input Voltage Range	0/6	0/6	V min/max	
Input Impedance	10	10	kΩ typ	Sampling; 1 GΩ when battery monitor is off
Accuracy	±2.5	±2	% max	External reference
	±3	±3	% max	Internal reference
LOGIC INPUTS				
Input High Voltage, V_{INH}	2.4	2.4	V min	
Input Low Voltage, V_{INL}	0.4	0.4	V max	
Input Current, I_{IN}	±1	±1	µA max	Typically 10 nA, V_{IN} = 0 V or $+V_{CC}$
Input Capacitance, C_{IN}[5]	10	10	pF max	

Parameter	AD7873A[1]	AD7873B[1]	Unit	Test Conditions/Comments
LOGIC OUTPUTS				
Output High Voltage, V_{OH}	V_{CC} – 0.2	V_{CC} – 0.2	V min	I_{SOURCE} = 250 µA; V_{CC} = 2.2 V to 5.25 V
Output Low Voltage, V_{OL}	0.4	0.4	V max	I_{SINK} = 250 µA
$\overline{PENIRQ}$ Output Low Voltage, V_{OL}	0.4	0.4	V max	100 kΩ pull-up; I_{SINK} = 250 µA
Floating-State Leakage Current	±10	±10	µA max	
Floating-State Output Capacitance[5]	10	10	pF max	
Output Coding	Straight (Natural) Binary			
CONVERSION RATE				
Conversion Time	12	12	DCLK cycles max	
Track-and-Hold Acquisition Time	3	3	DCLK cycles min	
Throughput Rate	125	125	kSPS max	
POWER REQUIREMENTS				
+V_{CC} (Specified Performance)	2.7/3.6	2.7/3.6	V min/max	Functional from 2.2 V to 5.25 V
I_{CC}[6]				Digital I/Ps = 0 V or V_{CC}
Normal Mode (f_{SAMPLE} = 125 kSPS)	380	380	µA max	Internal reference off, V_{CC} = 3.6 V, 240 µA typ
	670	670	µA typ	Internal reference on, V_{CC} = 3.6 V
Normal Mode (f_{SAMPLE} = 12.5 kSPS)	170	170	µA typ	Internal reference off, V_{CC} = 2.7 V, f_{DCLK} = 200 kHz
Normal Mode (Static)	150	150	µA typ	Internal reference off, V_{CC} = 3.6 V
	580	580	µA typ	Internal reference on, V_{CC} = 3.6 V
Shutdown Mode (Static)	1	1	µA max	200 nA typ
Power Dissipation[6]				
Normal Mode (f_{SAMPLE} = 125 kSPS)	1.368	1.368	mW max	Internal reference off, V_{CC} = 3.6 V
	2.412	2.412	mW typ	Internal reference on, V_{CC} = 3.6 V
Shutdown	3.6	3.6	µW max	V_{CC} = 3.6 V

[1] Temperature range as follows: A, B Versions: –40°C to +85°C.
[2] See the Terminology section.
[3] Difference between TEMP0 and TEMP1 measurement. No calibration necessary.
[4] Temperature drift is –2.1 mV/°C.
[5] Sample tested @ 25°C to ensure compliance.
[6] See the Power vs. Throughput Rate section.

TIMING SPECIFICATIONS

$T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted; V_{CC} = 2.7 V to 5.25 V, V_{REF} = 2.5 V.

Table 2. Timing Specifications[1]

Parameter	Limit at T_{MIN}, T_{MAX}	Unit	Description
f_{DCLK}[2]	10	kHz min	
	2	MHz max	
t_{ACQ}	1.5	µs min	Acquisition time
t_1	10	ns min	$\overline{CS}$ falling edge to first DCLK rising edge
t_2	60	ns max	$\overline{CS}$ falling edge to busy three-state disabled
t_3[3]	60	ns max	$\overline{CS}$ falling edge to DOUT three-state disabled
t_4	200	ns min	DCLK high pulse width
t_5	200	ns min	DCLK low pulse width
t_6	60	ns max	DCLK falling edge to BUSY rising edge
t_7	10	ns min	Data setup time prior to DCLK rising edge
t_8	10	ns min	Data valid to DCLK hold time
t_9[3]	200	ns max	Data access time after DCLK falling edge
t_{10}	0	ns min	$\overline{CS}$ rising edge to DCLK ignored
t_{11}	100	ns max	$\overline{CS}$ rising edge to BUSY high impedance
t_{12}[4]	100	ns max	$\overline{CS}$ rising edge to DOUT high impedance

[1] Sample tested at 25°C to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of V_{CC}) and timed from a voltage level of 1.6 V.
[2] Mark/space ratio for the DCLK input is 40/60 to 60/40.
[3] Measured with the load circuit of Figure 2 and defined as the time required for the output to cross 0.4 V or 2.0 V.
[4] t_{12} is derived from the measured time taken by the data outputs to change 0.5 V when loaded with the circuit of Figure 2. The measured number is then extrapolated back to remove the effects of charging or discharging the 50 pF capacitor. This means that the time, t_{12}, quoted in the timing characteristics is the true bus relinquish time of the part and is independent of the bus loading.

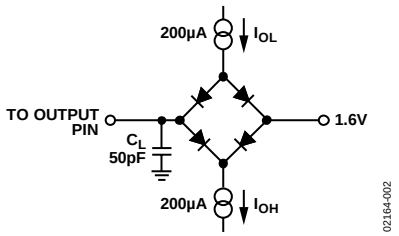


Figure 2. Load Circuit for Digital Output Timing Specifications

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
$+V_{CC}$ to GND	–0.3 V to +7 V
Analog Input Voltage to GND	–0.3 V to V_{CC} + 0.3 V
Digital Input Voltage to GND	–0.3 V to V_{CC} + 0.3 V
Digital Output Voltage to GND	–0.3 V to V_{CC} + 0.3 V
V_{REF} to GND	–0.3 V to V_{CC} + 0.3 V
Input Current to Any Pin Except Supplies[1]	±10 mA
Operating Temperature Range	
Commercial (A, B Versions)	–40°C to +85°C
Storage Temperature Range	–65°C to +150°C
Junction Temperature	150°C
Power Dissipation	450 mW
IR Reflow Soldering	
Peak Temperature	220°C (±5°C)
Time-to-Peak Temperature	10 sec to 30 sec
Ramp-Down Rate	6°C/sec max
Pb-free Parts Only	
Peak Temperature	250°C
Time-to-Peak Temperature	20 sec to 40 sec
Ramp-Up Rate	3°C/sec max
Ramp-Down Rate	6°C/sec max

[1] Transient currents of up to 100 mA do not cause SCR latch-up.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

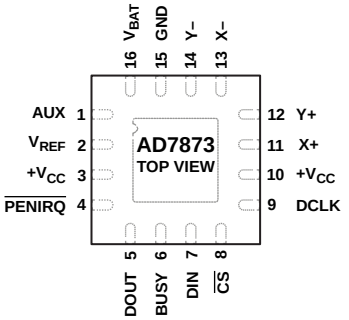
Table 4. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
16-Lead QSOP	149.97	38.8	°C/W
16-Lead TSSOP	150.4	27.6	°C/W
16-Lead LFCSP	135.7		°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS



NOTES
1. THE EXPOSED PAD IS NOT CONNECTED INTERNALLY. FOR INCREASED RELIABILITY OF THE SOLDER JOINTS AND MAXIMUM THERMAL CAPABILITY, IT IS RECOMMENDED THAT THE PAD BE SOLDERED TO GROUND PLANE.

Figure 3. LFCSP Pin Configuration

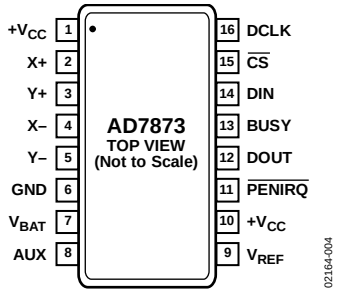


Figure 4. QSOP/TSSOP Pin Configuration

Table 5. Pin Function Descriptions

Pin No.			
LFCSP	**QSOP/ TSSOP**	**Mnemonic**	**Description**
3, 10	1, 10	$+V_{CC}$	Power Supply Input. The $+V_{CC}$ range for the AD7873 is from 2.2 V to 5.25 V. Both $+V_{CC}$ pins should be connected directly together.
11	2	X+	X+ Position Input. ADC Input Channel 1.
12	3	Y+	Y+ Position Input. ADC Input Channel 2.
13	4	X–	X– Position Input.
14	5	Y–	Y– Position Input. ADC Input Channel 3.
15	6	GND	Analog Ground. Ground reference point for all circuitry on the AD7873. All analog input signals and any external reference signals should be referred to this GND voltage.
16	7	V_{BAT}	Battery Monitor Input. ADC Input Channel 4.
1	8	AUX	Auxiliary Input. ADC Input Channel 5.
2	9	V_{REF}	Reference Output for the AD7873. Alternatively, an external reference can be applied to this input. The voltage range for the external reference is 1.0 V to $+V_{CC}$. For specified performance, it is 2.5 V on the AD7873. The internal 2.5 V reference is available on this pin for use external to the device. The reference output must be buffered before it is applied elsewhere in a system. A 0.1 µF capacitor is recommended between this pin and GND to reduce system noise effects.
4	11	$\overline{\text{PENIRQ}}$	Pen Interrupt. CMOS logic open-drain output (requires 10 kΩ to 100 kΩ pull-up resistor externally).
5	12	DOUT	Data Out. Logic output. The conversion result from the AD7873 is provided on this output as a serial data stream. The bits are clocked out on the falling edge of the DCLK input. This output is high impedance when $\overline{CS}$ is high.
6	13	BUSY	BUSY Output. Logic output. This output is high impedance when $\overline{CS}$ is high.
7	14	DIN	Data In. Logic Input. Data to be written to the AD7873 control register is provided on this input and is clocked into the register on the rising edge of DCLK (see the Control Register section).
8	15	$\overline{CS}$	Chip Select Input. Active low logic input. This input provides the dual function of initiating conversions on the AD7873 and enabling the serial input/output register.
9	16	DCLK	External Clock Input. Logic input. DCLK provides the serial clock for accessing data from the part. This clock input is also used as the clock source for the AD7873 conversion process.
	N/A[1]	EPAD	Exposed Pad. The exposed pad is not connected internally. For increased reliability of the solder joints and maximum thermal capability, it is recommended that the pad be soldered to the ground plane.

[1] N/A = not applicable.

TERMINOLOGY

Integral Nonlinearity
Integral nonlinearity is the maximum deviation from a straight line passing through the endpoints of the ADC transfer function. The endpoints of the transfer function are zero scale, a point 1 LSB below the first code transition, and full scale, a point 1 LSB above the last code transition.

Differential Nonlinearity
Differential nonlinearity is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Offset Error
Offset error is the deviation of the first code transition (00…000) to (00…001) from the ideal, that is, AGND + 1 LSB.

Gain Error
Gain error is the deviation of the last code transition (111…110) to (111…111) from the ideal (that is, V_{REF} – 1 LSB) after the offset error is adjusted out.

Track-and-Hold Acquisition Time
The track-and-hold amplifier enters the acquisition phase on the fifth falling edge of DCLK after the start bit has been detected. Three DCLK cycles are allowed for the track-and-hold acquisition time. The input signal is fully acquired to the 12-bit level within this time even with the maximum specified DCLK frequency. See the Analog Input section for more details.

On Resistance
On resistance is a measure of the ohmic resistance between the drain and source of the switch drivers.

TYPICAL PERFORMANCE CHARACTERISTICS

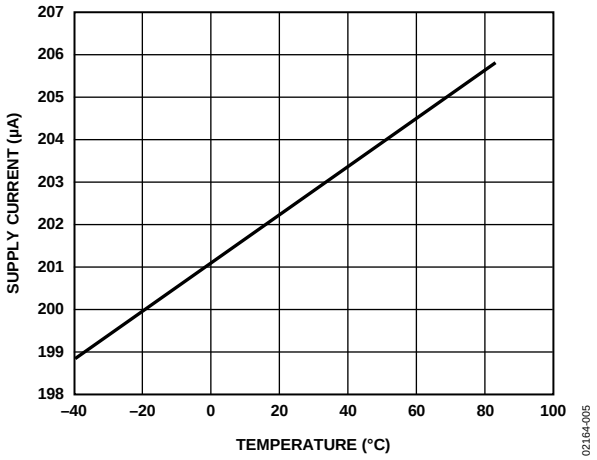


Figure 5. Supply Current vs. Temperature

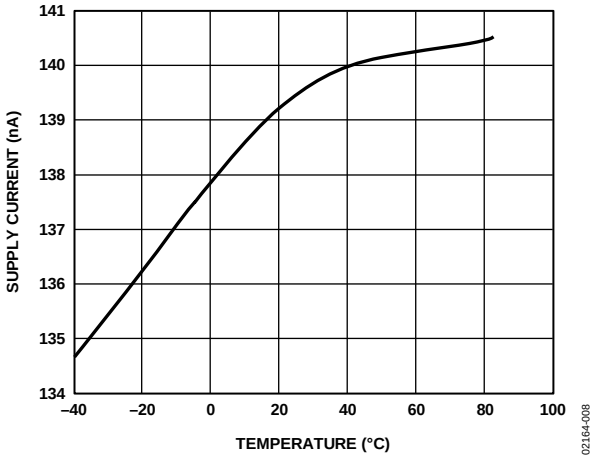


Figure 8. Power-Down Supply Current vs. Temperature

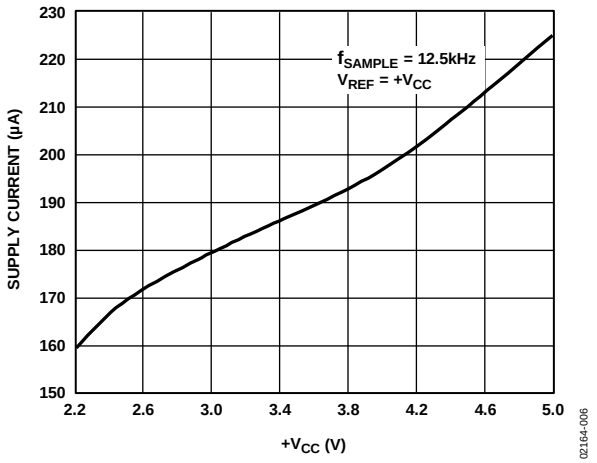


Figure 6. Supply Current vs. $+V_{CC}$

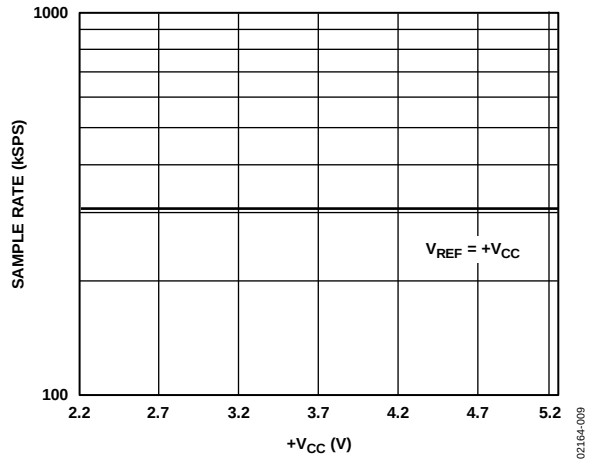


Figure 9. Maximum Sample Rate vs. $+V_{CC}$

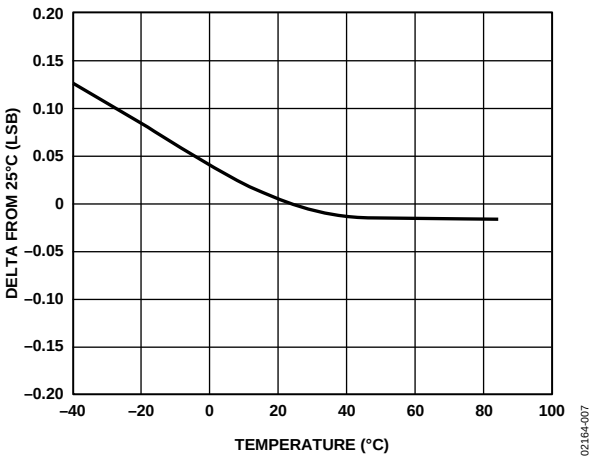


Figure 7. Change in Gain vs. Temperature

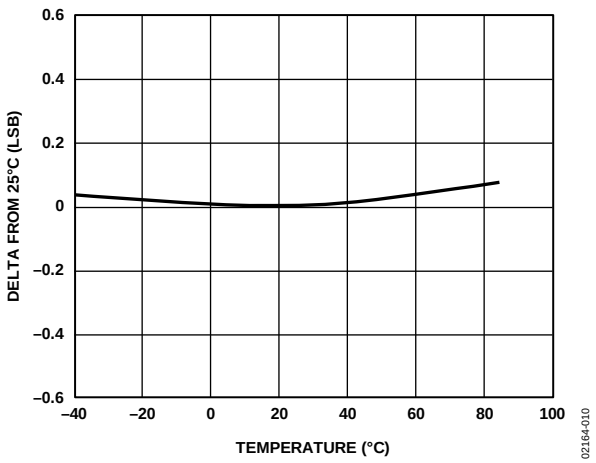


Figure 10. Change in Offset vs. Temperature

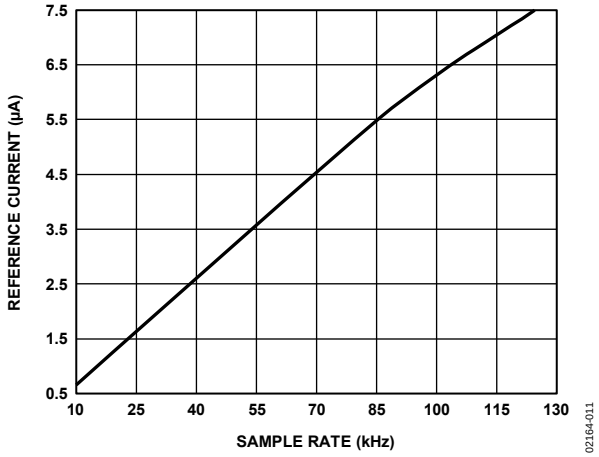


Figure 11. Reference Current vs. Sample Rate

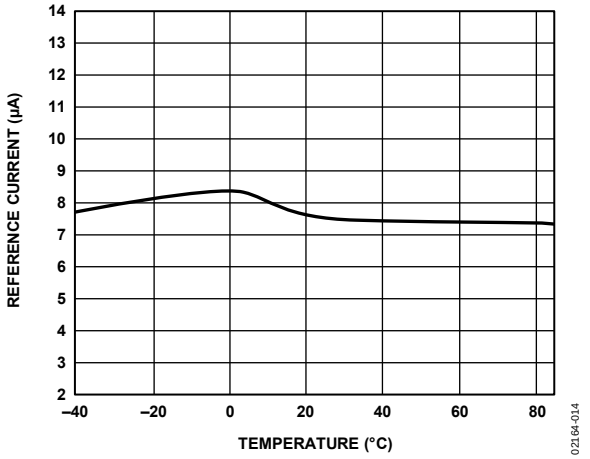


Figure 14. Reference Current vs. Temperature

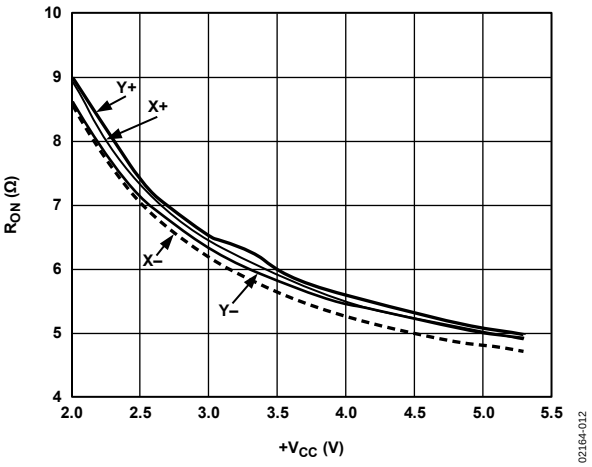


Figure 12. Switch On Resistance vs. $+V_{CC}$
(X+, Y+: $+V_{CC}$ to Pin; X–, Y–: Pin to GND)

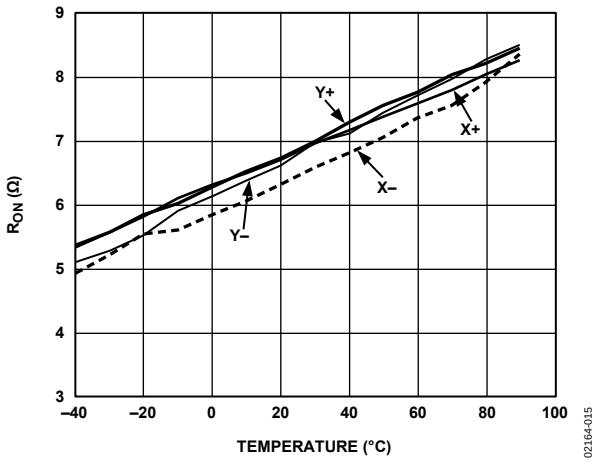


Figure 15. Switch On Resistance vs. Temperature
(X+, Y+: +VCC to Pin; X–, Y–: Pin to GND)

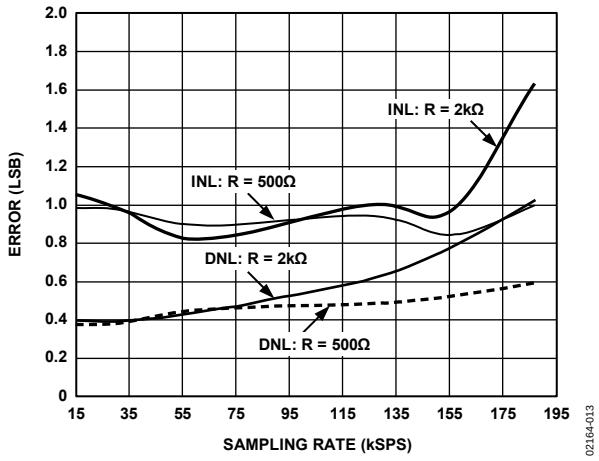


Figure 13. Linearity Error vs. Sampling Rate for Various R_{IN}

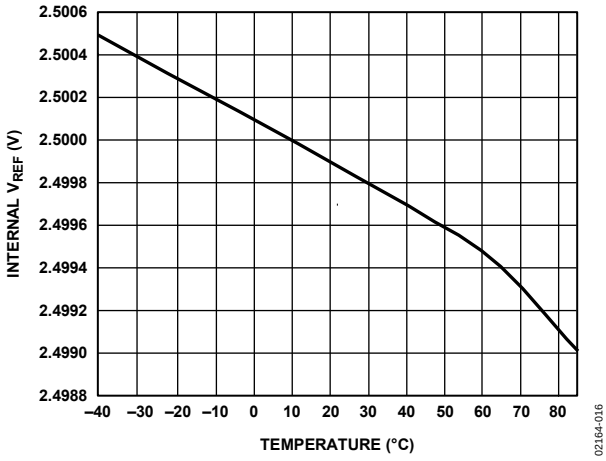


Figure 16. Internal V_{REF} vs. Temperature

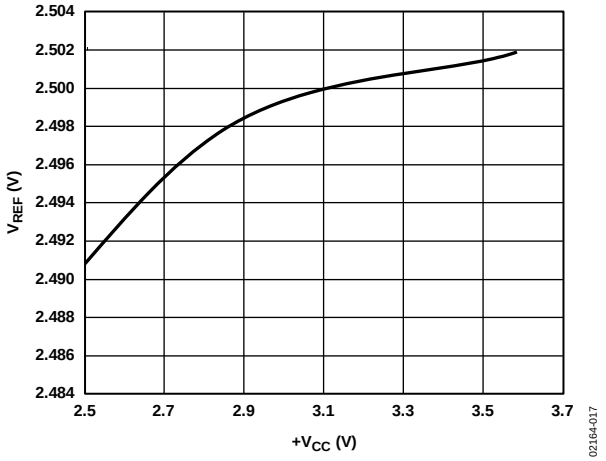


Figure 17. Internal V_{REF} vs. $+V_{CC}$

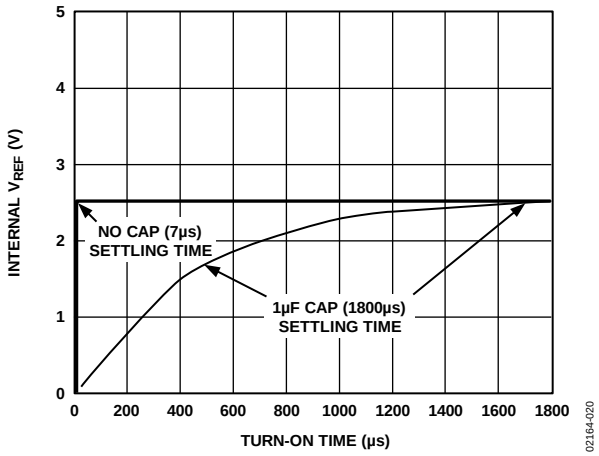


Figure 20. Internal V_{REF} vs. Turn-on Time

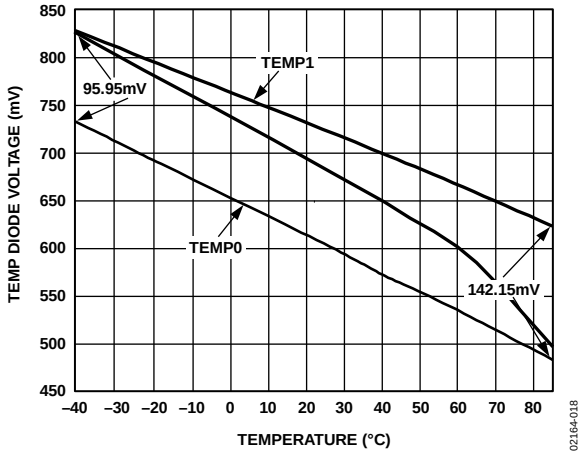


Figure 18. Temp Diode Voltage vs. Temperature (2.7 V Supply)

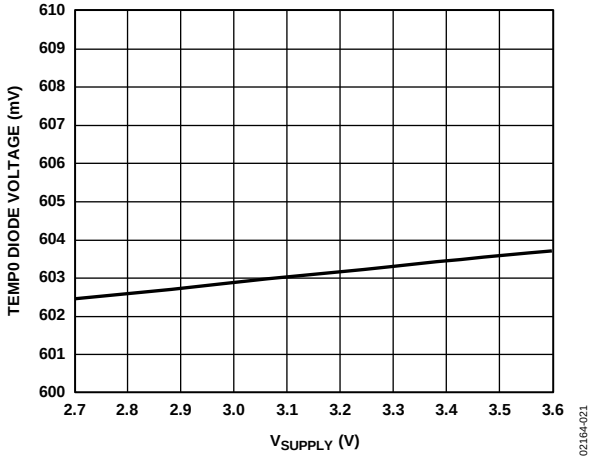


Figure 21. TEMP0 Diode Voltage vs. V_{SUPPLY} (25°C)

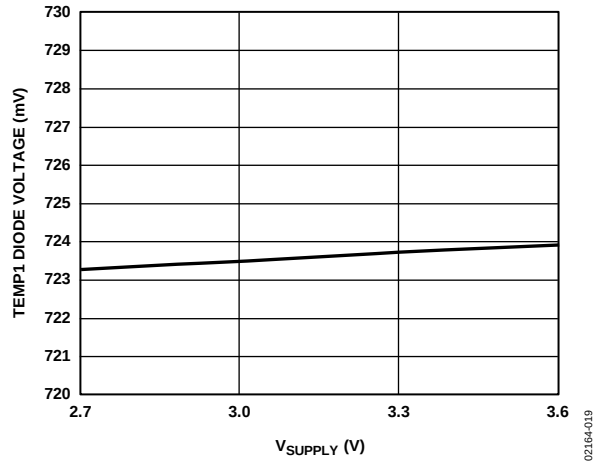


Figure 19. TEMP1 Diode Voltage vs. V_{SUPPLY} (25°C)

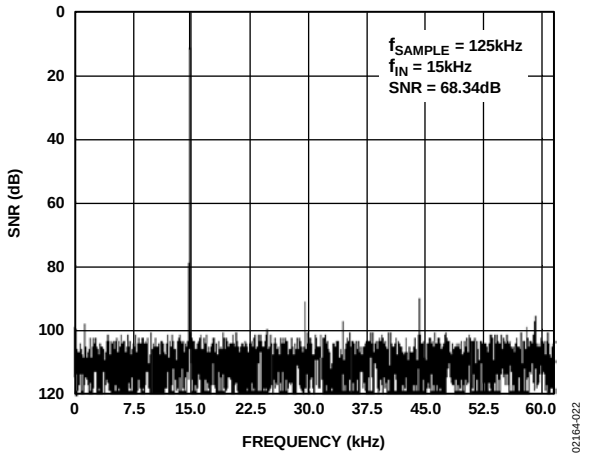


Figure 22. Auxiliary Channel Dynamic Performance (f_{SAMPLE} = 125 kHz, f_{INPUT} = 15 kHz)

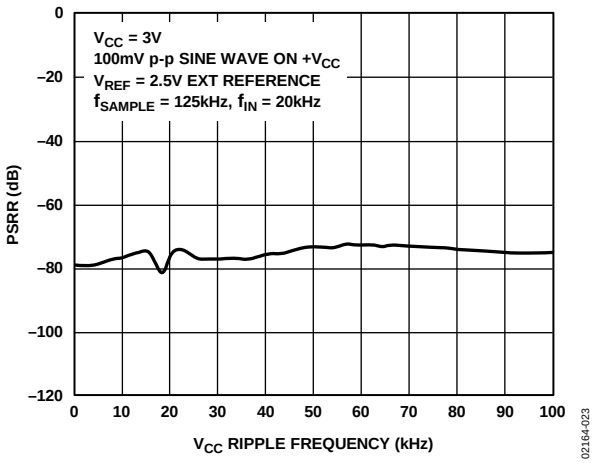


Figure 23. AC PSRR vs. Supply Ripple Frequency

Figure 23 shows the power supply rejection ratio vs. V_{DD} supply frequency for the AD7873. The power supply rejection ratio is defined as the ratio of the power in the ADC output at full-scale frequency, f, to the power of a 100 mV sine wave applied to the ADC V_{CC} supply of frequency f_S

$$PSSR \text{ (dB)} = 10\log(Pf/Pf_s)$$

where:

Pf is power at frequency, f, in ADC output.
Pf_s is power at frequency, f_s, coupled onto the ADC V_{CC} supply.

Here a 100 mV p-p sine wave is coupled onto the V_{CC} supply. Decoupling capacitors of 10 µF and 0.1 µF were used on the supply.

CIRCUIT INFORMATION

The AD7873 is a fast, low power, 12-bit, single-supply analog-to-digital converter (ADC). The AD7873 can be operated from a 2.2 V to 5.25 V supply. When operated from either a 5 V supply or a 3 V supply, the AD7873 is capable of throughput rates of 125 kSPS when provided with a 2 MHz clock.

The AD7873 provides the user with on-chip track-and-hold, multiplexer, ADC, reference, temperature sensor, and serial interface, housed in a tiny 16-lead QSOP, TSSOP, or LFCSP package, offering the user considerable space-saving advantages over alternative solutions. The serial clock input (DCLK) accesses data from the part and also provides the clock source for the successive approximation ADC. The analog input range is 0 V to V_{REF} (where the externally applied V_{REF} can be between 1 V and $+V_{CC}$). The AD7873 has a 2.5 V reference on-board with this reference voltage available for use externally if buffered.

The analog input to the ADC is provided via an on-chip multiplexer. This analog input can be any one of the X, Y, and Z panel coordinates, the battery voltage, or the chip temperature. The multiplexer is configured with low resistance switches that allow an unselected ADC input channel to provide power and an accompanying pin to provide ground for an external device. For some measurements, the on resistance of the switches could present a source of error. However, with a differential input to the converter and a differential reference architecture, this error can be negated.

ADC TRANSFER FUNCTION

The output coding of the AD7873 is straight binary. The designed code transitions occur at successive integer LSB values (that is, 1 LSB, 2 LSBs, and so on). The LSB size is $V_{REF}/4096$. The ideal transfer characteristic for the AD7873 is shown in Figure 24.

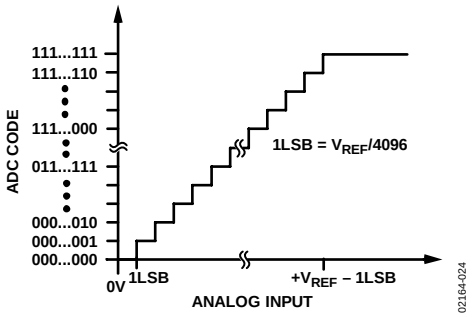


Figure 24. Transfer Characteristic

TYPICAL CONNECTION DIAGRAM

Figure 25 shows a typical connection diagram for the AD7873 in a touch screen control application. The AD7873 features an internal reference, but this can be overdriven with an external low impedance source between 1 V and $+V_{CC}$. The value of the reference voltage sets the input range of the converter. The conversion result is output MSB first, followed by the remaining 11 bits and three trailing zeros, depending on the number of clocks used per conversion (see the Serial Interface section). For applications where power consumption is a concern, the power management option should be used to improve power performance. See Table 8 for available power management options.

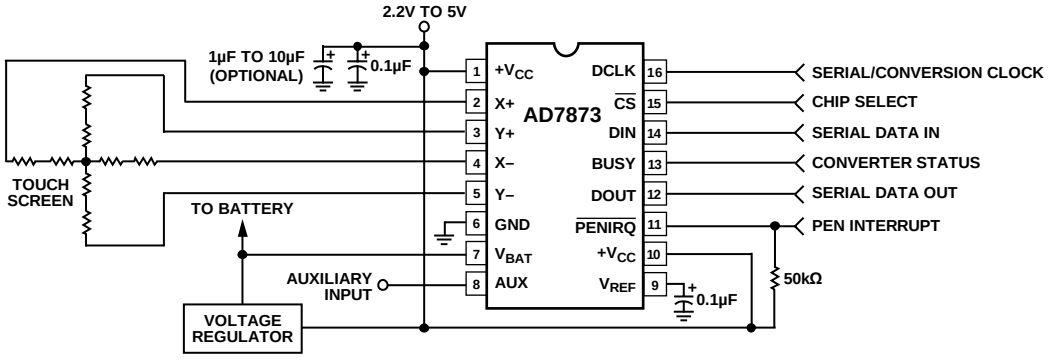


Figure 25. Typical Application Circuit

ANALOG INPUT

Figure 26 shows an equivalent circuit of the analog input structure of the AD7873 that contains a block diagram of the input multiplexer, the differential input of the ADC, and the differential reference.

Table 6 shows the multiplexer address corresponding to each analog input, both for the SER/$\overline{\text{DFR}}$ bit in the control register set high and low. The control bits are provided serially to the device via the DIN pin. For more information on the control register, see the Control Register section.

When the converter enters hold mode, the voltage difference between the +IN and –IN inputs (see Figure 26) is captured on the internal capacitor array. The input current on the analog inputs depends on the conversion rate of the device. During the sample period, the source must charge the internal sampling capacitor (typically 37 pF). Once the capacitor is fully charged, there is no further input current. The rate of charge transfer from the analog source to the converter is a function of conversion rate.

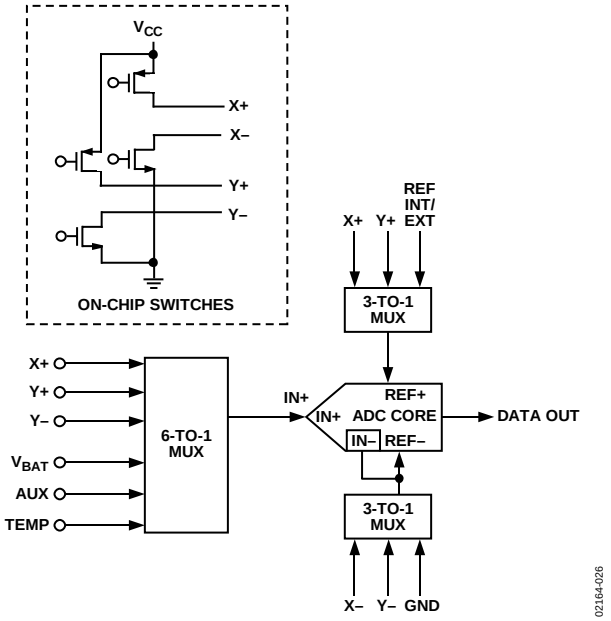


Figure 26. Equivalent Analog Input Circuit

Table 6. Analog Input, Reference, and Touch Screen Control

A2	A1	A0	SER/ $\overline{\text{DFR}}$	Analog Input	X Switches	Y Switches	+REF[1]	–REF[1]
0	0	0	1	TEMP0	Off	Off	V_{REF}	GND
0	0	1	1	X+	Off	On	V_{REF}	GND
0	1	0	1	VBAT	Off	Off	V_{REF}	GND
0	1	1	1	X+ (Z1)	X+ Off X– On	Y+ On Y– Off	V_{REF}	GND
1	0	0	1	Y– (Z2)	X+ Off X– On	Y+ On Y– Off	V_{REF}	GND
1	0	1	1	Y+	On	Off	V_{REF}	GND
1	1	0	1	AUX	Off	Off	V_{REF}	GND
1	1	1	1	TEMP1	Off	Off	V_{REF}	GND
0	0	0	0	**Invalid Address. Test Mode: Switches out the TEMP0 diode to the $\overline{\text{PENIRQ}}$ pin.**				
0	0	1	0	X+	Off	On	Y+	Y–
0	1	0	0	**Invalid Address**				
0	1	1	0	X+ (Z1)	X+ Off X– On	Y+ On Y– Off	Y+	X–
1	0	0	0	Y– (Z2)	X+ Off X– On	Y+ On Y– Off	Y+	X–
1	0	1	0	Y+	ON	Off	X+	X–
1	1	0	0	**Outputs Identity Code, 1000 0000 0000.**				
1	1	1	0	**Invalid address. Test mode: Switches out the TEMP1 diode to the $\overline{\text{PENIRQ}}$ pin.**				

[1] Internal node, not directly accessible by the user.

Acquisition Time

The track-and-hold amplifier enters tracking mode on the falling edge of the fifth DCLK after the start bit is detected (see Figure 35). The time required for the track-and-hold amplifier to acquire an input signal depends on how quickly the 37 pF input capacitance is charged. With zero source impedance on the analog input, three DCLK cycles are always sufficient to acquire the signal to the 12-bit level. With a source impedance (R_{IN}) on the analog input, the actual acquisition time required is calculated using the formula:

$$t_{ACQ} = 8.4 \times (R_{IN} + 100\ \Omega) \times 37\ \text{pF}$$

where R_{IN} is the source impedance of the input signal, and 100 Ω, 37 pF is the input RC. Depending on the frequency of DCLK used, three DCLK cycles may or may not be sufficient to acquire the analog input signal with various source impedance values.

Touch Screen Settling

In some applications, external capacitors could be required across the touch screen to filter noise associated with it, for example, noise generated by the LCD panel or backlight circuitry. The value of these capacitors causes a settling time requirement when the panel is touched. The settling time typically appears as a gain error. There are several methods for minimizing or eliminating this issue. The problem can be that the input signal, reference, or both, have not settled to their final value before the sampling instant of the ADC. Additionally, the reference voltage could still be changing during the conversion cycle. One option is to stop or slow down the DCLK for the required touch screen settling time. This allows the input and reference to stabilize for the acquisition time, resolving the issue for both single-ended and differential modes.

The other option is to operate the AD7873 in differential mode only for the touch screen, and program the AD7873 to keep the touch screen drivers on and not go into power-down (PD0 = PD1 = 1). Several conversions could be required, depending on the settling time required and the AD7873 data rate. Once the required number of conversions have been made, the AD7873 can then be placed in a power-down state on the last measurement. The last method is to use the 15-DCLK cycle mode, maintaining the touch screen drivers on until it is commanded by the processor to stop.

Internal Reference

The AD7873 has an internal reference voltage of 2.5 V. The internal reference is available on the V_{REF} pin for external use in the system; however, it must be buffered before it is applied elsewhere. The on-chip reference can be turned on or off with the power-down address, PD1 = 1 (see Table 8 and Figure 27). Typically, the reference voltage is only used in single-ended mode for battery monitoring, temperature measurement, and for using the auxiliary input. Optimal touch screen performance is achieved when using the differential mode. The power-up time of the 2.5 V reference is typically 10 µs without a load; however, a 0.1 µF capacitor on the V_{REF} pin is recommended for optimum performance because it affects the power-up time (see Figure 20).

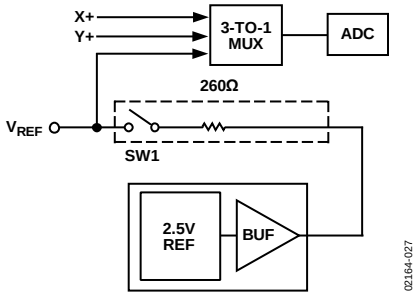


Figure 27. On-Chip Reference Circuitry

Reference Input

The voltage difference between +REF and −REF (see Figure 26) sets the analog input range. The AD7873 operates with a reference input in the range of 1 V to +V_{CC}. Figure 27 shows the on-chip reference circuitry on the AD7873. The internal reference on the AD7873 can be overdriven with an external reference; for best performance, however, the internal reference should be disabled when an external reference is applied, because SW1 in Figure 27 opens on the AD7873 when the internal reference is disabled. The on-chip reference always is available at the V_{REF} pin as long as the reference is enabled. The input impedance seen at the V_{REF} pin is approximately 260 Ω when the internal reference is enabled. When it is disabled, the input impedance seen at the V_{REF} pin is in the GΩ region.

When making touch screen measurements, conversions can be made in differential (ratiometric) mode or single-ended mode. If the SER/$\overline{\text{DFR}}$ bit is set to 1 in the control register, then a single-ended conversion is performed. Figure 28 shows the configuration for a single-ended Y coordinate measurement. The X+ input is connected to the analog-to-digital converter, the Y+ and Y− drivers are turned on, and the voltage on X+ is digitized. The conversion is performed with the ADC referenced from GND to V_{REF}. This V_{REF} is either the on-chip reference or the voltage applied at the V_{REF} pin externally, and is determined by the setting of the power management Bit PD0 and Bit PD1 (see Table 7). The advantage of this mode is that the switches that supply the external touch screen can be turned off once the acquisition is complete, resulting in a power savings. However, the on resistance of the Y drivers affects the input voltage that can be acquired. The full touch screen resistance could be in the order of 200 Ω to 900 Ω, depending on the manufacturer. Thus, if the on resistance of the switches is approximately 6 Ω, true full-scale and zero-scale voltages cannot be acquired, regardless of where the pen/stylus is on the touch screen. Note that the minimum touch screen resistance recommended for use with

the AD7873 is approximately 70 Ω. In this mode of operation, therefore, some voltage is likely to be lost across the internal switches, and it is unlikely that the internal switch resistance will track the resistance of the touch screen over temperature and supply, providing an additional source of error.

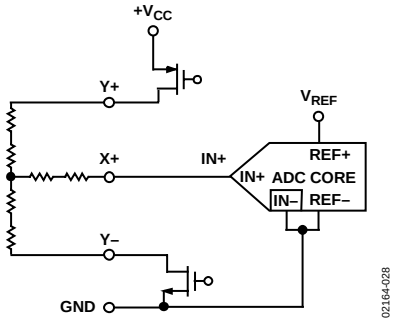


Figure 28. Single-Ended Reference Mode (SER/$\overline{DFR}$ = 1)

The alternative to this situation is to set the SER/$\overline{DFR}$ bit low. Again, making a Y coordinate measurement is considered, but now the +REF and –REF nodes of the ADC are connected directly to the Y+ and Y– pins. This means the analog-to-digital conversion is ratiometric. The result of the conversion is always a percentage of the external resistance, independent of how it could change with respect to the on resistance of the internal switches. Figure 29 shows the configuration for a ratiometric Y coordinate measurement.

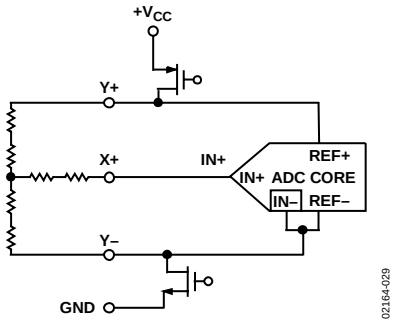


Figure 29. Differential Reference Mode (SER/$\overline{DFR}$ = 0)

The disadvantage of this mode of operation is that during both the acquisition phase and conversion process, the external touch screen must remain powered. This results in additional supply current for the duration of the conversion.

MEASUREMENTS

Temperature Measurement

Two temperature measurement options are available on the AD7873, the single conversion method and the differential conversion method. Both methods are based on an on-chip diode measurement.

In the single conversion method, a diode voltage is digitized and recorded at a fixed calibration temperature. Any subsequent polling of the diode provides an estimate of the ambient temperature through extrapolation from the calibration temperature diode result. This assumes a diode temperature drift of approximately –2.1 mV/°C. This method provides a resolution of approximately 0.3°C and a predicted accuracy of ±3°C.

The differential conversion method is a two-point measurement. The first measurement is performed with a fixed bias current into a diode, and the second measurement is performed with a fixed multiple of the bias current into the same diode. The voltage difference in the diode readings is proportional to absolute temperature and is given by the following formula:

$$\Delta V_{BE} = (kT / q) \times (\ln N)$$

where:

V_{BE} represents the diode voltage.
N is the bias current multiple.
k is Boltzmann's constant.
q is the electron charge.

This method provides more accurate absolute temperature measurement of ±2°C. However, the resolution is reduced to approximately 1.6°C. Assuming a current multiple of 105 (typical for the AD7873) taking Boltzmann's constant, k = 1.38054 ×10^{-23} electrons volts/degrees Kelvin, the electron charge q = 1.602189 × 10^{-19}, then T, the ambient temperature in degrees centigrade, can be calculated as follows:

$$\Delta V_{BE} = (kT / q) \times (\ln N)$$
$$T = (\Delta V_{BE} \times q) / (k \times \ln N)$$
$$T(°C) = 2.49 \times 10^{3} \times \Delta V_{BE} - 273\ K$$

where ΔV_{BE} is calculated from the difference in readings from the first conversion and second conversion.

Figure 30 shows a block diagram of the temperature measurement mode.

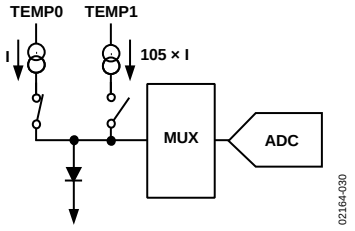


Figure 30. Block Diagram of Temperature Measurement Circuit

Battery Measurement

The AD7873 can monitor a battery voltage from 0 V to 6 V. Figure 31 shows a block diagram of a battery voltage monitored through the V_{BAT} pin. The voltage to the $+V_{CC}$ of the AD7873 is maintained at the desired supply voltage via the dc-to-dc regulator while the input to the regulator is monitored. This voltage on V_{BAT} is divided by 4 so that a 6 V battery voltage is presented to the ADC as 1.5 V. To conserve power, the divider is on only during the sampling of a voltage on V_{BAT}. Table 6 shows the control bit settings required to perform a battery measurement.

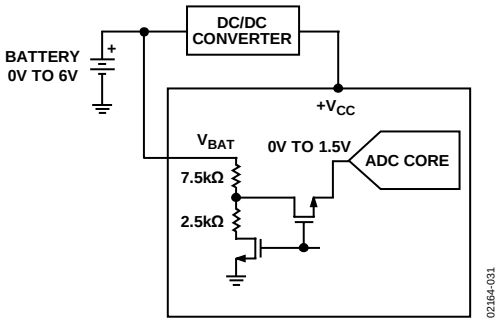


Figure 31. Block Diagram of Battery Measurement Circuit

Pressure Measurement

The pressure applied to the touch screen via a pen or finger can also be measured with the AD7873 with some simple calculations. The 8-bit resolution mode would be sufficient for this measurement, but the following calculations are shown with the 12-bit resolution mode. The contact resistance between the X and Y plates is measured, providing a good indication of the size of the depressed area and the applied pressure. The area of the spot touched is proportional to the size of the object touching it. The size of this resistance (R_{TOUCH}) can be calculated using two different methods.

The first method requires the user to know the total resistance of the X-plate tablet. Three touch screen conversions are required, a measurement of the X-position, Z_1-position, and Z_2-position (see Figure 32). The following equation calculates the touch resistance:

$$R_{TOUCH} = (R_{XPLATE}) \times (X_{POSITION} / 4095) \times [(Z_2 / Z_1) - 1]$$

The second method requires that the resistance of both the X-plate and Y-plate tablets are known. Again three touch screen conversions are required, a measurement of the X-position, Y-position, and Z_1-position (see Figure 32).

The following equation also calculates the touch resistance:

$$R_{TOUCH} = \{(R_{XPLATE} / Z_1) \times (X_{POSITION} / 4095) \times [(4096 / Z_1) - 1]\} - [R_{YPLATE} \times (Y_{POSITION} / 4095)]$$

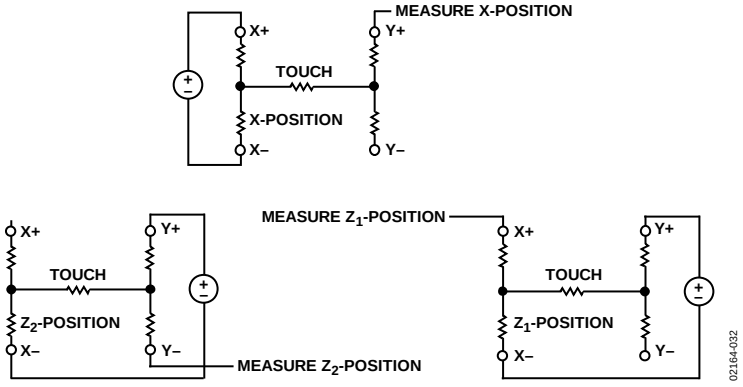


Figure 32. Pressure Measurement Block Diagram

PEN INTERRUPT REQUEST

The pen interrupt equivalent circuitry is outlined in Figure 33. By connecting a pull-up resistor (10 kΩ to 100 kΩ) between $+V_{CC}$ and this CMOS logic open-drain output, the $\overline{\text{PENIRQ}}$ output remains high normally. If $\overline{\text{PENIRQ}}$ is enabled (see Table 8), when the touch screen connected to the AD7873 is touched by a pen or finger, the $\overline{\text{PENIRQ}}$ output goes low, initiating an interrupt to a microprocessor. This can then instruct a control word to be written to the AD7873 to initiate a conversion. This output can also be enabled between conversions during power-down (see Table 8), allowing power-up to be initiated only when the screen is touched. The result of the first touch screen coordinate conversion after power-up is valid, assuming any external reference is settled to the 12-bit or 8-bit level as required.

Figure 34 assumes that the $\overline{\text{PENIRQ}}$ function was enabled in the last write or that the part was just powered up so $\overline{\text{PENIRQ}}$ is enabled by default. Once the screen is touched, the $\overline{\text{PENIRQ}}$ output goes low a time t_{PEN} later. This delay is approximately 5 µs, assuming a 10 nF touch screen capacitance, and varies with the touch screen resistance actually used. Once the START bit is detected, the pen interrupt function is disabled and the $\overline{\text{PENIRQ}}$ cannot respond to screen touches. The $\overline{\text{PENIRQ}}$ output remains low until the fourth falling edge of DCLK after the START bit is clocked in, at which point it returns high as soon as possible, irrespective of the touch screen capacitance. This does not mean that the pen interrupt function is now enabled again because the power-down bits have not yet been loaded to the control register. Regardless of whether $\overline{\text{PENIRQ}}$ is to be enabled again, the $\overline{\text{PENIRQ}}$ output normally always idles high. Assuming the $\overline{\text{PENIRQ}}$ is enabled again as shown in Figure 34, then once the conversion is complete, the $\overline{\text{PENIRQ}}$ output again responds to a screen touch. The fact that $\overline{\text{PENIRQ}}$ returns high almost immediately after the fourth falling edge of DCLK means the user avoids any spurious interrupts on the microprocessor or DSP, which can occur if the interrupt request line on the micro/DSP were unmasked during or toward the end of conversion and the $\overline{\text{PENIRQ}}$ pin was still low. Once the next start bit is detected by the AD7843, the $\overline{\text{PENIRQ}}$ function is again disabled.

If the control register write operation overlaps with the data read, a start bit is always detected prior to the end of conversion, meaning that even if the $\overline{\text{PENIRQ}}$ function is enabled in the control register, it is disabled by the start bit again before the end of the conversion is reached, so the $\overline{\text{PENIRQ}}$ function effectively cannot be used in this mode. However, as conversions are occurring continuously, the $\overline{\text{PENIRQ}}$ function is not necessary and is therefore redundant.

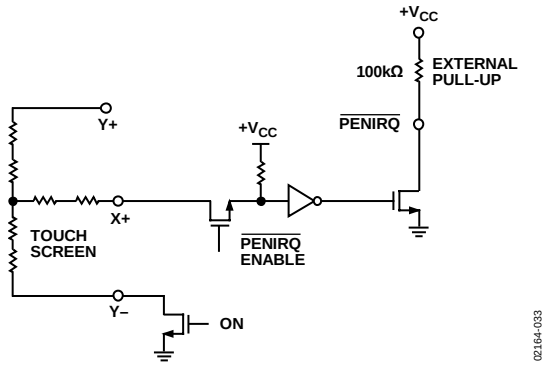


Figure 33. $\overline{\text{PENIRQ}}$ Functional Block Diagram

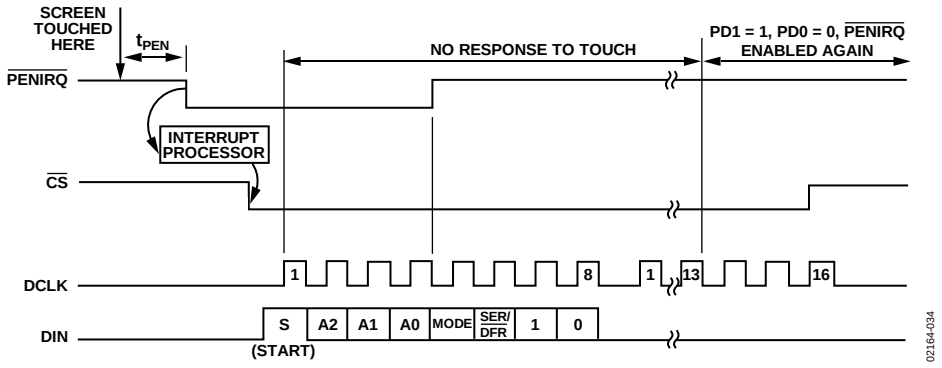


Figure 34. $\overline{\text{PENIRQ}}$ Timing Diagram

CONTROL REGISTER

The control word provided to the ADC via the DIN pin is shown in Table 7. This provides the conversion start, channel addressing, ADC conversion resolution, configuration, and power-down of the AD7873. Table 7 provides detailed information on the order and description of these control bits within the control word.

Initiate START

The first bit, the S bit, must always be set to 1 to initiate the start of the control word. The AD7873 ignores any inputs on the DIN line until the start bit is detected.

Channel Addressing

The next three bits in the control register, A2, A1, and A0, select the active input channel(s) of the input multiplexer (see Table 6 and Figure 26), touch screen drivers, and the reference inputs.

Mode

The MODE bit sets the resolution of the analog-to-digital converter. With a 0 in this bit, the following conversion has 12 bits of resolution. With a 1 in this bit, the following conversion has eight bits of resolution.

SER/$\overline{DFR}$

The SER/$\overline{DFR}$ bit controls the reference mode, set to either single-ended or differential when a 1 or a 0 is written to this bit, respectively. The differential mode is also referred to as the ratiometric conversion mode. This mode is optimum for X-position, Y-position, and pressure-touch measurements. The reference is derived from the voltage at the switch drivers, which is almost the same as the voltage to the touch screen. In this case, a separate reference voltage is not needed because the reference voltage to the ADC is the voltage across the touch screen. In single-ended mode, the reference voltage to the converter is always the difference between the V_{REF} and GND pins. See Table 6 and Figure 26 through Figure 29 for further information.

If X-position, Y-position, and pressure touch are measured in single-ended mode, an external reference voltage or $+V_{CC}$ is required for maximum dynamic range. The internal reference can be used for these single-ended measurements; however, a loss in dynamic range is incurred. If an external reference is used, the AD7873 should also be powered from the external reference. Because the supply current required by the device is so low, a precision reference can be used as the supply source to the AD7873. It might also be necessary to power the touch screen from the reference, which can require 5 mA to 10 mA. A REF19x voltage reference can source up to 30 mA, and, as such, could supply both the ADC and the touch screen. Care must be taken, however, to ensure that the input voltage applied to the ADC does not exceed the reference voltage and therefore the supply voltage. See the Absolute Maximum Ratings section.

Note that the differential mode can only be used for X-position, Y-position, and pressure touch measurements. All other measurements require single-ended mode.

PD0 and PD1

The power management options are selected by programming the power management bits, PD0 and PD1, in the control register. Table 8 summarizes the options available and the internal reference voltage configurations. The internal reference can be turned on or off independent of the analog-to-digital converter, allowing power saving between conversions using the power management options. On power-up, PD0 defaults to 0, while PD1 defaults to 1.

MSB							LSB
S	A2	A1	A0	MODE	SER/DFR	PD1	PD0

Table 7. Control Register Bit Function Description

Bit No.	Mnemonic	Comment
7	S	Start Bit. The control word starts with the first high bit on DIN. A new control word can start every 15th DCLK cycle when in the 12-bit conversion mode or every 11th DCLK cycle when in 8-bit conversion mode.
6 to 4	A2 to A0	Channel Select Bits. These three address bits along with the SER/DFR bit control the setting of the multiplexer input, switches, and reference inputs, as detailed in Table 6.
3	MODE	12-Bit/8-Bit Conversion Select Bit. This bit controls the resolution of the following conversion. With a 0 in this bit, the conversion has 12-bit resolution or, with a 1 in this bit, 8-bit resolution.
2	SER/$\overline{DFR}$	Single-Ended/Differential Reference Select Bit. Together with Bit A2 to Bit A0, this bit controls the setting of the multiplexer input, switches, and reference inputs as described in Table 6.
1, 0	PD1, PD0	Power Management Bits. These two bits decode the power-down mode of the AD7873 as shown in Table 8.

Table 8. Power Management Options

PD1	PD0	$\overline{\text{PENIRQ}}$	Description
0	0	Enabled	This configuration results in immediate power-down of the on-chip reference as soon as PD1 is set to 0. The ADC powers down only between conversions. When PD0 is set to 0, the conversion is performed first and the ADC powers down upon completion of that conversion (or upon the rising edge of $\overline{CS}$, if it occurs first). At the start of the next conversion, the ADC instantly powers up to full power. This means if the device is being used in the differential mode, or an external reference is used, there is no need for additional delays to ensure full operation and the very first conversion is valid. The Y– switch is on while in power-down. When the device is performing differential table conversions, the reference and reference buffer do not attempt to power up with Bit PD1 and Bit PD0 programmed in this way.
0	1	Enabled	This configuration results in switching the reference off immediately and the ADC on permanently. When the device is performing differential tablet conversions, the reference and reference buffer do not attempt to power up with Bit PD1 and Bit PD0 programmed in this way.
1	0	Enabled	This configuration results in switching the reference on and powering the ADC down between conversions. The ADC powers down only between conversions. When PD0 is set to 0, the conversion is performed first, and the ADC powers down upon completion of the conversion (or upon the rising edge of CS if it occurs first). At the start of the next conversion, the ADC instantly powers up to full power. There is no need for additional delays to ensure full operation as the reference remains permanently powered up.
1	1	Disabled	This configuration results in always keeping the device powered up. The reference and the ADC are on.

POWER VS. THROUGHPUT RATE

By using the power-down options on the AD7873 when not converting, the average power consumption of the device decreases at lower throughput rates. Figure 35 shows how, as the throughput rate is reduced while maintaining the DCLK frequency at 2 MHz, the device remains in its power-down state longer and the average current consumption over time drops accordingly.

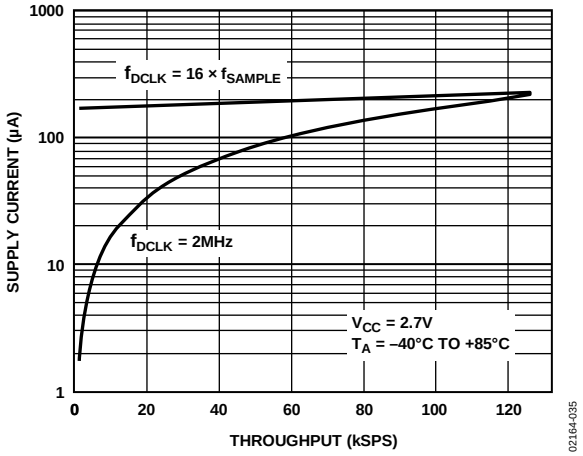


Figure 35. Supply Current vs. Throughput (µA)

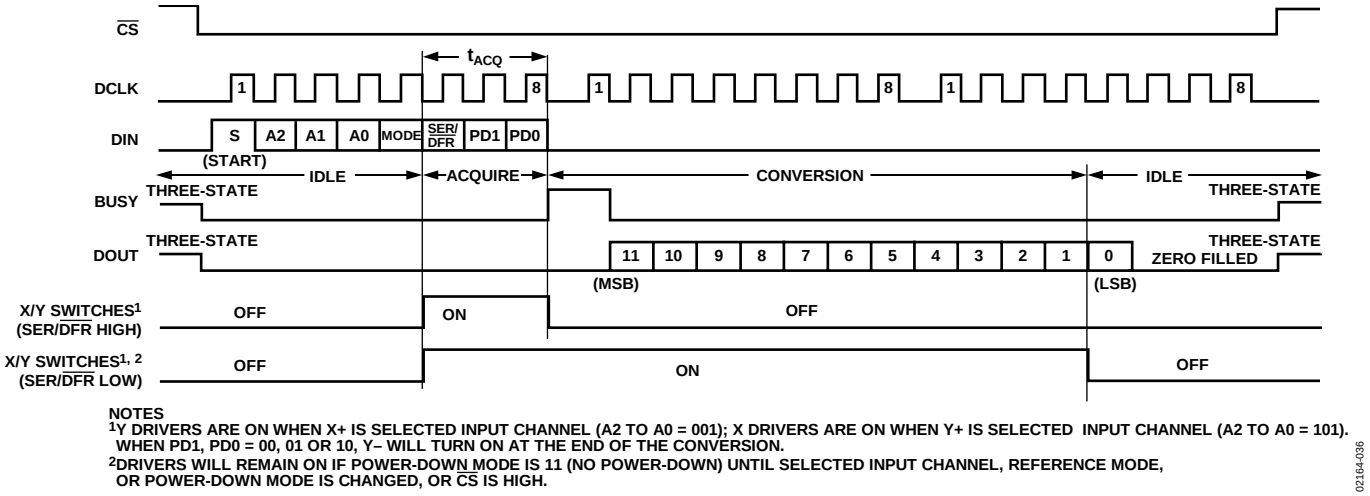
For example, if the AD7873 is operated in a 24-DCLK continuous sampling mode, with a throughput rate of 10 kSPS and a DCLK of 2 MHz, and the device is placed in the power-down mode between conversions, (PD0, PD1 = 0, 0), that is, the ADC shuts down between conversions but the reference remains powered down permanently, then the current consumption is calculated as follows. The current consumption during normal operation with a 2 MHz DCLK is 210 µA (V_{CC} = 2.7 V). Assuming an external reference is used, the power-up time of the ADC is instantaneous, so when the part is converting, it consumes 210 µA. In this mode of operation, the part powers up on the fourth falling edge of DCLK after the start bit is recognized. It goes back into power-down at the end of conversion on the 20th falling edge of DCLK, meaning that the part consumes 210 µA for 16 DCLK cycles only, 8 µs during each conversion cycle. If the throughput rate is 10 kSPS, the cycle time is 100 µs and the average power dissipated during each cycle is (8/100) × (210 µA) = 16.8 µA.

SERIAL INTERFACE

Figure 36 shows the typical operation of the serial interface of the AD7873. The serial clock provides the conversion clock and also controls the transfer of information to and from the AD7873. One complete conversion can be achieved with 24 DCLK cycles.

The $\overline{CS}$ signal initiates the data transfer and conversion process. The falling edge of $\overline{CS}$ takes the BUSY output and the serial bus out of three-state. The first eight DCLK cycles are used to write to the control register via the DIN pin. The control register is updated in stages as each bit is clocked in. Once the converter has enough information about the following conversion to set the input multiplexer and switches appropriately, the converter enters the acquisition mode and, if required, the internal switches are turned on. During acquisition mode, the reference input data is updated. After the three DCLK cycles of acquisition, the control word is complete (the power management bits are now updated) and the converter enters conversion mode. At this point, track-and-hold goes into hold mode, the input signal is sampled, and the BUSY output goes high (BUSY returns low on the next falling edge of DCLK). The internal switches can also turn off at this point if in single-ended mode, battery-monitor mode, or temperature measurement mode.

The next 12 DCLK cycles are used to perform the conversion and to clock out the conversion result. If the conversion is ratiometric (SER/$\overline{DFR}$ low), the internal switches are on during the conversion. A 13th DCLK cycle is needed to allow the DSP/micro to clock in the LSB. Three more DCLK cycles clock out the three trailing zeros and complete the 24 DCLK transfer. The 24 DCLK cycles can be provided from a DSP or via three bursts of eight clock cycles from a microcontroller.



NOTES
[1]Y DRIVERS ARE ON WHEN X+ IS SELECTED INPUT CHANNEL (A2 TO A0 = 001); X DRIVERS ARE ON WHEN Y+ IS SELECTED INPUT CHANNEL (A2 TO A0 = 101). WHEN PD1, PD0 = 00, 01 OR 10, Y– WILL TURN ON AT THE END OF THE CONVERSION.
[2]DRIVERS WILL REMAIN ON IF POWER-DOWN MODE IS 11 (NO POWER-DOWN) UNTIL SELECTED INPUT CHANNEL, REFERENCE MODE, OR POWER-DOWN MODE IS CHANGED, OR $\overline{CS}$ IS HIGH.

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Figure 36. Conversion Timing, 24 DCLKS per Conversion Cycle, 8-Bit Bus Interface. No DCLK delay required with dedicated serial port.

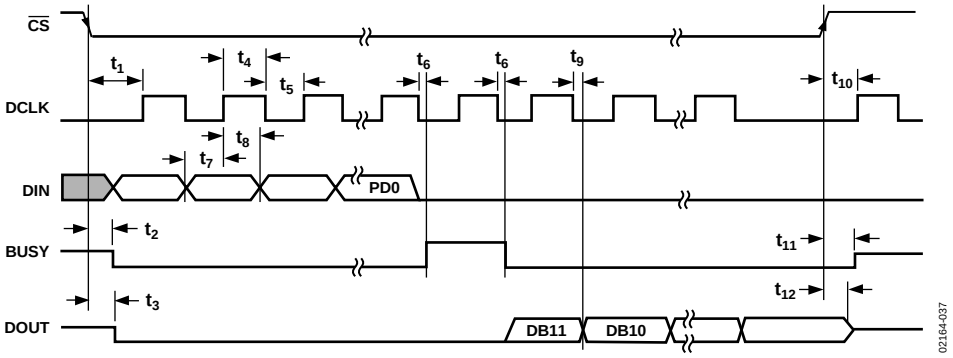


Figure 37. Detail Timing Diagram

16 Clocks per Cycle

The control bits for the next conversion can be overlapped with the current conversion to allow for a conversion every 16 DCLK cycles, as shown in Figure 38. This timing diagram also allows the possibility of communication with other serial peripherals between each byte (eight DCLKs) transfer between the processor and the converter. However, the conversion must complete within a short enough time frame to avoid capacitive droop effects that could distort the conversion result. It should also be noted that the AD7873 is fully powered while other serial communications are taking place between byte transfers.

15 Clocks per Cycle

Figure 39 shows the fastest way to clock the AD7873. This scheme does not work with most microcontrollers or DSPs because they are not capable of generating a 15 clock cycle per serial transfer. However, some DSPs allow the number of clocks per cycle to be programmed. This method can also be used with FPGAs (field programmable gate arrays) or ASICs (application specific integrated circuits). As in the 16 clocks per cycle case, the control bits for the next conversion are overlapped with the current conversion to allow a conversion every 15 DCLK cycles using 12 DCLKs to perform the conversion and 3 DCLKs to acquire the analog input. This effectively increases the throughput rate of the AD7873 beyond that used for the specifications that are tested using 16 DCLKs per cycle, and DCLK = 2 MHz.

8-Bit Conversion

The AD7873 can be set up to operate in an 8-bit mode rather than a 12-bit mode by setting the MODE bit in the control register to 1. This mode allows a faster throughput rate to be achieved, assuming 8-bit resolution is sufficient. When using 8-bit mode, a conversion is complete four clock cycles earlier than in 12-bit mode. This can be used with serial interfaces that provide 12 clock transfers, or two conversions can be completed with three 8-clock transfers. The throughput rate increases by 25% as a result of the shorter conversion cycle, but the conversion itself can occur at a faster clock rate because the internal settling time of the AD7873 is not as critical, because settling to eight bits is all that is required. The clock rate can be as much as 50% faster. The faster clock rate and fewer clock cycles combine to provide double the conversion rate.

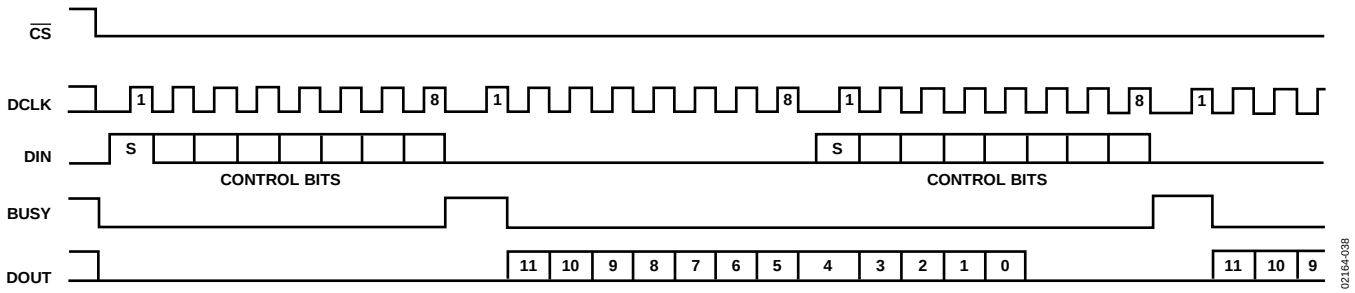


Figure 38. Conversion Timing, 16 DCLKs per Cycle, 8-Bit Bus Interface. No DCLK delay required with dedicated serial port.

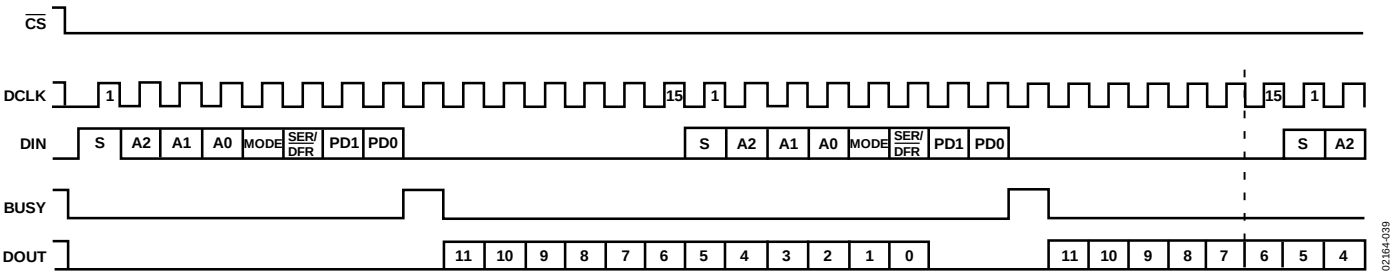


Figure 39. Conversion Timing, 15 DCLKs per Cycle, Maximum Throughput Rate

GROUNDING AND LAYOUT

For information on grounding and layout considerations for the AD7873, refer to Application Note AN-577, *Layout and Grounding Recommendations for Touch Screen Digitizers*.

PCB DESIGN GUIDELINES FOR CHIP SCALE PACKAGE

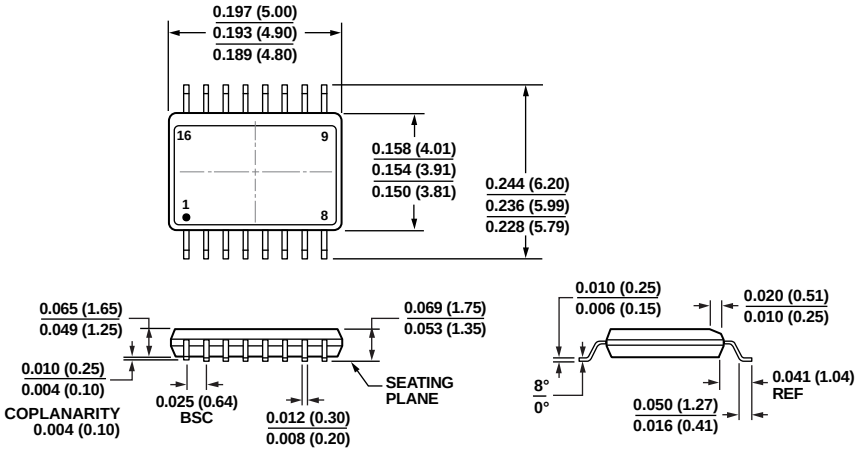
The lands on the chip scale package (CP-32) are rectangular. The printed circuit board pad for these should be 0.1 mm longer than the package land length and 0.05 mm wider than the package land width. The land should be centered on the pad. This ensures that the solder joint size is maximized.

The bottom of the chip scale package has a central thermal pad. The thermal pad on the printed circuit board should be at least as large as this exposed pad. On the printed circuit board, there should be a clearance of at least 0.25 mm between the thermal pad and the inner edges of the pad pattern. This ensures that shorting is avoided.

Thermal vias can be used on the printed circuit board thermal pad to improve thermal performance of the package. If vias are used, they should be incorporated in the thermal pad at 1.2 mm pitch grid. The via diameter should be between 0.3 mm and 0.33 mm and the via barrel should be plated with 1 oz. copper to plug the via.

The user should connect the printed circuit board thermal pad to GND.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-137-AB

CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

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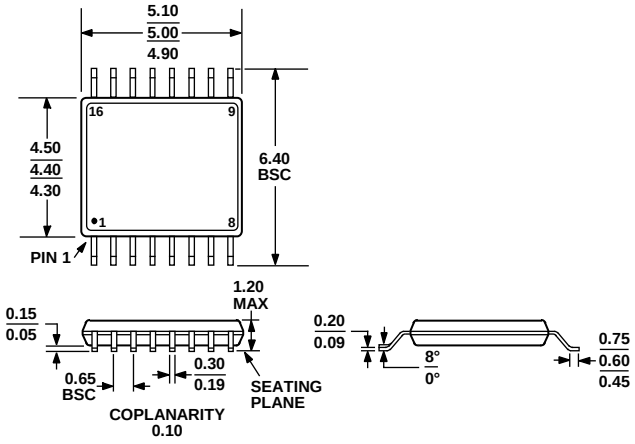
Figure 40. 16-Lead Shrink Small Outline Package [QSOP]
(RQ-16)
Dimensions shown in inches and (millimeters)



COMPLIANT TO JEDEC STANDARDS MO-153-AB

Figure 41. 16-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-16)
Dimensions shown in millimeters

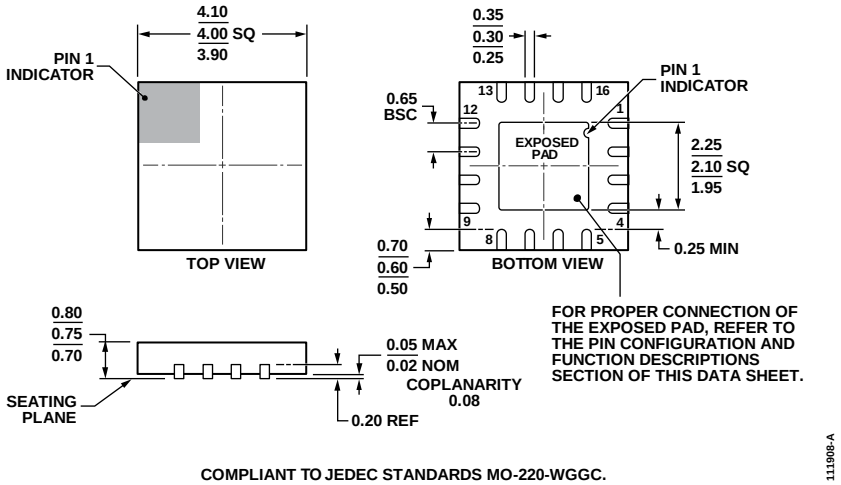


Figure 42. 16-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
4 mm × 4 mm Body, Very Very Thin Quad
(CP-16-23)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Linearity Error (LSB)[2]	Package Option[3]
AD7873ARQZ	–40°C to +85°C	16-Lead QSOP	±2	RQ-16
AD7873ARQZ-REEL	–40°C to +85°C	16-Lead QSOP	±2	RQ-16
AD7873ARQZ-REEL7	–40°C to +85°C	16-Lead QSOP	±2	RQ-16
AD7873BRQZ	–40°C to +85°C	16-Lead QSOP	±1	RQ-16
AD7873BRQZ-REEL	–40°C to +85°C	16-Lead QSOP	±1	RQ-16
AD7873BRQZ-REEL7	–40°C to +85°C	16-Lead QSOP	±1	RQ-16
AD7873ARUZ	–40°C to +85°C	16-Lead TSSOP	±2	RU-16
AD7873ARUZ-REEL	–40°C to +85°C	16-Lead TSSOP	±2	RU-16
AD7873ARUZ-REEL7	–40°C to +85°C	16-Lead TSSOP	±2	RU-16
AD7873ACPZ	–40°C to +85°C	16-Lead LFCSP_WQ	±2	CP-16-23
AD7873ACPZ-REEL	–40°C to +85°C	16-Lead LFCSP_WQ	±2	CP-16-23
AD7873ACPZ-REEL7	–40°C to +85°C	16-Lead LFCSP_WQ	±2	CP-16-23
EVAL-AD7873EBZ		Evaluation Board		

[1] Z = RoHS Compliant Part.
[2] Linearity error here refers to integral linearity error.
[3] RQ = QSOP = 0.15 inch quarter size outline package; RU = TSSOP, CP = LFCSP.

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