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12/02—Revision 0: Initial Version

SPECIFICATIONS

V_{DD} = 2.7 V to 5.5 V, $V_A < V_{DD}$, V_B = 0 V, −40°C < T_A < +105°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ[1]	Max	Unit
DC CHARACTERISTICS—RHEOSTAT MODE						
Resolution	N				6	Bits
Resistor Differential Nonlinearity[2]	R-DNL					
10 kΩ, 50 kΩ, 100 kΩ		R_{WB}, V_A = NC	−0.5	+0.05	+0.5	LSB
1 kΩ		R_{WB}, V_A = NC	−1	+0.25	+1	LSB
Resistor Nonlinearity[2]	R-INL					
10 kΩ, 50 kΩ, 100 kΩ		R_{WB}, V_A = NC	−0.5	+0.10	+0.5	LSB
1 kΩ		R_{WB}, V_A = NC	−5	+2	+5	LSB
Nominal Resistance Tolerance[3]	$\Delta R_{AB}/R_{AB}$	T_A = 25°C				
10 kΩ, 50 kΩ, 100 kΩ			−30		+30	%
Nominal Resistance, 1 kΩ	R_{AB}		0.8	1.2	1.6	kΩ
Rheostat Mode Temperature Coefficient[4]	$(\Delta R_{AB}/R_{AB})/\Delta T$	Wiper = NC		300		ppm/°C
Wiper Resistance	R_W	$I_W = V_{DD}/R$, V_{DD} = 3 V or 5 V		60	100	Ω
DC CHARACTERISTICS—POTENTIOMETER DIVIDER MODE						
Differential Nonlinearity[5]	DNL		−0.5	+0.1	+0.5	LSB
Integral Nonlinearity[5]	INL		−0.5		+0.5	LSB
Voltage Divider[4] Temperature Coefficient	$(\Delta V_W/V_W)/\Delta T$	Code = 0x20		10		ppm/°C
Full-Scale Error	V_{WFSE}	Code = 0x3F	−1		0	LSB
10 kΩ, 50 kΩ, 100 kΩ			−1		0	LSB
1 kΩ			−6		0	LSB
Zero-Scale Error	V_{WZSE}	Code = 0x00	−6		0	LSB
10 kΩ, 50 kΩ, 100 kΩ			0		1	LSB
1 kΩ			0		5	LSB
RESISTOR TERMINALS						
Voltage Range[6]	V_A, V_B, V_W		GND		V_{DD}	V
Capacitance[7] A, B	C_A, C_B	f = 5 MHz, measured to GND, code = 0x20		25		pF
Capacitance[7] W	C_W	f = 1 MHz, measured to GND, code = 0x20		55		pF
Common-Mode Leakage	I_{CM}	$V_A = V_B = V_W$		1		nA
DIGITAL INPUTS AND OUTPUTS						
Input Logic High (SDA and SCL)[8]	V_{IH}		$0.7 \times V_{DD}$		V_{DD} + 0.5	V
Input Logic Low (SDA and SCL)[8]	V_{IL}		−0.5		$0.3 \times V_{DD}$	V
Input Logic High (AD0)	V_{IH}		3.0		V_{DD}	V
Input Logic Low (AD0)	V_{IL}	V_{IN} = 0 V or 5 V	0		0.4	V
Input Logic Current	I_{IL}			0.01	1	µA
Input Capacitance[7]	C_{IL}			3		pF
Output Logic Low (SDA)	V_{OL}				0.4	V
Three-State Leakage Current	I_{OZ}				±1	µA
Output Capacitance[7]	C_{OZ}			3		pF
POWER SUPPLIES						
Power Supply Range	V_{DD}		2.7		5.5	V
OTP Power Supply[8, 9]	V_{DD_OTP}	T_A = 25°C	5.0	5.25	5.5	V
Supply Current	I_{DD}	V_{IH} = 5 V or V_{IL} = 0 V		0.1	5	µA
OTP Supply Current[8, 10,11]	I_{DD_OTP}	T_A = 25°C, V_{DD_OTP} = 5 V		100		mA
Power Dissipation[12]	P_{DISS}	V_{IH} = 5 V or V_{IL} = 0 V, V_{DD} = 5 V		0.5	27.5	µW
Power Supply Sensitivity	PSRR	R_{AB} = 1 kΩ	−0.3		+0.3	%/%
	PSRR	R_{AB} = 10 kΩ, 50 kΩ, 100 kΩ	−0.05		+0.05	%/%

Parameter	Symbol	Test Conditions/Comments	Min	Typ[1]	Max	Unit
DYNAMIC CHARACTERISTICS[7, 13, 14]						
Bandwidth, −3 dB	BW_1 kΩ	R_{AB} = 1 kΩ, code = 0x20		6000		kHz
	BW_10 kΩ	R_{AB} = 10 kΩ, code = 0x20		600		kHz
	BW_50 kΩ	R_{AB} = 50 kΩ, code = 0x20		110		kHz
	BW_100 kΩ	R_{AB} = 100 kΩ, code = 0x20		60		kHz
Total Harmonic Distortion	THD_W	V_A = 1 V rms, R_{AB} = 1 kΩ, V_B = 0 V, f = 1 kHz		0.05		%
Adjustment Settling Time	t_{S1}	V_A = 5 V ± 1 LSB error band, V_B = 0 V, measured at V_W		5		µs
Power-Up Settling Time—After Fuses Blown	t_{S2}	V_A = 5 V ± 1 LSB error band, V_B = 0 V, measured at V_W, V_{DD} = 5 V		5		µs
Resistor Noise Voltage	e_{N_WB}	R_{AB} = 1 kΩ, f = 1 kHz, code = 0x20		3		nV/√Hz
INTERFACE TIMING CHARACTERISTICS[7, 14, 15]		Applies to all parts				
SCL Clock Frequency	f_{SCL}				400	kHz
t_{BUF} Bus Free Time Between Stop and Start	t_1		1.3			µs
$t_{HD;\,STA}$ Hold Time (Repeated Start)	t_2	After this period, the first clock pulse is generated	0.6			µs
t_{LOW} Low Period of SCL Clock	t_3		1.3			µs
t_{HIGH} High Period of SCL Clock	t_4		0.6		50	µs
$t_{SU;\,STA}$ Setup Time for Start Condition	t_5		0.6			µs
$t_{HD;\,DAT}$ Data Hold Time	t_6				0.9	µs
$t_{SU;\,DAT}$ Data Setup Time	t_7		0.1			µs
t_F Fall Time of Both SDA and SCL Signals	t_8				0.3	µs
t_R Rise Time of Both SDA and SCL Signals	t_9				0.3	µs
$t_{SU;\,STO}$ Setup Time for Stop Condition	t_{10}		0.6			µs
OTP Program Time	t_{11}			400		ms

[1] Typical values represent average readings at 25°C, V_{DD} = 5 V, and V_{SS} = 0 V.
[2] Resistor position nonlinearity error, R-INL, is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from ideal between successive tap positions. Parts are guaranteed monotonic.
[3] $V_{AB} = V_{DD}$, wiper (V_W) = no connect.
[4] $\Delta R_{WB}/\Delta T = \Delta R_{WA}/\Delta T$. Temperature coefficient is code-dependent; see the Typical Performance Characteristics section.
[5] INL and DNL are measured at V_W. INL with the RDAC configured as a potentiometer divider similar to a voltage output DAC. V_W with the RDAC configured as a potentiometer divider similar to a voltage output DAC. $V_A = V_{DD}$ and V_B = 0 V. DNL specification limits of ±1 LSB maximum are guaranteed monotonic operating conditions.
[6] The A, B, and W resistor terminals have no limitations on polarity with respect to each other.
[7] Guaranteed by design; not subject to production test.
[8] The minimum voltage requirement on the V_{IH} is 0.7 × V_{DD}. For example, V_{IH} min = 3.5 V when V_{DD} = 5 V. It is typical for the SCL and SDA resistors to be pulled up to V_{DD}. However, care must be taken to ensure that the minimum V_{IH} is met when the SCL and SDA are driven directly from a low voltage logic controller without pull-up resistors.
[9] Different from the operating power supply; the power supply for OTP is used one time only.
[10] Different from the operating current; the supply current for OTP lasts approximately 400 ms for the one time it is needed.
[11] See Figure 28 for the energy plot during the OTP program.
[12] P_{DISS} is calculated from ($I_{DD} \times V_{DD}$). CMOS logic level inputs result in minimum power dissipation.
[13] Bandwidth, noise, and settling time depend on the terminal resistance value chosen. The lowest R value results in the fastest settling time and highest bandwidth. The highest R value results in the minimum overall power consumption.
[14] All dynamic characteristics use V_{DD} = 5 V.
[15] See Figure 29 for the location of the measured values.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 2.

Parameter	Rating
V_{DD} to GND	−0.3 V +6.5 V
V_A, V_B, V_W to GND	GND, V_{DD}
Maximum Current	
I_{WB}, I_{WA} Pulsed	±20 mA
I_{WB} Continuous (R_{WB} ≤ 1 kΩ, A Open)[1]	±4 mA
I_{WA} Continuous (R_{WA} ≤ 1 kΩ, B Open)	±4 mA
Digital Input and Output Voltage to GND	0 V, V_{DD}
Operating Temperature Range	−40°C to +105°C
Maximum Junction Temperature (T_J max)	150°C
Storage Temperature	−65°C to +150°C
Reflow Soldering	
Peak Temperature	260°C
Time at Peak Temperature	20 sec to 40 sec
Thermal Resistance θ_{JA}, SOT-23[2]	230°C/W

[1] Maximum terminal current is bounded by the maximum current handling of the switches, the maximum power dissipation of the package; the maximum applied voltage across any two of the A, B, and W terminals at a given resistance.

[2] Package power dissipation = (T_J max − T_A)/θ_{JA}.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

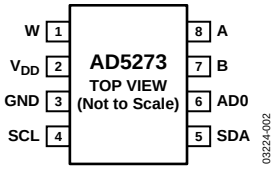

Figure 2. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	W	Wiper Terminal W. GND ≤ V_W ≤ V_{DD}.
2	V_{DD}	Positive Power Supply. Specified for non-OTP operation from 2.7 V to 5.5 V. For OTP programming, V_{DD_OTP} must be set within the window of 5 V to 5.5 V for all end to end resistance options, and be capable of sourcing 100 mA.
3	GND	Common Ground.
4	SCL	Serial Clock Input. Requires a pull-up resistor. If it is driven directly from a logic controller without the pull-up resistor, ensure that the V_{IH} minimum is 0.7 × V_{DD}.
5	SDA	Serial Data Input/Output. Requires a pull-up resistor. If it is driven directly from a logic controller without the pull-up resistor, ensure that the V_{IH} minimum is 0.7 × V_{DD}.
6	AD0	I^2C Device Address Bit. Allows a maximum of two AD5273 devices to be addressed.
7	B	Resistor Terminal B. GND ≤ V_B ≤ V_{DD}.
8	A	Resistor Terminal A. GND ≤ V_A ≤ V_{DD}.

TYPICAL PERFORMANCE CHARACTERISTICS

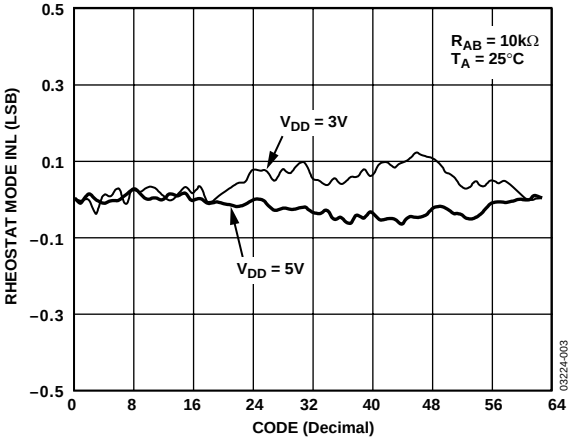

Figure 3. R_{INL} vs. Code vs. Supply Voltages

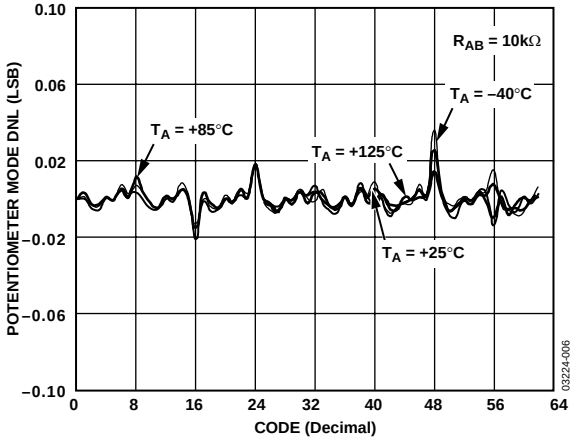

Figure 6. DNL vs. Code vs. Temperature

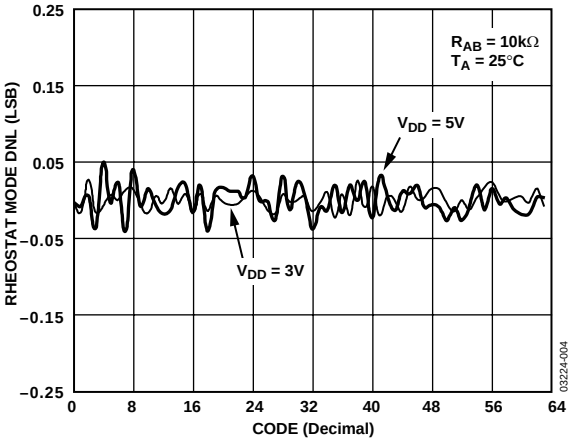

Figure 4. R_{DNL} vs. Code vs. Supply Voltages

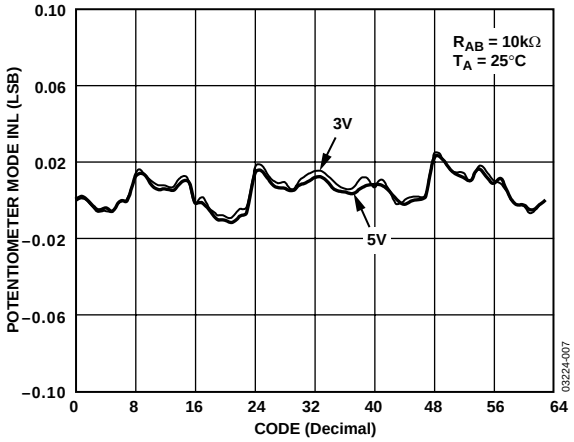

Figure 7. INL vs. Code vs. Supply Voltages

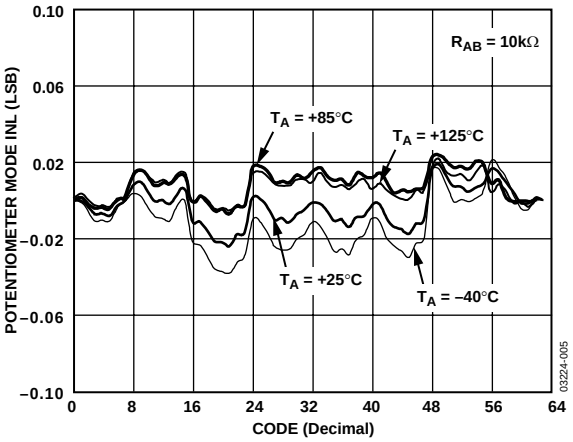

Figure 5. INL vs. Code vs. Temperature

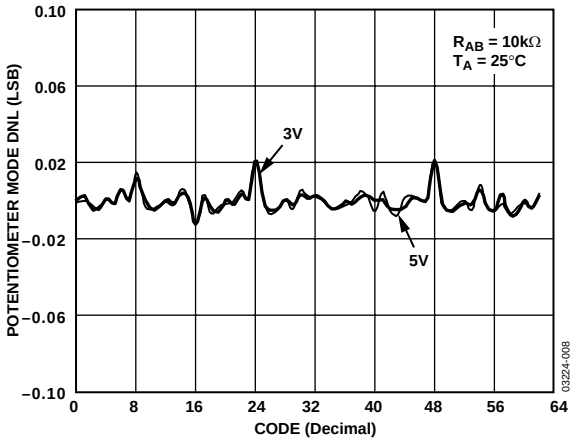

Figure 8. DNL vs. Code vs. Supply Voltages

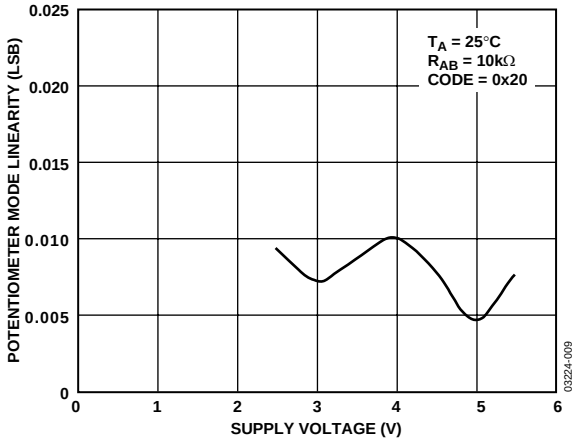

Figure 9. INL vs. Supply Voltage

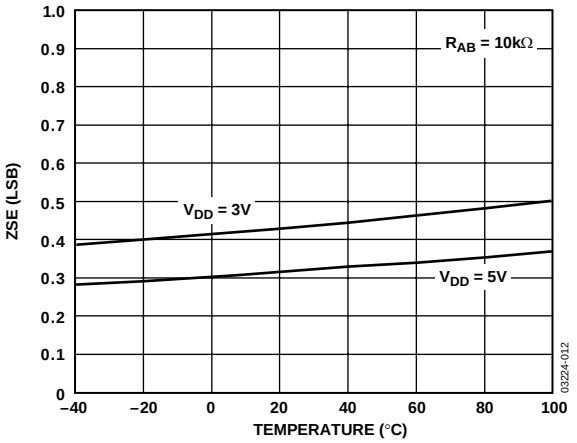

Figure 12. Zero-Scale Error

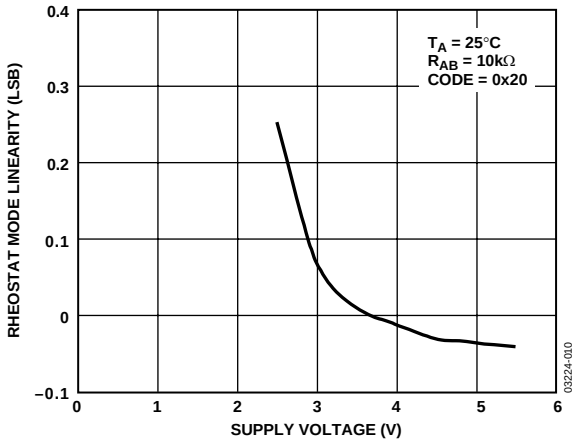

Figure 10. R_{INL} vs. Supply Voltage

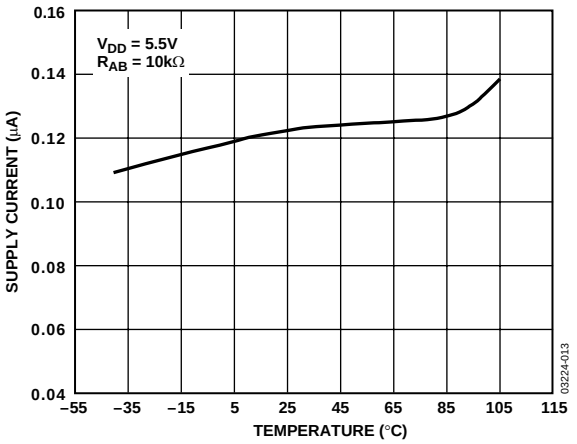

Figure 13. Supply Current vs. Temperature

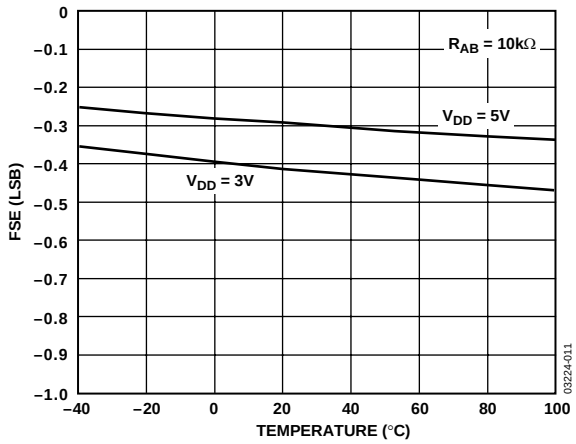

Figure 11. Full-Scale Error

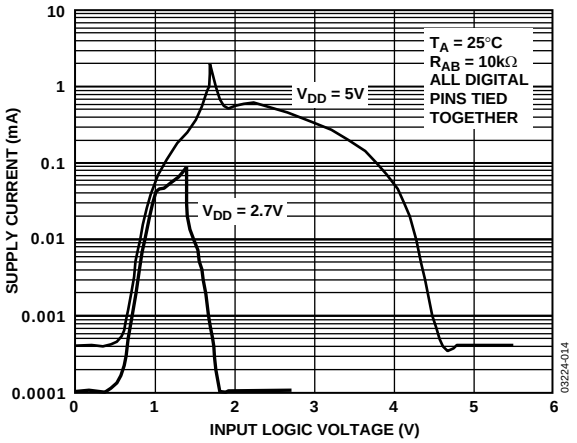

Figure 14. Supply Current vs. Digital Input Voltage

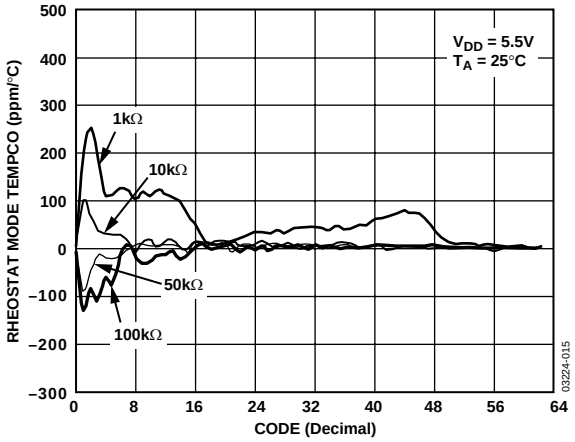

Figure 15. Rheostat Mode Tempco ($\Delta R_{WB}/R_{WB}$)/ΔT vs. Code

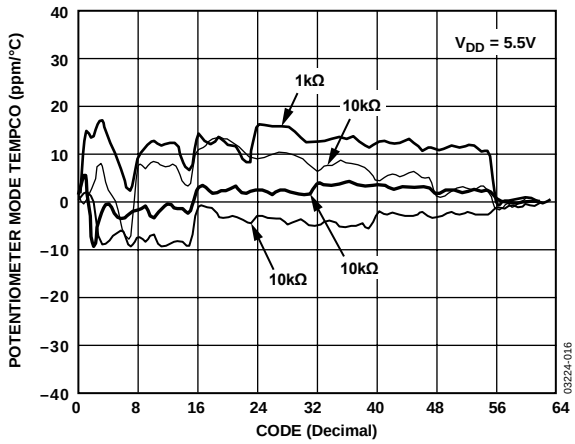

Figure 16. Potentiometer Mode Tempco ($\Delta V_W/V_W$)/ΔT vs. Code

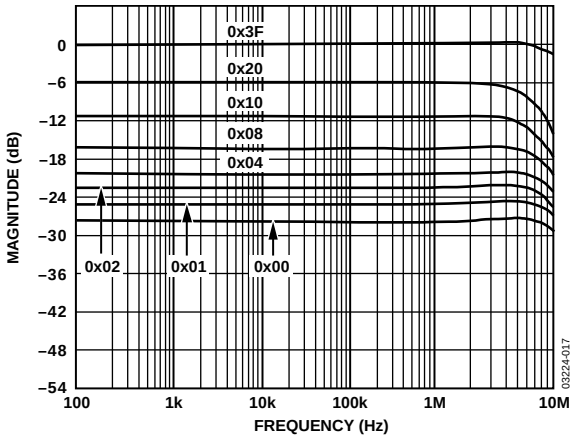

Figure 17. Gain vs. Frequency vs. Code, R_{AB} = 1 kΩ

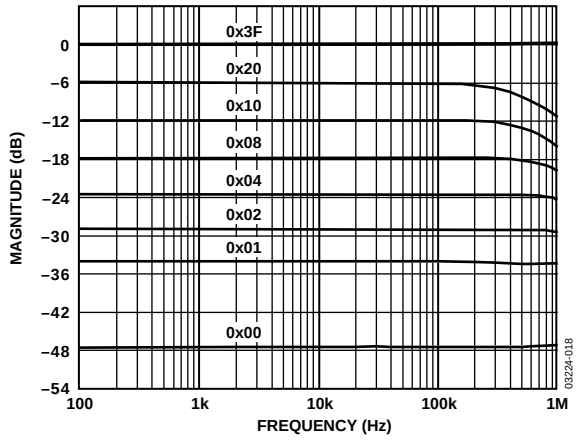

Figure 18. Gain vs. Frequency vs. Code, R_{AB} = 10 kΩ

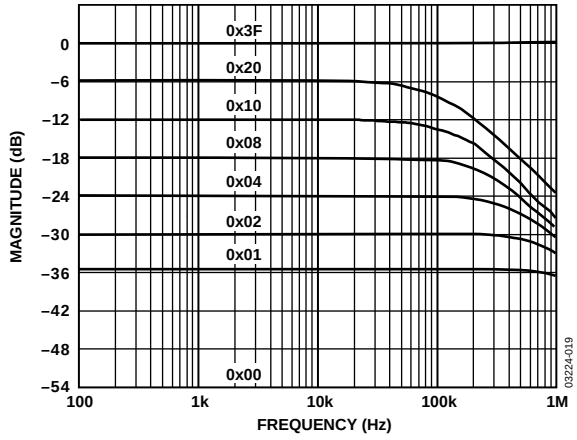

Figure 19. Gain vs. Frequency vs. Code, R_{AB} = 50 kΩ

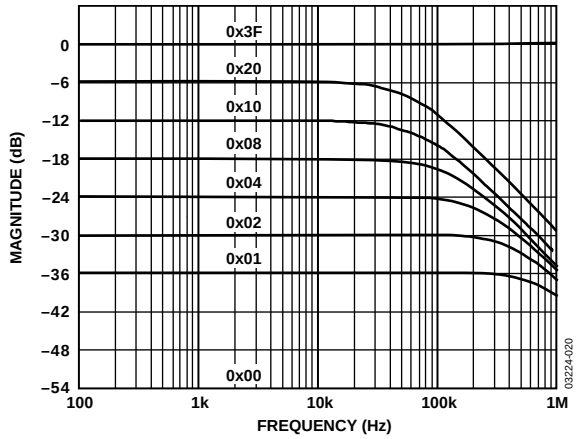

Figure 20. Gain vs. Frequency vs. Code, R_{AB} = 100 kΩ

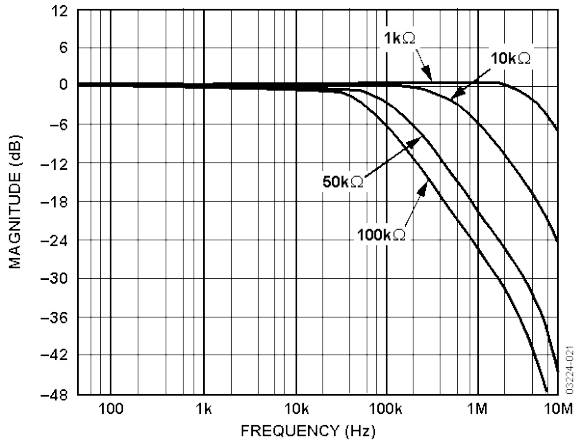

Figure 21. −3 dB Bandwidth

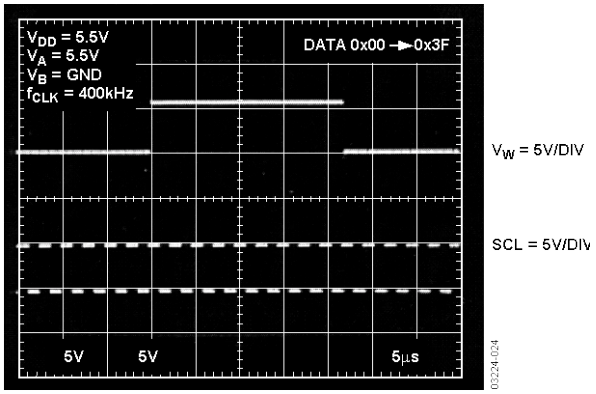

Figure 24. Large Settling Time

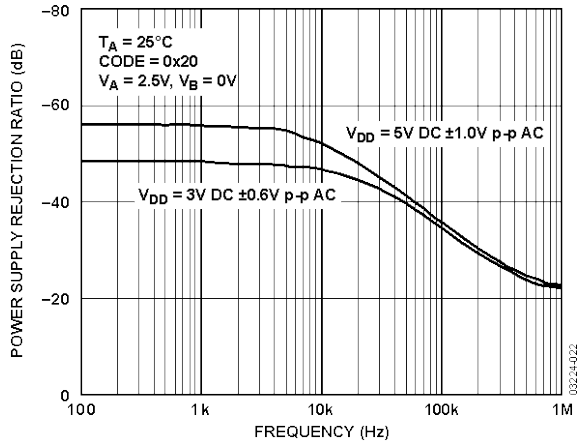

Figure 22. PSRR vs. Frequency

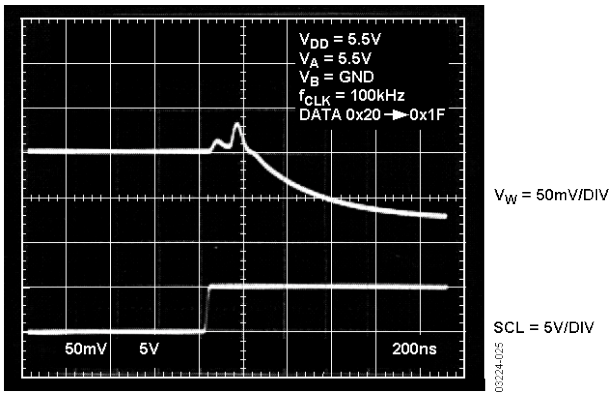

Figure 25. Midscale Glitch Energy

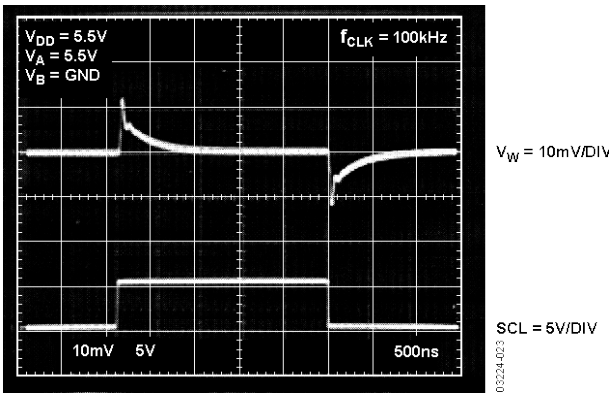

Figure 23. Digital Feedthrough

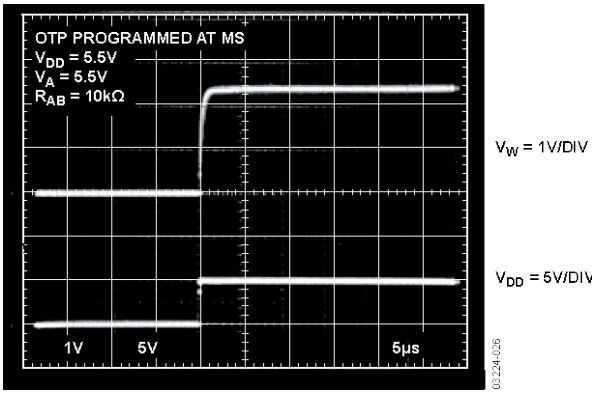

Figure 26. Power-Up Settling Time After Fuses Blown

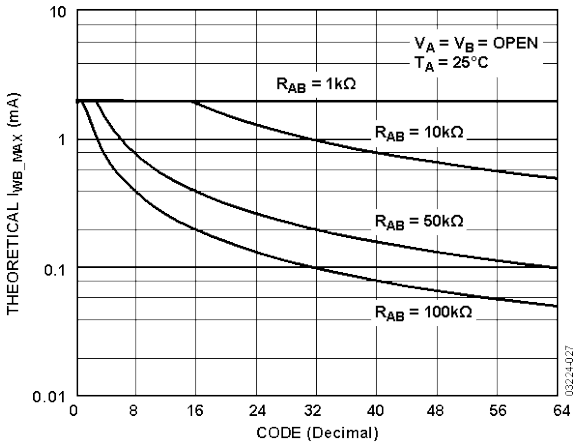

Figure 27. I_{WB_MAX} vs. Code

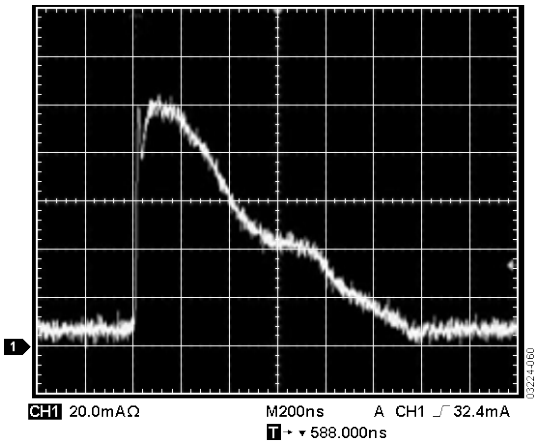

Figure 28. OTP Program Energy Plot for Single Fuse

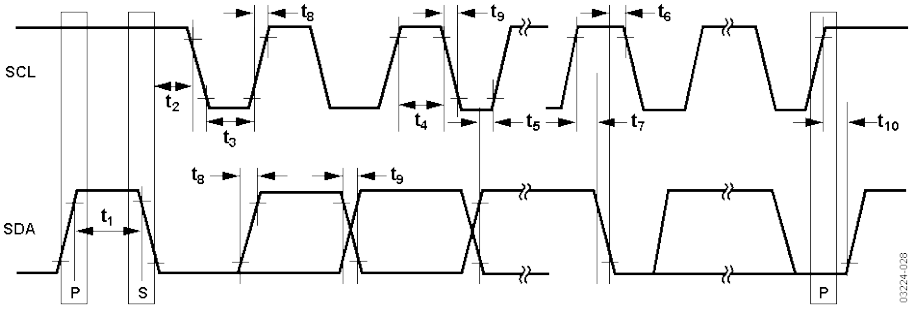

Figure 29. Interface Timing Diagram

THEORY OF OPERATION

The AD5273 is a one-time programmable (OTP), set-and-forget, 6-bit digital potentiometer. The AD5273 allows unlimited 6-bit adjustments prior to the OTP. OTP technology is a proven cost-effective alternative over EEMEM in one-time memory programming applications. The AD5273 employs fuse link technology to achieve the memory retention of the resistance setting function. It comprises six data fuses, which control the address decoder for programming the RDAC, one user mode test fuse for checking setup error, and one programming lock fuse for disabling any further programming once the data fuses are programmed correctly.

ONE-TIME PROGRAMMING

Prior to OTP activation, the AD5273 presets to midscale during power-on. After the wiper is set to the desired position, the resistance can be permanently set by programming the T bit and the one-time V_{DD_OTP} to high and by coding the part properly (see Figure 31). To blow the fuses to achieve a given nonvolatile setting, the fuse link technology of the AD5273 requires a V_{DD_OTP} from 5 V to 5.5 V for all end to end resistance options. During operation, however, V_{DD} can be 2.7 V to 5.5 V. Therefore, a system supply that is lower than V_{DD_OTP} requires an external supply for OTP. The user is allowed only one attempt to blow the fuses. If the user fails to blow the fuses on the first attempt, the fuse structure may change such that they can never be blown, regardless of the energy applied during subsequent events. For details, see the Power Supply Considerations section.

The device control circuit has two validation bits, E1 and E0, that can be read back in the read mode to check the programming status, as shown in Figure 32. Users should always read back the validation bits to ensure that the fuses are properly blown. After the fuses have been blown, all fuse latches are enabled upon subsequent power-on; therefore, the output corresponds to the stored setting. Figure 30 shows a detailed functional block diagram.

SDA Bit Definitions and Descriptions

S = start condition.

P = stop condition.

A = acknowledge.

X = don't care.

T = OTP programming bit. Logic 1 programs wiper position permanently.

D5, D4, D3, D2, D1, D0 = data bits.

E1, E0 = OTP validation bits.

0, 0 = ready to program.

0, 1 = test fuse not blown successfully. (For factory setup checking purpose only. Users should not see these combinations.)

1, 0 = fatal error. Do not retry. Discard the unit.

1, 1 = programmed successfully. No further adjustments possible.

AD0 = I²C device address bit. Allows maximum of two AD5273s to be addressed.

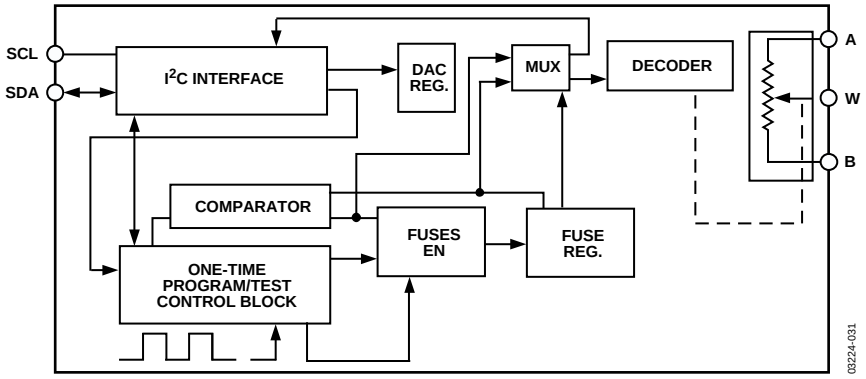

Figure 30. Detailed Functional Block Diagram

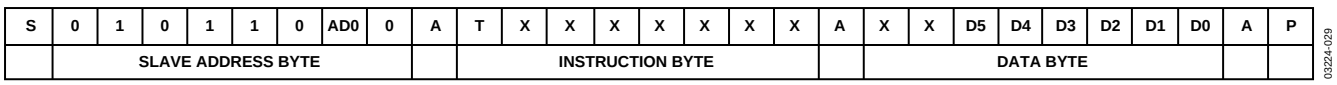

Figure 31. SDA Write Mode Bit Format

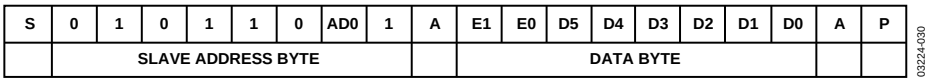

Figure 32. SDA Read Mode Bit Format

VARIABLE RESISTANCE AND VOLTAGE FOR RHEOSTAT MODE

If only the W-to-B or W-to-A terminals are used as variable resistors, the unused A or B terminal can be opened or shorted with W. This operation is called rheostat mode (see Figure 33).

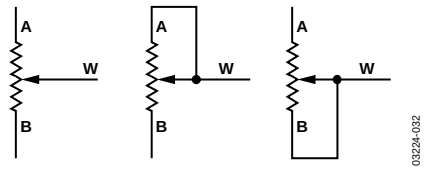

Figure 33. Rheostat Mode Configuration

The nominal resistance, R_{AB}, of the RDAC has 64 contact points accessed by the wiper terminal, plus the B terminal contact if R_{WB} is considered. The 6-bit data in the RDAC latch is decoded to select one of the 64 settings. Assuming that a 10 kΩ part is used, the wiper's first connection starts at Terminal B for Data Register 0x00. This connection yields a minimum of 60 Ω resistance between Terminal W and Terminal B because of the 60 Ω wiper contact resistance. The second connection is the first tap point, which corresponds to 219 Ω ($R_W = 1 \times R_{AB}/63 + R_W$) for Data Register 0x01, and so on. Each LSB data value increase moves the wiper up the resistor ladder until the last tap point is reached at 10,060 Ω ($63 \times R_{AB}/63 + R_W$). Figure 34 shows a simplified diagram of the equivalent RDAC circuit. The general equation determining R_{WB} is

$$R_{WB}(D) = \frac{D}{63} \times R_{AB} + R_W \quad (1)$$

where:
D is the decimal equivalent of the 6-bit binary code.
R_{AB} is the end-to-end resistance.
R_W is the wiper resistance contributed by the on resistance of the internal switch.

Table 4. R_{WB} vs. Codes; R_{AB} = 10 kΩ; Terminal A Opened

D (Dec)	R_{WB} (Ω)	Output State
63	10,060	Full scale ($R_{AB} + R_W$)
32	5139	Midscale
1	219	1 LSB
0	60	Zero scale (wiper contact resistance)

Because a finite wiper resistance of 60 Ω is present in the zero-scale condition, care should be taken to limit the current flow between W and B in this state to a maximum pulse current of 20 mA. Otherwise, degradation or possible destruction of the internal switch contact can occur.

Similar to the mechanical potentiometer, the resistance of the RDAC between the Wiper W and Terminal A also produces a complementary resistance, R_{WA}. When these terminals are used, Terminal B can be opened or shorted to W. Setting the resistance value for R_{WA} starts at a maximum value of resistance and decreases as the data loaded in the latch increases in value.

The general equation for this operation is

$$R_{WA}(D) = \frac{63 - D}{63} \times R_{AB} + R_W \quad (2)$$

Table 5. R_{WA} vs. Codes; R_{AB} =10 kΩ; Terminal B Opened

D (Dec)	R_{WA} (Ω)	Output State
63	60	Full scale
32	4980	Midscale
1	9901	1 LSB
0	10,060	Zero scale

The typical distribution of the resistance tolerance from device to device is process-lot dependent, and it is possible to have ±30% tolerance.

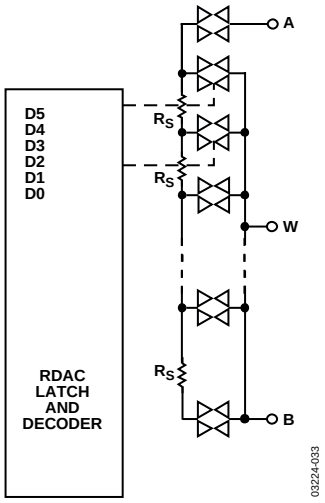

Figure 34. AD5273 Equivalent RDAC Circuit

VARIABLE RESISTANCE AND VOLTAGE FOR POTENTIOMETER MODE

If all three terminals are used, the operation is called the potentiometer mode. The most common configuration is the voltage divider operation (see Figure 35).

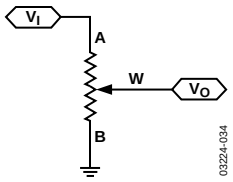

Figure 35. Potentiometer Mode Configuration

Ignoring the effect of the wiper resistance, the transfer function is simply

$$V_W(D) = \frac{D}{63} V_A \quad (3)$$

A more accurate calculation, which includes the wiper resistance effect, yields

$$V_W(D) = \frac{\frac{D}{63} R_{AB} + R_W}{R_{AB} + 2R_W} V_A \quad (4)$$

Unlike rheostat mode where the absolute tolerance is high, potentiometer mode yields an almost ratiometric function of D/63 with a relatively small error contributed by the R_W terms. Therefore, the tolerance effect is almost cancelled. Although the

ent temperature coefficients, the ratiometric adjustment also reduces the overall temperature coefficient effect to 5 ppm/°C, except at low value codes where R_W dominates.

Potentiometer mode includes op amp feedback resistor networks and other voltage scaling applications. Terminal A, Terminal W, and Terminal B can in fact be input or output terminals, provided that $|V_{AB}|$, $|V_{WA}|$, and $|V_{WB}|$ do not exceed V_{DD} to GND.

ESD PROTECTION

Digital inputs SDA and SCL are protected with a series input resistor and parallel Zener ESD structures (see Figure 36).

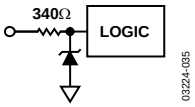

Figure 36. ESD Protection of Digital Pins

TERMINAL VOLTAGE OPERATING RANGE

There are also ESD protection diodes between V_{DD} and the RDAC terminals. The V_{DD} of AD5273 therefore defines their voltage boundary conditions (see Figure 37). Supply signals present on Terminal A, Terminal B, and Terminal W that exceed V_{DD} are clamped by the internal forward-biased diodes.

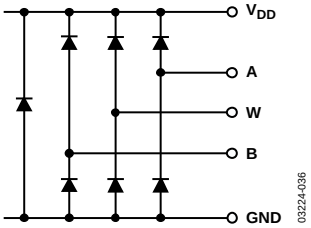

Figure 37. Maximum Terminal Voltages Set by V_{DD}

POWER-UP/POWER-DOWN SEQUENCES

Because of the ESD protection diodes, it is important to power V_{DD} first before applying any voltages to Terminal A, Terminal B, and Terminal W. Otherwise, the diode is forward-biased such that V_{DD} is powered unintentionally and can affect the rest of the user's circuits. The ideal power-up sequence is in the following order: GND, V_{DD}, digital inputs, and $V_A/V_B/V_W$. The order of powering V_A, V_B, V_W, and digital inputs is not important as long as they are powered after V_{DD}. Similarly, V_{DD} should be powered down last.

POWER SUPPLY CONSIDERATIONS

To minimize the package pin count, both OTP and normal operating voltage supplies are applied to the same V_{DD} terminal of the AD5273. The AD5273 employs fuse link technology that requires from 5 V to 5.5 V for all end to end resistance options, for blowing the internal fuses to achieve a given setting, but normal V_{DD} can be in the range of 2.7 V to 5.5 V after completing the fuse programming process. As a result, dual voltage supplies and isolation are needed if the system V_{DD} is outside the required V_{DD_OTP} range. For successful OTP, the fuse programming supply (either an on-board regulator or rack-mount power supply) must be rated at 5 V to 5.5 V for all end to end resistance options, and be capable of sourcing 100 mA for 400 ms. When fuse programming is completed, the V_{DD_OTP} supply can be removed to allow normal operation of 2.7 V to 5.5 V; the device then reduces the current consumption to the µA range.

When operating systems at 2.7 V, use of the bidirectional low threshold P-Ch MOSFETs is recommended for the supply's isolation. As shown in Figure 38, this assumes that the 2.7 V system voltage is applied first and that the P1 and P2 gates are pulled to ground, thus turning on P1 first and then P2. As a result, V_{DD} of the AD5273 approaches 2.7 V. When the AD5273 setting is found, the factory tester applies the V_{DD_OTP} to both the V_{DD} and the MOSFETs' gates, thus turning off P1 and P2. The OTP command should be executed at this time to program the AD5273 while the 2.7 V source is protected. Once the fuse programming is complete, the tester withdraws the V_{DD_OTP} and the AD5273's setting is fixed permanently.

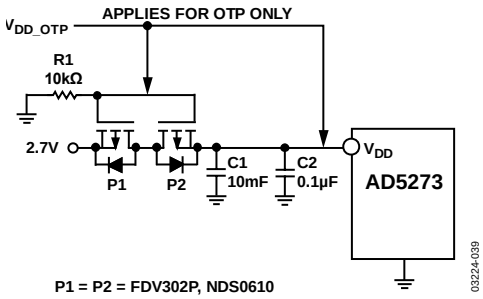

Figure 38. OTP Supply Isolated from the 2.7 V Normal Operating Supply

The AD5273 achieves the OTP function through blowing internal fuses. Users should always apply the recommended OTP programming voltage at the first fuse programming attempt. Failure to comply with this requirement can lead to a change in fuse structures, rendering programming inoperable.

Care should be taken when SCL and SDA are driven from a low voltage logic controller. Users must ensure that the logic high level is between $0.7 \times V_{DD}$ and V_{DD}. Refer to the Level Shift for Different Voltages Operation section.

Poor PCB layout introduces parasitics that can affect fuse programming. Therefore, it is recommended to add a 10 µF tantalum capacitor in parallel with a 1 nF ceramic capacitor as close as possible to the V_{DD} pin. The type and value chosen for both capacitors are important. This combination of capacitor values provides a fast response and larger supply current handling with minimum supply drop during transients. As a result, these capacitors increase the OTP programming success by not inhibiting the proper energy needed to blow the internal fuses. Additionally, C1 minimizes transient disturbance and low frequency ripple, while C2 reduces high frequency noise during normal operation.

CONTROLLING THE AD5273

I²C CONTROLLER PROGRAMMING

Write Bit Patterns

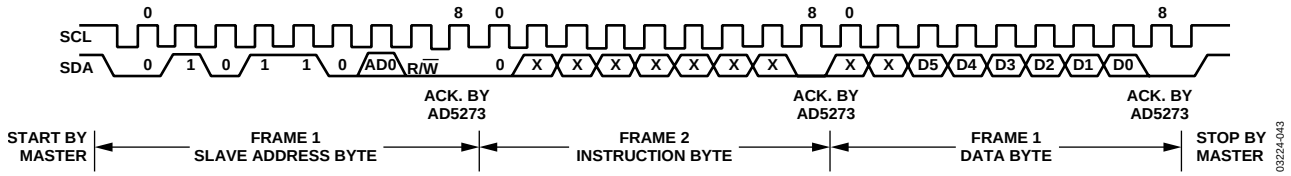

Figure 39. Writing to the RDAC Register

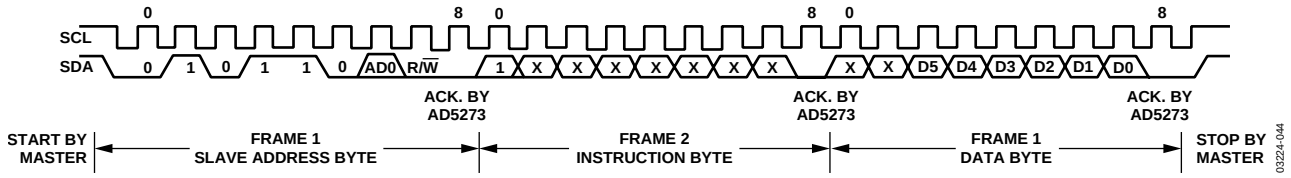

Figure 40. Activating One-Time Programming

Read Bit Pattern

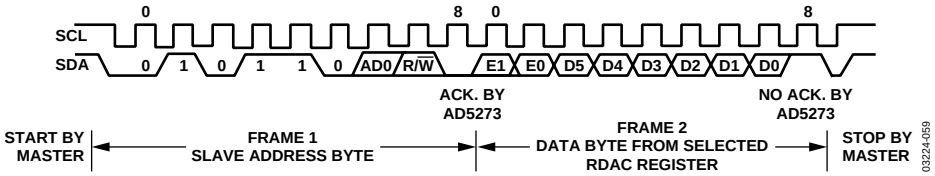

Figure 41. Reading Data from the RDAC Register

For users who do not use the software solution, the AD5273 can be controlled via an I²C-compatible serial bus and is connected to this bus as a slave device. Referring to Figure 39, Figure 40, and Figure 41, the 2-wire I²C serial bus protocol operates as follows:

1. The master initiates data transfer by establishing a start condition. A start condition is defined as a high-to-low transition on the SDA line while SCL is high, as shown in Figure 39. The byte following the start condition is the slave address byte, which consists of six MSBs defined as 010110. The next bit is AD0; it is an I²C device address bit. Depending on the states of the AD0 bits, two AD5273s can be addressed on the same bus, as shown in Figure 42. The last LSB is the R/$\overline{W}$ bit, which determines whether data is read from or written to the slave device.

   The slave address corresponding to the transmitted address responds by pulling the SDA line low during the ninth clock pulse (this is termed the acknowledge bit). At this stage, all other devices on the bus remain idle while the selected device waits for data to be written to or read from its serial register.

2. A write operation contains one more instruction byte than the read operation. The instruction byte in the write mode follows the slave address byte. The MSB of the instruction byte labeled T is the OTP bit. After acknowledging the instruction byte, the last byte in the write mode is the data byte. Data is transmitted over the serial bus in sequences of nine clock pulses (eight data bits followed by an acknowledge bit). The transitions on the SDA line must occur during the low period of SCL and remain stable during the high period of SCL, as shown in Figure 39.

3. In read mode, the data byte follows immediately after the acknowledgment of the slave address byte. Data is transmitted over the serial bus in sequences of nine clock pulses (slight difference from write mode, there are eight data bits followed by a no acknowledge bit). Similarly, the transitions on the SDA line must occur during the low period of SCL and remain stable during the high period of SCL, as shown in Figure 41.

4. When all data bits have been read or written, a stop condition is established by the master. A stop condition is defined as a low-to-high transition on the SDA line while SCL is high. In write mode, the master pulls the SDA line high during the 10th clock pulse to establish a stop condition, as shown in Figure 39 and Figure 40. In read mode, the master issues a no acknowledge for the ninth clock pulse, that is, the SDA line remains high. The master then brings the SDA line low before the 10th clock pulse, which goes high to establish a stop condition, as shown in Figure 41.

   A repeated write function gives the user flexibility to update the RDAC output continuously, except after permanent programming, when the part is addressed and receives instructions only once. During the write cycle, each data byte updates the RDAC output. For example, after the RDAC has acknowledged its slave address and instruction bytes, the RDAC output updates after these two bytes. If another byte is written to the RDAC while it is still addressed to a specific slave device with the same instruction, this byte updates the output of the selected slave device. If different instructions are needed, the write mode must be started again with a new slave address, instruction, and data bytes. Similarly, a repeated read function of the RDAC is also allowed.

CONTROLLING TWO DEVICES ON ONE BUS

Figure 42 shows two AD5273 devices on the same serial bus. Each has a different slave address because the state of each AD0 pin is different. This allows each device to operate independently. The master device output bus line drivers are open-drain pull-down in a fully I²C-compatible interface.

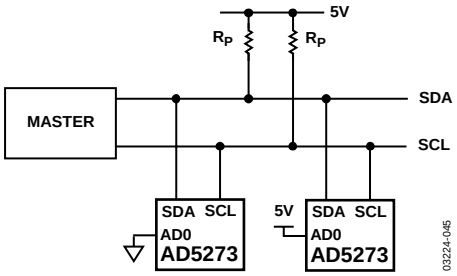

Figure 42. Two AD5273 Devices on One Bus

APPLICATIONS INFORMATION

DAC

It is common to buffer the output of the digital potentiometer as a DAC. The buffer minimizes the load dependence and delivers higher current to the load, if needed.

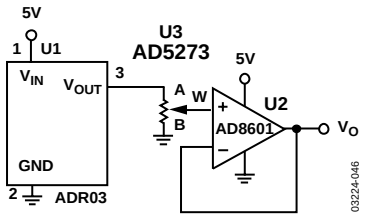

Figure 43. Programmable Voltage Reference (DAC)

PROGRAMMABLE VOLTAGE SOURCE WITH BOOSTED OUTPUT

For applications that require high current adjustment, such as a laser diode driver or tunable laser, consider a booster voltage source, as shown in Figure 44.

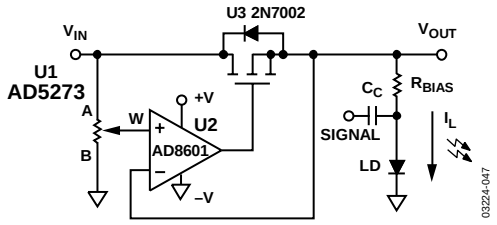

Figure 44. Programmable Booster Voltage Source

In this circuit, the inverting input of the op amp forces the V_{OUT} to be equal to the wiper voltage set by the digital potentiometer. The load current is then delivered by the supply via the N-Channel FET, N_1. N_1 power handling must be adequate to dissipate $(V_{IN} - V_{OUT}) \times I_L$ power. This circuit can source a maximum of 100 mA with a 5 V supply. For precision applications, a voltage reference, such as the ADR421, ADR03, or ADR3420, can be applied at Terminal A of the digital potentiometer.

PROGRAMMABLE CURRENT SOURCE

A programmable current source can be implemented with the circuit shown in Figure 45. The load current is the voltage across Terminal B to Terminal W of the AD5273 divided by R_S. At zero scale, Terminal A of the AD5273 is −2.048 V, which makes the wiper voltage clamped at ground potential. Depending on the load, Equation 5 is therefore valid only at certain codes. For example, when the compliance voltage, V_L, equals half of V_{REF}, the current can be programmed from midscale to full scale of the AD5273.

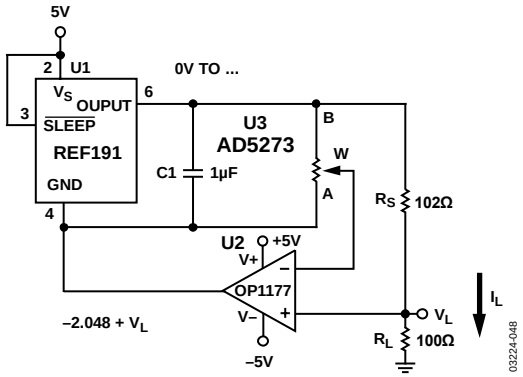

Figure 45. Programmable Current Source

$$I_L = \frac{(V_{REF} \times D)/64}{R_S} \mid 32 \le D \le 63 \quad (5)$$

GAIN CONTROL COMPENSATION

As shown in Figure 46, the digital potentiometers are commonly used in gain controls or sensor transimpedance amplifier signal conditioning applications.

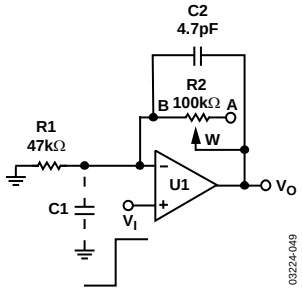

Figure 46. Typical Noninverting Gain Amplifier

In both applications, one of the digital potentiometer terminals is connected to the op amp inverting node with finite terminal capacitance, C1. It introduces a zero for the 1 β_o term with 20 dB/dec, whereas a typical op amp GBP has −20 dB/dec characteristics. A large R2 and finite C1 can cause this zero's frequency to fall well below the crossover frequency. Therefore, the rate of closure becomes 40 dB/dec and the system has a 0° phase margin at the crossover frequency. The output may ring, or in the worst case, oscillate when the input is a step function. Similarly, it is also likely to ring when switching between two gain values because this is equivalent to a step change at the input. To reduce the effect of C1, users should also configure Terminal B or Terminal A rather than Terminal W at the inverting node.

Depending on the op amp GBP, reducing the feedback resistor may extend the zero's frequency far enough to overcome the problem. A better approach is to include a compensation capacitor, C2, to cancel the effect caused by C1. Optimum compensation occurs when R1 × C1 = R2 × C2, but this is not an option because of the variation of R2. As a result, users can use the relationship described and scale C2 as if R2 were at its maximum value. However, doing so may overcompensate by slowing down the settling time when R2 is set to low values. To avoid this problem, C2 should be found empirically for a given application. In general, setting C2 in the range of a few picofarads to no more than a few tenths of a picofarad is usually adequate for compensation.

There is also a Terminal W capacitance connected to the output (not shown); its effect on stability is less significant; therefore, compensation is not necessary unless the op amp is driving a large capacitive load.

PROGRAMMABLE LOW-PASS FILTER

In ADC applications, it is common to include an antialiasing filter to band-limit the sampling signal. To minimize various system redesigns, users can use two 1 kΩ AD5273s to construct a generic second-order Sallen-Key low-pass filter. Because the AD5273 is a single-supply device, the input must be dc offset when an ac signal is applied to avoid clipping at ground. This is illustrated in Figure 47. The design equations are

$$\frac{V_O}{V_I} = \frac{\omega_O^2}{S^2 + \frac{\omega_O}{Q}S + \omega_O^2} \quad (6)$$

$$\omega_O = \sqrt{\frac{1}{R1R2C1C2}} \quad (7)$$

$$Q = \frac{1}{R1C1} + \frac{1}{R2C2} \quad (8)$$

Users can first select some convenient values for the capacitors. To achieve maximally flat bandwidth where Q = 0.707, let C1 be twice the size of C2 and let R1 = R2. As a result, R1 and R2 can be adjusted to the same setting to achieve the desired bandwidth.

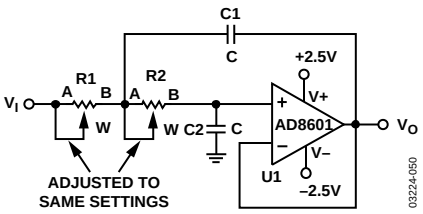

Figure 47. Sallen Key Low-Pass Filter

LEVEL SHIFT FOR DIFFERENT VOLTAGES OPERATION

If the SCL and SDA signals come from a low voltage logic controller and are below the minimum V_{IH} level (0.7 × V_{DD}), level-shift the signals for successful read/write communication between the AD5273 and the controller. Figure 48 shows one of the implementations. For example, when SDA1 is 2.5 V, M1 turns off, and SDA2 becomes 5 V. When SDA1 is 0 V, M1 turns on, and SDA2 approaches 0 V. As a result, proper level-shifting is established. M1 and M2 should be low threshold N-Channel power MOSFETs, such as FDV301N.

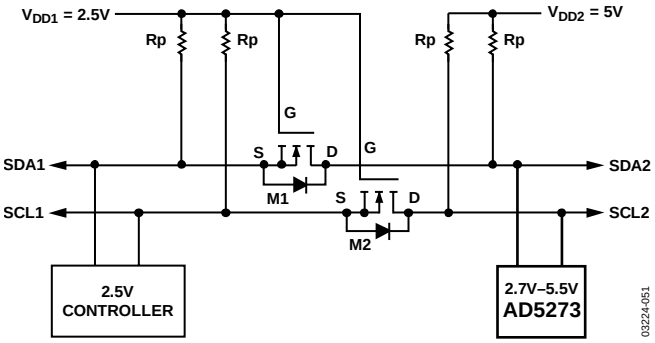

Figure 48. Level Shift for Different Voltages Operation

RDAC CIRCUIT SIMULATION MODEL

The internal parasitic capacitances and the external capacitive loads dominate the ac characteristics of the digital potentiometers. Configured as a potentiometer divider, the −3 dB bandwidth of the AD5273 (1 kΩ resistor) measures 6 MHz at half scale. Figure 17 to Figure 20 provide the large signal BODE plot characteristics of the four available resistor versions: 1 kΩ, 10 kΩ, 50 kΩ, and 100 kΩ. Figure 49 shows a parasitic simulation model. The code following Figure 49 provides a macro model net list for the 1 kΩ device.

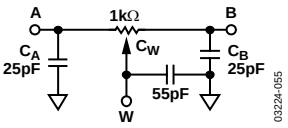

Figure 49. Circuit Simulation Model for RDAC = 1 kΩ

Macro Model Net List for RDAC

```
.PARAM D = 63, RDAC = 1E3
*
.SUBCKT DPOT (A,W,B)
*
CA A 0 25E-12
RWA A W {(1-D/63)*RDAC+60}
CW W 0 55E-12
RWB W B {D/63*RDAC+60}
CB B 0 25E-12
*
.ENDS DPOT
```

OUTLINE DIMENSIONS

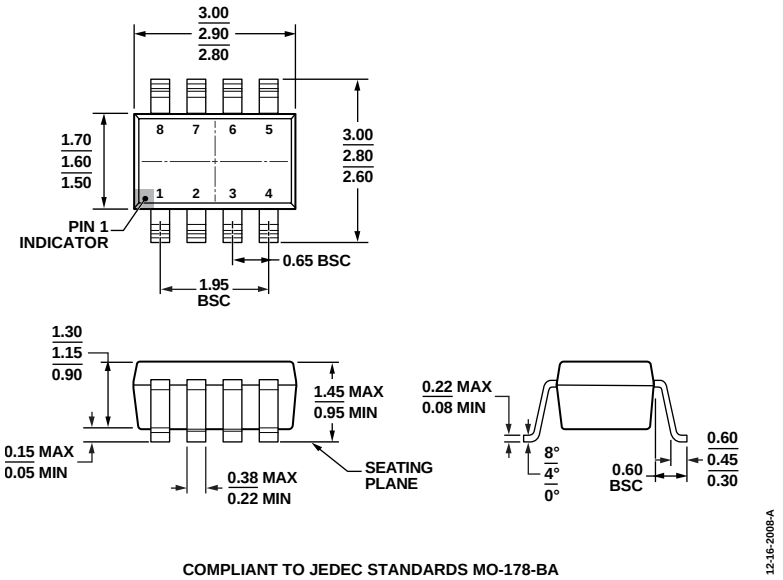

Figure 50. 8-Lead Small Outline Transistor Package [SOT-23]
(RJ-8)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	R_{AB} (kΩ)	Temperature Range	Package Option	Package Description	Ordering Quantity	Branding
AD5273BRJZ1-R2	1	−40°C to +105°C	RJ-8	8-Lead SOT-23	250	DD8
AD5273BRJZ1-REEL7	1	−40°C to +105°C	RJ-8	8-Lead SOT-23	3,000	DD8
AD5273BRJZ10-R2	10	−40°C to +105°C	RJ-8	8-Lead SOT-23	250	DD9
AD5273BRJZ10-R7	10	−40°C to +105°C	RJ-8	8-Lead SOT-23	3,000	DD9
AD5273BRJZ50-REEL7	50	−40°C to +105°C	RJ-8	8-Lead SOT-23	3,000	DDC
AD5273BRJZ100-R2	100	−40°C to +105°C	RJ-8	8-Lead SOT-23	250	DDD
AD5273BRJZ100-R7	100	−40°C to +105°C	RJ-8	8-Lead SOT-23	3,000	DDD
EVAL-AD5273DBZ				Evaluation Board		

[1] Z = RoHS Compliant Part.

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).