TABLE OF CONTENTS

REVISION HISTORY

4/16—Rev. B to Rev. C

Changes to Applications Section and General Description Section ... 1
Changed Digital Inputs and Outputs Parameter to Digital Inputs Parameter, Table 1 ... 3
Changed Digital Inputs and Outputs Parameter to Digital Inputs Parameter, Table 2 ... 4
Changes to Ordering Guide ... 19

4/12—Rev. A to Rev. B

Changes to Rheostat Operation Section, Table 7, and Table 8 ... 13
Changes to Voltage Output Operation Section ... 14
Deleted Evaluation Board Section and Figure 45, Renumbered Sequentially ... 15
Changes to Table 13 ... 17
Updated Outline Dimensions ... 19
Changes to Ordering Guide ... 19

4/09—Rev. 0 to Rev. A

Changes to DC Characteristics—Rheostat Mode Parameter and to DC Characteristics—Potentiometer Divider Mode Parameter, Table 1 ... 3
Moved Figure 3 ... 5
Updated Outline Dimensions ... 19
Changes to Ordering Guide ... 19

1/04—Revision 0: Initial Version

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SPECIFICATIONS

ELECTRICAL CHARACTERISTICS: 2.5 kΩ VERSION

V_{DD} = 5 V ± 10%, or 3 V ± 10%; $V_A = V_{DD}$; V_B = 0 V; −40°C < T_A < +125°C; unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
DC CHARACTERISTICS—RHEOSTAT MODE						
Resistor Differential Nonlinearity[2]	R-DNL	R_{WB}, V_A = no connect	−2	±0.1	+2	LSB
Resistor Integral Nonlinearity[2]	R-INL	R_{WB}, V_A = no connect	−14	±2	+14	LSB
Nominal Resistor Tolerance[3]	ΔR_{AB}	T_A = 25°C	−20		+55	%
Resistance Temperature Coefficient	$(\Delta R_{AB}/R_{AB})/\Delta T$	$V_{AB} = V_{DD}$, wiper = no connect		35		ppm/°C
Wiper Resistance	R_{WB}	Code = 0x00, V_{DD} = 5 V		160	200	Ω
DC CHARACTERISTICS—POTENTIOMETER DIVIDER MODE[4]						
Differential Nonlinearity[5]	DNL		−1.5	±0.1	+1.5	LSB
Integral Nonlinearity[5]	INL		−2	±0.6	+2	LSB
Voltage Divider Temperature Coefficient	$(\Delta V_W/V_W)/\Delta T$	Code = 0x80		15		ppm/°C
Full-Scale Error	V_{WFSE}	Code = 0xFF	−14	−5.5	0	LSB
Zero-Scale Error	V_{WZSE}	Code = 0x00	0	4.5	12	LSB
RESISTOR TERMINALS						
Voltage Range[6]	V_A, V_B, V_W		GND		V_{DD}	V
Capacitance A, B[7]	C_A, C_B	f = 1 MHz, measured to GND, code = 0x80		45		pF
Capacitance W[7]	C_W	f = 1 MHz, measured to GND, code = 0x80		60		pF
Shutdown Supply Current[8]	I_{A_SD}	V_{DD} = 5.5 V		0.01	1	µA
Common-Mode Leakage	I_{CM}	$V_A = V_B = V_{DD}/2$		1		nA
DIGITAL INPUTS						
Input Logic High	V_{IH}	V_{DD} = 5 V	2.4			V
Input Logic Low	V_{IL}	V_{DD} = 5 V			0.8	V
Input Logic High	V_{IH}	V_{DD} = 3 V	2.1			V
Input Logic Low	V_{IL}	V_{DD} = 3 V			0.6	V
Input Current	I_{IL}	V_{IN} = 0 V or 5 V			±1	µA
Input Capacitance[7]	C_{IL}			5		pF
POWER SUPPLIES						
Power Supply Range	$V_{DD\ RANGE}$		2.7		5.5	V
Supply Current	I_{DD}	V_{IH} = 5 V or V_{IL} = 0 V		3.5	6	µA
Power Dissipation[9]	P_{DISS}	V_{IH} = 5 V or V_{IL} = 0 V, V_{DD} = 5 V			30	µW
Power Supply Sensitivity	PSS	V_{DD} = 5 V ± 10%, code = midscale		±0.02	±0.08	%/%
DYNAMIC CHARACTERISTICS[10]						
Bandwidth, −3 dB	BW	Code = 0x80		4.8		MHz
Total Harmonic Distortion	THD_W	V_A = 1 V rms, V_B = 0 V, f = 1 kHz		0.1		%
V_W Settling Time	t_S	V_A = 5 V, V_B = 0 V, ±1 LSB error band		1		µs
Resistor Noise Voltage Density	e_{N_WB}	R_{WB} = 1.25 kΩ, R_S = 0		3.2		nV/√Hz

[1] Typical specifications represent average readings at 25°C and V_{DD} = 5 V.
[2] Resistor position nonlinearity error, R-INL, is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from the ideal between successive tap positions. Parts are guaranteed monotonic.
[3] $V_A = V_{DD}$, V_B = 0 V, wiper (V_W) = no connect.
[4] Specifications apply to all VRs.
[5] INL and DNL are measured at V_W with the RDAC configured as a potentiometer divider similar to a voltage output digital-to-analog converter (DAC). $V_A = V_{DD}$ and V_B = 0 V. DNL specification limits of ±1 LSB maximum are guaranteed monotonic operating conditions.
[6] Resistor Terminal A, Resistor Terminal B, and Resistor Terminal W have no limitations on polarity with respect to each other.
[7] Guaranteed by design, but not subject to production test.
[8] Measured at the A terminal. The A terminal is open circuited in shutdown mode.
[9] P_{DISS} is calculated from ($I_{DD} \times V_{DD}$). CMOS logic level inputs result in minimum power dissipation.
[10] All dynamic characteristics use V_{DD} = 5 V.

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ELECTRICAL CHARACTERISTICS: 10 kΩ, 50 kΩ, AND 100 kΩ VERSIONS

V_{DD} = 5 V ± 10%, or 3 V ± 10%; $V_A = V_{DD}$; V_B = 0 V; −40°C < T_A < 125°C; unless otherwise noted.

Table 2.

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
DC CHARACTERISTICS—RHEOSTAT MODE						
Resistor Differential Nonlinearity[2]	R-DNL	R_{WB}, V_A = no connect	−1	±0.1	+1	LSB
Resistor Integral Nonlinearity[2]	R-INL	R_{WB}, V_A = no connect	−2.5	±0.25	+2.5	LSB
Nominal Resistor Tolerance[3]	ΔR_{AB}	T_A = 25°C	−20		+20	%
Resistance Temperature Coefficient	$(\Delta R_{AB}/R_{AB})/\Delta T$	$V_{AB} = V_{DD}$, wiper = no connect		35		ppm/°C
Wiper Resistance	R_{WB}	Code = 0x00, V_{DD} = 5 V		160	200	Ω
DC CHARACTERISTICS—POTENTIOMETER DIVIDER MODE[4]						
Differential Nonlinearity[5]	DNL		−1	±0.1	+1	LSB
Integral Nonlinearity[5]	INL		−1	±0.3	+1	LSB
Voltage Divider Temperature Coefficient	$(\Delta V_W/V_W)/\Delta T$	Code = 0x80		15		ppm/°C
Full-Scale Error	V_{WFSE}	Code = 0xFF	−2.5	−1	0	LSB
Zero-Scale Error	V_{WZSE}	Code = 0x00	0	1	2.5	LSB
RESISTOR TERMINALS						
Voltage Range[6]	V_A, V_B, V_W		GND		V_{DD}	V
Capacitance A, B[7]	C_A, C_B	f = 1 MHz, measured to GND, code = 0x80		45		pF
Capacitance W[7]	C_W	f = 1 MHz, measured to GND, code = 0x80		60		pF
Shutdown Supply Current[8]	I_{A_SD}	V_{DD} = 5.5 V		0.01	1	µA
Common-Mode Leakage	I_{CM}	$V_A = V_B = V_{DD}/2$		1		nA
DIGITAL INPUTS						
Input Logic High	V_{IH}	V_{DD} = 5 V	2.4			V
Input Logic Low	V_{IL}	V_{DD} = 5 V			0.8	V
Input Logic High	V_{IH}	V_{DD} = 3 V	2.1			V
Input Logic Low	V_{IL}	V_{DD} = 3 V			0.6	V
Input Current	I_{IL}	V_{IN} = 0 V or 5 V			±1	µA
Input Capacitance	C_{IL}			5		pF
POWER SUPPLIES						
Power Supply Range	$V_{DD\ RANGE}$		2.7		5.5	V
Supply Current	I_{DD}	V_{IH} = 5 V or V_{IL} = 0 V		3.5	6	µA
Power Dissipation	P_{DISS}	V_{IH} = 5 V or V_{IL} = 0 V, V_{DD} = 5 V			30	µW
Power Supply Sensitivity	PSS	V_{DD} = 5 V ± 10%, code = midscale		±0.02	±0.08	%/%
DYNAMIC CHARACTERISTICS						
Bandwidth, −3 dB	BW	R_{AB} = 10 kΩ/50 kΩ/100 kΩ, code = 0x80		600/100/40		kHz
Total Harmonic Distortion	THD_W	V_A = 1 V rms, V_B = 0 V, f = 1 kHz, R_{AB} = 10 kΩ		0.1		%
V_W Settling Time	t_S	V_A = 5 V, V_B = 0 V, ±1 LSB error band		2		µs
Resistor Noise Voltage Density	e_{N_WB}	R_{WB} = 5 kΩ, R_S = 0		9		nV/√Hz

[1] Typical specifications represent average readings at 25°C and V_{DD} = 5 V.
[2] Resistor position nonlinearity error, R-INL, is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from the ideal between successive tap positions. Parts are guaranteed monotonic.
[3] $V_A = V_{DD}$, V_B = 0 V, wiper (V_W) = no connect.
[4] Specifications apply to all VRs.
[5] INL and DNL are measured at V_W with the RDAC configured as a potentiometer divider similar to a voltage output DAC. $V_A = V_{DD}$ and V_B = 0 V. DNL specification limits of ±1 LSB maximum are guaranteed monotonic operating conditions.
[6] Resistor Terminal A, Resistor Terminal B, and Resistor Terminal W have no limitations on polarity with respect to each other.
[7] Guaranteed by design, but not subject to production test.
[8] Measured at the A terminal. The A terminal is open circuited in shutdown mode.

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TIMING CHARACTERISTICS: ALL VERSIONS

V_{DD} = 5 V ± 10%, or 3 V ± 10%; $V_A = V_{DD}$; V_B = 0 V; −40°C < T_A < +125°C; unless otherwise noted.

Table 3.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
I²C INTERFACE TIMING CHARACTERISTICS[1]						
SCL Clock Frequency	f_{SCL}		0		400	kHz
Bus-Free Time Between Stop and Start, t_{BUF}	t_1		1.3			µs
Hold Time (Repeated Start), $t_{HD;STA}$	t_2	After this period, the first clock pulse is generated.	0.6			µs
Low Period of SCL Clock, t_{LOW}	t_3		1.3			µs
High Period of SCL Clock, t_{HIGH}	t_4		0.6			µs
Setup Time for Repeated Start Condition, $t_{SU;STA}$	t_5		0.6			µs
Data Hold Time, $t_{HD;DAT}$[2]	t_6				0.9	µs
Data Setup Time, $t_{SU;DAT}$	t_7		100			ns
Fall Time of Both SDA and SCL Signals, t_F	t_8				300	ns
Rise Time of Both SDA and SCL Signals, t_R	t_9				300	ns
Setup Time for Stop Condition, $t_{SU;STO}$	t_{10}		0.6			µs

[1] See the timing diagrams for the locations of measured values (that is, see Figure 3 and Figure 45 to Figure 48).
[2] The maximum $t_{HD;DAT}$ must be met only if the device does not stretch the low period (t_{LOW}) of the SCL signal.

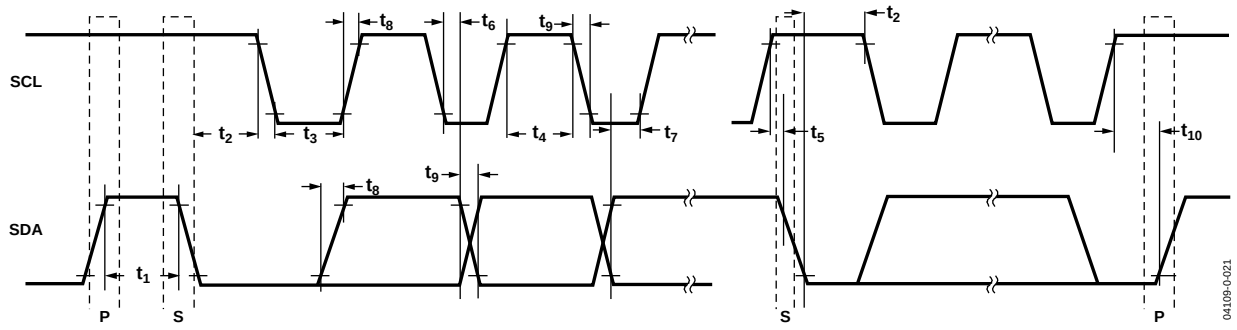

Figure 3. I²C Interface Detailed Timing Diagram

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ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 4.

Parameter	Rating
V_{DD} to GND	−0.3 V to +7 V
V_A, V_B, V_W to GND	V_{DD}
Terminal Current, Ax to Bx, Ax to Wx, Bx to Wx[1]	
Pulsed	±20 mA
Continuous	±5 mA
Digital Inputs and Output Voltage to GND	0 V to 7 V
Operating Temperature Range	−40°C to +125°C
Maximum Junction Temperature (T_{JMAX})	150°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C
Thermal Resistance, θ_{JA} for 10-Lead MSOP[2]	230°C/W

[1]The maximum terminal current is bound by the maximum current handling of the switches, the maximum power dissipation of the package, and the maximum applied voltage across any two of the A, B, and W terminals at a given resistance.
[2]The package power dissipation is ($T_{JMAX} - T_A$)/θ_{JA}.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

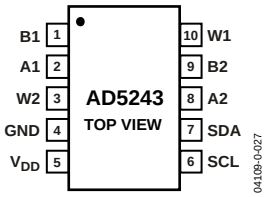

Figure 4. AD5243 Pin Configuration

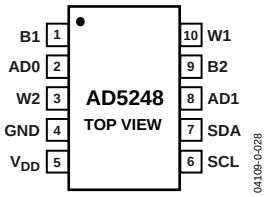

Figure 5. AD5248 Pin Configuration

Table 5. AD5243 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	B1	B1 Terminal.
2	A1	A1 Terminal.
3	W2	W2 Terminal.
4	GND	Digital Ground.
5	V_{DD}	Positive Power Supply.
6	SCL	Serial Clock Input. Positive-edge triggered.
7	SDA	Serial Data Input/Output.
8	A2	A2 Terminal.
9	B2	B2 Terminal.
10	W1	W1 Terminal.

Table 6. AD5248 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	B1	B1 Terminal.
2	AD0	Programmable Address Bit 0 for Multiple Package Decoding.
3	W2	W2 Terminal.
4	GND	Digital Ground.
5	V_{DD}	Positive Power Supply.
6	SCL	Serial Clock Input. Positive-edge triggered.
7	SDA	Serial Data Input/Output.
8	AD1	Programmable Address Bit 1 for Multiple Package Decoding.
9	B2	B2 Terminal.
10	W1	W1 Terminal.

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TYPICAL PERFORMANCE CHARACTERISTICS

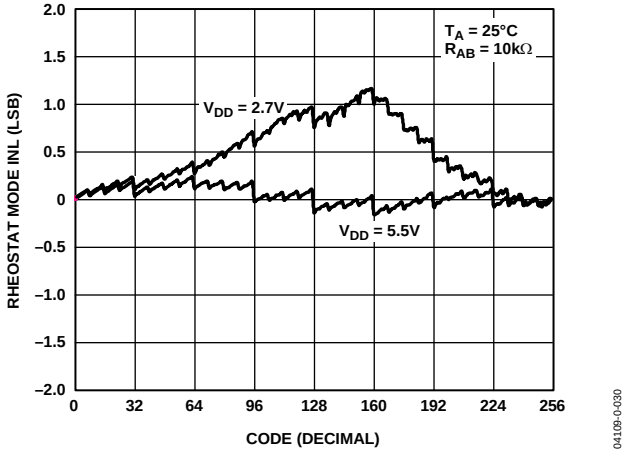

Figure 6. R-INL vs. Code vs. Supply Voltages

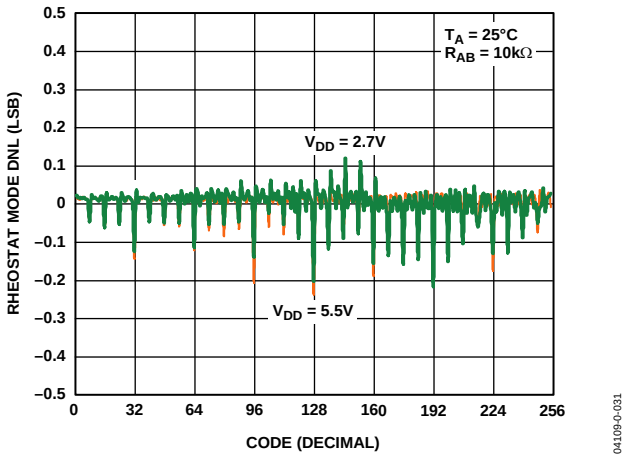

Figure 7. R-DNL vs. Code vs. Supply Voltages

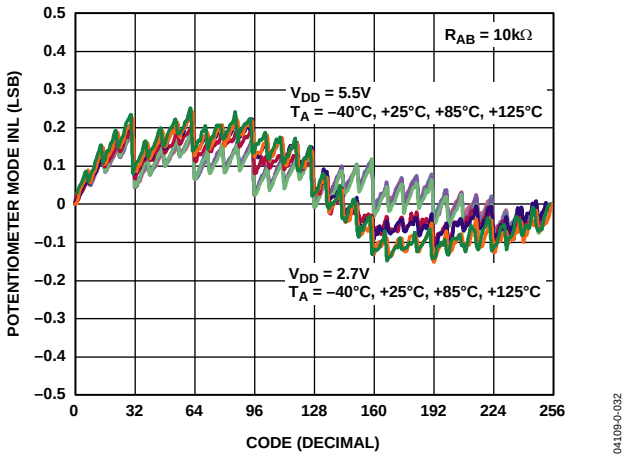

Figure 8. INL vs. Code vs. Temperature

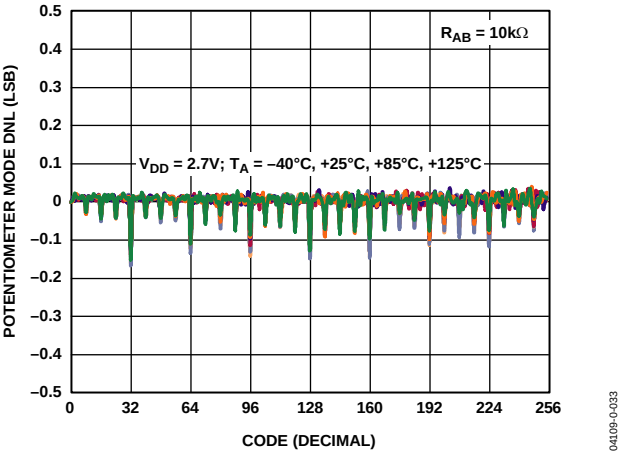

Figure 9. DNL vs. Code vs. Temperature

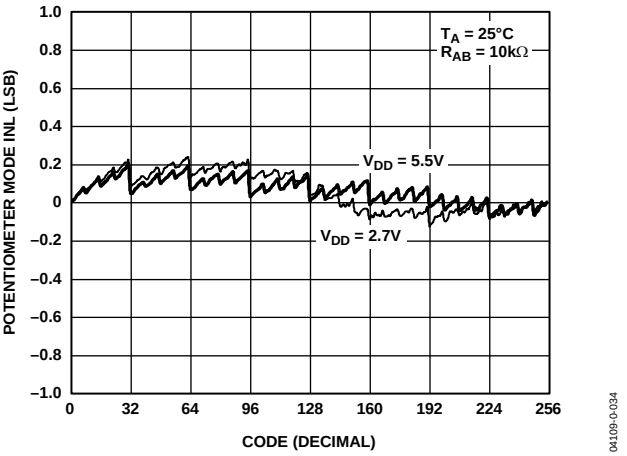

Figure 10. INL vs. Code vs. Supply Voltages

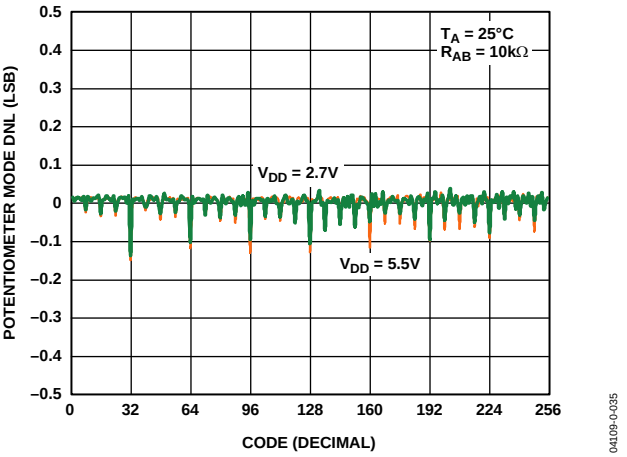

Figure 11. DNL vs. Code vs. Supply Voltages

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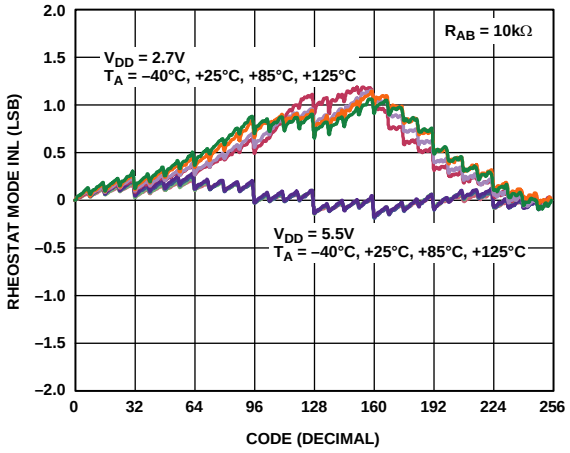

Figure 12. R-INL vs. Code vs. Temperature

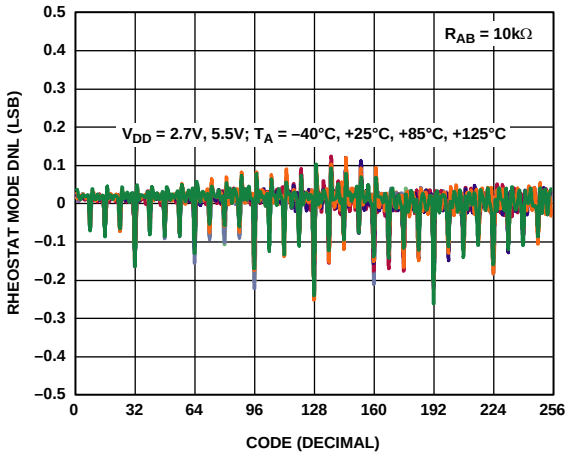

Figure 13. R-DNL vs. Code vs. Temperature

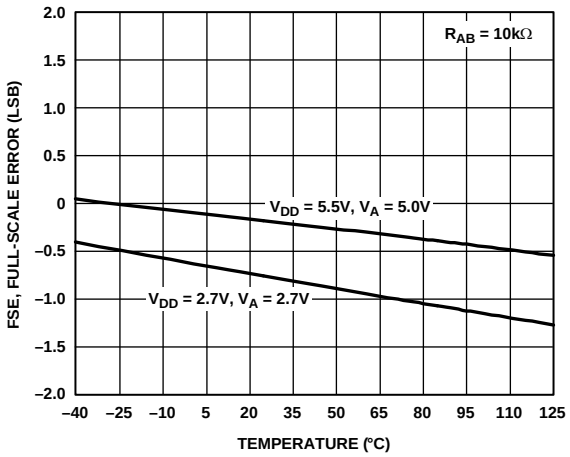

Figure 14. Full-Scale Error vs. Temperature

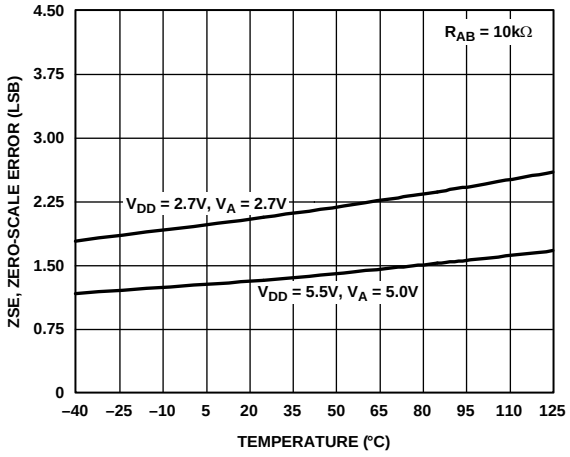

Figure 15. Zero-Scale Error vs. Temperature

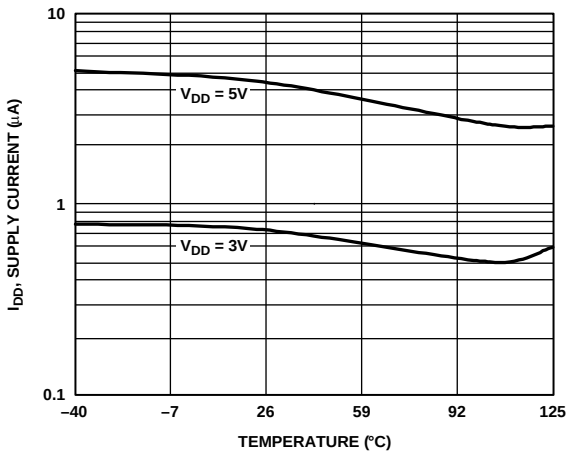

Figure 16. Supply Current vs. Temperature

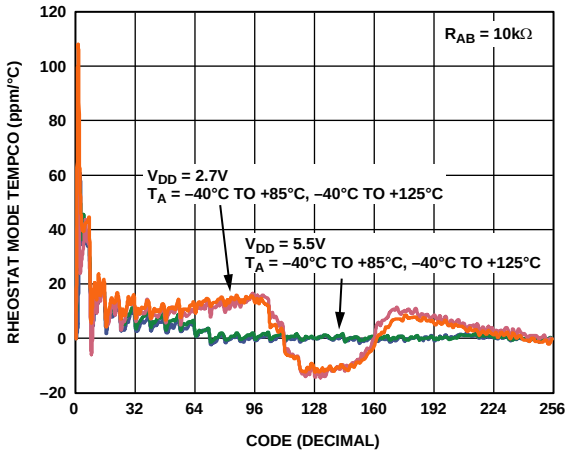

Figure 17. Rheostat Mode Tempco $\Delta R_{WB}/\Delta T$ vs. Code

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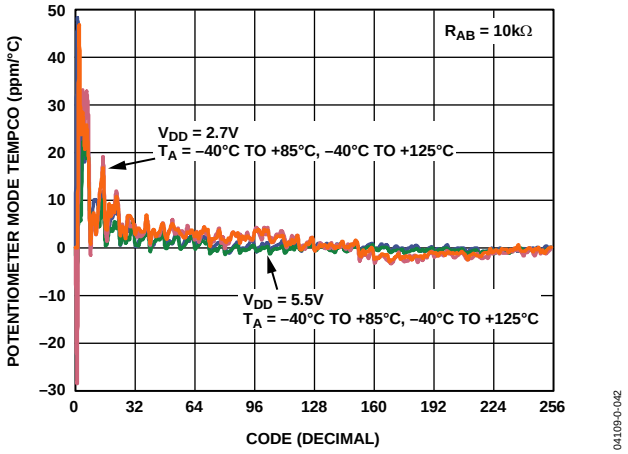

Figure 18. Potentiometer Mode Tempco $\Delta V_{WB}/\Delta T$ vs. Code

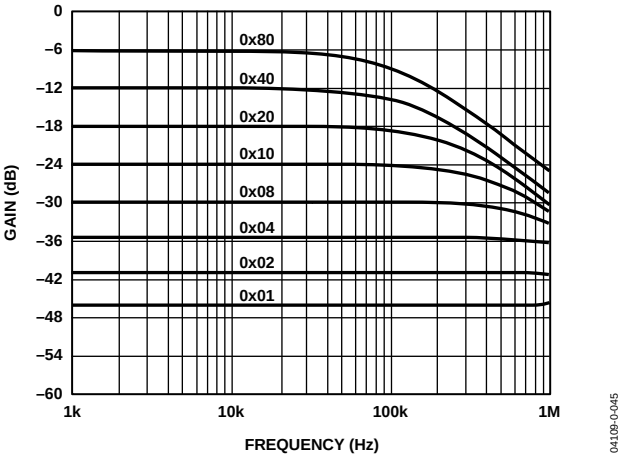

Figure 21. Gain vs. Frequency vs. Code, R_{AB} = 50 kΩ

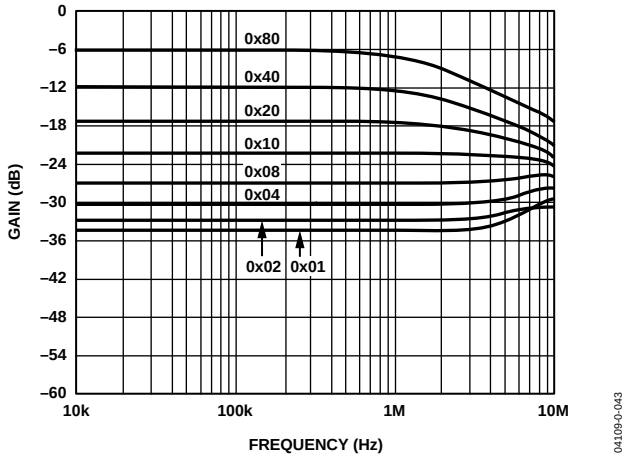

Figure 19. Gain vs. Frequency vs. Code, R_{AB} = 2.5 kΩ

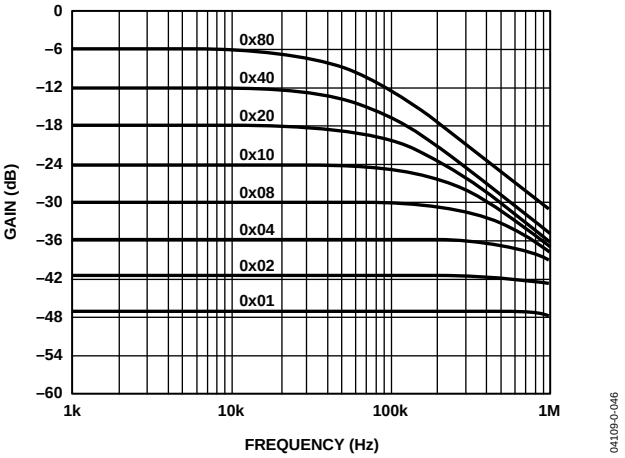

Figure 22. Gain vs. Frequency vs. Code, R_{AB} = 100 kΩ

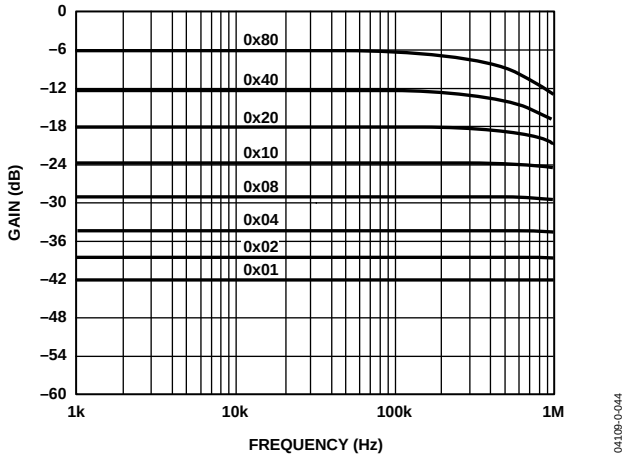

Figure 20. Gain vs. Frequency vs. Code, R_{AB} = 10 kΩ

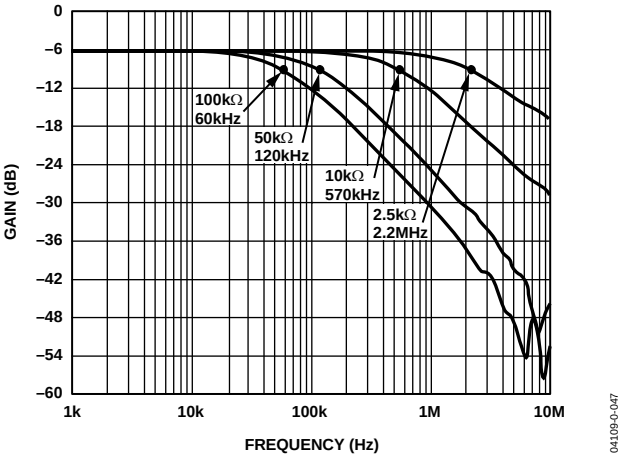

Figure 23. –3 dB Bandwidth at Code = 0x80

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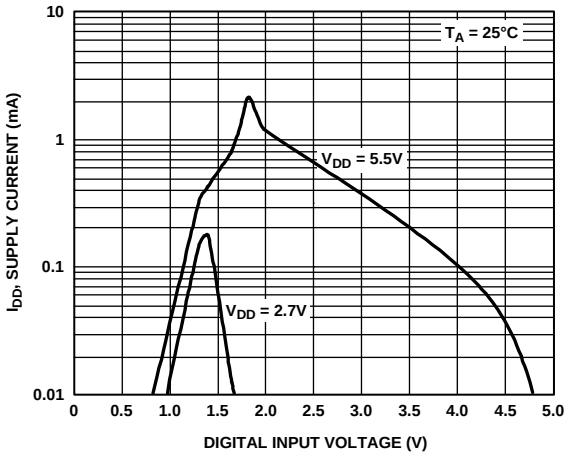

Figure 24. Supply Current vs. Digital Input Voltage

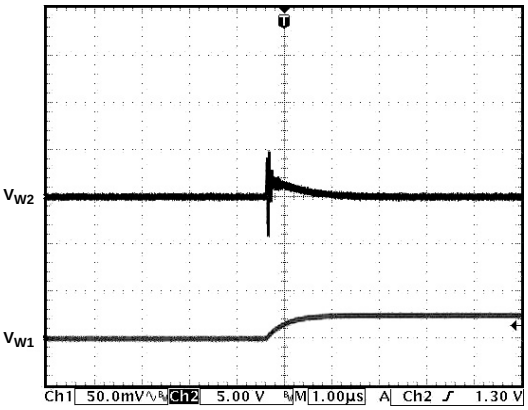

Figure 27. Analog Crosstalk

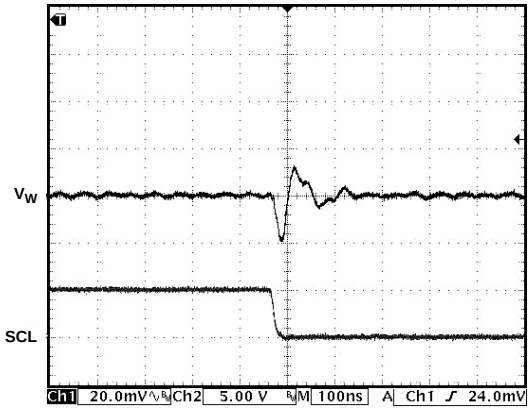

Figure 25. Digital Feedthrough

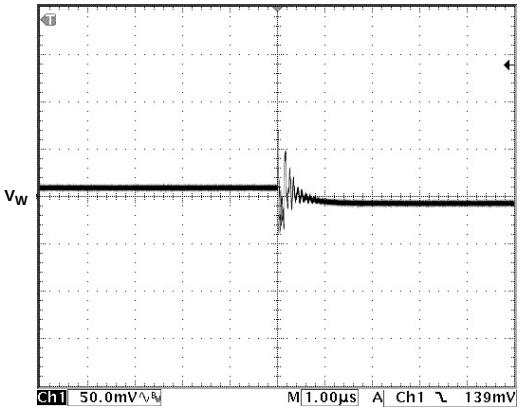

Figure 28. Midscale Glitch, Code 0x80 to Code 0x7F

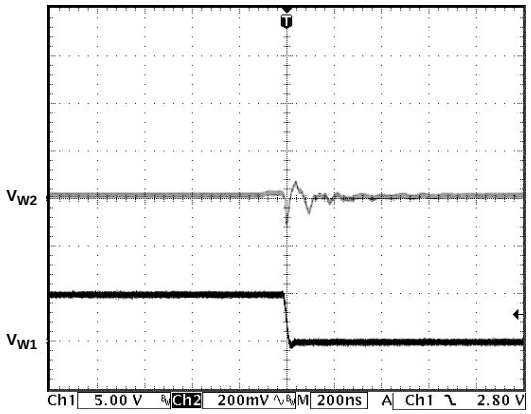

Figure 26. Digital Crosstalk

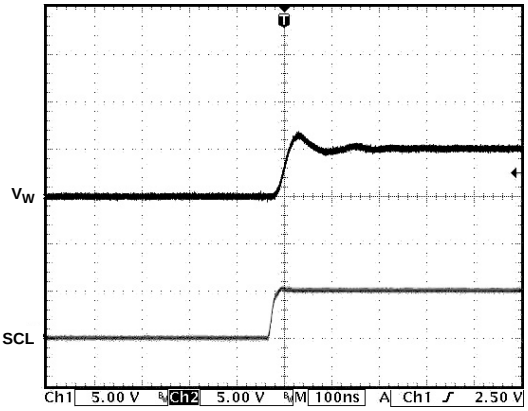

Figure 29. Large-Signal Settling Time

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TEST CIRCUITS

Figure 30 through Figure 36 illustrate the test circuits that define the test conditions used in the product specification tables (see Table 1 and Table 2).

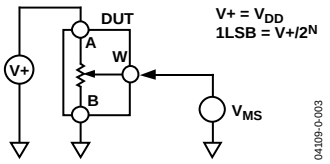

Figure 30. Test Circuit for Potentiometer Divider Nonlinearity Error (INL, DNL)

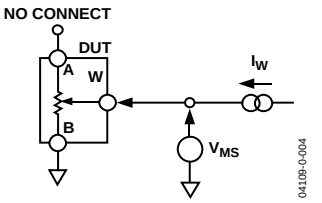

Figure 31. Test Circuit for Resistor Position Nonlinearity Error (Rheostat Operation: R-INL, R-DNL)

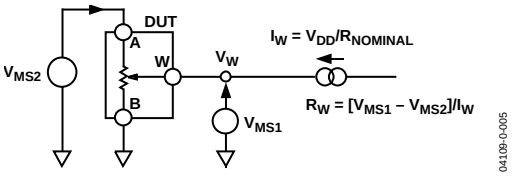

Figure 32. Test Circuit for Wiper Resistance

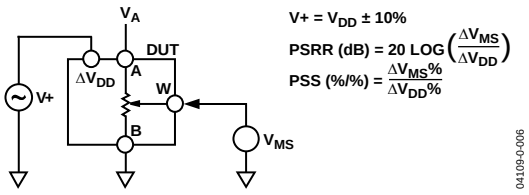

Figure 33. Test Circuit for Power Supply Sensitivity (PSS, PSSR)

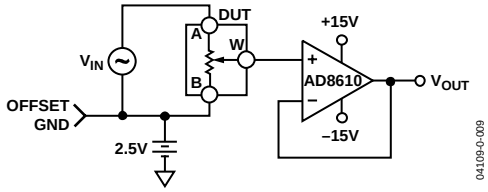

Figure 34. Test Circuit for Gain vs. Frequency

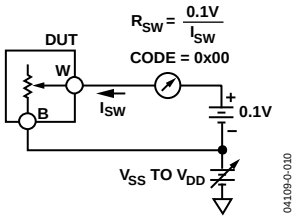

Figure 35. Test Circuit for Incremental On Resistance

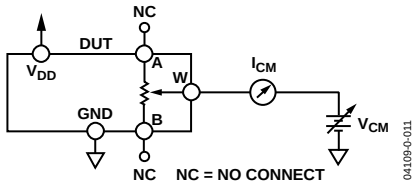

Figure 36. Test Circuit for Common-Mode Leakage Current

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THEORY OF OPERATION

The AD5243/AD5248 are 256-position, digitally controlled variable resistor (VR) devices.

An internal power-on preset places the wiper at midscale during power-on, which simplifies the fault condition recovery at power-up.

PROGRAMMING THE VARIABLE RESISTOR AND VOLTAGE

Rheostat Operation

The nominal resistance of the RDAC between Terminal A and Terminal B is available in 2.5 kΩ, 10 kΩ, 50 kΩ, and 100 kΩ. The nominal resistance (R_{AB}) of the VR has 256 contact points accessed by the wiper terminal and the B terminal contact. The 8-bit data in the RDAC latch is decoded to select one of the 256 possible settings.

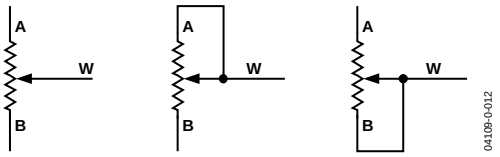

Figure 37. Rheostat Mode Configuration

Assuming that a 10 kΩ part is used, the first connection of the wiper starts at the B terminal for Data 0x00. Because there is a 160 Ω wiper contact resistance, such a connection yields a minimum of 320 Ω (2 × 160 Ω) resistance between Terminal W and Terminal B. The second connection is the first tap point, which corresponds to 359 Ω ($R_{WB} = R_{AB}/256 + 2 \times R_W$ = 39 Ω + 2 × 160 Ω) for Data 0x01. The third connection is the next tap point, representing 398 Ω (2 × 39 Ω + 2 × 160 Ω) for Data 0x02, and so on. Each LSB data value increase moves the wiper up the resistor ladder until the last tap point is reached at 10,281 Ω ($R_{AB} + 2 \times R_W$).

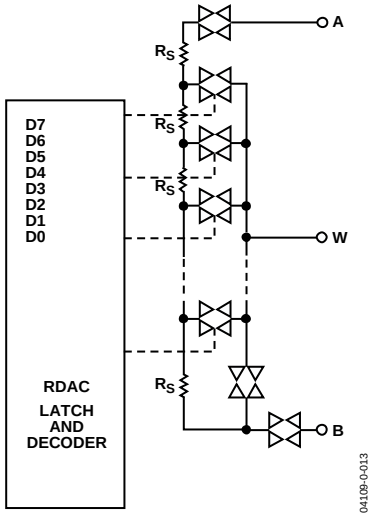

Figure 38. AD5243 Equivalent RDAC Circuit

The general equation determining the digitally programmed output resistance between W and B is

$$R_{WB}(D) = \frac{D}{256} \times R_{AB} + 2 \times R_W \quad (1)$$

where:
D is the decimal equivalent of the binary code loaded in the 8-bit RDAC register.
R_{AB} is the end-to-end resistance.
R_W is the wiper resistance contributed by the on resistance of the internal switch.

In summary, if R_{AB} is 10 kΩ and the A terminal is open circuited, the following output resistance, R_{WB}, is set for the indicated RDAC latch codes.

Table 7. Codes and Corresponding R_{WB} Resistance

D (Dec)	R_{WB} (Ω)	Output State
255	10,281	Full scale (R_{AB} − 1 LSB + 2 × R_W)
128	5380	Midscale
1	359	1 LSB + 2 × R_W
0	320	Zero scale (wiper contact resistance)

Note that in the zero-scale condition, a finite wiper resistance of 320 Ω is present. Care should be taken to limit the current flow between W and B in this state to a maximum pulse current of no more than 20 mA. Otherwise, degradation or possible destruction of the internal switch contact may occur.

Similar to the mechanical potentiometer, the resistance of the RDAC between Wiper W and Terminal A also produces a digitally controlled complementary resistance, R_{WA}. When these terminals are used, the B terminal can be opened. Setting the resistance value for R_{WA} starts at a maximum value of resistance and decreases as the data loaded in the latch increases in value. The general equation for this operation is

$$R_{WA}(D) = \frac{256 - D}{256} \times R_{AB} + 2 \times R_W \quad (2)$$

When R_{AB} is 10 kΩ and the B terminal is open circuited, the output resistance, R_{WA}, is set according to the RDAC latch codes, as listed in Table 8.

Table 8. Codes and Corresponding R_{WA} Resistance

D (Dec)	R_{WA} (Ω)	Output State
255	359	Full scale
128	5320	Midscale
1	10,280	1 LSB + 2 × R_W
0	10,320	Zero scale

Typical device-to-device matching is process-lot dependent and may vary by up to ±30%. Because the resistance element is processed in thin-film technology, the change in R_{AB} with temperature has a very low temperature coefficient of 35 ppm/°C.

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PROGRAMMING THE POTENTIOMETER DIVIDER

Voltage Output Operation

The digital potentiometer easily generates a voltage divider at wiper to B and wiper to A, proportional to the input voltage at A to B. Unlike the polarity of V_{DD} to GND, which must be positive, voltage across A to B, W to A, and W to B can be at either polarity.

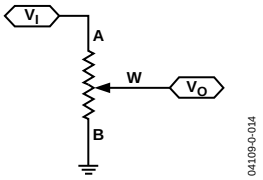

Figure 39. Potentiometer Mode Configuration

If ignoring the effect of the wiper resistance for approximation, connecting the A terminal to 5 V and the B terminal to ground produces an output voltage at the wiper to B, starting at 0 V up to 1 LSB less than 5 V. Each LSB of voltage is equal to the voltage applied across Terminal A and Terminal B divided by the 256 positions of the potentiometer divider. The general equation defining the output voltage at V_W with respect to ground for any valid input voltage applied to Terminal A and Terminal B is

$$V_W(D) = \frac{D}{256}V_A + \frac{256-D}{256}V_B \quad (3)$$

Operation of the digital potentiometer in the divider mode results in more accurate operation over temperature. Unlike in the rheostat mode, the output voltage is dependent mainly on the ratio of the internal resistors, R_{WA} and R_{WB}, not on the absolute values. Therefore, the temperature drift reduces to 15 ppm/°C.

ESD PROTECTION

All digital inputs are protected with a series of input resistors and parallel Zener ESD structures, as shown in Figure 40 and Figure 41. This applies to the SDA, SCL, AD0, and AD1 digital input pins (AD5248 only).

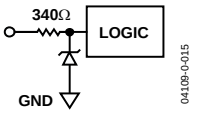

Figure 40. ESD Protection of Digital Pins

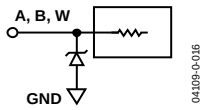

Figure 41. ESD Protection of Resistor Terminals

TERMINAL VOLTAGE OPERATING RANGE

The AD5243/AD5248 V_{DD} and GND power supply defines the boundary conditions for proper 3-terminal digital potentiometer operation. Supply signals present on the A, B, and W terminals that exceed V_{DD} or GND are clamped by the internal forward-biased diodes (see Figure 42).

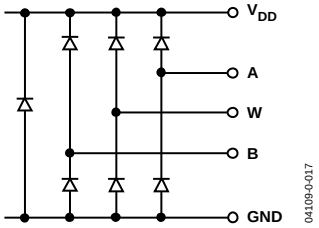

Figure 42. Maximum Terminal Voltages Set by V_{DD} and GND

POWER-UP SEQUENCE

Because the ESD protection diodes limit the voltage compliance at the A, B, and W terminals (see Figure 42), it is important to power V_{DD}/GND before applying voltage to the A, B, and W terminals; otherwise, the diode is forward-biased such that V_{DD} is powered unintentionally and may affect the rest of the user's circuit. The ideal power-up sequence is in the following order: GND, V_{DD}, digital inputs, and then V_A, V_B, and V_W. The relative order of powering V_A, V_B, V_W, and the digital inputs is not important, as long as they are powered after V_{DD}/GND.

LAYOUT AND POWER SUPPLY BYPASSING

It is a good practice to employ compact, minimum lead length layout design. The leads to the inputs should be as direct as possible with a minimum conductor length. Ground paths should have low resistance and low inductance.

Similarly, it is also good practice to bypass the power supplies with quality capacitors for optimum stability. Supply leads to the device should be bypassed with disc or chip ceramic capacitors of 0.01 µF to 0.1 µF. Low ESR 1 µF to 10 µF tantalum or electrolytic capacitors should also be applied at the supplies to minimize any transient disturbance and low frequency ripple (see Figure 43). In addition, note that the digital ground should be joined remotely to the analog ground at one point to minimize the ground bounce.

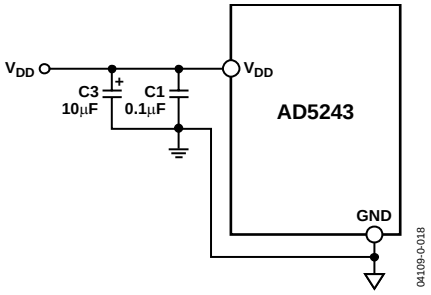

Figure 43. Power Supply Bypassing

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CONSTANT BIAS TO RETAIN RESISTANCE SETTING

For users who desire nonvolatility but cannot justify the additional cost of an EEMEM, the AD5243/AD5248 can be considered low cost alternatives by maintaining a constant bias to retain the wiper setting. The AD5243/AD5248 are designed specifically for low power applications, allowing low power consumption even in battery-operated systems. The graph in Figure 44 demonstrates the power consumption from a 3.4 V, 450 mAhr Li-Ion cell phone battery connected to the AD5243/AD5248. The measurement over time shows that the device draws approximately 1.3 μA and consumes negligible power. Over a course of 30 days, the battery is depleted by less than 2%, the majority of which is due to the intrinsic leakage current of the battery itself.

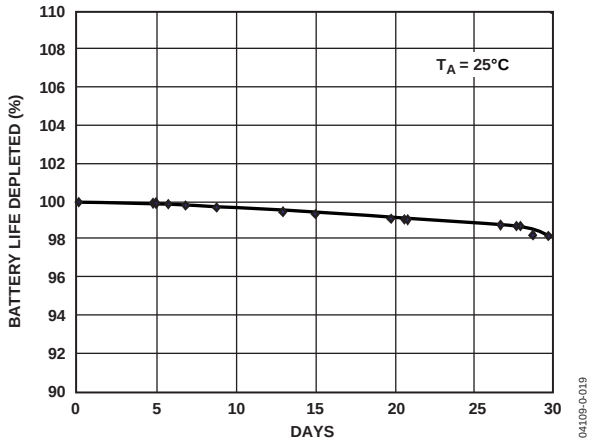

Figure 44. Battery Operating Life Depletion

This demonstrates that constantly biasing the potentiometer can be a practical approach. Most portable devices do not require the removal of batteries for the purpose of charging. Although the resistance setting of the AD5243/AD5248 is lost when the battery needs replacement, such events occur rather infrequently such that this inconvenience is justified by the lower cost and smaller size offered by the AD5243/AD5248. If total power is lost, the user should be provided with a means to adjust the setting accordingly.

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I²C INTERFACE

I²C COMPATIBLE, 2-WIRE SERIAL BUS

The 2-wire, I²C-compatible serial bus protocol operates as follows:

1. The master initiates data transfer by establishing a start condition, which is when a high-to-low transition on the SDA line occurs while SCL is high (see Figure 45). The following byte is the slave address byte, which consists of the slave address followed by an R/$\overline{W}$ bit (this bit determines whether data is read from or written to the slave device). The AD5243 has a fixed slave address byte, whereas the AD5248 has two configurable address bits, AD0 and AD1 (see Figure 10).

   The slave whose address corresponds to the transmitted address responds by pulling the SDA line low during the ninth clock pulse (this is called the acknowledge bit). At this stage, all other devices on the bus remain idle while the selected device waits for data to be written to or read from its serial register. If the R/$\overline{W}$ bit is high, the master reads from the slave device. On the other hand, if the R/$\overline{W}$ bit is low, the master writes to the slave device.

2. In the write mode, the second byte is the instruction byte. The first bit (MSB) of the instruction byte is the RDAC subaddress select bit. A logic low selects Channel 1 and a logic high selects Channel 2.

   The second MSB, SD, is a shutdown bit. A logic high causes an open circuit at Terminal A while shorting the wiper to Terminal B. This operation yields almost 0 Ω in rheostat mode or 0 V in potentiometer mode. It is important to note that the shutdown operation does not disturb the contents of the register. When the AD5243 or AD5248 is brought out of shutdown, the previous setting is applied to the RDAC. In addition, during shutdown, new settings can be programmed. When the part is returned from shutdown, the corresponding VR setting is applied to the RDAC.

   The remainder of the bits in the instruction byte are don't care bits (see Figure 10).

   After acknowledging the instruction byte, the last byte in write mode is the data byte. Data is transmitted over the serial bus in sequences of nine clock pulses (eight data bits followed by an acknowledge bit). The transitions on the SDA line must occur during the low period of SCL and remain stable during the high period of SCL (see Figure 45 and Figure 46).

3. In the read mode, the data byte follows immediately after the acknowledgment of the slave address byte. Data is transmitted over the serial bus in sequences of nine clock pulses (a slight difference with the write mode, where there are eight data bits followed by an acknowledge bit). Similarly, the transitions on the SDA line must occur during the low period of SCL and remain stable during the high period of SCL (see Figure 47 and Figure 48).

   Note that the channel of interest is the one that is previously selected in write mode. If users need to read the RDAC values of both channels, they need to program the first channel in write mode and then change to read mode to read the first channel value. After that, the user must return the device to write mode with the second channel selected and read the second channel value in read mode. It is not necessary for users to issue the Frame 3 data byte in write mode for subsequent readback operation. Users should refer to Figure 47 and Figure 48 for the programming format.

4. After all data bits have been read or written, a stop condition is established by the master. A stop condition is defined as a low-to-high transition on the SDA line while SCL is high. In write mode, the master pulls the SDA line high during the 10th clock pulse to establish a stop condition (see Figure 45 and Figure 46). In read mode, the master issues a no acknowledge for the ninth clock pulse (that is, the SDA line remains high). The master then brings the SDA line low before the 10th clock pulse, which goes high to establish a stop condition (see Figure 47 and Figure 48).

   A repeated write function provides the user with the flexibility of updating the RDAC output multiple times after addressing and instructing the part only once. For example, after the RDAC has acknowledged its slave address and instruction bytes in write mode, the RDAC output updates on each successive byte. If different instructions are needed, however, the write/read mode must restart with a new slave address, instruction, and data byte. Similarly, a repeated read function of the RDAC is also allowed.

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Write Mode

Table 9. AD5243 Write Mode

S	0	1	0	1	1	1	1	W	A	A0	SD	X	X	X	X	X	X	A	D7	D6	D5	D4	D3	D2	D1	D0	A	P
	Slave address byte									Instruction byte									Data byte									

Table 10. AD5248 Write Mode

S	0	1	0	1	1	AD1	AD0	W	A	A0	SD	X	X	X	X	X	X	A	D7	D6	D5	D4	D3	D2	D1	D0	A	P
	Slave address byte									Instruction byte									Data byte									

Read Mode

Table 11. AD5243 Read Mode

S	0	1	0	1	1	1	1	R	A	D7	D6	D5	D4	D3	D2	D1	D0	A	P
	Slave address byte									Data byte									

Table 12. AD5248 Read Mode

S	0	1	0	1	1	AD1	AD0	R	A	D7	D6	D5	D4	D3	D2	D1	D0	A	P
	Slave address byte									Data byte									

Table 13. SDA Bits Descriptions

Bit	Description
S	Start condition.
P	Stop condition.
A	Acknowledge.
AD0, AD1	Package pin-programmable address bits.
X	Don't care.
$\overline{W}$	Write.
R	Read.
A0	RDAC subaddress select bit.
SD	Shutdown connects wiper to B terminal and open circuits the A terminal. It does not change the contents of the wiper register.
D7, D6, D5, D4, D3, D2, D1, D0	Data bits.

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I²C CONTROLLER PROGRAMMING

Write Bit Patterns

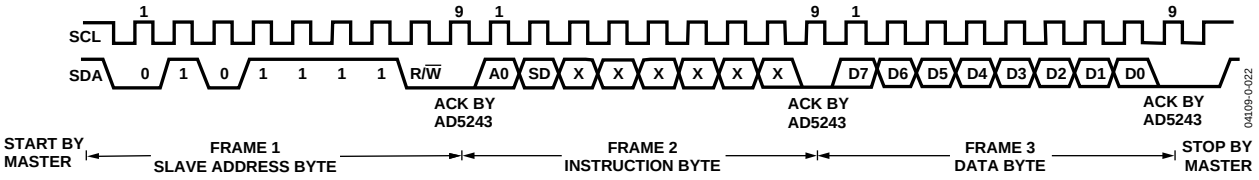

Figure 45. Writing to the RDAC Register—AD5243

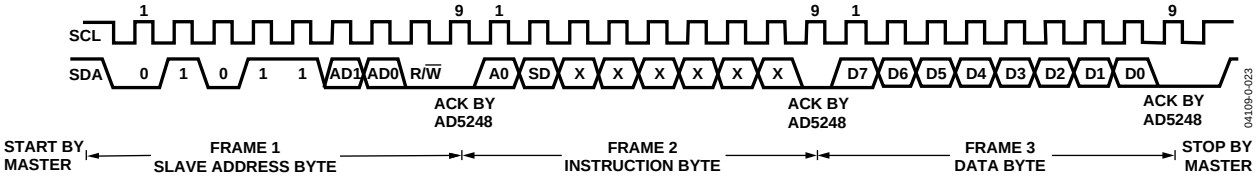

Figure 46. Writing to the RDAC Register—AD5248

Read Bit Patterns

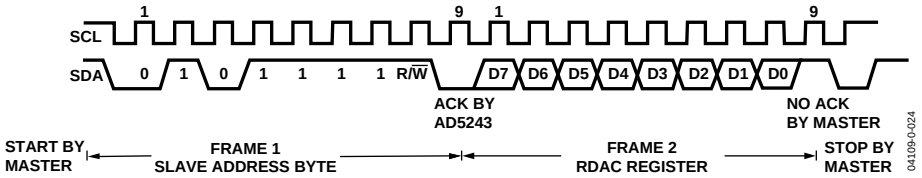

Figure 47. Reading Data from a Previously Selected RDAC Register in Write Mode—AD5243

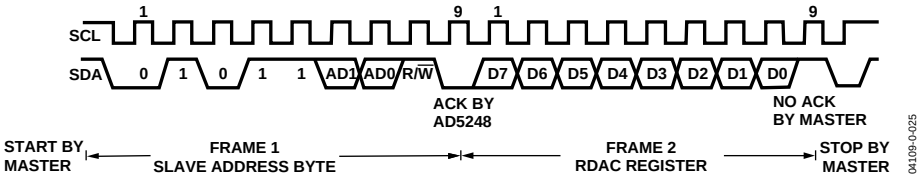

Figure 48. Reading Data from a Previously Selected RDAC Register in Write Mode—AD5248

Multiple Devices on One Bus (Applies Only to AD5248)

Figure 49 shows four AD5248 devices on the same serial bus. Each has a different slave address because the states of their AD0 and AD1 pins are different. This allows each device on the bus to be written to or read from independently. The master device output bus line drivers are open-drain pull-downs in a fully I²C-compatible interface.

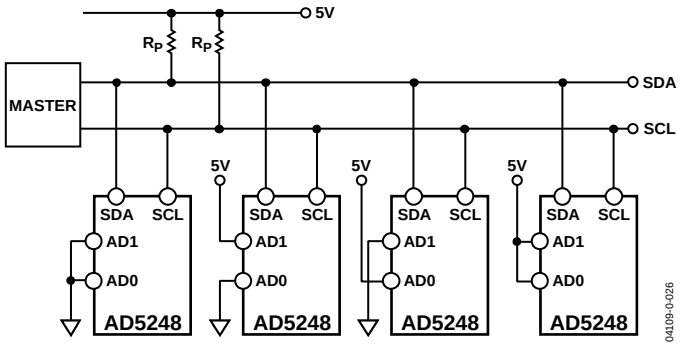

Figure 49. Multiple AD5248 Devices on One I²C Bus

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OUTLINE DIMENSIONS

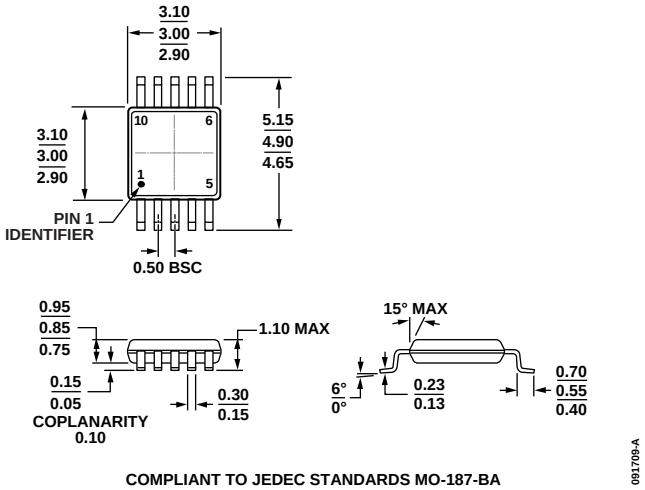

Figure 50. 10-Lead Mini Small Outline Package [MSOP]
(RM-10)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2]	R_{AB}	Temperature	Package Description	Package Option	Branding
AD5243BRM2.5	2.5 kΩ	−40°C to +125°C	10-Lead MSOP	RM-10	D0L
AD5243BRM10	10 kΩ	−40°C to +125°C	10-Lead MSOP	RM-10	D0M
AD5243BRM100	100 kΩ	−40°C to +125°C	10-Lead MSOP	RM-10	D0P
AD5243BRMZ2.5	2.5 kΩ	−40°C to +125°C	10-Lead MSOP	RM-10	D9X
AD5243BRMZ2.5-RL7	2.5 kΩ	−40°C to +125°C	10-Lead MSOP	RM-10	D9X
AD5243BRMZ10	10 kΩ	−40°C to +125°C	10-Lead MSOP	RM-10	D0M
AD5243BRMZ10-RL7	10 kΩ	−40°C to +125°C	10-Lead MSOP	RM-10	D0M
AD5243BRMZ50	50 kΩ	−40°C to +125°C	10-Lead MSOP	RM-10	D0N
AD5243BRMZ50-RL7	50 kΩ	−40°C to +125°C	10-Lead MSOP	RM-10	D0N
AD5243BRMZ100	100 kΩ	−40°C to +125°C	10-Lead MSOP	RM-10	D0P
AD5243BRMZ100-RL7	100 kΩ	−40°C to +125°C	10-Lead MSOP	RM-10	D0P
EVAL-AD5243SDZ			Evaluation Board		
AD5248BRM100	100 kΩ	−40°C to +125°C	10-Lead MSOP	RM-10	D1J
AD5248BRMZ2.5	2.5 kΩ	−40°C to +125°C	10-Lead MSOP	RM-10	D1F
AD5248BRMZ2.5-RL7	2.5 kΩ	−40°C to +125°C	10-Lead MSOP	RM-10	D1F
AD5248BRMZ10	10 kΩ	−40°C to +125°C	10-Lead MSOP	RM-10	D8Z
AD5248BRMZ10-RL7	10 kΩ	−40°C to +125°C	10-Lead MSOP	RM-10	D8Z
AD5248BRMZ50	50 kΩ	−40°C to +125°C	10-Lead MSOP	RM-10	D90
AD5248BRMZ50-RL7	50 kΩ	−40°C to +125°C	10-Lead MSOP	RM-10	D90
AD5248BRMZ100	100 kΩ	−40°C to +125°C	10-Lead MSOP	RM-10	D91
AD5248BRMZ100-RL7	100 kΩ	−40°C to +125°C	10-Lead MSOP	RM-10	D91

[1] Z = RoHS Compliant Part.
[2] The evaluation board is shipped with the 10 kΩ R_{AB} resistor option; however, the board is compatible with all available resistor value options.

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NOTES

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

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