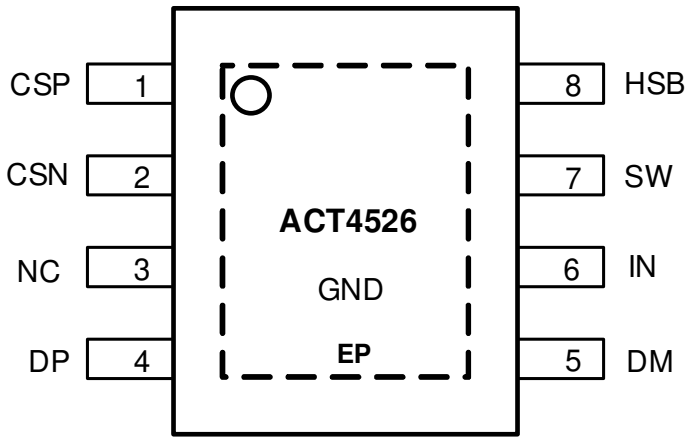
ORDERING INFORMATION

PART NUMBER	OPERATION TEMPERATURE RANGE	PACKAGE	FREQUENCY	PACKING
ACT4526YH-T	-40°C to 85°C	SOP-8EP	125kHz	TAPE & REEL

PIN CONFIGURATION



SOP-8EP

Top View

PIN DESCRIPTIONS

PIN	NAME	DESCRIPTION
1	CSP	Voltage Feedback Input. Connect to node of the inductor and output capacitor. CSP and CSN Kevin sense is recommended.
2	CSN	Negative input terminal of output current sense. Connect to the negative terminal of current sense resistor
3	NC	Not connected.
4	DP	Data Line Positive Input. Connected to D+ of attached portable device data line. This pin passes 8kV HBM ESD.
5	DM	Data Line Negative Input. Connected to D- of attached portable device data line. This pin passes 8kV HBM ESD.
6	IN	Power Supply Input. Bypass this pin with a 10μF ceramic capacitor to GND, placed as close to the IC as possible.
7	SW	Power Switching Output to External Inductor.
8	HSB	High Side Bias Pin. This provides power to the internal high-side MOSFET gate driver. Connect a 22nF capacitor from HSB pin to SW pin.
9	GND	Ground and Heat Dissipation Pad. Connect this exposed pad to large ground copper area with copper and vias.

ABSOLUTE MAXIMUM RATINGS①

PARAMETER	VALUE	UNIT
IN to GND	-0.3 to 40	V
SW to GND	-1 to V_{IN} + 1	V
HSB to GND	V_{SW} - 0.3 to V_{SW} + 7	V
CSP, CSN to GND	-0.3 to +15	V
All other pins to GND	-0.3 to +6	V
Junction to Ambient Thermal Resistance	46	°C/W
Operating Junction Temperature	-40 to 150	°C
Storage Junction Temperature	-55 to 150	°C
Lead Temperature (Soldering 10 sec.)	300	°C

①: Do not exceed these limits to prevent damage to the device. Exposure to absolute maximum rating conditions for long periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = 12V, T_A = 25˚C, unless otherwise specified.)

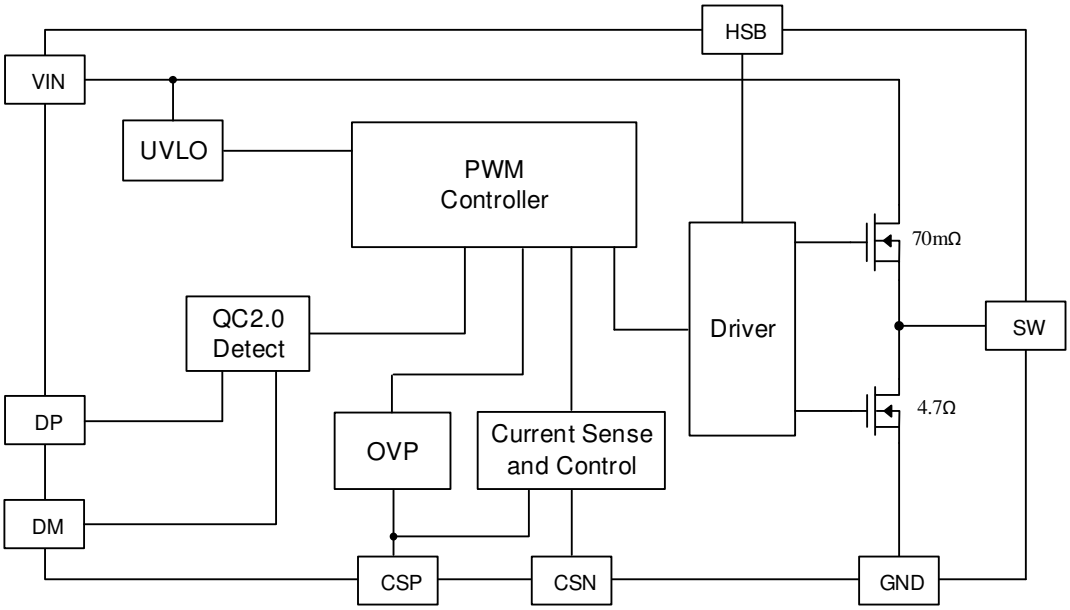
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Over Voltage Protection	VIN_OVP	Rising	40	42	44	V
Input Over Voltage Hysteresis				4		V
Input Over Voltage Response Time	T_VIN_OVP	VIN step from 30V to 45V		250		ns
Input Under Voltage Lockout (UVLO)	VIN	Rising		4.5		V
Input UVLO Hysteresis				200		mV
Input Voltage Power Good Deglitch Time		No OVP		40		ms
		No UVP		10		us
Input Standby Current		Vin=12V, Vout=5.1V, Iload=0		500		uA
Output Voltage Regulation	CSP		5.05 9.0 11.95	5.1 9.1 12.1	5.15 9.2 12.25	V
Output Over Voltage Protection (OVP)		Output rising		5.7 10.1 13.5		V
Output Over Voltage Deglitch Time				1.0		us
Output Voltage Cord Compensation		Output current 2.4A	-15%	200	+15%	mV
Output Under Voltage Protection (UVP)	VOUT	VOUT falling	-10%	3.2	10%	V
UVP Hysteresis	VOUT	VOUT rising		0.2		V
UVP Deglitch Time	VOUT			10		us
UVP Blanking Time at Startup				3.5		ms
Output Constant Current Limit		Rcs=25mΩ	2.50	2.65	2.80	A
Hiccup Waiting Time				4.13		S
Top FET Cycle by Cycle Current Limit			4.5	5.8		A
Top FET Rdson				70		mΩ
Bottom FET Rdson				4.7		Ω
Maximum Duty Cycle			99			%
Switching Frequency			-10%	125	+10%	kHz
Soft-Start Time				2.0		ms

ELECTRICAL CHARACTERISTICS

(V_{IN} = 12V, T_A = 25˚C, unless otherwise specified.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Out Voltage Ripples		Cout=470uF/22uF ceramic		80		mV
VOUT Discharge Current		For high to lower voltage transitions		60		mA
Voltage transition time for QC 2.0 transition		12V-5V			100	ms
		5V-12V			100	ms
Line Transient Response		Input 12V-40V-12V with 1V/us slew rate, Vout=5V, Iload=0A and 2.4A	4.75		5.25	V
Load Transient Response	Vout=5V	80mA-1.0A-80mA load with 0.1A/us slew rate	4.9	5.15	5.4	V
	Vout=9V	80mA-1.0A-80mA load with 0.1A/us slew rate	8.7	9.1	9.5	V
	Vout=12V	80mA-1.0A-80mA load with 0.1A/us slew rate	11.6	12.1	12.6	V
Thermal Shut Down				160		°C
Thermal Shut Down Hysteresis				30		°C
ESD of DP, DM		HBM		8		kV

FUNCTIONAL BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

Output Current Sensing and Regulation

Sense resistor is connected to CSP and CSN. The sensed differential voltage is compared with interval reference to regulate current. CC loop and CV loop are in parallel. The current loop response is allowed to have slower response compared to voltage loop. However, during current transient response, the inductor current overshoot/undershoot should be controlled within +/-25% to avoid inductor saturation.

Cycle-by-Cycle Current Control

The conventional cycle-by-cycle peak current mode is implemented with high-side FET current sense.

Input Over Voltage Protection

The converter is disabled if the input voltage is above 42V (+/-2V). Device resumes operation automatically 40ms after OVP is cleared.

Output Over Voltage Protection

Device stops switching when output over-voltage is sensed, and resumes operation automatically when output voltage drops to OVP - hysteresis.

Output Over Voltage Discharge

Discharge circuit starts to discharge output through CSP pins when output over voltage is detected. Discharge circuit brings 12V down to 5V in less than 100ms.

Output Under-Voltage Protection / Hiccup Mode

There is a under voltage protection (UVP) threshold. If the UVP threshold is hit for 10us, an over current or short circuit is assumed, and the converter goes into hiccup mode by disabling the converter and restarts after hiccup waiting period.

Cord Compensation

In some applications, the output voltage is increased with output current to compensate the potential voltage drop across output cable. The compensation is based on the high side feedback resistance.

The compensation voltage is derived as:

$\Delta Vout = (V_{CSP}-V_{CSN})*K$

Where K=3.03

This voltage difference could be added on the reference or turning the (V_{CSP}-V_{CSN}) voltage into a sink current at FB pin to pull Vout higher than programmed voltage.

The cord compensation loop should be very slow to avoid potential disturbance to the voltage loop. The voltage loop should be sufficiently stable on various cord compensation setting.

Thermal Shutdown

If the T_J increases beyond 160°C, ACT4526 goes into HZ mode and the timer is preserved until T_J drops by 30°C.

APPLICATIONS INFORMATION

Inductor Selection

The inductor maintains a continuous current to the output load. This inductor current has a ripple that is dependent on the inductance value.

Higher inductance reduces the peak-to-peak ripple current. The trade off for high inductance value is the increase in inductor core size and series resistance, and the reduction in current handling capability. In general, select an inductance value L based on ripple current requirement:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN}\, f_{SW}\, I_{LOADMAX}\, K_{RIPPLE}} \quad (1)$$

Where VIN is the input voltage, VOUT is the output voltage, fSW is the switching frequency, ILOADMAX is the maximum load current, and KRIPPLE is the ripple factor. Typically, choose KRIPPLE = 30% to correspond to the peak-to-peak ripple current being 30% of the maximum load current.

With a selected inductor value the peak-to-peak inductor current is estimated as:

$$I_{LPK-PK} = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{L \times V_{IN} \times f_{SW}} \quad (2)$$

The peak inductor current is estimated as:

$$I_{LPK} = I_{LOADMAX} + \frac{1}{2} I_{LPK-PK} \quad (3)$$

The selected inductor should not saturate at I_{LPK}. The maximum output current is calculated as:

$$I_{OUTMAX} = I_{LIM} - \frac{1}{2} I_{LPK-PK} \quad (4)$$

L_{LIM} is the internal current limit.

Input Capacitor

The input capacitor needs to be carefully selected to maintain sufficiently low ripple at the supply input of the converter. A low ESR capacitor is highly recommended. Since large current flows in and out of this capacitor during switching, its ESR also affects efficiency.

The input capacitance needs to be higher than 10µF. The best choice is the ceramic type. However, low ESR tantalum or electrolytic types may also be used provided that the RMS ripple current rating is higher than 50% of the output current. The input capacitor should be placed close to the IN and GND pins of the IC, with the shortest traces possible. In the case of tantalum or electrolytic types, a ceramic capacitor is recommended to parallel with tantalum or electrolytic capacitor, which should be placed right next to the IC.

Output Capacitor

The output capacitor also needs to have low ESR to keep low output voltage ripple. The output ripple voltage is:

$$V_{RIPPLE} = I_{LPK-PK}\left(R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{OUT}}\right) \quad (5)$$

Where I_{OUTMAX} is the maximum output current, K_{RIPPLE} is the ripple factor, R_{ESR} is the ESR of the output capacitor, f_{SW} is the switching frequency, L is the inductor value, and C_{OUT} is the output capacitance. In the case of ceramic output capacitors, R_{ESR} is very small and does not contribute to the ripple. Therefore, a lower capacitance value can be used for ceramic type. In the case of tantalum or electrolytic capacitors, the ripple is dominated by R_{ESR} multiplied by the ripple current. In that case, the output capacitor is chosen to have sufficiently low ESR.

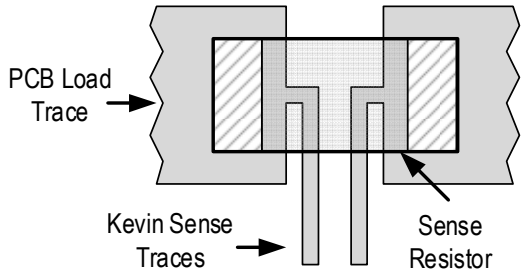
For ceramic output capacitor, typically choose a capacitance of about 22µF. For tantalum or electrolytic capacitors, choose a capacitor with less than 50mΩ ESR. If an 330µF or 470µF electrolytic capacitor is used, where ripple is dominantly caused by ESR, an 2.2uF ceramic in parallel is recommended.

Rectifier Schottky Diode

Use a Schottky diode as the rectifier to conduct current when the High-Side Power Switch is off. The Schottky diode must have current rating higher than the maximum output current and a reverse voltage rating higher than the maximum input voltage. Further more, the low forward voltage Schottky is preferable for high efficiency and smoothly operation.

Current Sense Resistor

The traces leading to and from the sense resistor can be significant error sources. With small value sense resistors, trace resistance shared with the load can cause significant errors. It is recommended to connect the sense resistor pads directly to the CSP and CSN pins using “Kelvin” or “4-wire” connection techniques as shown below.



Current Limit Setting

If output current hits current limit, output voltage drops to keep the current to a constant value.

The following equation calculates the constant current limit.

$$ILimit\ (A) = \frac{66\ mV}{Rcs\ (m\Omega)} \quad (6)$$

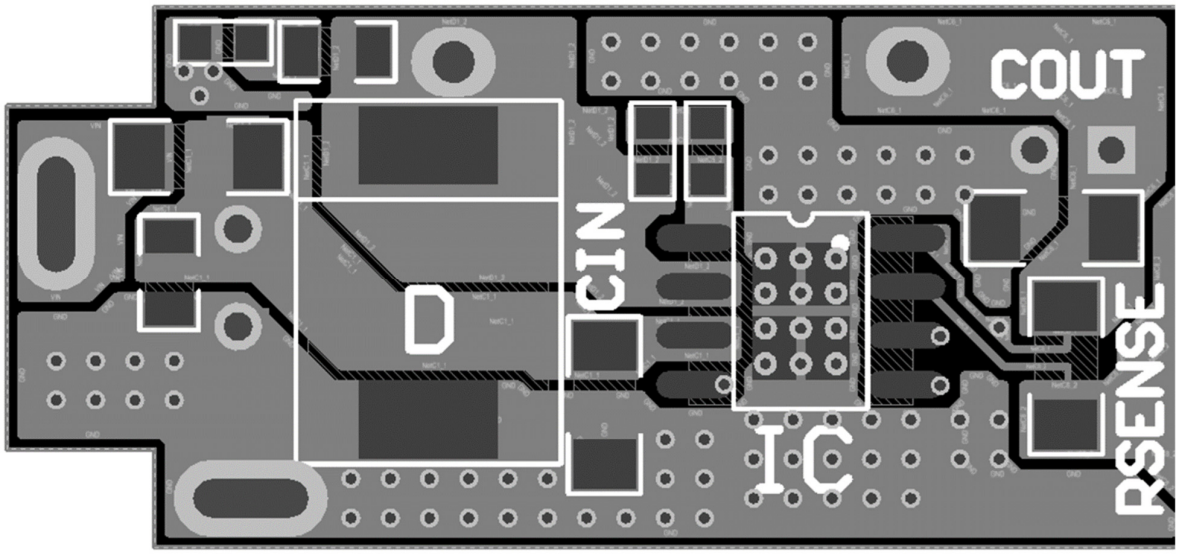
Where Rcs is current sense resistor.

PCB Layout Guidance

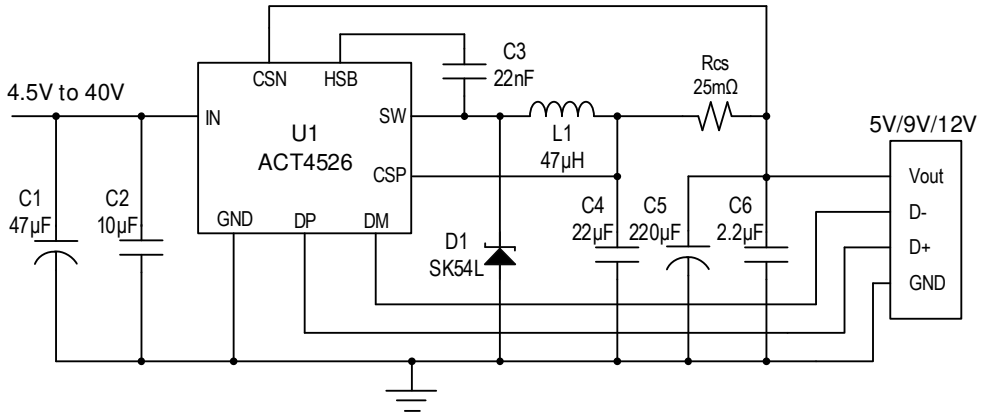
When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the IC.

1) Arrange the power components to reduce the AC loop size consisting of C_{IN}, V_{IN} pin, SW pin and the Schottky diode.
2) The high power loss components, e.g. the controller, Schottky diode, and the inductor should be placed carefully to make the thermal spread evenly on the board.
3) Place input decoupling ceramic capacitor C_{IN} as close to VIN pin as possible. C_{IN} should be connected to power GND with several vias or short and wide copper trace.
4) Schottky anode pad and IC exposed pad should be placed close to ground clips in CLA applications.
5) Use “Kelvin” or “4-wire” connection techniques from the sense resistor pads directly to the CSP and CSN1, CSN2 pins. The CSP and CSN1, CSN2 traces should be in parallel to avoid interference.
6) Place multiple vias between top and bottom GND planes for best heat dissipation and noise immunity.
7) Use short traces connecting HSB-C_{HSB}-SW loop.
8) SW pad is noise node switching from V_{IN} to GND. It should be isolated away from the rest of circuit for good EMI and low noise operation.

Example PCB Layout



Typical Application Circuit



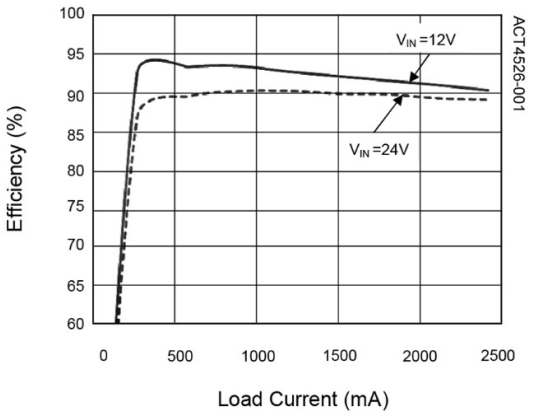
BOM List for 2.4A QC Car Charger

ITEM	REFERENCE	DESCRIPTION	MANUFACTURER	QTY
1	U1	IC, ACT4526, SOP-8EP	Active-Semi	1
2	C1	Capacitor, Electrolytic, 47µF/35V	Murata, TDK	1
3	C2	Capacitor, Ceramic, 10µF/25V, 1206, SMD	Murata, TDK	1
4	C3	Capacitor, Ceramic, 22nF/25V, 0603, SMD	Murata, TDK	1
5	C4	Capacitor, Ceramic, 22µF/16V, 1206, SMD	Murata, TDK	1
6	C5	Capacitor, Electrolytic, 220µF/16V	Murata, TDK	1
7	C6	Capacitor, Ceramic, 2.2µF/16V, 0805, SMD	Murata, TDK	1
8	L1	Inductor, 47µH, 3.5A, 20%		1
9	D1	Diode, Schottky, 40V/5A, SK54L	Panjit	1
10	Rcs	Chip Resistor, 25mΩ, 1206, 1/2W, 1%	SART	1

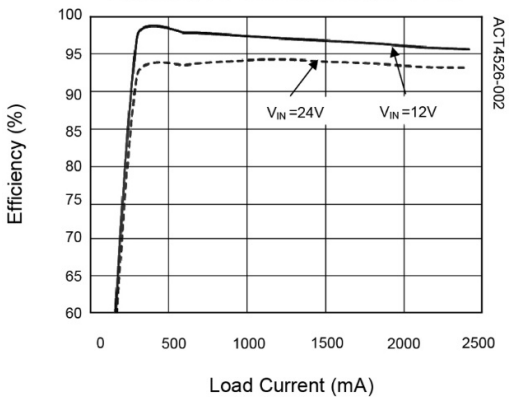
TYPICAL PERFORMANCE CHARACTERISTICS

(Schematic as shown in typical application circuit, Ta = 25°C, unless otherwise specified)

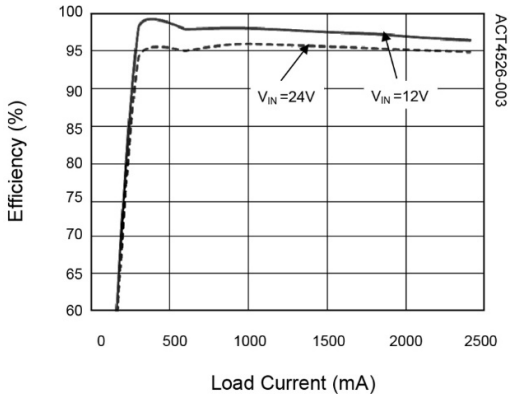
Efficiency vs. Load current (5V Vout)



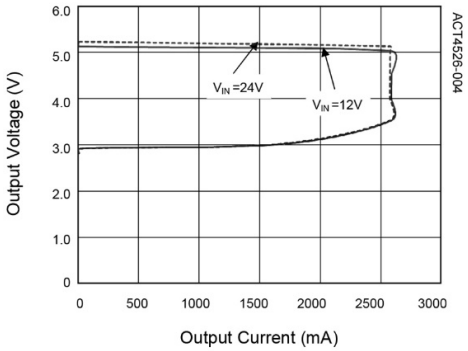
Efficiency vs. Load current (9V Vout)



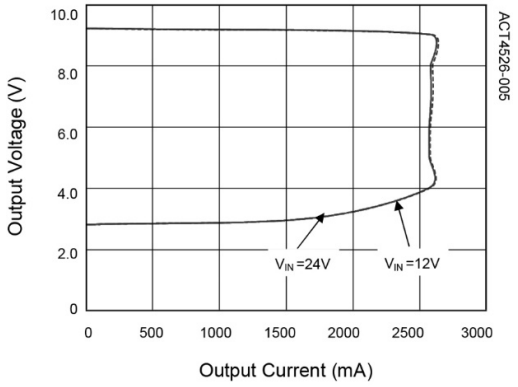
Efficiency vs. Load current (12V Vout)



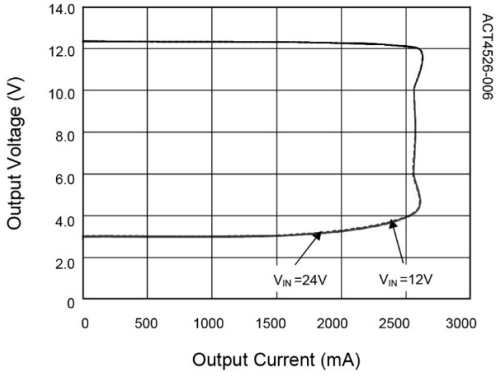
Output CC/CV Curve (5V Vout)



Output CC/CV Curve (9V Vout)



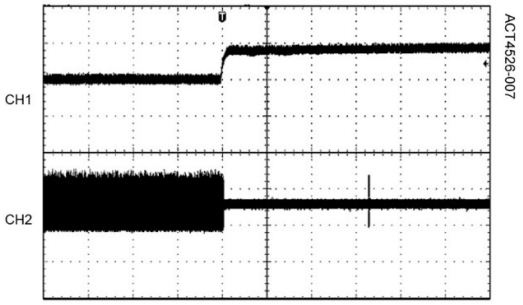
Output CC/CV Curve (12V Vout)



TYPICAL PERFORMANCE CHARACTERISTICS

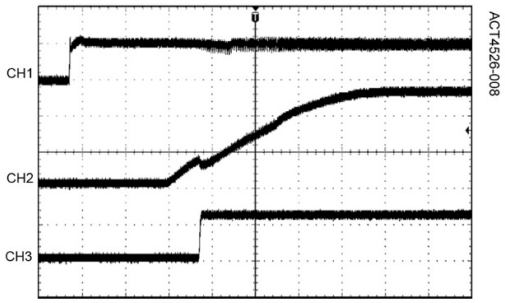
(Schematic as shown in typical application circuit, Ta = 25°C, unless otherwise specified)

Output Over Voltage (5V Vout)



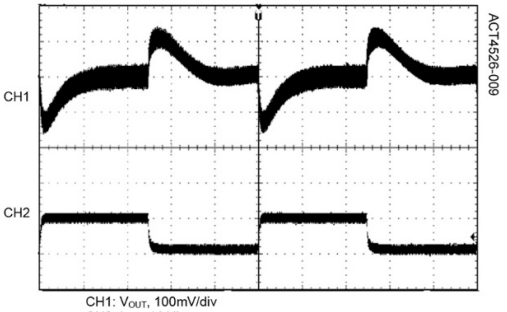
CH1: V_{OUT}, 1V/div
CH2: SW, 10V/div
TIME: 1ms/div

Start up into CC Mode



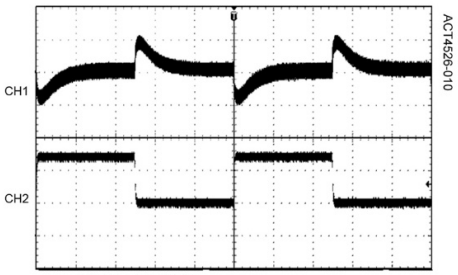
CH1: V_{IN}, 10V/div
CH2: V_{OUT}, 2V/div
CH3: I_{OUT}, 2A/div
TIME: 400µs/div

Load Transient (80mA-1A-80mA)
Vin=12V, Vout=5V



CH1: V_{OUT}, 100mV/div
CH2: I_{OUT}, 1A/div
TIME: 400us//div

Load Transient (1A-2.4A-1A)
Vin=12V, Vout=5V

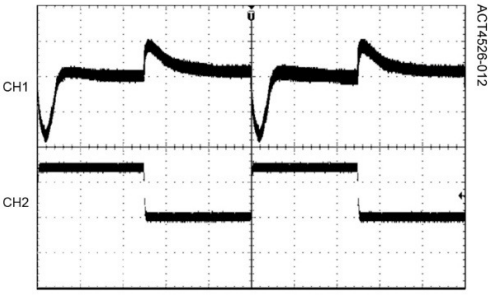


CH1: V_{OUT}, 200mV/div
CH2: I_{OUT}, 1A/div
TIME: 400us//div

Load Transient (80mA-1A-80mA)
Vin=12.6V, Vout=12V

CH1: V_{OUT}, 200mV/div
CH2: I_{OUT}, 1A/div
TIME: 400us//div

Load Transient (1A-2.4A-1A)
Vin=12.6V, Vout=12V

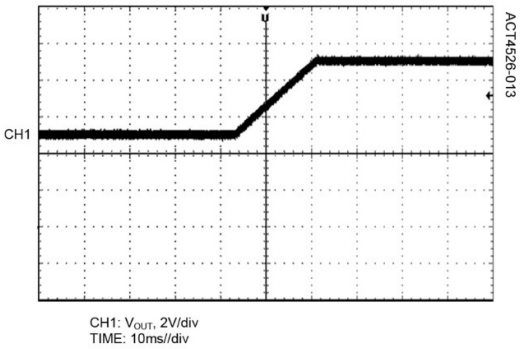


CH1: V_{OUT}, 200mV/div
CH2: I_{OUT}, 1A/div
TIME: 400us//div

TYPICAL PERFORMANCE CHARACTERISTICS

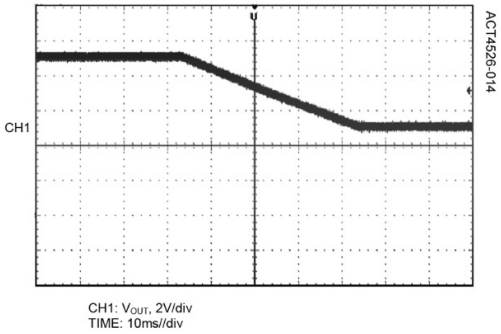
(Schematic as shown in typical application circuit, Ta = 25°C, unless otherwise specified)

Voltage Transient (5V-9V)



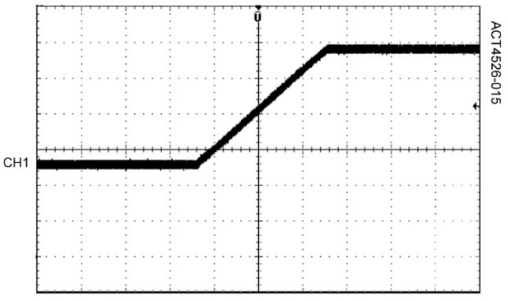
CH1: V_{OUT}, 2V/div
TIME: 10ms//div

Voltage Transient (9V-5V)



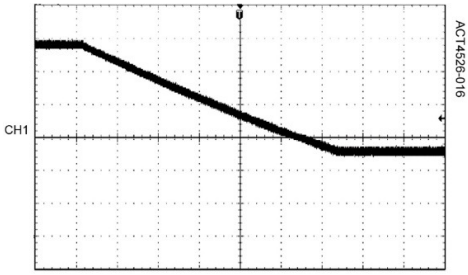
CH1: V_{OUT}, 2V/div
TIME: 10ms//div

Voltage Transient (5V-12V)



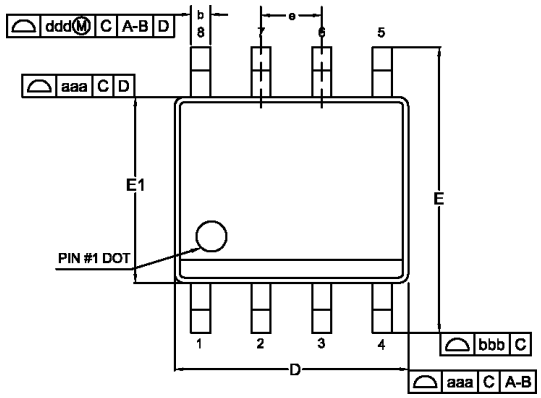
CH1: V_{OUT}, 2V/div
TIME: 10ms//div

Voltage Transient (12V-5V)

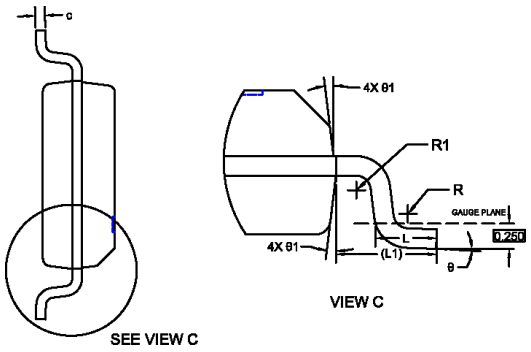


CH1: V_{OUT}, 2V/div
TIME: 10ms//div

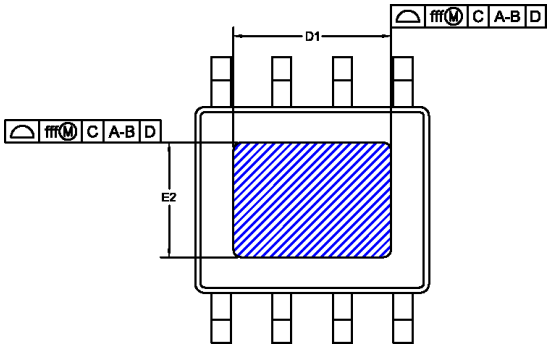
PACKAGE OUTLINE AND DIMENSIONS



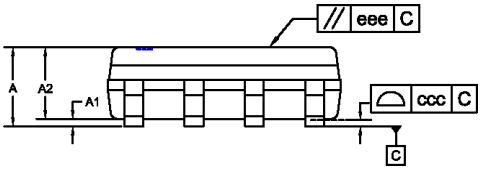
Top View



Side View



Bottom View



Side View

Dimensional Ref.			
REF.	Min.	Nom.	Max.
A	1.370	--	1.730
A1	0.025	--	0.150
A2	1.250	--	--
b	0.360	--	0.480
c	0.170	--	0.250
D	4.900BSC		
E	6.000BSC		
E1	3.900BSC		
D1	3.300BSC		
E2	2.400BSC		
e	1.270 BSC		
L	0.500	--	1.000
L1	1.040REF.		
R	0.070	--	--
R1	0.070	--	--
θ	0°	--	8°
θ1	5°	--	15°
Tol. of Form&Position			
aaa	0.10		
bbb	0.20		
ccc	0.10		
ddd	0.25		
eee	0.10		
fff	0.15		

Notes

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5-2009.
2. All DIMENSIONS ARE IN MILLIMETERS.
3. UNILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

Product Compliance

This part complies with RoHS directive 2011/65/EU as amended by (EU) 2015/863.

This part also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Web: www.qorvo.com **Tel: 1-844-890-8163**

Email: customer.support@qorvo.com

For technical questions and application information:

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