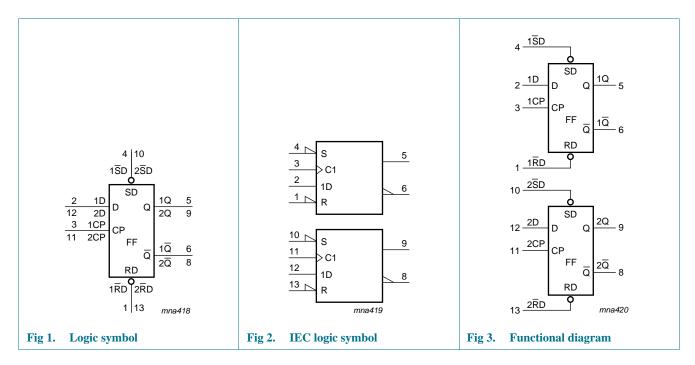
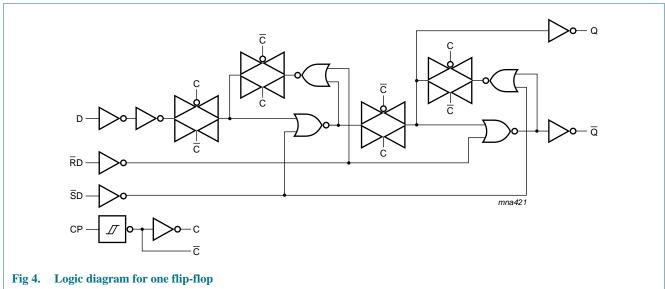
Table 1.
 Ordering information ...continued

Type number	Package								
	Temperature range	Name	Description	Version					
74HC74PW	−40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads;	SOT402-1					
74HCT74PW			body width 4.4 mm						
74HC74BQ	-40 °C to +125 °C DHVQFN1		plastic dual in-line compatible thermal enhanced very	SOT762-1					
74HCT74BQ			thin quad flat package; no leads; 14 terminals; body $2.5 \times 3 \times 0.85$ mm						

4. Functional diagram



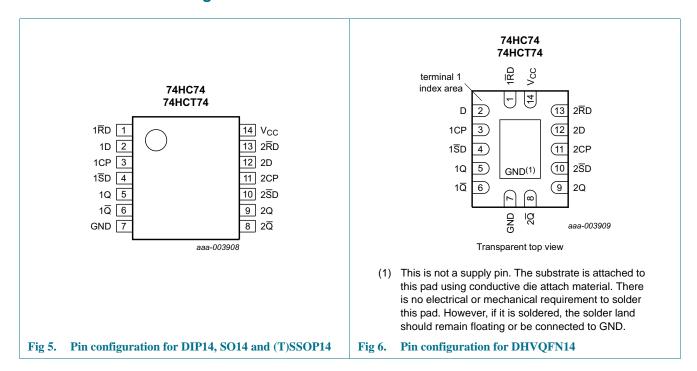


74HC_HCT74

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5. Pinning information

5.1 Pinning



5.2 Pin description

Table 2. Pin description

IUDIC Z.	i ili description	
Symbol	Pin	Description
1RD	1	asynchronous reset-direct input (active LOW)
1D	2	data input
1CP	3	clock input (LOW-to-HIGH, edge-triggered)
1SD	4	asynchronous set-direct input (active LOW)
1Q	5	output
1Q	6	complement output
GND	7	ground (0 V)
2Q	8	complement output
2Q	9	output
2SD	10	asynchronous set-direct input (active LOW)
2CP	11	clock input (LOW-to-HIGH, edge-triggered)
2D	12	data input
2RD	13	asynchronous reset-direct input (active LOW)
V_{CC}	14	supply voltage

6. Functional description

Table 3. Function table[1]

Input		Output			
nSD	nRD	nCP	nD	nQ	nQ
L	Н	X	X	Н	L
Н	L	Χ	Χ	L	Н
L	L	Χ	Χ	Н	Н

^[1] H = HIGH voltage level; L = LOW voltage level; X = don't care.

Table 4. Function table[1]

Input		Output			
nSD	nRD	nCP	nD	nQ _{n+1}	nQ _{n+1}
Н	Н	\uparrow	L	L	Н
Н	Н	\uparrow	Н	Н	L

^[1] H = HIGH voltage level; L = LOW voltage level; ↑ = LOW-to-HIGH transition; Q_{n+1} = state after the next LOW-to-HIGH CP transition; X = don't care.

7. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7	V
I _{IK}	input clamping current	$V_I < -0.5 \text{ V or } V_I > V_{CC} + 0.5 \text{ V}$	-	±20	mA
I _{OK}	output clamping current	$V_O < -0.5 \text{ V or } V_O > V_{CC} + 0.5 \text{ V}$	-	±20	mA
Io	output current	$V_{O} = -0.5 \text{ V to } (V_{CC} + 0.5 \text{ V})$	-	±25	mA
I _{CC}	supply current		-	+100	mA
I _{GND}	ground current		-100	-	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	DIP14 package	<u>[1]</u> -	750	mW
		SO14, (T)SSOP14 and DHVQFN14 packages	[1] -	500	mW

^[1] For DIP14 package: P_{tot} derates linearly with 12 mW/K above 70 $^{\circ}\text{C}.$

For SO14 package: Ptot derates linearly with 8 mW/K above 70 °C.

For (T)SSOP14 packages: Ptot derates linearly with 5.5 mW/K above 60 °C.

For DHVQFN14 packages: P_{tot} derates linearly with 4.5 mW/K above 60 $^{\circ}\text{C}.$

74HC_HCT74

4 of 21

8. Recommended operating conditions

Table 6. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions		74HC74		•	74HCT74	ı	Unit
			Min	Тур	Max	Min	Тур	Max	
V_{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
VI	input voltage		0	-	V_{CC}	0	-	V_{CC}	V
Vo	output voltage		0	-	V_{CC}	0	-	V_{CC}	V
T _{amb}	ambient temperature		-40	+25	+125	-40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate	$V_{CC} = 2.0 \text{ V}$	-	-	625	-	-	-	ns/V
		$V_{CC} = 4.5 \text{ V}$	-	1.67	139	-	1.67	139	ns/V
		$V_{CC} = 6.0 \text{ V}$	-	-	83	-	-	-	ns/V

9. Static characteristics

Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	T _{amb} =	–40 °C to	+85 °C	$T_{amb} = -40^{\circ}$	C to +125 °C	Unit
			Min	Typ[1]	Max	Min	Max	
74HC74								
V _{IH}	HIGH-level	V _{CC} = 2.0 V	1.5	1.2	-	1.5	-	V
	input voltage	V _{CC} = 4.5 V	3.15	2.4	-	3.15	-	V
		$V_{CC} = 6.0 \text{ V}$	4.2	3.2	-	4.2	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 2.0 V	-	0.8	0.5	-	0.5	V
		V _{CC} = 4.5 V	-	2.1	1.35	-	1.35	V
		$V_{CC} = 6.0 \text{ V}$	-	2.8	1.8	-	1.8	V
V _{OH} HIGH-level	$V_I = V_{IH}$ or V_{IL}							
	output voltage	$I_{O} = -4.0 \text{ mA}; V_{CC} = 4.5 \text{ V}$	3.84	4.32	-	3.7	-	V
		$I_{O} = -5.2 \text{ mA}; V_{CC} = 6.0 \text{ V}$	5.34	5.81	-	5.2	-	V
V_{OL}		$V_I = V_{IH}$ or V_{IL}						
	output voltage	$I_{O} = 4.0 \text{ mA}; V_{CC} = 4.5 \text{ V}$	-	0.15	0.33	-	0.4	V
		$I_{O} = 5.2 \text{ mA}; V_{CC} = 6.0 \text{ V}$	-	0.16	0.33	-	0.4	V
ı	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 6.0 \text{ V}$	-	-	±1.0	-	±1.0	μΑ
CC	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 6.0$ V	-	-	40	-	80	μΑ
Cı	input capacitance			3.5				pF
74HCT7	4							
V _{IH}	HIGH-level input voltage	V _{CC} = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	V
V _{IL}	LOW-level input voltage	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	-	1.2	0.8	-	0.8	V

74HC_HCT7

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 Table 7.
 Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	T _{amb} =	-40 °C to	+85 °C	T _{amb} = -40 °	Unit	
			Min	Typ[1]	Max	Min	Max	
V_{OH}	HIGH-level	$V_I = V_{IH}$ or V_{IL} ; $V_{CC} = 4.5 \text{ V}$		'				'
	output voltage	$I_O = -4 \text{ mA}$	3.84	4.32	-	3.7	-	V
V_{OL}		$V_I = V_{IH}$ or V_{IL} ; $V_{CC} = 4.5 \text{ V}$						
	output voltage	$I_{O} = 4.0 \text{ mA}$	-	0.15	0.33	-	0.4	V
I	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 5.5 \text{ V}$	-	-	±1.0	-	±1.0	μА
I _{CC}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5 \text{ V}$	-	-	40	-	80	μА
Δl _{CC} additional supply current		$\begin{split} &V_{I} = V_{CC} - 2.1 \text{ V;} \\ &\text{other inputs at } V_{CC} \text{ or GND;} \\ &V_{CC} = 4.5 \text{ V to } 5.5 \text{ V;} \\ &I_{O} = 0 \text{ A} \end{split}$						
		per input pin; nD, nRD inputs	-	70	315	-	343	μА
		per input pin; nSD, nCP input	-	80	360	-	392	μА
C _I	input capacitance			3.5				pF

^[1] All typical values are measured at T_{amb} = 25 °C.

10. Dynamic characteristics

Table 8. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); $C_L = 50 \text{ pF}$ unless otherwise specified; for test circuit see Figure 9.

Symbol	Parameter	Conditions		T _{amb} :	= –40 °C to	+85 °C	$T_{amb} = -40$	°C to +125 °C	Unit
				Min	Typ[1]	Max	Min	Max	
74HC74			,		1		1	•	'
t _{pd}	propagation delay	nCP to nQ, n \overline{Q} ; see Figure 7	[2]						
		V _{CC} = 2.0 V		-	47	220	-	265	ns
		V _{CC} = 4.5 V		-	17	44	-	53	ns
		$V_{CC} = 5 \text{ V}; C_L = 15 \text{ pF}$		-	14	-	-	-	ns
		$V_{CC} = 6.0 \text{ V}$		-	14	37	-	45	ns
	$n\overline{S}D$ to nQ , $n\overline{Q}$; see Figure 8	[2]							
		$V_{CC} = 2.0 \text{ V}$		-	50	250	-	300	ns
		$V_{CC} = 4.5 \text{ V}$		-	18	50	-	60	ns
		$V_{CC} = 5 \text{ V}; C_L = 15 \text{ pF}$		-	15	-	-	-	ns
		$V_{CC} = 6.0 \text{ V}$		-	14	43	-	51	ns
		nRD to nQ, nQ; see Figure 8	[2]						
		$V_{CC} = 2.0 \text{ V}$		-	52	250	-	300	ns
		$V_{CC} = 4.5 \text{ V}$		-	19	50	-	60	ns
		$V_{CC} = 5 \text{ V}; C_L = 15 \text{ pF}$		-	16	-	-	-	ns
		$V_{CC} = 6.0 \text{ V}$		-	15	43	-	51	ns
t _t	transition	nQ, nQ; see Figure 7	[3]						
	time	$V_{CC} = 2.0 \text{ V}$		-	19	95	-	110	ns
		$V_{CC} = 4.5 \text{ V}$		-	7	19	-	22	ns
		$V_{CC} = 6.0 \text{ V}$		-	6	16	-	19	ns
t_{W}	pulse width	nCP HIGH or LOW; see Figure 7							
		$V_{CC} = 2.0 \text{ V}$		100	19	-	120	-	ns
		$V_{CC} = 4.5 \text{ V}$		20	7	-	24	-	ns
		$V_{CC} = 6.0 \text{ V}$		17	6	-	20	-	ns
		nSD, nRD LOW; see <u>Figure 8</u>							
		$V_{CC} = 2.0 \text{ V}$		100	19	-	120	-	ns
		$V_{CC} = 4.5 \text{ V}$		20	7	-	24	-	ns
		$V_{CC} = 6.0 \text{ V}$		17	6	-	20	-	ns
t _{rec}	recovery	nSD, nRD; see Figure 8							
	time	$V_{CC} = 2.0 \text{ V}$		40	3	-	45	-	ns
		$V_{CC} = 4.5 \text{ V}$		8	1	-	9	-	ns
		$V_{CC} = 6.0 \text{ V}$		7	1	-	8	-	ns

74HC_HCT74

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 Table 8.
 Dynamic characteristics ...continued

Voltages are referenced to GND (ground = 0 V); $C_L = 50 \text{ pF}$ unless otherwise specified; for test circuit see Figure 9.

Symbol	Parameter	Conditions		T _{amb} :	= -40 °C to	+85 °C	T _{amb} = -40	°C to +125 °C	Unit
				Min	Typ[1]	Max	Min	Max	
t _{su}	set-up time	nD to nCP; see Figure 7		1			I	1	
		V _{CC} = 2.0 V		75	6	-	90	-	ns
		V _{CC} = 4.5 V		15	2	-	18	-	ns
		V _{CC} = 6.0 V		13	2	-	15	-	ns
t _h	hold time	nD to nCP; see Figure 7							
		V _{CC} = 2.0 V		3	-6	-	3	-	ns
		V _{CC} = 4.5 V		3	-2	-	3	-	ns
		V _{CC} = 6.0 V		3	-2	-	3	-	ns
f _{max}	maximum	nCP; see Figure 7							
···an	frequency	V _{CC} = 2.0 V		4.8	23	-	4.0	-	MHz
		V _{CC} = 4.5 V		24	69	-	20	-	MHz
		$V_{CC} = 5 \text{ V}; C_L = 15 \text{ pF}$		-	76	-	-	-	MHz
		V _{CC} = 6.0 V		28	82	-	24	-	MHz
C _{PD}	power dissipation capacitance	$C_L = 50 \text{ pF}; f = 1 \text{ MHz};$ $V_I = \text{GND to } V_{CC}$	[4]	-	24	-	-	-	pF
74HCT7	4								
t _{pd}	propagation delay	nCP to nQ, n \overline{Q} ; see Figure 7	[2]						
		V _{CC} = 4.5 V		-	18	44	-	53	ns
		$V_{CC} = 5 \text{ V}; C_L = 15 \text{ pF}$		-	15	-	-	-	ns
		\overline{NSD} to \overline{NQ} ; see Figure 8	[2]						
		$V_{CC} = 4.5 \text{ V}$		-	23	50	-	60	ns
		$V_{CC} = 5 \text{ V}; C_L = 15 \text{ pF}$		-	18	-	-	-	ns
		nRD to nQ, nQ; see Figure 8	[2]						
		V _{CC} = 4.5 V		-	24	50	-	60	ns
		$V_{CC} = 5 \text{ V}; C_L = 15 \text{ pF}$		-	18	-	-	-	ns
t _t	transition	nQ, nQ; see Figure 7	[3]						
	time	V _{CC} = 4.5 V		-	7	19	-	22	ns
t _W	pulse width	nCP HIGH or LOW; see Figure 7							
		V _{CC} = 4.5 V		23	9	-	27	-	ns
		nSD, nRD LOW; see Figure 8							
		V _{CC} = 4.5 V		20	9	-	24	-	ns
t _{rec}	recovery	nSD, nRD; see Figure 8							
	time	V _{CC} = 4.5 V		8	1	-	9	-	ns
t _{su}	set-up time	nD to nCP; see Figure 7							
	•	V _{CC} = 4.5 V		15	5	-	18	-	ns

Product data sheet

74HC_HCT74

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Table 8. Dynamic characteristics ...continued

Voltages are referenced to GND (ground = 0 V); $C_L = 50 \text{ pF}$ unless otherwise specified; for test circuit see Figure 9.

Symbol	ol Parameter Conditions			T _{amb} =	= -40 °C to	+85 °C	$T_{amb} = -40 ^{\circ}\text{C} \text{ to } +125 ^{\circ}\text{C}$		Unit
				Min	Typ[1]	Max	Min	Max	
t _h hold time	nD to nCP; see Figure 7								
		$V_{CC} = 4.5 \text{ V}$		3	-3	-	3	-	ns
f _{max} maximu	maximum	nCP; see Figure 7							
	frequency	$V_{CC} = 4.5 \text{ V}$		22	54	-	18	-	MHz
		$V_{CC} = 5 \text{ V}; C_L = 15 \text{ pF}$		-	59	-	-	-	MHz
C _{PD}	power dissipation capacitance	C_L = 50 pF; f = 1 MHz; V_I = GND to V_{CC} - 1.5 V	[4]	-	29	-	-	-	pF

- [1] All typical values are measured at T_{amb} = 25 °C.
- [2] t_{pd} is the same as t_{PLH} and t_{PHL} .
- [3] t_t is the same as t_{THL} and t_{TLH} .
- [4] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$$P_D = C_{PD} \times V_{CC}{}^2 \times f_i \times N + \sum (C_L \times V_{CC}{}^2 \times f_o)$$
 where:

 f_i = input frequency in MHz;

fo = output frequency in MHz;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

 $\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

11. Waveforms

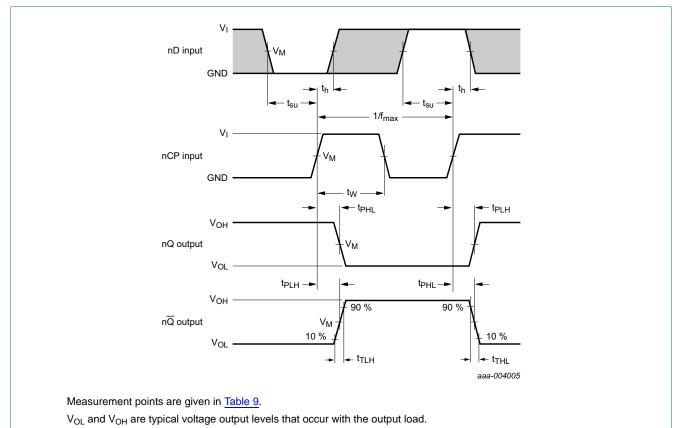


Fig 7. Input to output propagation delay, output transition time, clock input pulse width and maximum frequency

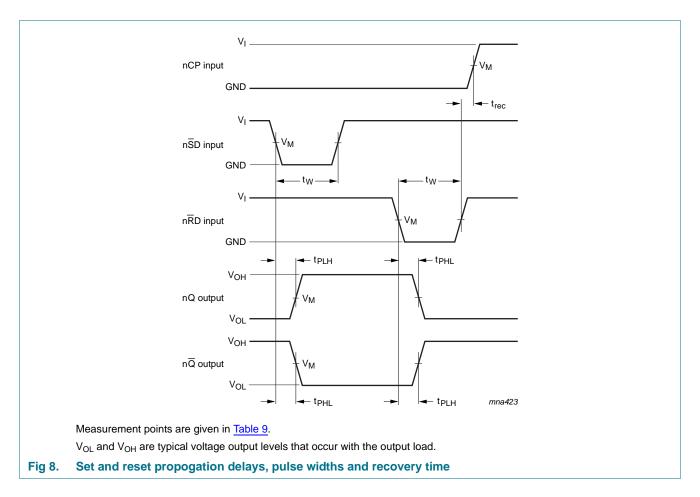
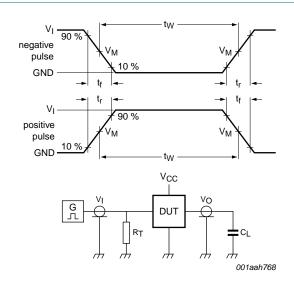


Table 9. Measurement points

Туре	Input	Output
	V _M	V _M
74HC74	0.5V _{CC}	0.5V _{CC}
74HCT74	1.3 V	1.3 V



Test data is given in Table 10.

Definitions test circuit:

 R_T = Termination resistance should be equal to output impedance Z_0 of the pulse generator.

 C_L = Load capacitance including jig and probe capacitance.

R_L = Load resistance.

S1 = Test selection switch.

Fig 9. Test circuit for measuring switching times

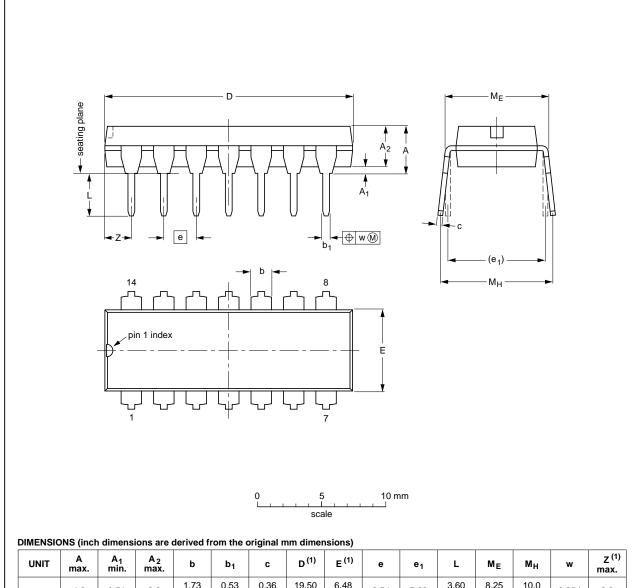
Table 10. Test data

Туре	Input		Load		Test	
	VI	t _r , t _f	C _L	R _L		
74HC74	V _{CC}	6 ns	15 pF, 50 pF	1 kΩ	t _{PLH} , t _{PHL}	
74HCT74	3 V	6 ns	15 pF, 50 pF	1 kΩ	t _{PLH} , t _{PHL}	

12. Package outline

DIP14: plastic dual in-line package; 14 leads (300 mil)

SOT27-1



	•					•									
UNIT	A max.	A ₁ min.	A ₂ max.	b	b ₁	С	D ⁽¹⁾	E (1)	е	e ₁	L	ME	Мн	w	Z ⁽¹⁾ max.
mm	4.2	0.51	3.2	1.73 1.13	0.53 0.38	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.2
inches	0.17	0.02	0.13	0.068 0.044	0.021 0.015	0.014 0.009	0.77 0.73	0.26 0.24	0.1	0.3	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.087

Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

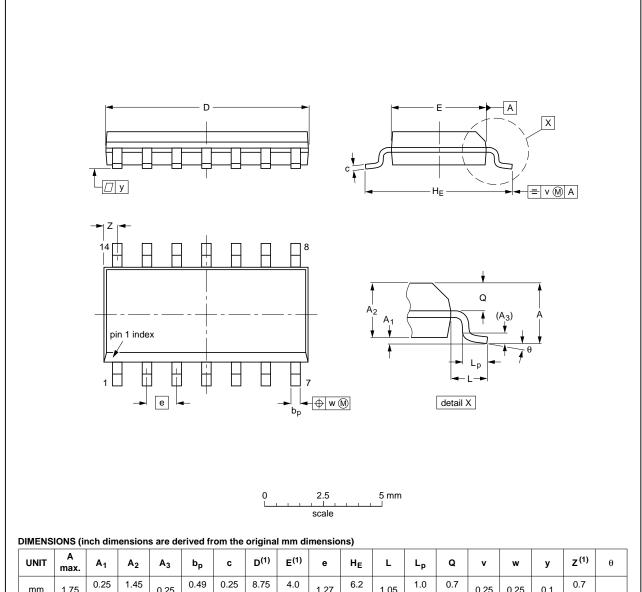
OUTLINE		REFER	ENCES	EUROPEAN	ISSUE DATE
VERSION	IEC	JEDEC	JEITA	PROJECTION	ISSUE DATE
SOT27-1	050G04	MO-001	SC-501-14		99-12-27 03-02-13

Fig 10. Package outline SOT27-1 (DIP14)

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SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1



UNIT	A max.	A ₁	A ₂	A ₃	bp	С	D ⁽¹⁾	E ⁽¹⁾	е	HE	L	Lp	Q	v	w	у	z ⁽¹⁾	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8°
inches	0.069	0.010 0.004	0.057 0.049	0.01	1	0.0100 0.0075	0.35 0.34	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	0°

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

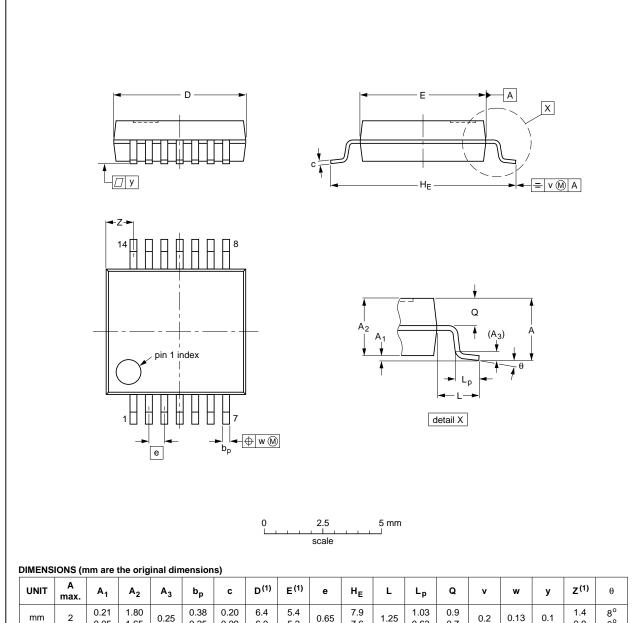
OUTLINE		REFER	ENCES	EUROPEAN	ISSUE DATE
VERSION	IEC	JEDEC	JEITA	PROJECTION	ISSUE DATE
SOT108-1	076E06	MS-012			99-12-27 03-02-19

Fig 11. Package outline SOT108-1 (SO14)

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SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm

SOT337-1



UNIT	A max.	A ₁	A ₂	A ₃	b _p	С	D ⁽¹⁾	E ⁽¹⁾	Ф	HE	L	Lp	ø	v	w	у	Z ⁽¹⁾	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.4 0.9	8° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

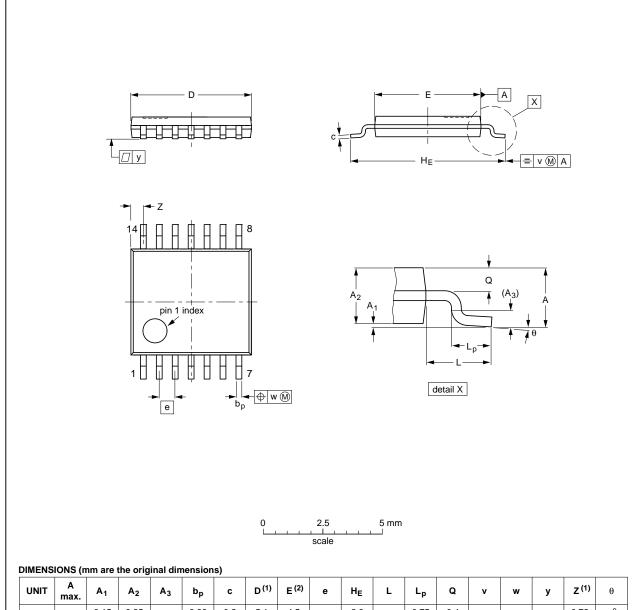
OUTLINE		REFER	ENCES	EUROPEAN	ISSUE DATE
VERSION	IEC	JEDEC	JEITA	PROJECTION	ISSUE DATE
SOT337-1		MO-150			-99-12-27 03-02-19

Fig 12. Package outline SOT337-1 (SSOP14)

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TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1



UNIT	A max.	A ₁	A ₂	A ₃	bp	С	D ⁽¹⁾	E (2)	е	HE	L	Lp	Q	v	w	у	Z ⁽¹⁾	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8° 0°

- 1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
- 2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE		REFER	ENCES	EUROPEAN	ISSUE DATE
VERSION	IEC	JEDEC	JEITA	PROJECTION	ISSUE DATE
SOT402-1		MO-153			99-12-27 03-02-18
301402-1		WIO-133			

Fig 13. Package outline SOT402-1 (TSSOP14)

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DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm SOT762-1

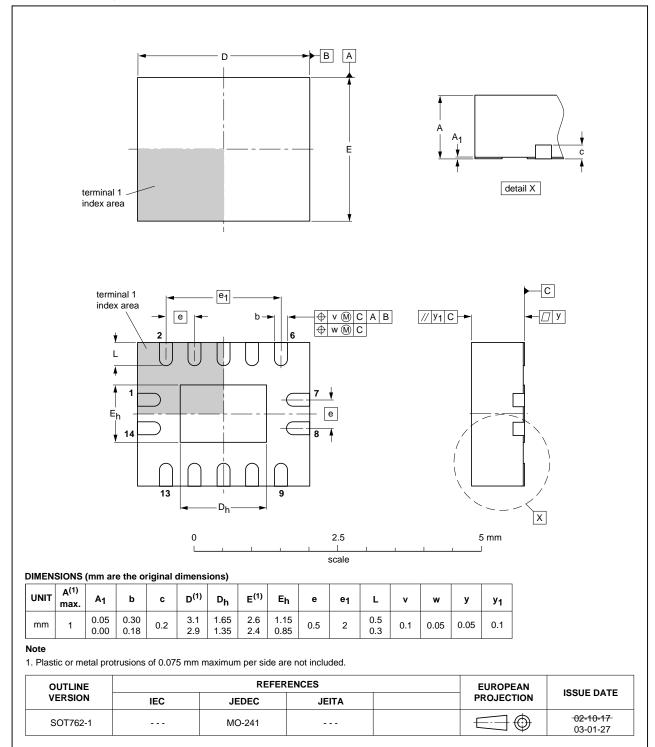


Fig 14. Package outline SOT762-1 (DHVQFN14)

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13. Abbreviations

Table 11. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
ESD	ElectroStatic Discharge
НВМ	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes				
74HC_HCT74 v.4	20120827	Product data sheet	-	74HC_HCT74 v.3				
Modifications:	 The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. Legal texts have been adapted to the new company name where appropriate. 							
	Logarioxio	mave been adapted to the	c new company name	с много арргорнаю.				
74HC_HCT74 v.3	20030710	Product data sheet	-	74HC_HCT74_CNV v.2				
74HC_HCT74_CNV v.2	19980223	Product specification	-	-				

15. Legal information

15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions"
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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Dual D-type flip-flop with set and reset; positive edge-trigger

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17. Contents

1	General description
2	Features and benefits
3	Ordering information
4	Functional diagram 2
5	Pinning information 3
5.1	Pinning
5.2	Pin description
6	Functional description 4
7	Limiting values 4
8	Recommended operating conditions 5
9	Static characteristics 5
10	Dynamic characteristics
11	Waveforms
12	Package outline
13	Abbreviations
14	Revision history
15	Legal information
15.1	Data sheet status
15.2	Definitions
15.3	Disclaimers
15.4	Trademarks20
16	Contact information 20
17	Contents

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