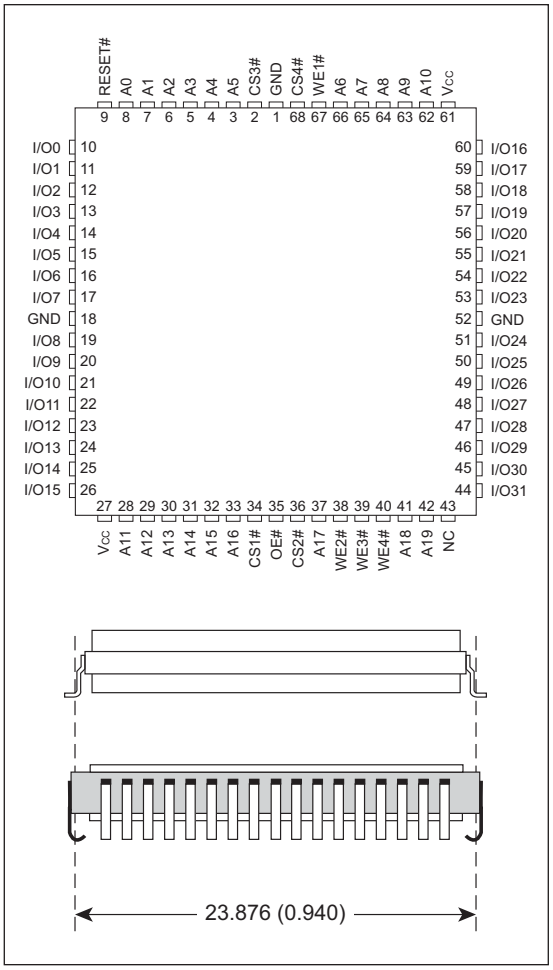
PIN CONFIGURATION FOR WF1M32B-XG2UX3

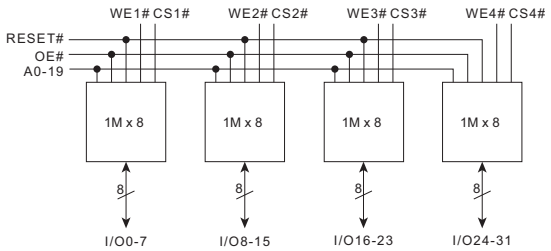
TOP VIEW



PIN DESCRIPTION

I/O0-31	Data Inputs/Outputs
A0-19	Address Inputs
WE1-4#	Write Enables
CS1-4#	Chip Selects
OE#	Output Enable
RESET#	Reset/Powerdown
Vcc	Power Supply
GND	Ground

BLOCK DIAGRAM



The Microsemi 68 lead G2U CQFP fills the same fit and function as the JEDEC 68 lead CQFJ or 68 PLCC. But the G2U has the TCE and lead inspection advantage of the CQFP form.

ABSOLUTE MAXIMUM RATINGS

Parameter		Unit
Operating Temperature (M, Q)	-55 to +125	°C
Supply Voltage Range (V_{CC})	-0.5 to +4.0	V
Signal Voltage Range	-0.5 to Vcc +0.5	V
Storage Temperature Range	-65 to +150	°C
Lead Temperature (soldering, 10 seconds)	+300	°C
Endurance (write/erase cycles)	1,000,000 min.	cycles

NOTES:
1. Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

CAPACITANCE

T_A = +25°C

Parameter	Symbol	Conditions	Max	Unit
OE# capacitance	C_{OE}	V_{IN} = 0 V, f = 1.0 MHz	50	pF
WE1-4# capacitance	C_{WE}	V_{IN} = 0 V, f = 1.0 MHz	20	pF
CS1-4# capacitance	C_{CS}	V_{IN} = 0 V, f = 1.0 MHz	20	pF
Data I/O capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V, f = 1.0 MHz	20	pF
Address input capacitance	C_{AD}	V_{IN} = 0 V, f = 1.0 MHz	50	pF

This parameter is guaranteed by design but not tested.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	3.0	3.6	V
Input High Voltage	V_{IH}	0.7 x V_{CC}	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	-0.5	+0.8	V
Operating Temp. (Mil.)	T_A	-55	+125	°C
Operating Temp. (Ind.)	T_A	-40	+85	°C
Operating Temp. (Com.)	T_A	0	+70	°C

DATA RETENTION

Parameter	Test Conditions	Min	Unit
Minimum Pattern Data Retention Time	150°C	10	Years
	125°C	20	Years

DC CHARACTERISTICS – CMOS COMPATIBLE

Parameter	Symbol	Conditions	Min	Max	Unit
Input Leakage Current	I_{LI}	V_{CC} = $V_{CC\ MAX}$, V_{IN} = GND or V_{CC}		10	µA
Output Leakage Current	I_{LOx32}	V_{CC} = $V_{CC\ MAX}$, V_{OUT} = GND or V_{CC}		10	µA
V_{CC} Active Current for Read (1)	I_{CC1}	CS# = V_{IL}, OE# = V_{IH}, f = 5MHz		120	mA
V_{CC} Active Current for Program or Erase (2)	I_{CC2}	CS# = V_{IL}, OE# = V_{IH}		140	mA
V_{CC} Standby Current	I_{CC3}	CS#, RESET# = V_{CC} ± 0.3V		200	µA
Output Low Voltage	V_{OL}	I_{OL} =4.0 mA, V_{CC} = $V_{CC\ MIN}$		0.45	V
Output High Voltage	V_{OH1}	I_{OH} = -2.0 mA, V_{CC} = $V_{CC\ MIN}$	2.4		V
Low V_{CC} Lock-Out Voltage (3)	V_{LKO}		2.3	2.5	V

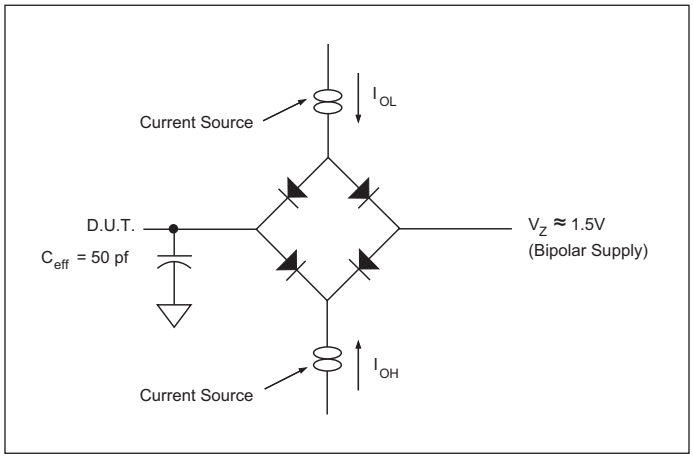
NOTES:
1. The current listed as typically less than 8 mA/MHz, with OE# at V_{IH}.
2. I_{CC} active while Embedded Algorithm (program or erase) is in progress.
3. Guaranteed by design, but not tested.

AC CHARACTERISTICS – WRITE/ERASE/PROGRAM OPERATIONS – CS# CONTROLLED

Parameter	Symbol		-100		-120		-150		Unit
			Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{AVAV}	t_{WC}	100		120		150		ns
Write Enable Setup Time	t_{WLEL}	t_{WS}	0		0		0		ns
Chip Select Pulse Width	t_{ELEH}	t_{CP}	50		50		50		ns
Address Setup Time	t_{AVEL}	t_{AS}	0		0		0		ns
Data Setup Time	t_{DVEH}	t_{DS}	50		50		50		ns
Data Hold Time	t_{EHDX}	t_{DH}	0		0		0		ns
Address Hold Time	t_{ELAX}	t_{AH}	50		50		50		ns
Chip Select Pulse Width High	t_{EHEL}	t_{CPH}	20		20		20		ns
Duration of Byte Programming Operation (1)	t_{WHWH1}			300		300		300	µs
Sector Erase Time	t_{WHWH2}			21		21		21	sec
Read Recovery Time (2)	t_{GHEL}		0		0		0		µs
Chip Programming Time				50		50		50	sec

NOTES:
1. Typical value for t_{WHWH1} is 9µs.
2. Guaranteed by design, but not tested.

AC TEST CIRCUIT



AC TEST CONDITIONS

Parameter	Typ	Unit
Input Pulse Levels	V_{IL} = 0, V_{IH} = 2.5	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

NOTES:
V_Z is programmable from -2V to +7V.
I_{OL} & I_{OH} programmable from 0 to 16mA.
Tester Impedance Z0 = 75 Ω.
V_Z is typically the midpoint of V_{OH} and V_{OL}.
I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.
ATE tester includes jig capacitance.

AC CHARACTERISTICS – WRITE/ERASE/PROGRAM OPERATIONS – WE# CONTROLLED

Parameter	Symbol		-100		-120		-150		Unit
			Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{AVAV}	t_{WC}	100		120		150		ns
Chip Select Setup Time	t_{ELWL}	t_{CS}	0		0		0		ns
Write Enable Pulse Width	t_{WLWH}	t_{WP}	50		50		65		ns
Address Setup Time	t_{AVWL}	t_{AS}	0		0		0		ns
Data Setup Time	t_{DVWH}	t_{DS}	50		50		65		ns
Data Hold Time	t_{WHDX}	t_{DH}	0		0		0		ns
Address Hold Time	t_{WLAX}	t_{AH}	50		50		65		ns
Write Enable Pulse Width High	t_{WHWL}	t_{WPH}	30		30		35		ns
Duration of Byte Programming Operation (1)	t_{WHWH1}			300		300		300	µs
Sector Erase	t_{WHWH2}			15		15		15	sec
Read Recovery Time before Write (3)	t_{GHWL}		0		0		0		µs
V_{CC} Setup Time	t_{VCS}		50		50		50		µs
Chip Programming Time				50		50		50	sec
Output Enable Setup Time		t_{OES}	0		0		0		ns
Output Enable Hold Time (2)		t_{OEH}	10		10		10		ns

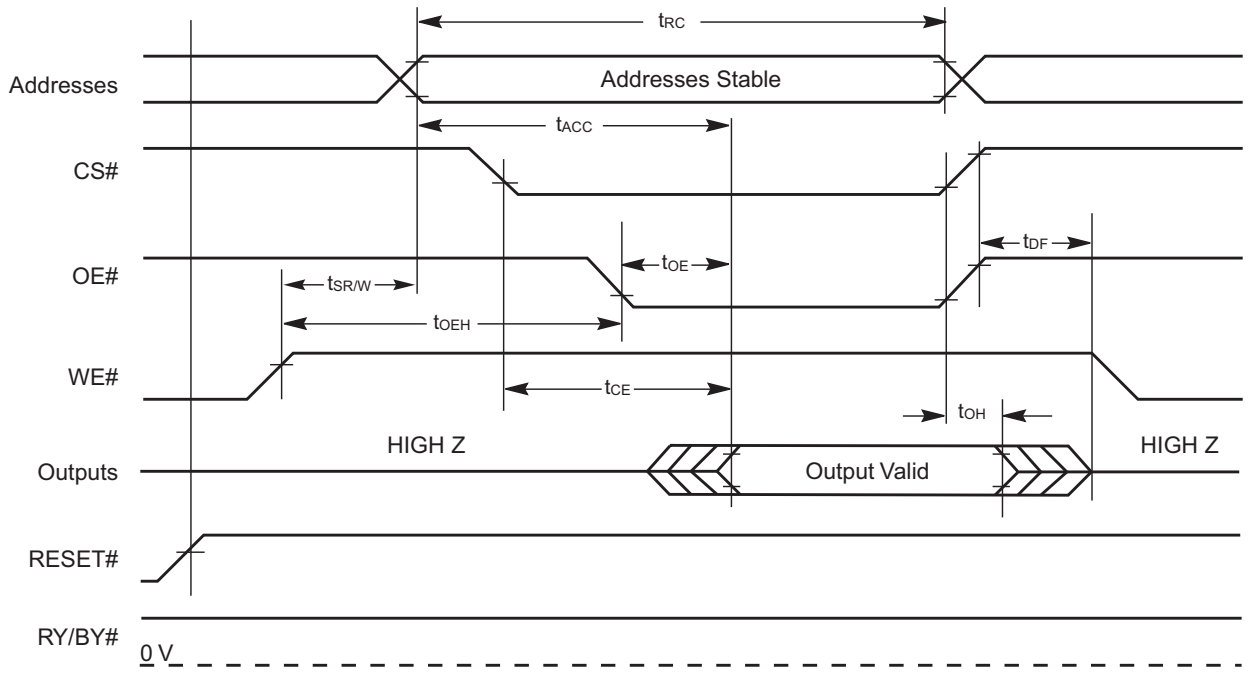
NOTES:
1. Typical value for t_{WHWH1} is 9µs.
2. For Toggle and Data Polling.
3. Guaranteed by design, but not tested.

AC CHARACTERISTICS – READ-ONLY OPERATIONS

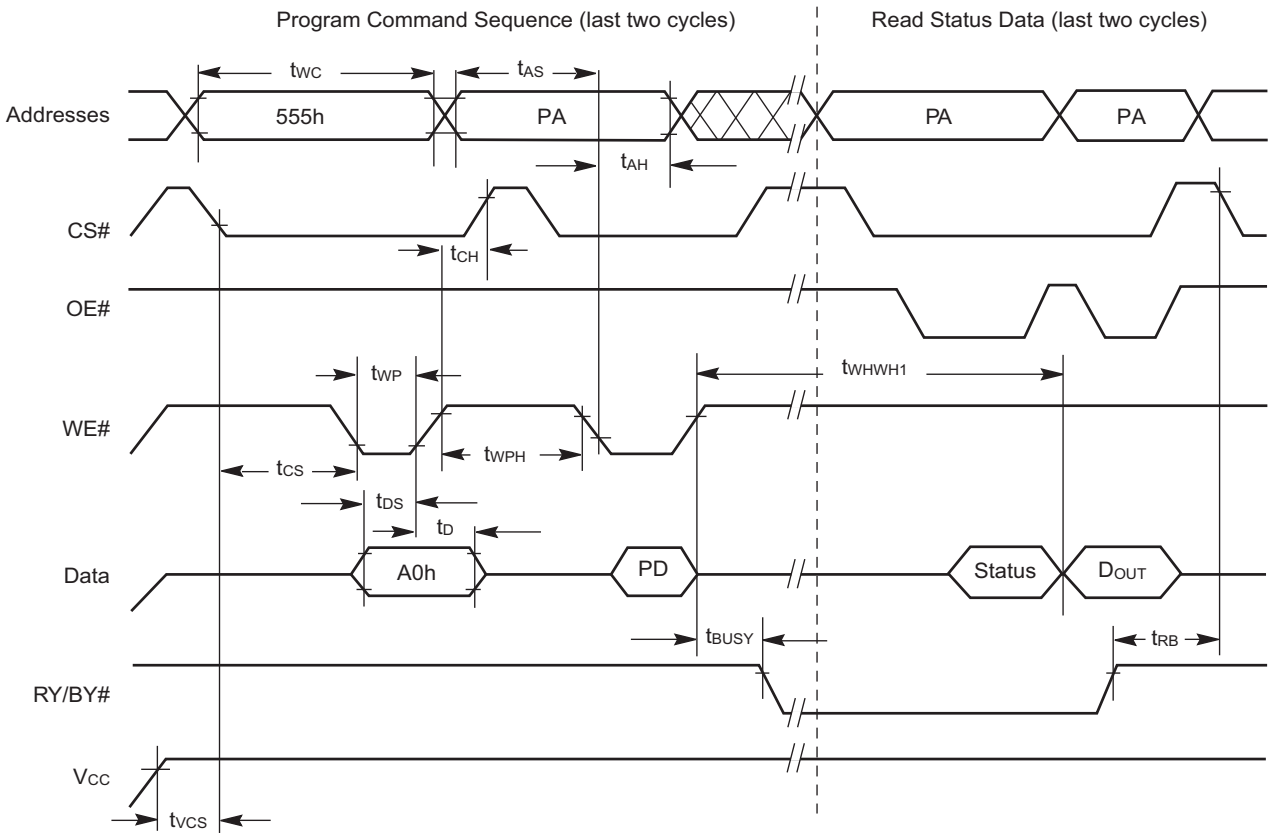
Parameter	Symbol		-100		-120		-150		Unit
			Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{AVAV}	t_{RC}	100		120		150		ns
Address Access Time	t_{AVQV}	t_{ACC}		100		120		150	ns
Chip Select Access Time	t_{ELQV}	t_{CE}		100		120		150	ns
Output Enable to Output Valid	t_{GLQV}	t_{OE}		40		50		55	ns
Chip Select High to Output High Z (1)	t_{EHQZ}	t_{DF}		30		30		40	ns
Output Enable High to Output High Z (1)	t_{GHQZ}	t_{DF}		30		30		40	ns
Output Hold from Addresses, CS# or OE# Change, whichever is First (1)	t_{AXQX}	t_{OH}	0		0		0		ns

1. Guaranteed by design, not tested.

AC WAVEFORMS FOR READ OPERATIONS

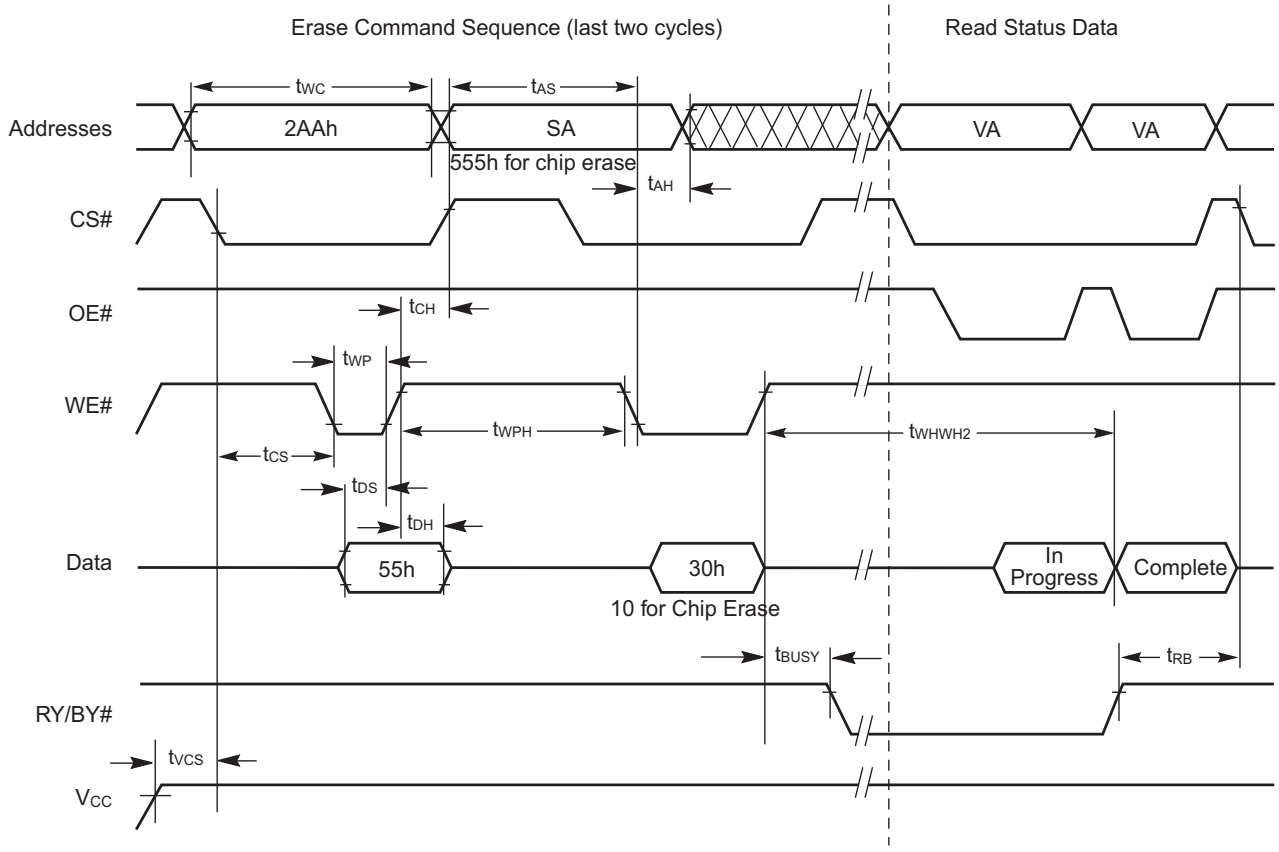


WRITE/ERASE/PROGRAM OPERATION, WE# CONTROLLED



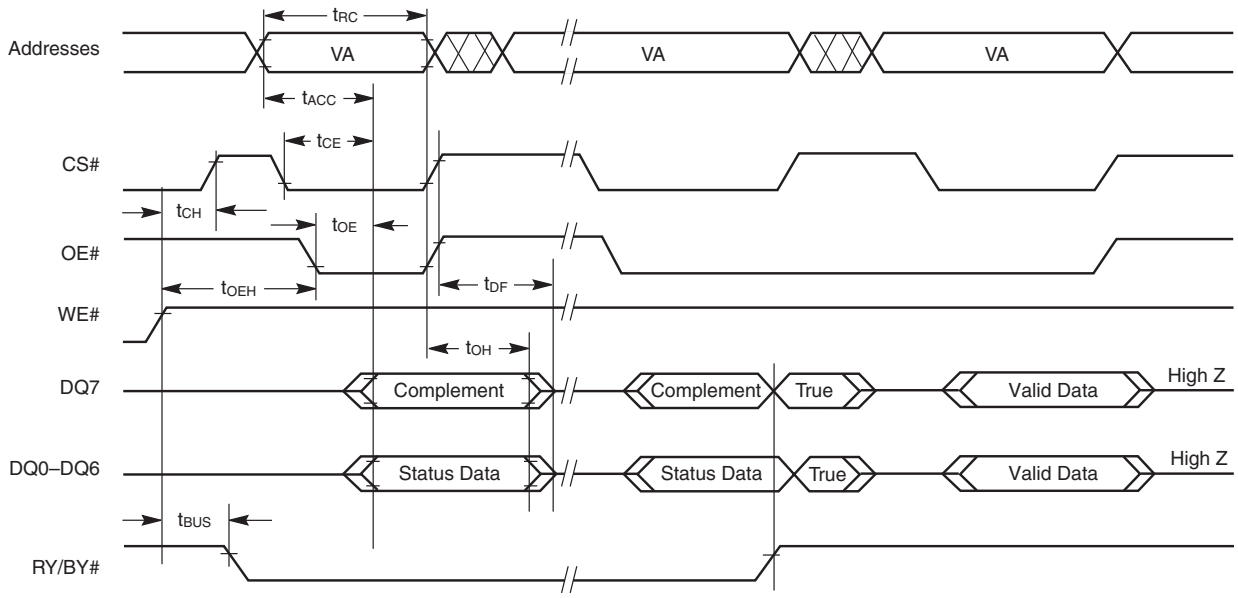
NOTE: PA = program address, PD = program data, D_{OUT} is the true data at the program address.

AC WAVEFORMS CHIP/SECTOR ERASE OPERATIONS



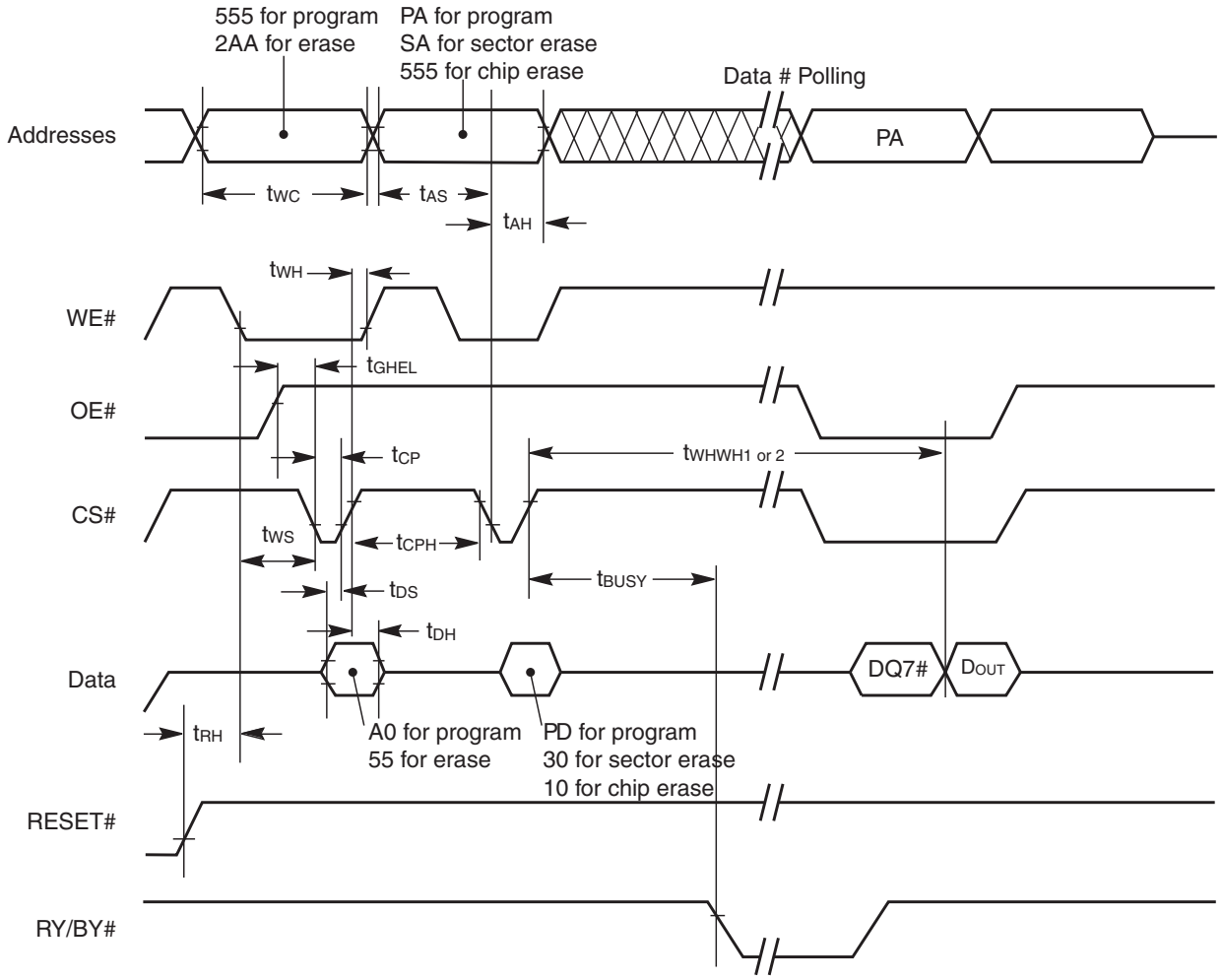
NOTE: SA = sector address (for Sector Erase), VA = Valid Address for reading status data

AC WAVEFORMS FOR DATA# POLLING DURING EMBEDDED ALGORITHM OPERATIONS



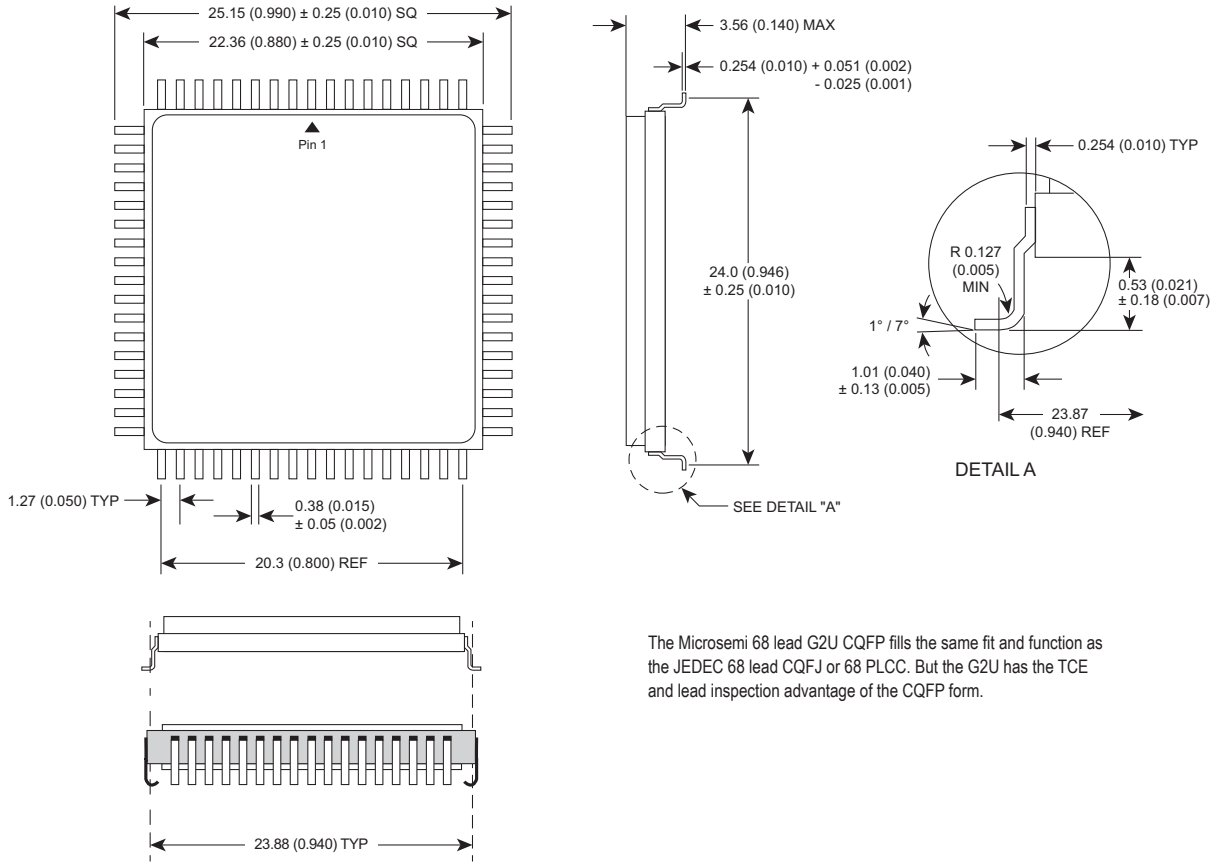
NOTE: VA = Valid address. Illustration shows first status cycle after command sequence, last status read cycle, and array data read cycle

ALTERNATE CS# CONTROLLED PROGRAMMING OPERATION TIMINGS



NOTES:
1. PA = program address, PD = program data, DQ7# = complement of the data written to the device, DOUT = data written to the device.
2. Figure indicates the last two bus cycles of command sequence.

PACKAGE 510 – 68 LEAD, CERAMIC QUAD FLAT PACK, CQFP (G2U)



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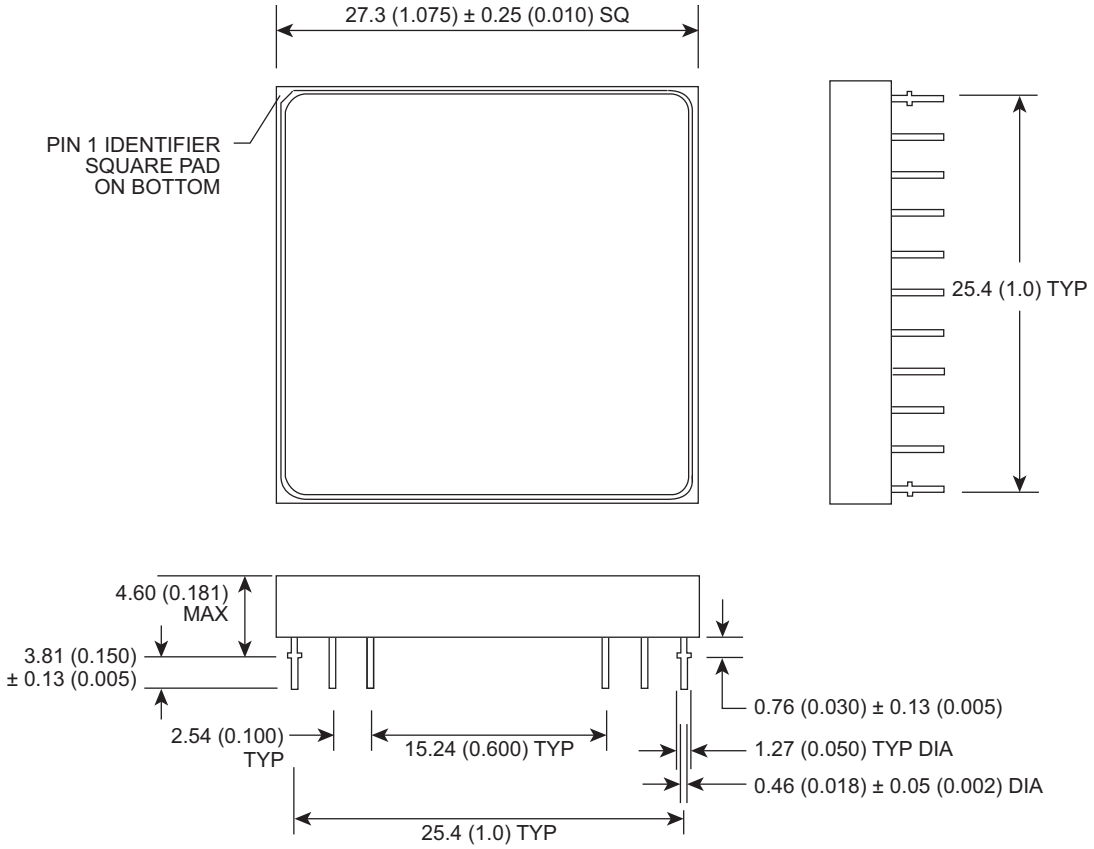
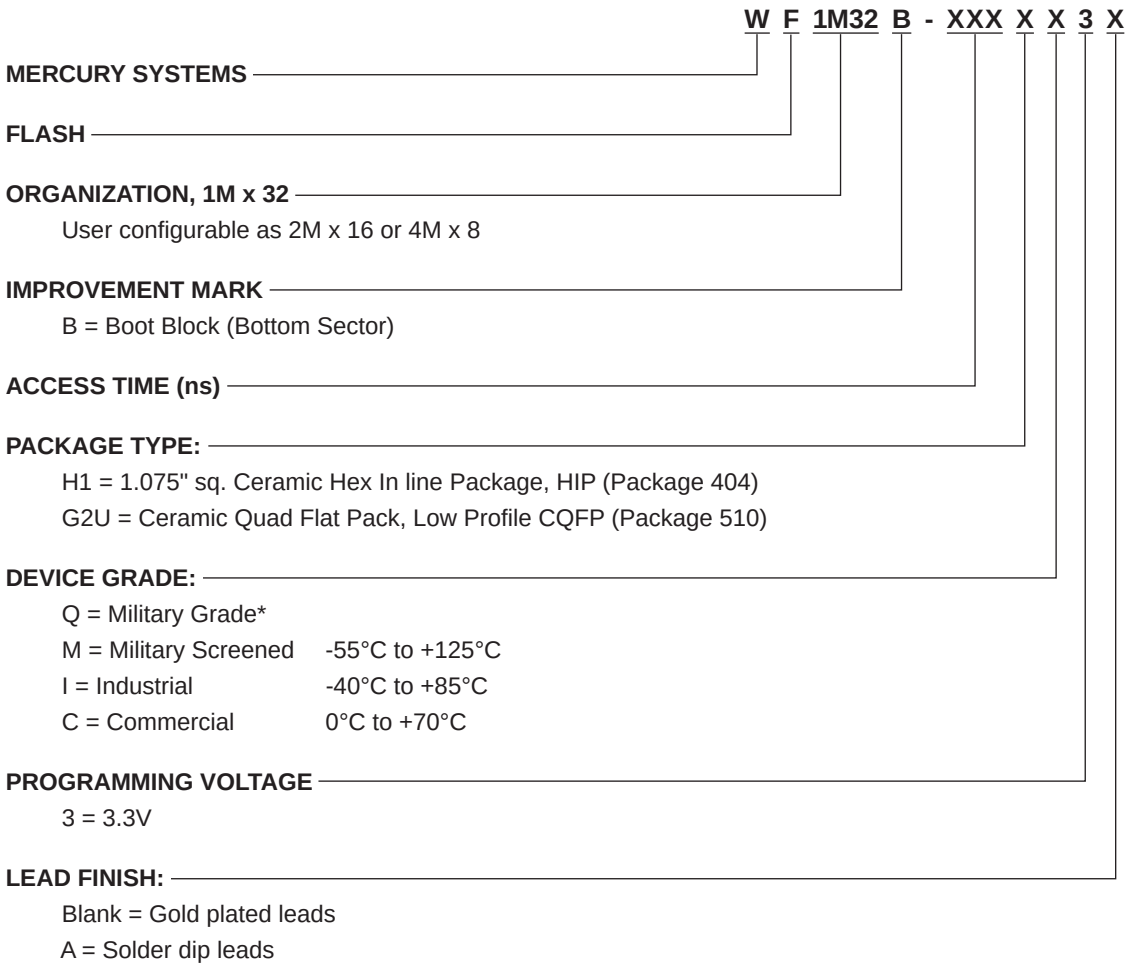
ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

PACKAGE 404: 66 PIN, PGA TYPE, CERAMIC HEX-IN-LINE PACKAGE, HIP (H1)



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

ORDERING INFORMATION



* This product is processed the same as the 5962-XXXXXHXX product but all test and mechanical requirements are per the Mercury Systems data sheet.

Document Title

1Mx32 3.3V NOR FLASH MODULE

Revision History

Rev #	History	Release Date	Status
Rev 8	Changes (Pg. 1-14) 8.1 Change document layout from White Electronic Designs to Microsemi 8.2 Add document Revision History page	June 2011	Final
Rev 9	Changes (Pg. 1, 14) 9.1 Add "NOR" to headline	August 2011	Final
Rev 10	Changes (Pg. 1, 2, 3, 4, 5, 6, 7, 8, 9, 10) 10.1 Change "in byte mote" to "each chip" in the first sub-bullet under Sector Architecture 10.2 Add "#" to WE1-4, CS1-4, OE and RESET in Pin Description on page 2 10.3 Add (M, Q) to Operation Temperature in Absolute Maximum Ratings chart 10.4 Add "#" to CS1-4 in Capacitance chart on page 3 10.5 Delete subhead from DC Characteristics – CMOS Compatible chart 10.6 Update DC Characteristics – CMOS Compatible chart 10.7 Update AC Characteristics chart...CS# Controlled 10.8 Update AC Characteristics chart...WE# Controlled 10.9 Update AC Characteristics chart...Read-Only Operations 10.10 Update AC Waveforms For Read Operations diagram 10.11 Update Write/Erase/Program Operation, WE# Controlled diagram 10.12 Update AC Waveforms Chip/Sector Erase Operations diagram 10.13 Update AC Waveforms For Data# Polling During Embedded Algorithm Operations diagram 10.14 Alternate CS# Controlled Programming Operation Timings	April 2012	Final
Rev 11	Changes (Pg. 1, 3, 12, 13) 11.1 Change 66 pin package type from 400 (H1) to 401 (H) 11.2 Add commercial operating temperature to *Recommended Operating Conditions* chart	June 2012	Final
Rev 12	Changes (Pg. 1) 12.1 Delete 1.0mA standby	December 2012	Final
Rev 13	Change (Pg. 13) 13.1 Changed Device Grade "Q" description from "MIL-STD-883 Compliant" to "MIL-PRF-38534 Class H Compliant."	May 2014	Final
Rev 14	Change (Pg. 13) 14.1 Changed Device Grade "Q" description from "MIL-PRF-38534 Class H Compliant" to "Military Grade."	August 2014	Final
Rev 15	Change (Pg. 12) 15.1 Change 66 pin package type from 401 (H) to 404 (H1)	December 2014	Final
Rev 16	Change (Pg. 11) (ECN 9936) 16.1 Update package dimensions	April 2016	Final
Rev 17	Changes (Pg. All) (ECN 10156) 17.1 Change document layout from Microsemi to Mercury Systems	August 2016	Final