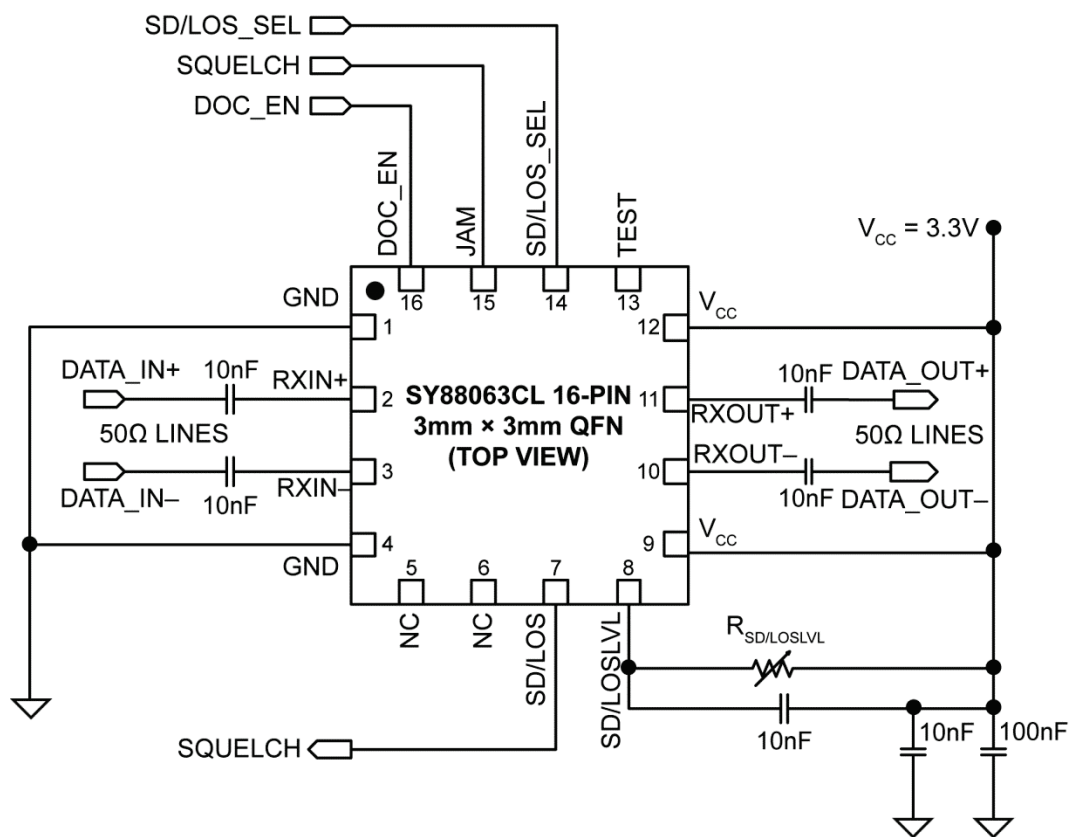


Typical Application Circuit

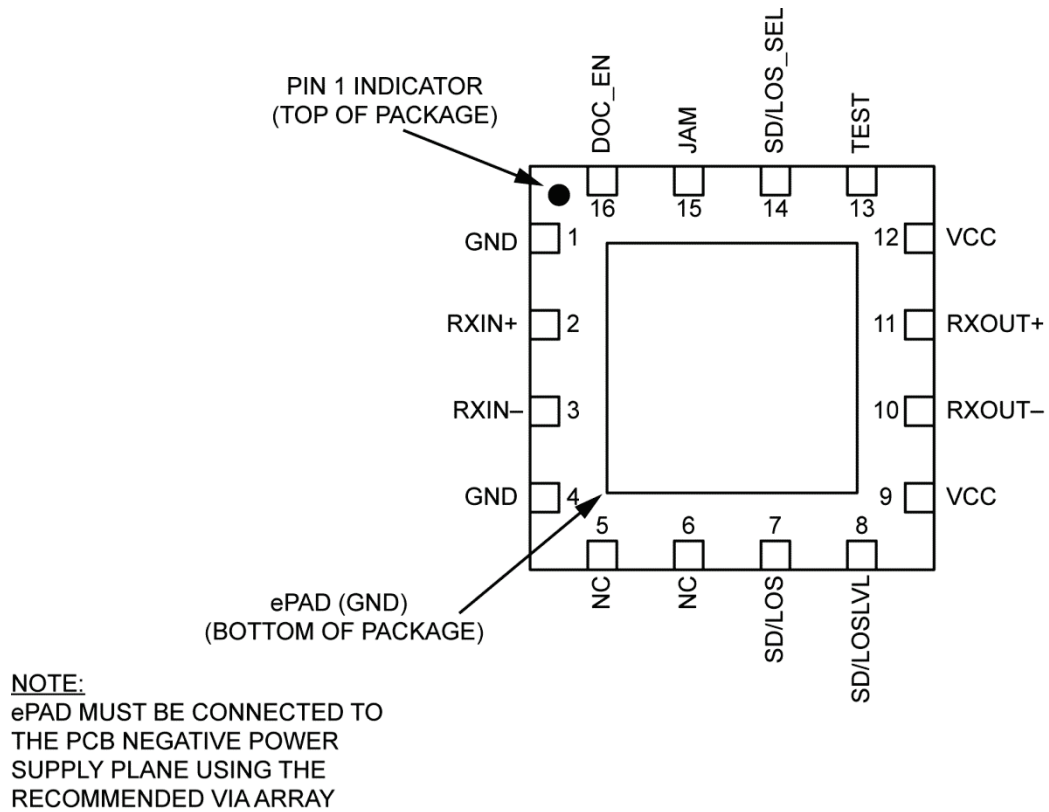


Ordering Information

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY88063CLMG	3mm × 3mm QFN-16	Industrial	063C with Pb-Free bar-line indicator	NiPdAu Pb-Free
SY88063CLMG TR <sup>(1)</sup>	3mm × 3mm QFN-16	Industrial	063C with Pb-Free bar-line indicator	NiPdAu Pb-Free

Note:  
1. Tape and reel.

## Pin Configuration



**16-Pin 3mm × 3mm QFN  
(Top View)**

## Pin Description

Pin #	Pin Name	Pin Type	Functional Description
1	GND	Negative Supply Rail	Negative Supply Rail. Connect to the PCB negative power supply plane that is also connected to the ePAD.
2	RXIN+	High-Speed Data Input	Differential Noninverting Data Input. LVPECL/CML compatible. AC-coupled with 10nF (high-frequency, low-ESR capacitor is recommended). Internally terminated with 50Ω to $V_{CC} - 0.9V$ . AC-coupled only.
3	RXIN-	High-Speed Data Input	Differential Inverting Data Input. LVPECL/CML-compatible. AC-coupled with 10nF (high-frequency, low-ESR capacitor is recommended). Internally terminated by 50Ω to $V_{CC} - 0.9V$ . AC-coupled only.
4	GND	Negative Supply Rail	Negative Supply Rail. Connect to the PCB negative power supply plane that is also connected to the ePAD.
5	NC	No Connect	No Connect. Do not connect to logic circuits or power supply rails.
6	NC	No Connect	No Connect. Do not connect to logic circuits or power supply rails.
7	SD/LOS	Open Collector Logic Output	Output Status Indicator. Loss-of-signal (LOS) or signal detect (SD) open collector output externally terminated with 5kΩ to 10kΩ resistor to $V_{CC}$ . TTL compatible. LOS = High when RXIN± amplitude falls below the threshold set at the SD/LOSLVL pin. SD = Low when RXIN± amplitude falls below the threshold set at the SD/LOSLVL pin.
8	SD/LOSLVL	Analog Input	Analog control input. Sets the trigger threshold for the LOS or SD status indicator signals. If SD/LOS_SEL = High (LOS selected), connect a resistor from the SD/LOSLVL pin (loss of signal threshold level) to $V_{CC}$ to adjust the LOS_Assert threshold for the RXIN± data inputs. If SD/LOS_SEL = Low (SD selected), connect a resistor from the SD/LOSLVL pin (signal detect threshold level) to $V_{CC}$ to adjust the SD_De-assert threshold for the RXIN± data inputs.
9, 12	$V_{CC}$	Positive Supply Rail	Positive power supply input. Bypass with a 0.1μF capacitor in parallel with a 0.01μF low-ESR capacitor to GND as close as possible to the $V_{CC}$ pin.
10	RXOUT-	High-Speed Data Output	Differential inverting data output. CML compatible and internally terminated by 50Ω to $V_{CC}$ . Can be AC- or DC-coupled to downstream devices.
11	RXOUT+	High-Speed Data Output	Differential noninverting data output. CML compatible and internally terminated by 50Ω to $V_{CC}$ . Can be AC- or DC-coupled to downstream devices.
13	TEST	Test Pin	Factory test pin. For factory use only. Do not connect to logic circuits or power supply rails.
14	SD/LOS_SEL	Logic Level Input	Input control signal. TTL-compatible logic input signal to select LOS or SD as the output signal. Internal ~18kΩ pull-up to $V_{CC}$ . Default = High (NC): LOS selected – normal operation LOS/SD_SEL = Low: SD selected and JAM operation is inverted
15	JAM	Logic Level Input	Input control signal. TTL-compatible input signal that enables or disables the RXOUT± output signals. Internal 27kΩ pull-up resistor to $V_{CC}$ . Can be connected to SD/LOS to form a SQUELCH function. When SD/LOS_SEL = High Default = High and RXOUT± outputs are disabled. Low = RXOUT± outputs are enabled Operation is inverted when SD/LOS_SEL = Low and SD is selected.

Pin #	Pin Name	Pin Type	Functional Description
16	DOC_EN	Logic Level Input	<p>Input Control Signal. TTL-compatible logic input signal that enables or disables the digital offset correction (DOC) circuit.</p> <p>Default:</p> <p>DOC_EN = High = Enable with internal 18k<math>\Omega</math> pull-up to V<sub>CC</sub> if not connected to an external logic low or high signal.</p> <p>DOC_EN = Low disables the digital offset correction function.</p> <p>Toggling the DOC_EN signal from high to low to high will cause a reset of the DOC circuitry and initiate a new DOC routine to lock in new DOC values.</p> <p><b>Note:</b> Digital offset correction is not applied to large input signals.</p>
ePAD	GND	Negative Supply Rail	<p>Exposed Thermal Pad. Must be soldered to PCB plane connected to the negative supply rail. The recommended via array is needed to remove heat from the device.</p>

**Absolute Maximum Ratings<sup>(2)</sup>**

Supply Voltage ( $V_{CC}$ )	0V to +4.0V
Input Voltage ( $RXIN\pm$ )	$V_{CC} - 1.5V$ to $V_{CC}$
CML Output Voltage ( $V_{OUT}$ )	$V_{CC} - 1.0V$ to $V_{CC} + 0.5V$
JAM Voltage	0 to $V_{CC}$
SD/LOSLVL Voltage	$V_{CC} - 1.3V$ to $V_{CC}$
Lead Temperature (soldering, 20s)	260°C
Storage Temperature ( $T_s$ )	-65°C to +150°C

**Operating Ratings<sup>(3)</sup>**

Supply Voltage ( $V_{CC}$ )	+3.0V to +3.6V
Ambient Temperature ( $T_A$ )	-40°C to +85°C
Junction Temperature ( $T_J$ )	-40°C to +120°C
Package Thermal Resistance <sup>(4)</sup>	3mm × 3mm QFN-16
( $\theta_{JA}$ ) Still-air	60°C/W
( $\psi_{JB}$ )	33°C/W

**DC Electrical Characteristics**

$V_{CC} = 3.0$  to  $3.6V$ ;  $T_A = -40^\circ C$  to  $+85^\circ C$ , typical values at  $V_{CC} = 3.3V$ ,  $T_A = 25^\circ C$ .

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$I_{CC}$	Power Supply Current	Note 5		60	75	mA
SD/LOSLVL	SD or LOS Threshold Voltage		$V_{CC} - 1.3$		$V_{CC}$	V
$V_{OH}$	$RXOUT\pm$ High Voltage		$V_{CC} - 0.020$	$V_{CC} - 0.005$	$V_{CC}$	V
$V_{OL}$	$RXOUT\pm$ Low Voltage		$V_{CC} - 0.400$	$V_{CC} - 0.350$	$V_{CC} - 0.300$	V
$V_{OS\_DOC\_ON}$	Differential Output Offset	Digital Offset Correction = ON		$\pm 10$		mV
$Z_0$	Single-Ended Output Impedance		45	50	55	$\Omega$
$Z_I$	Single-Ended Input Impedance		45	50	55	$\Omega$

**Notes:**

- Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this datasheet. Exposure to absolute maximum ratings conditions may affect device reliability.
- The datasheet limits are not guaranteed if the device is operated beyond the recommended operating conditions.
- Package thermal resistance assumes that the exposed pad is soldered (or equivalent) to the devices most negative potential on the PCB.  $\psi_{JB}$  and  $\theta_{JA}$  assumes still air and a 4-layer PCB, unless otherwise stated. It also assumes that the recommended via pattern and via sizes on the PCB are used.
- DOC is enabled, outputs  $RXOUT\pm$  are loaded with external 50 $\Omega$  loads, and the outputs are enabled.

## TTL DC Electrical Characteristics

$V_{CC} = 3.0$  to  $3.6V$ ;  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ , typical values at  $V_{CC} = 3.3V$ ,  $T_A = 25^{\circ}C$ .

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$V_{IH}$	JAM, DOC_EN, SD/LOS_SEL Input High Voltage		2.0			V
$V_{IL}$	JAM, DOC_EN, SD/LOS_SEL Input Low Voltage				0.8	V
$I_{IH}$	JAM, DOC_EN, SD/LOS_SEL Input High Current	$V_{IN} = 2.7V$			20	$\mu A$
		$V_{IN} = V_{CC}$			100	
$I_{IL}$	JAM, DOC_EN, SD/LOS_SEL Input Low Current	$V_{IN} = 0.4V$	-0.3			mA
$V_{OH}$	SD or LOS Output High Level	Sourcing 100 $\mu A$	2.4			V
$V_{OL}$	SD or LOS Output Low Level	Sinking 2mA			0.4	V

## AC Electrical Characteristics

$V_{CC} = 3.3V \pm 10\%$ ,  $T_A = -40^\circ C$  to  $+85^\circ C$ . Typical values at  $V_{CC} = 3.3V$ ,  $T_A = 25^\circ C$ ;  $R_{LOAD} = 50\Omega$  to  $V_{CC}$ .

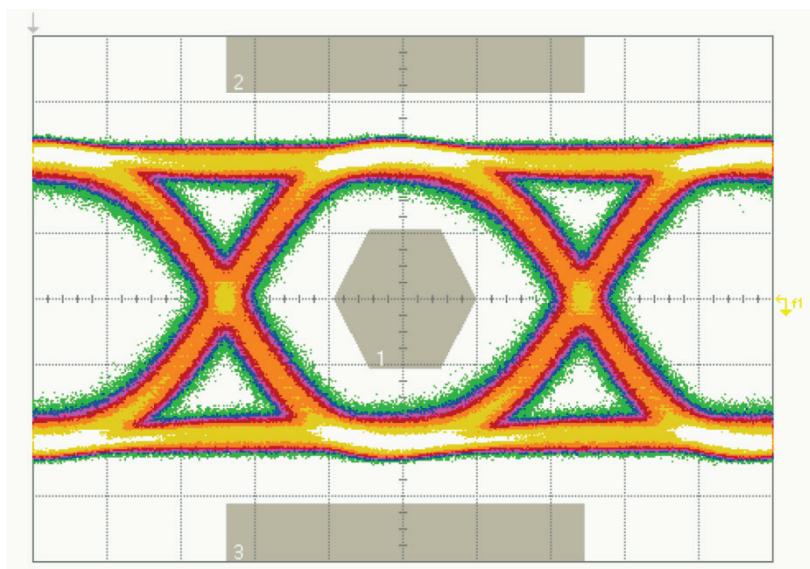
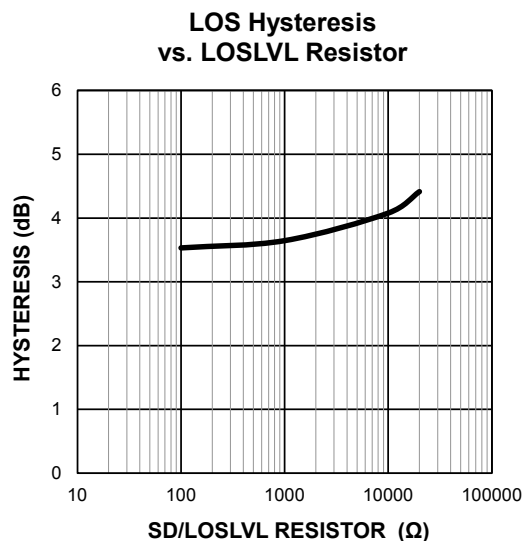
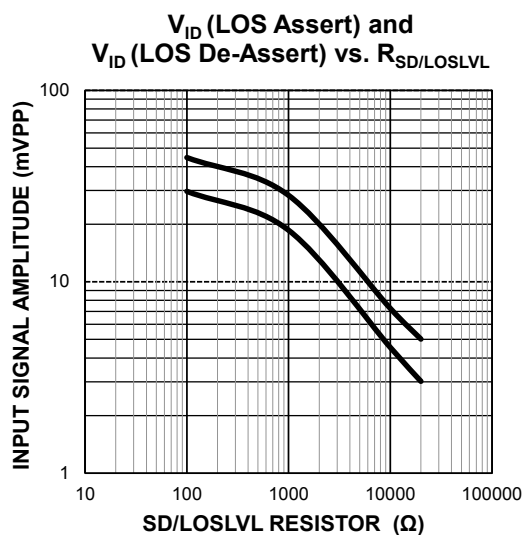
Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$t_r, t_f$	Output Rise/Fall Time (20% to 80%)	Note 6		25	40	ps
$t_{JITTER}$	Deterministic	Note 7		10		ps
	Random	Note 8		1		
$V_{ID\_11.3G}$	Differential Input Voltage Swing	Note 9. See Figure 1.	5		1800	mV <sub>PP</sub>
$V_{ID\_12.5G}$	Differential Input Voltage Swing	Note 9. See Figure 1.	10		1800	mV <sub>PP</sub>
$V_{OD}$	Differential Output Voltage Swing	Note 6	600	700	800	mV <sub>PP</sub>
$t_{LOS\_D}, t_{LOS\_A}$ $t_{SD\_D}, t_{SD\_A}$	LOS De-assert, LOS Assert Time SD De-assert, SD Assert Time	Note 10		75	120	ns
$LOS_{AL\_20k}$	Low LOS Assert Level	$R_{LOSLVL} = 20k\Omega$ , Note 9		3		mV <sub>PP</sub>
$LOS_{DL\_20k}$	Low LOS De-assert Level	$R_{LOSLVL} = 20k\Omega$ , Note 9		5		mV <sub>PP</sub>
$HYS_{L\_20k}$	Low LOS Hysteresis	$R_{LOSLVL} = 20k\Omega$ , Note 11	2	4.4	6	dB
$LOS_{AM\_10k}$	Medium LOS Assert Level	$R_{LOSLVL} = 10k\Omega$ , Note 9		4.5		mV <sub>PP</sub>
$LOS_{DM\_10k}$	Medium LOS De-assert Level	$R_{LOSLVL} = 10k\Omega$ , Note 9		7.3		mV <sub>PP</sub>
$HYS_{M\_10k}$	Medium LOS Hysteresis	$R_{LOSLVL} = 10k\Omega$ , Note 11	2	4.1	6	dB
$LOS_{AH1\_1k}$	High1 LOS Assert Level	$R_{LOSLVL} = 1k\Omega$ , Note 9		18.6		mV <sub>PP</sub>
$LOS_{DH1\_1k}$	High1 LOS De-assert Level	$R_{LOSLVL} = 1k\Omega$ , Note 9		28.3		mV <sub>PP</sub>
$HYS_{H1\_1k}$	High1 LOS Hysteresis	$R_{LOSLVL} = 1k\Omega$ , Note 11	2	3.6	6	dB
$LOS_{AH2\_100}$	High2 LOS Assert Level	$R_{LOSLVL} = 100\Omega$ , Note 9		29.7		mV <sub>PP</sub>
$LOS_{DH2\_100}$	High2 LOS De-assert Level	$R_{LOSLVL} = 100\Omega$ , Note 9		44.6		mV <sub>PP</sub>
$HYS_{H2\_100}$	High2 LOS Hysteresis	$R_{LOSLVL} = 100\Omega$ , Note 11	2	3.5	6	dB
$A_{V(Diff)\_063C}$	Differential Voltage Gain			44		dB
$S_{21\_063C}$	Single-Ended Small-Signal Gain		32	38		dB
$t_{DOC\_DELAY}$	DOC Delay Time			15		$\mu s$
$t_{DOC\_LOCK}$	DOC Lock Time			150		$\mu s$

### Note:

- Amplifier is in limiting mode. Input is a 200MHz square wave.
- Deterministic jitter is measured using 10Gbps K28.5 pattern,  $V_{ID} = 20mV_{PP}$ .
- Random jitter is measured using 10Gbps K28.7 pattern,  $V_{ID} = 20mV_{PP}$ .
- See "Typical Operating Characteristics" for a graph showing how to choose a particular  $R_{LOSLVL}$  for a particular LOS assert and its associated de-assert amplitude.
- In real world applications, the LOS de-assert/assert time can be strongly influenced by the RC time constant of the AC-coupling capacitor and the 50 $\Omega$  input termination. To keep this time low, use a decoupling capacitor with the lowest value that is allowed by the data rate and the number of consecutive identical bits in the application (typical values are in the range of 0.001 $\mu F$  to 0.1 $\mu F$ ).
- This specification defines electrical hysteresis as 20log (LOS de-assert/LOS assert). The ratio between optical hysteresis and electrical hysteresis is found to vary between 1.5 and 2, depending on the level of received optical power and ROSA characteristics.

## Typical Operating Characteristics

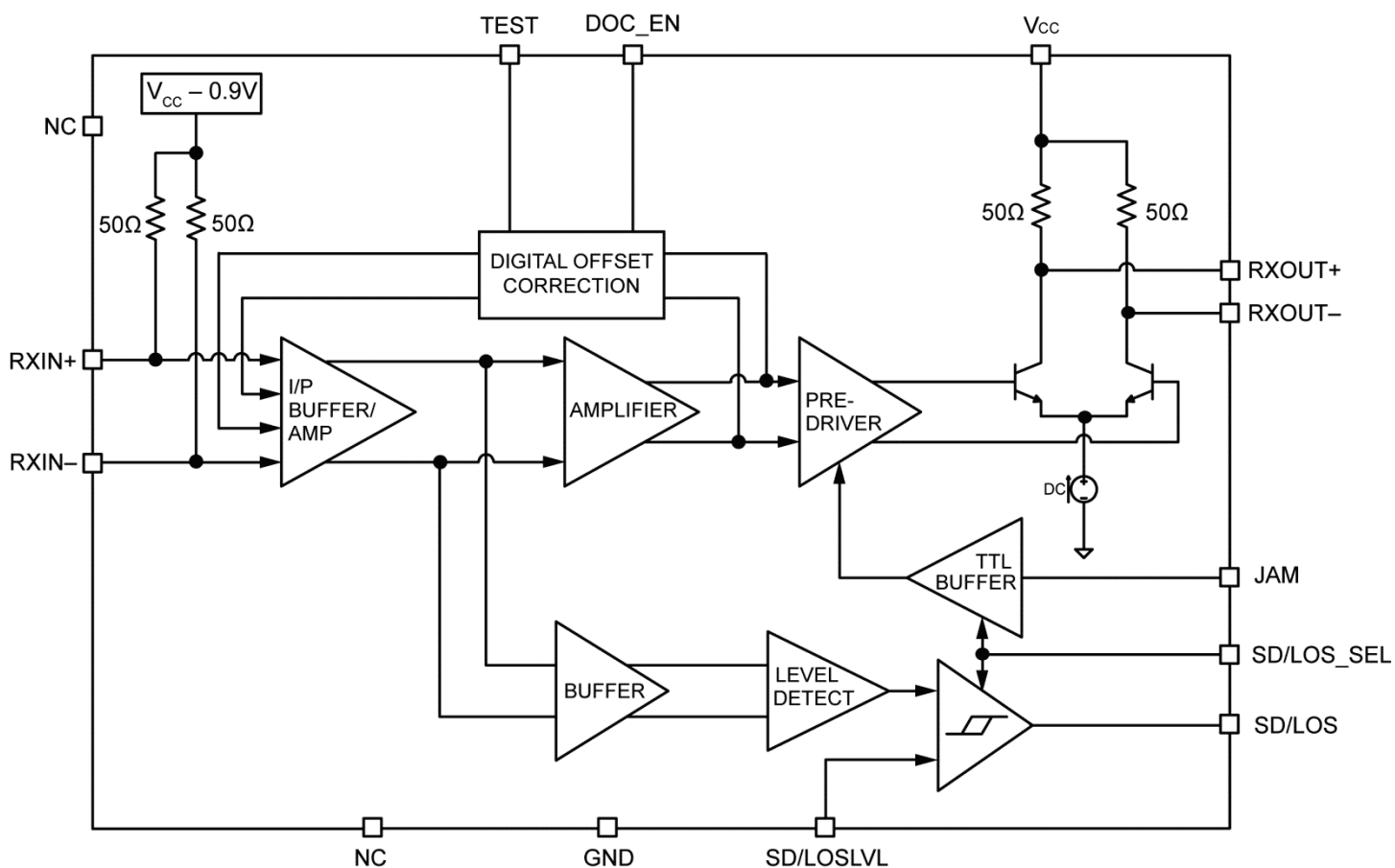
$V_{CC} = 3.3V$ ,  $T_A = 25^\circ C$ ,  $R_{LOAD} = 50\Omega$  to  $V_{CC}$ , unless otherwise stated.



Linear Mode 10.3G Output with 5mV<sub>PP</sub> Differential Input Signal



## Functional Block Diagram



## Functional Description

The SY88063CL is a high-sensitivity, high-bandwidth limiting post amplifier. It operates from a single +3.3V power supply across the entire industrial temperature range of  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ .

Signals with data rates from 1.0625Gbps to 12.5Gbps and amplitudes as small as  $5\text{mV}_{\text{pp}}$  are supported. Figure 1 shows the allowed input voltage swing.

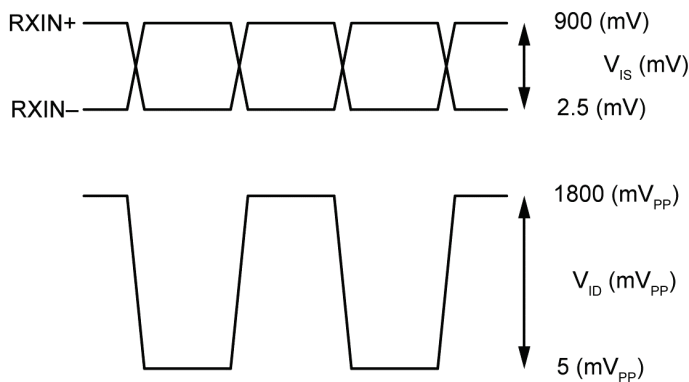


Figure 1.  $V_{\text{IS}}$  and  $V_{\text{ID}}$  Definition

The SY88063CL has a selectable SD or LOS status output signal that can be fed back to the JAM input to perform the SQUELCH function for output stability if there is no signal at the input. SD/LOSLVL sets the sensitivity of the input amplitude detection.

The SY88063CL has a user-selectable, integrated digital offset correction function to cancel internally generated output offsets.

### Input Amplifier/Buffer

Figure 2 shows a simplified schematic of the input stage. The high sensitivity of the input amplifier allows signals as small as  $5\text{mV}_{\text{pp}}$  to be detected and amplified. The input amplifier allows input signals as large as  $1800\text{mV}_{\text{pp}}$ . Input small signals are amplified with a typical 44dB differential voltage gain.

### Output Buffer

The SY88063CL CML output buffer is designed to drive  $50\Omega$  impedance transmission lines and is internally terminated with  $50\Omega$  to  $V_{\text{CC}}$ . Figure 3 shows a simplified schematic of the output stage.

### Signal Detect/Loss-of-Signal (SD/LOS)

The SY88063CL generates a user-selectable (SD/LOS\_SEL pin) signal detect (SD) or loss-of-signal (LOS) open-collector TTL output, as shown in Figure 4. LOS is used to determine whether the input amplitude is too small to be considered as a valid input. LOS asserts high if the input amplitude falls below the threshold set by

SD/LOSLVL and de-asserts low otherwise. LOS can be fed back to the JAM input to perform the SQUELCH function and to maintain output stability under a LOS condition. JAM de-asserts the true output signal low without removing the input signals. Typically, 4dB LOS hysteresis is provided to prevent chattering.

When SD/LOS\_SEL is used to select the SD output on the SD/LOS pin, SD is asserted when the differential input signal amplitude exceeds the level set by the SD/LOSLVL resistor. The JAM operation is inverted when SD is selected.

### Signal Detect/Loss-of-Signal Level Setting

A programmable SD/LOS level set pin (SD/LOSLVL) sets the threshold of the input amplitude detection. Connecting an external resistor between  $V_{\text{CC}}$  and SD/LOSLVL sets the threshold voltage. This voltage ranges from  $V_{\text{CC}}$  to  $V_{\text{CC}} - 1.3\text{V}$ . The external resistor creates a voltage divider between  $V_{\text{CC}}$  and  $V_{\text{CC}} - 1.3\text{V}$ , as shown in Figure 5.

### Hysteresis

The SY88063CL provides typically 4dB LOS electrical hysteresis, which is defined as  $20\log(V_{\text{IN\_LOS\_De-Assert}} \div V_{\text{IN\_LOS\_Assert}})$ . Because the relationship of the voltage output of the ROSA to optical power at its input is linear, the optical hysteresis is typically half of the electrical hysteresis reported in the datasheet. In practice the ratio between electrical and optical hysteresis is found to be between 1.5 and 1.8. Thus, 4dB electrical hysteresis corresponds to an optical hysteresis within the range of 2dB to 2.4dB.

### Digital Offset Correction (DOC)

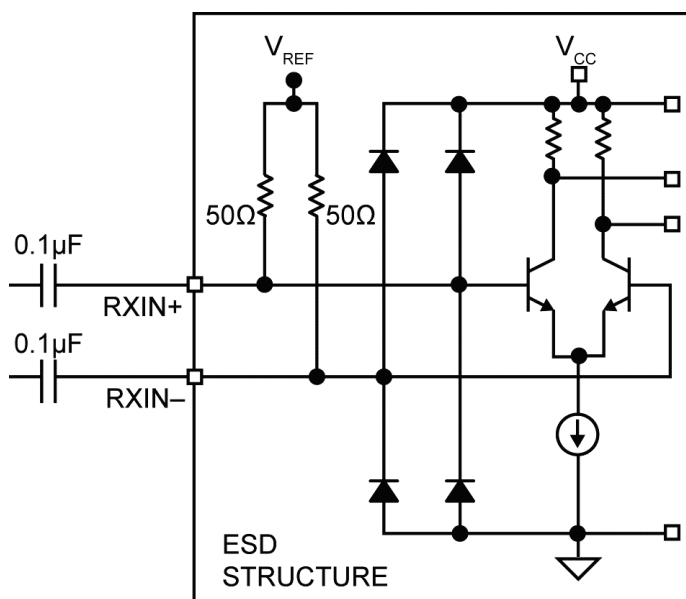
The digital offset correction (DOC) circuit compensates for the inherent offsets found in high-gain amplifier circuits and minimizes the offset seen at the outputs. DOC is a user-selectable feature using the DOC\_EN pin as defined in the "Pin Description" table.

Conventional analog offset compensation techniques may be susceptible to drift from long continuous identical digit (CID) patterns. They can also add additional cost due to the extra DAC and manufacturing setup time needed to optimize each individual module. The SY88063CL avoids both of these issues and provides a performance/cost optimized solution.

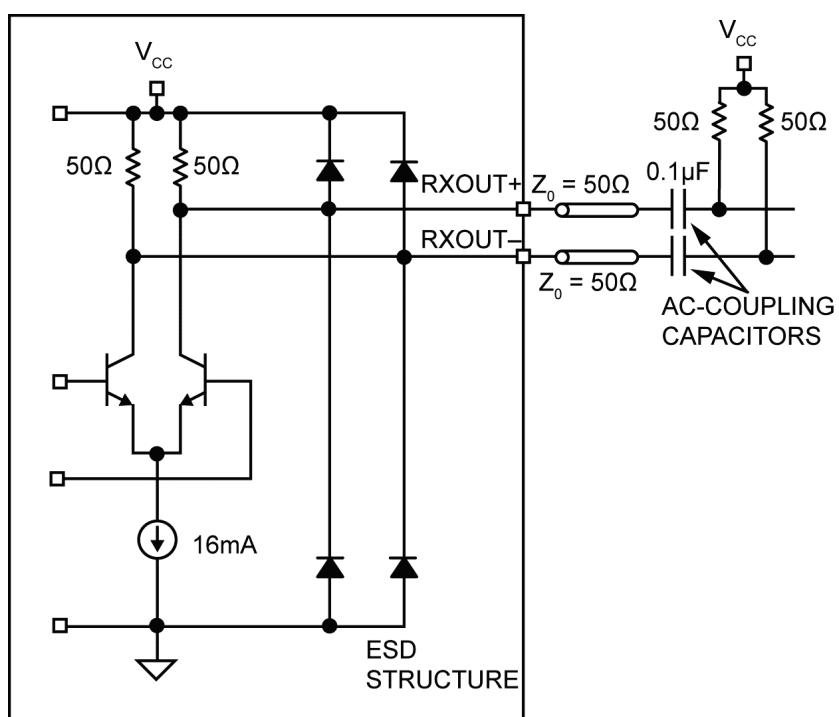
The DOC circuitry automatically detects any internal device offsets and locks the correction values but does not apply offset correction to large input signals.

The DOC is enabled by default unless DOC\_EN is pulled low by an external logic level signal. It can be reset by toggling the DOC\_EN pin high-to-low-to-high. The DOC reset routine typically completes in  $200\mu\text{s}$ .

## Functional Circuit Structures



### Figure 2. Input Structure



### Figure 3. Output Structure

## Functional Circuit Structures (Continued)

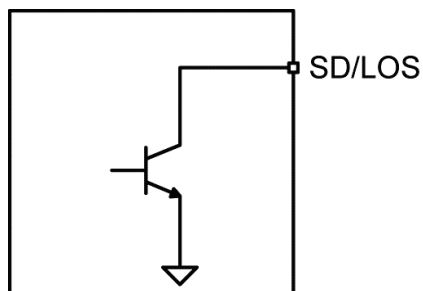


Figure 4. SD/LOS Output Structure

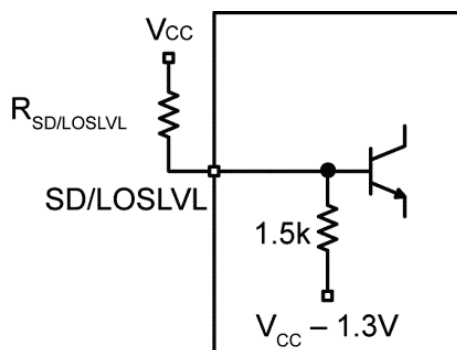
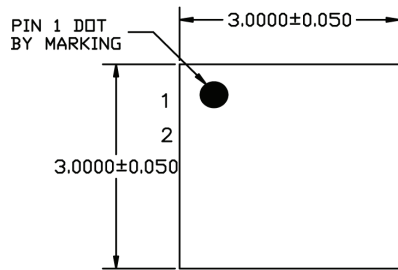


Figure 5. SD/LOSLVL Setting Circuit

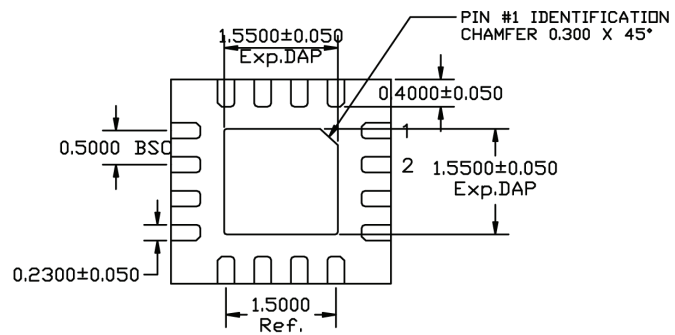
## Related Product and Support Documentation

Document Number	Title	Application Note Link
AN-45	Notes on Sensitivity and Hysteresis in Micrel Post Amplifiers	<a href="http://www.micrel.com/PDF/HBW/App-Notes/an-45.pdf">www.micrel.com/ PDF/HBW/App-Notes/an-45.pdf</a>
SY88053CL_63CL_EB	SY88053CL/SY88063CL Evaluation Board	<a href="http://www.micrel.com/PDF/Eval-Board/SY88053CL_63CL_EB.pdf">http://www.micrel.com/ PDF/Eval-Board/SY88053CL_63CL_EB.pdf</a>

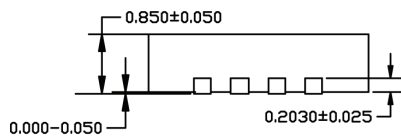
## Package Information<sup>(12)</sup>



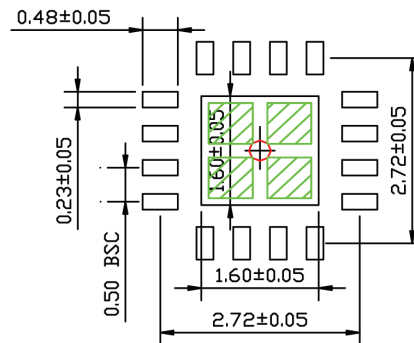
TOP VIEW  
NOTE: 1, 2, 3



BOTTOM VIEW  
NOTE: 1, 2, 3



SIDE VIEW  
NOTE: 1, 2, 3



RECOMMENDED LAND PATTERN  
NOTE: 4, 5

- NOTE:
1. MAX PACKAGE WARPAGE IS 0.05 MM
  2. MAX ALLOWABLE BURR IS 0.076MM IN ALL DIRECTIONS
  3. PIN #1 IS ON TOP WILL BE LASER MARKED
  4. RED CIRCLE IN LAND PATTERN INDICATE THERMAL VIA. SIZE SHOULD BE 0.30-0.3M IN DIAMETER AND SHOULD BE CONNECTED TO GND FOR MAX THERMAL PERFORMANCE
  5. GREEN RECTANGLES (SHADED AREA) INDICATE SOLDER STENCIL OPENING ON EXPOSED PAD AREA. SIZE SHOULD BE 0.60x0.60 MM IN SIZE, 0.20 MM SPACING.

### 16-Pin (3mm × 3mm) QFN-16

#### Note:

12. Package information is correct as of the publication date. For updates and most current information, go to [www.micrel.com](http://www.micrel.com).

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