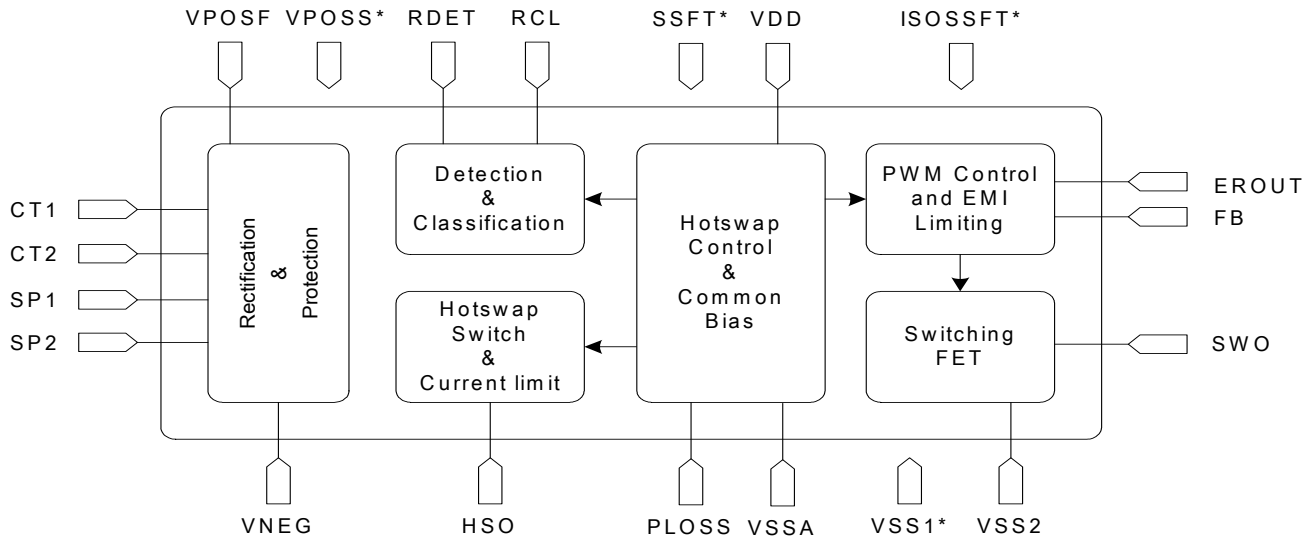
Functional Block Diagram



Note: Original pin names shown for compatibility reasons, but SSFT, ISOSSFT, VPOSS, and VSS1 are not internally connected.

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1. Electrical Specifications

Table 1. Recommended Operating Conditions

Description	Symbol	Min	Typ	Max	Units
|CT1 – CT2| or |SP1 – SP2|	VPORT	2.8	—	57	V
Ambient Operating Temperature	TA	–40	25	85	°C

Note: Unless otherwise noted, all voltages referenced to VNEG. All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at nominal supply voltage and ambient temperature unless otherwise noted.

Table 2. Absolute Maximum Ratings[1]

Type	Description	Rating	Unit
Voltage	CT1 to CT2[2]	–100 to 100	V
	SP1 to SP2[2]	–100 to 100	
	VPOS	–0.7 to 100	
	HSO	–0.7 to 100	
	V_{SS1}, V_{SS2}, or V_{SSA}	–0.7 to 100	
	V_{SS1} to V_{SS2} or V_{SSA}	–0.3 to 0.3	
	SWO[3]	–0.7 to 100	
	$\overline{\text{PLOSS}}$ to VPOS	–100 to 0.7	
	RDET	–0.7 to 100	
	VDD to VSS1, VSS2, or VSSA	–0.3 to 5.5	
Peak Current	CT1, CT2, SP1, SP2[2]	–5 to 5	A
	VPOS[2]	–5 to 5	
DC Current[4]	CT1,CT2,SP1,SP2	–0.2 to 0.2	A
Ambient Temperature	Storage	–65 to 150	°C
	Operating	–40 to 85	

Notes:
1. Unless otherwise noted, all voltages referenced to VNEG. Permanent device damage may occur if the maximum ratings are exceeded. Functional operation should be restricted to those conditions specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may adversely affect device reliability.
2. Si3402 provides internal protection from certain transient surge voltages on these pins. Please refer to “AN956: Si3402-B POE PD Controller Design Guide” for details.
3. SWO is referenced to V_{SS2}.
4. Higher dc current is possible in the application, but only utilizing external bridge diodes. Refer to “AN956: Si3402-B-POE-PD Controller Design Guide” for more information.

Table 3. Electrical Characteristics

Parameter	Description	Min	Typ	Max	Unit
VPORT	Detection[1]	2.7	—	11	V
	Classification	14	—	22	
	UVLO turn-off for rising voltages (switching regulator turns ON)	—	37	42	
	UVLO turn-on for falling voltages (switching regulator turns OFF)	30	32	36	
	Integrated Transient Surge Clamp Voltage[2]	—	100	—	
Input Offset Current	VPORT < 10 V	—	—	10	µA
Diode Bridge Leakage	VPORT = 57 V	—	—	25	µA
IPORT Classification[3]	Class 0	0	—	4	mA
	Class 1	9	—	12	
	Class 2	17	—	20	
	Class 3	26	—	30	
IPORT Operating Current[4]	37 V ≤ VPORT ≤ 57 V	—	2	3.1	mA
Current Limit[5]	Inrush	—	140	—	mA
	Operating	470	—	680	mA
Hotswap FET On-Resistance	37 V ≤ VPORT ≤ 57 V	1	—	3	Ω
Power Loss ($\overline{\text{PLOSS}}$) VPORT Threshold	VPOS - (Greater of CT1 or CT2), or VPOS - (Greater of SP1 or SP2)	1	1.5	2	V
Switcher Frequency		—	350	—	kHz
Maximum Switcher Duty Cycle		—	50	75	%
Switcher Output Transient Voltage[6]		—	—	100	V
Switching FET On-Resistance		0.3	0.5	1.3	Ω
Switching FET Peak Current		—	—	2.4	A

Notes:

1. Assumes use of internal diode bridge or external Schottky bridge.
2. Transient surge as defined in IEEE 802.3 is applied across CT1-CT2 or SP1-SP2.
3. The classification currents are guaranteed only when recommended RCLASS resistors are used, as specified in Table 7.
4. IPORT includes full operating current of switching regulator controller.
5. The PD interface includes dual-level input current limit. At turn-on, before the HSO load capacitor is charged, the current limit is set at the inrush level. After the capacitor has been charged within ~0.4 V of VNEG, the operating current limit is engaged. This higher current limit remains active until the UVLO lower limit has been tripped or until the hotswap switch is sufficiently current-limited to cause a foldback of the HSO voltage. For more information, see "3.2.5. Dual Input Current Limit and Switcher Turn-On" on page 12.
6. For switcher output transient voltage control with isolated applications, please use a voltage snubber circuit. Refer to “AN956: Si3402-B POE PD Controller Design Guide” for additional guidance on voltage snubber circuit design.
7. Applies to non-isolated applications only.

Table 3. Electrical Characteristics (Continued)

Parameter	Description	Min	Typ	Max	Unit
Regulated Feedback @ Pin FB[7]	DC Avg.	1.30	1.35	1.40	V
VDD Accuracy	0-5 mA and UVLO OFF (Switching regulator ON)	4.5	—	5.5	V
Thermal Shutdown	Junction temperature	—	160	—	ºC
Thermal Shutdown Hysteresis		—	25	—	ºC

Notes:

1. Assumes use of internal diode bridge or external Schottky bridge.
2. Transient surge as defined in IEEE 802.3 is applied across CT1-CT2 or SP1-SP2.
3. The classification currents are guaranteed only when recommended RCLASS resistors are used, as specified in Table 7.
4. IPORT includes full operating current of switching regulator controller.
5. The PD interface includes dual-level input current limit. At turn-on, before the HSO load capacitor is charged, the current limit is set at the inrush level. After the capacitor has been charged within ~0.4 V of VNEG, the operating current limit is engaged. This higher current limit remains active until the UVLO lower limit has been tripped or until the hotswap switch is sufficiently current-limited to cause a foldback of the HSO voltage. For more information, see "3.2.5. Dual Input Current Limit and Switcher Turn-On" on page 12.
6. For switcher output transient voltage control with isolated applications, please use a voltage snubber circuit. Refer to “AN956: Si3402-B POE PD Controller Design Guide” for additional guidance on voltage snubber circuit design.
7. Applies to non-isolated applications only.

Table 4. Total Power Dissipation

Description	Test Condition	Min	Typ	Max	Unit
Power Dissipation	VPORT = 50 V, V_{OUT} = 5 V, 2 A	—	1.2	—	W
Power Dissipation*	VPORT = 50 V, V_{OUT} = 5 V, 2 A w/ diode bridges bypassed	—	0.7	—	W

***Note:** It is recommended that the on-chip diode bridges be bypassed when input power requirements are >10 W or in thermally-constrained applications. For more information, see “AN956: Si3402-B POE PD Controller Design Guide”.

Table 5. Package Thermal Characteristics

Parameter	Symbol	Test Condition	Typ	Unit
Thermal Resistance (Junction to Ambient)	θ_{JA}	Still air; assumes a minimum of nine thermal vias are connected to a 2 in^2 heat spreader plane for the package “pad” node (VNEG).	45.1	°C/W

2. Typical Application Schematics*

***Note:** These are simplified schematics. See “AN956: Si3402-B POE PD Controller Design Guide” for more information.

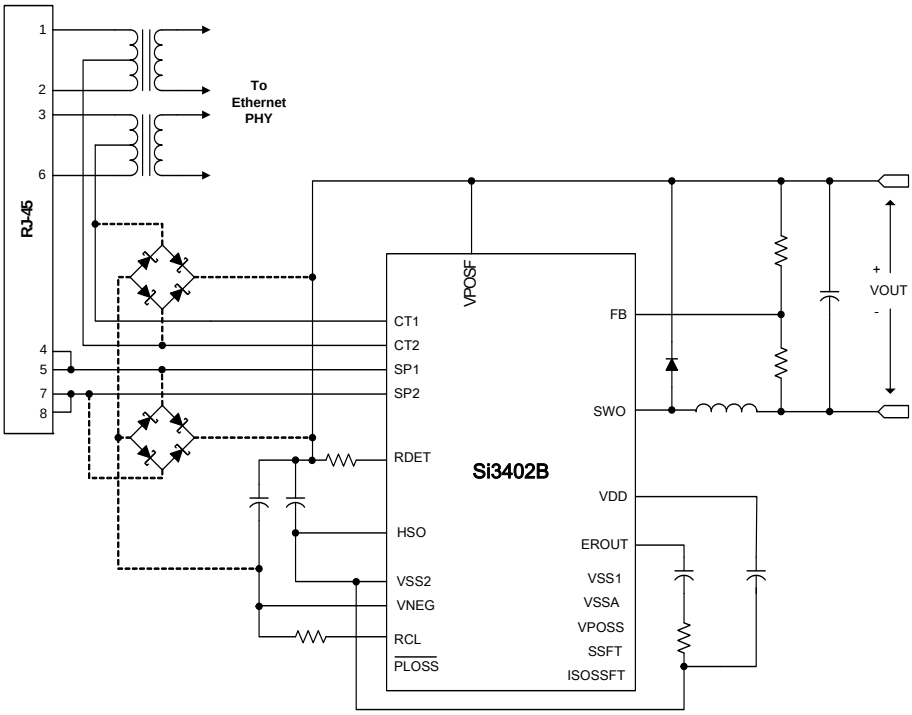


Figure 1. Schematic—Non-Isolated Buck Topology*

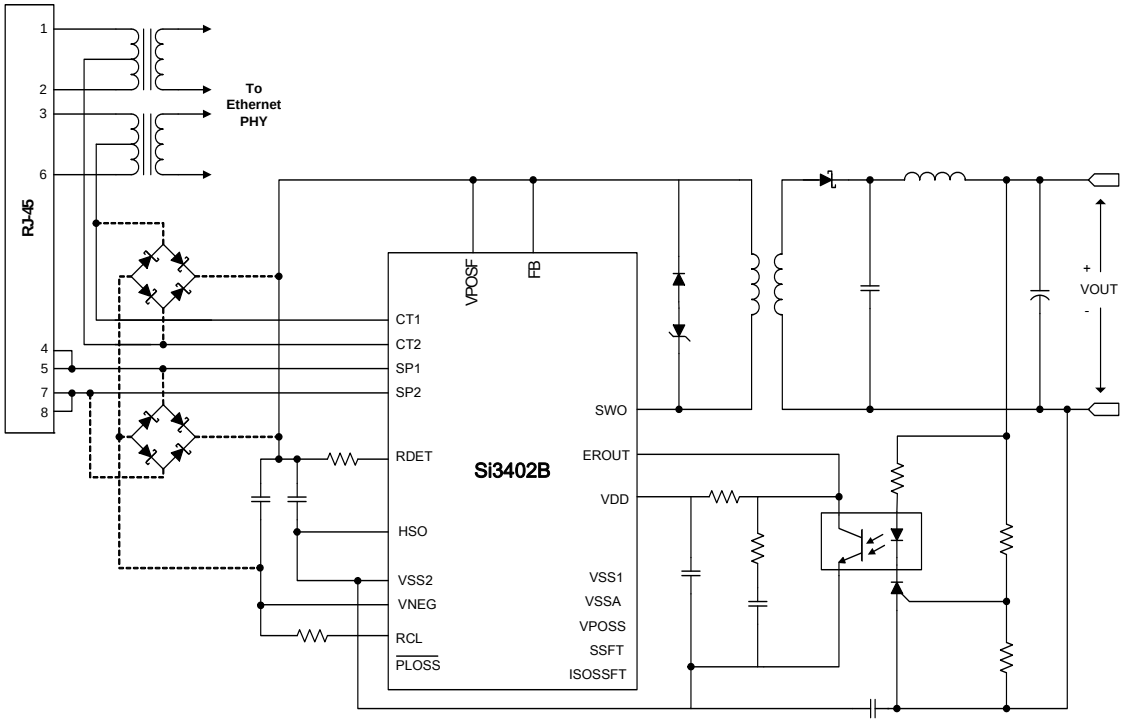


Figure 2. Schematic—Isolated Flyback Topology

3. Functional Description

The Si3402 consists of two major functions: a hotswap controller/interface and a complete pulse-width-modulated switching regulator (controller and power FET).

3.1. Overview

The hotswap interface of the Si3402 provides the complete front end of an IEEE 802.3-compliant PD. The Si3402 also includes two full diode bridges, a transient voltage surge suppressor, detection circuit, classification current source, and dual-level hotswap current limiting switch. This high level of integration enables direct connection to the RJ-45 connector, simplifies system design, and provides significant advantages for reliability and protection. The Si3402 requires only four standard external components (detection resistor, optional classification resistor, load capacitor, and input capacitor) to create a fully IEEE 802.3-compliant interface.

The Si3402 integrates a complete pulse-width modulated switching regulator that includes the controller and power FET. The switching regulator utilizes a constant frequency pulse-width modulated controller optimized for all possible load conditions in PoE applications. The regulator integrates a low on-resistance (Ron) switching power MOSFET that minimizes power dissipation, increases overall regulator efficiency, and simplifies system design. An integrated error amplifier, precision reference, and soft-start feature provide the flexibility of using a non-isolated buck regulator topology or an isolated flyback regulator topology.

The Si3402 is designed to operate with both IEEE 802.3-compliant Power Sourcing Equipment (PSE) and pre-standard (legacy) PSEs that do not adhere to the IEEE 802.3 specified inrush current limits. The Si3402 is compatible with compliant and legacy PSEs because it uses two levels for the hotswap current limits. By setting the initial inrush current limit to a low level, a PD based on the Si3402 minimizes the current drawn from either a compliant or legacy PSE during startup. After powering up, the Si3402 automatically switches to a higher-level current limit, thereby allowing the PD to consume up to 12.95 W (the max power allowed by the IEEE 802.3 specification).

Excessive power cycling or short circuit faults will engage the thermal overload protection to prevent the on-chip power MOSFETs from exceeding their safe and reliable operating ranges. The switching regulator power MOSFET has been designed and sized to withstand the high peak currents created when converting a high-voltage, low-current supply into a low-voltage, high-current supply.

3.2. PD Hotswap Controller

The Si3402 hotswap controller changes its mode of operation based on the input voltage applied to the high-voltage supply inputs (CT1, CT2, SP1, SP2), the IEEE 802.3-defined modes of operation, and internal controller requirements. Table 6 defines the modes of operation for the hotswap interface.

Table 6. Hotswap Interface Modes

Input Voltage (|CT1-CT2| or |SP1-SP2|)	Si3402 Mode
0 to 2.7 V	Inactive
2.7 to 11 V	Detection signature
11 to 14 V	Transition region
14 to 22 V	Classification signature
22 to 42 V	Transition region
37 up to 57 V	Switcher operating mode (hysteresis limit based on rising input voltage)
57 down to 32 V	Switcher operating mode (hysteresis limit based on falling input voltage)

Figure 3 provides a representation of the input lines, protection, and hotswap circuits on the Si3402.

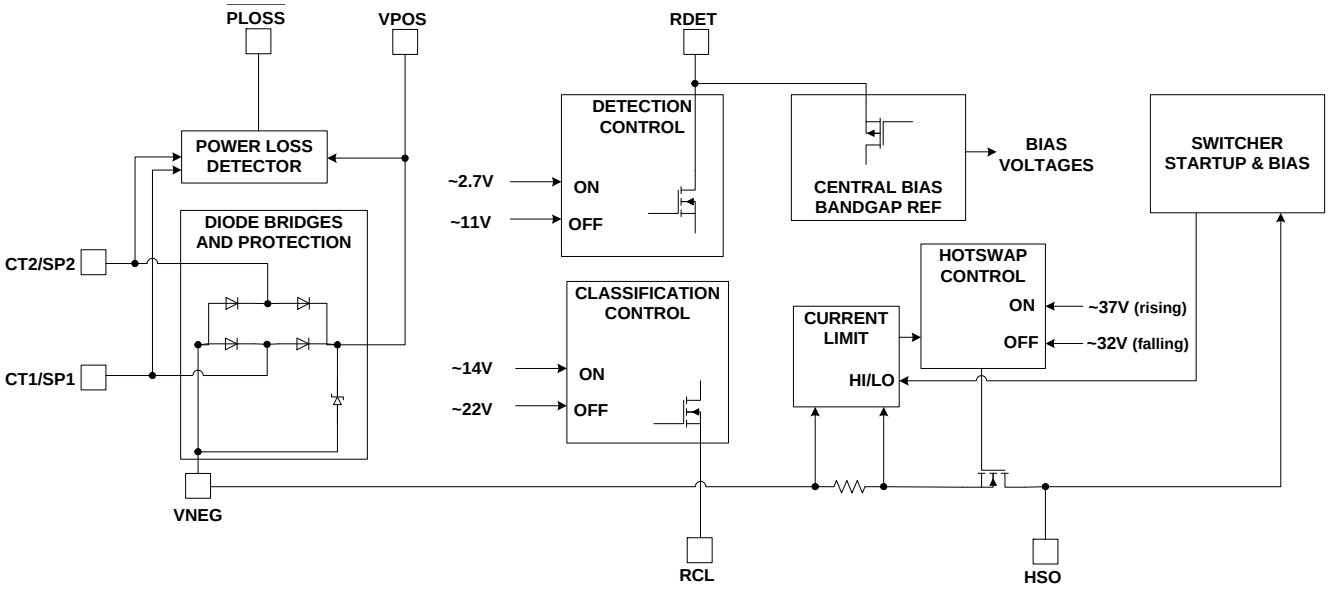


Figure 3. Input Lineside and Hotswap Block Diagram

3.2.1. Rectification Diode Bridges and Surge Suppressor

The IEEE 802.3 specification defines the input voltage at the RJ-45 connector of the PD with no reference to polarity. In other words, the PD must be able to accept power of either polarity at each of its inputs. This requirement necessitates the use of two sets of diode bridges, one for the CT1 and CT2 pins and one for the SP1 and SP2 pins to rectify the voltage. Furthermore, the standard requires that a PD withstand a high-voltage transient surge as defined in the IEEE 802.3 specification. Typically, the diode bridge and the surge suppressor have been implemented externally, adding cost and complexity to the PD system design.

The diode bridge* and the surge suppressor have been integrated into the Si3402, thus reducing system cost and design complexity.

***Note:** It is recommended that the on-chip diode bridges be bypassed when input power requirements are >10 W or in thermally-constrained applications. For more information, see “AN956: Si3402-B POE PD Controller Design Guide”.

By integrating the diode bridges, the Si3402 gains access to the input side of the diode bridge. Monitoring the voltage at the input of the diode bridges instead of the voltage across the load capacitor provides the earliest indication of a power loss. This true early power loss indicator, $\overline{\text{PLOSS}}$, provides the PD’s processor a bit of time to save states and shut down gracefully before the load capacitor discharges below the minimum IEEE 802.3-specified operating voltage of 36 V. Integration of the surge suppressor enables optimization of the clamping voltage and guarantees protection of all connected circuitry.

As an added benefit, the transient surge suppressor, when tripped, actively disables the hotswap interface and switching regulator, preventing downstream circuits from encountering the high-energy transients.

3.2.2. Detection

In order to identify a device as a valid PD, a PSE will apply a voltage in the range of 2.8 to 10 V on the cable and look for a valid signature resistance. The Si3402 will react to voltages in this range by connecting the external 24.3 kΩ detection resistor between VPOS and VNEG. This external resistor and internal low-leakage control circuitry create the proper signature to alert the PSE that a valid PD has been detected and is ready to have power applied. The internal hotswap switch is disabled during this time to prevent the switching regulator and attached load circuitry from generating errors in the detection signature.

Since the Si3402 integrates the diode bridges, the IC can compensate for the voltage and resistance effects of the diode bridges. The IEEE 802.3 specification requires that the PSE use a multi-point, $\Delta V/\Delta I$ measurement technique to remove the diode-induced dc offset from the signature resistance measurement. However, the specification does not address the diode's nonlinear resistance and the error induced in the signature resistor measurement. Since the diode's resistance appears in series with the signature resistor, the PD system must find some way of compensating for this error. In systems where the diode bridges are external, compensation is difficult and suffers from errors. Since the diode bridges are integrated in the Si3402, the IC can compensate for this error by offsetting resistance across all operating conditions and thus meeting the IEEE 802.3 requirements.

3.2.3. Classification

Once the PSE has detected a valid PD, the PSE may classify the PD for one of five power levels or classes. A class is based on the expected power consumption of the powered device. An external resistor sets the nominal class current that can then be read by the PSE to determine the proper power requirements of the PD.

When the PSE presents a fixed voltage between 15.5 V and 20.5 V to the PD, the Si3402 asserts the class current from VPOS through the RCL resistor. The resistor values associated with each class are shown in Table 7.

Table 7. Class Resistor Values

Class	Usage	Peak Power Levels	Nominal Class Current	RCL Resistor (1%, 1/16 W)
0	Default	0.44 to 12.95 W	< 4 mA	> 681 Ω (or open circuit)
1	Optional	0.44 to 3.84 W	10.5 mA	140 Ω
2	Optional	3.84 to 6.49 W	18.5 mA	75.0 Ω
3	Optional	6.49 to 12.95 W	28 mA	48.7 Ω

3.2.4. Under Voltage Lockout

The Si3402 incorporates an undervoltage lockout (UVLO) circuit to monitor the line voltage and determine when to apply power to the integrated switching regulator. Before power is applied to the switching regulator, the hotswap switch output (HSO) pin is high-impedance and typically follows VPOS as the input is ramped (due to the discharged switcher supply capacitor). When the input voltage rises above the UVLO turn-off voltage (typicall 37 V), several things happen:

1. The Si3402 begins to turn on the internal hotswap power MOSFET (HSSW).
2. The switcher supply capacitor begins to charge up under the current limit control of the Si3402.
3. The HSO pin transitions from VPOS to VNEG.

The Si3402 includes hysteretic UVLO circuits to maintain power to the load until the input voltage falls below the UVLO turn-on voltage (typically 32 V). Once the input voltage falls below that threshold, the HSSW is turned off (note that the switching regulator also turns off). Figure 4 provides a visual depiction of the UVLO feature.

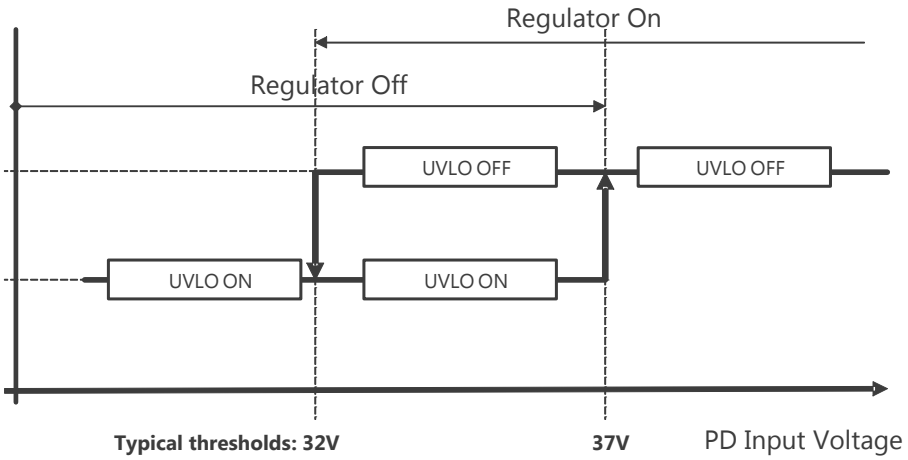


Figure 4. UVLO Behavior and Threshold Voltages

3.2.5. Dual Input Current Limit and Switcher Turn-On

The Si3402 implements dual input current limits. While the HSSW is charging the switcher supply capacitor, the Si3402 maintains a low current limit. The switching regulator is disabled until the voltage across the HSSW becomes sufficiently low, indicating the switcher supply capacitor is almost completely charged. When this threshold is reached, the switcher is activated, and the hotswap current limit is increased.

The Si3402 stays in the high-level input current limit mode until the input voltage drops below the UVLO turn-on threshold or excessive power is dissipated in the hotswap switch.

An additional feature of the current limit circuitry is current limiting in the event of a fault condition. When the current limit is switched to the higher level, 470 mA of current can be drawn by the PD. Should a fault cause more than this current to be consumed, the HSSW goes into a temporary 10 mA current limit mode and turns off the switcher. After 90 ms have elapsed, and if the switcher supply capacitor is recharged, the HSSW turns back on in the 470 mA limit mode, and enables the switcher.

3.2.6. Power Loss Indicator

A situation can occur in which power is lost at the input of the diode bridge and the hotswap controller does not detect the fault due to the VPOS to VNEG capacitor maintaining the voltage. In such a situation, the PD can remain operational for hundreds of microseconds despite the PSE having removed the line voltage. If it is recognized early enough, the time from power loss to power failure can provide valuable time to gracefully shut down an application.

Due to integration of the diode bridges, the Si3402 is able to instantaneously detect the removal of the line voltage and provide that early warning signal to the PD application. The $\overline{\text{PLOSS}}$ pin is an open drain output that pulls up to VPOS when the voltage difference between VPOSS and CTx or SPx is smaller than 1.5 V. When VPOSS-CTx or VPOSS-SPx voltage become >1.5 V, the output becomes high-impedance, allowing an external pull-down resistor to change the logic state of $\overline{\text{PLOSS}}$. The benefit of this indicator is that the powered device may include a microcontroller that can quickly save its memory or operational state before draining the supply capacitors and powering itself down. This feature can help improve overall manageability in applications, such as wireless access points.

3.3. Isolated and Non-Isolated Application Topologies

Power over Ethernet (PoE) applications fall into two broad categories, isolated and non-isolated. Non-isolated systems can be used when the powered device is self-contained and does not provide external conductors to the user or another application. Non-isolated applications include wireless access points and security cameras. In these applications, there is no explicit need for dc isolation between the switching regulator output and the hotswap interface. An isolated system must be used when the powered device interfaces with other self-powered equipment or has external conductors accessible to the user or other applications. For proper operation, the regulated output supply of the switching regulator must not have a dc electrical path to the hotswap interface or switching regulator primary side. Isolated applications include point-of-sale terminals where the user can touch the grounded metal chassis.

The application determines the converter topology. An isolated application will require a flyback transformer-based switching topology while a non-isolated application can use an inductor-based buck converter topology. In the isolated case, dc isolation is achieved through a transformer in the forward path and a voltage reference plus opto-isolator in the feedback path. The application circuit shown in Figure 2 is an example of such a topology. The non-isolated application in Figure 1 makes use of a single inductor as the energy conversion element, and the feedback signal is directly supplied into the internal error amplifier. As can be seen from the application circuits, the isolated topology has an increased number of components, thus increasing the bill of materials (BOM) and system footprint. To optimize cost and ease implementation, each application should be evaluated for its isolated or non-isolated requirements.

3.4. Switching Regulator

Figure 5 gives a representation of the Switching Regulator.

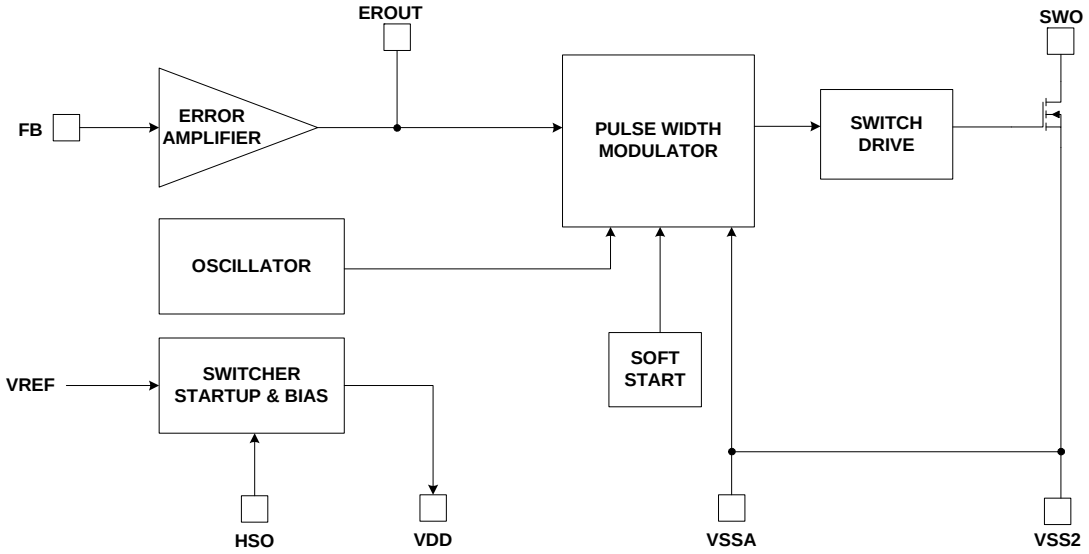


Figure 5. Switching Regulator Block Diagram

3.4.1. Switcher Startup

The switching regulator is disabled until the hotswap interface has both identified itself to the PSE and charged the supply capacitor needed to filter the switching regulator's high-current transients. Once the supply capacitor is charged, the hotswap controller engages the internal bias currents and supplies used by the switcher. Additionally, the soft-start current begins to charge the internal soft-start capacitor.

Ramping this voltage slowly allows the switching regulator to bring up the regulated output voltage in a controlled manner. Controlling the initial startup of the regulated voltage restrains power dissipation in the switching FET and prevents overshoot and ringing in the output supply voltage and PD input current.

3.4.2. Switching Regulator Operation

The switching regulator of the Si3402 is a constant-frequency, pulse-width-modulated controller (PWM) integrated with switching power FETs. The design is optimized for the output power range defined by the IEEE 802.3 specification.

Once the hotswap interface has ensured proper turn-on of the switching regulator controller, the switcher is fully operational. An internal free-running oscillator and internal precision voltage reference are fed into the pulse-width modulator. The output of the error amplifier (either internal for non-isolated applications or external for isolated applications) is also routed into the PWM controller.

The PWM controls the switching FET drive circuitry. A significant advantage of integrating the switching power FET onto the same monolithic IC as the switching regulator controller is the ability to precisely adjust the drive strength and timing, resulting in high regulator efficiency. Furthermore, current-limiting circuitry protects the switching FET. Thermal overload protection provides a secondary level of protection.

The flexibility of the Si3402's switching regulator allows the system designer to realize either the isolated or non-isolated application circuitry using a single device. In operation, the integration of the switching FET allows tighter control and more efficient operation than a general-purpose switching regulator coupled with a general-purpose external FET.

3.4.3. Flyback Snubber

Large voltage transients can be generated by the inductive kick associated with the leakage inductance of the primary side of the flyback transformer used in isolated applications. A snubber is necessary to limit these voltage transients. Refer to “AN956: Si3402-B PoE PD Design Guide” for more information on the snubber.

3.5. Output Voltage and Thermal Considerations

The Si3402-B supports a wide range of output voltages for IEEE 802.3-compliant Class 0-3 designs. Because the Si3402-B integrates the switching FET and HSSW, the case temperature of the Si3402-B will depend heavily on the output power and the thermal relief provided in the PCB design. For a given output power, the integrated HSSW will dissipate more power when configured for lower output voltages because the current passing through it is higher.

The user should closely follow the hardware design guidelines provided in “AN956: Si3402-B PoE PD Controller Design Guide” to ensure a robust PoE PD solution, particularly for low output voltage Class 3 designs.

4. Pin Descriptions

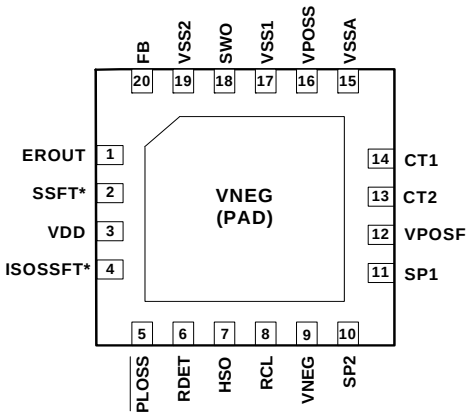


Table 8. Si3402 Pin Descriptions (Top View)

Pin#	Name	Description
1	EROUT	Error-amplifier output and PWM input; directly connected to opto-coupler in isolated application.
2	SSFT*	The non-isolated soft-start function is internal on the Si3402-B. Therefore, this pin is not internally connected.
3	VDD	5 V supply rail for switcher; provides drive for opto-coupler.
4	ISOSSFT*	The isolated soft-start function is internal on the Si3402-B. Therefore, this pin is not internally connected.
5	$\overline{\text{PLOSS}}$	Early power loss indicator; open drain output is pulled to VPOS when VPORT is applied.
6	RDET	Input pin for external precision detection resistor; also used for establishing absolute current reference.
7	HSO	Hotswap switch output; connects to VNEG through hotswap switch.
8	RCL	Input pin for external precision classification resistor; float if optional RCLASS is unused.
9, Pad	VNEG	Rectified high-voltage supply, negative rail. Must be connected to thermal PAD node (VNEG) on package bottom. This thermal pad must be connected to VNEG (pin #9) as well as a 2 in^2 heat spreader plane using a minimum of nine thermal vias.
10	SP2	High-voltage supply input from spare pair; polarity-insensitive.
11	SP1	High-voltage supply input from spare pair; polarity-insensitive.
12	VPOSF	Rectified high-voltage supply, positive rail (force node)
13	CT2	High-voltage supply input from center tap of Ethernet transformer; polarity-insensitive.
14	CT1	High-voltage supply input from center tap of Ethernet transformer; polarity-insensitive.
15	VSSA	Analog ground. In new designs, VSSA can be left floating for easier PCB layout, and VSS2 used as analog ground. VSSA is internally connected to VSS2.
16	VPOSS*	The positive rail sense node function is no longer implemented. Therefore, this pin is not internally connected.
17	VSS1*	This former negative supply rail pin is no longer implemented. Therefore, this pin is not internally connected.
18	SWO	Switching transistor output; drain of switching N-FET.
19	VSS2	Negative supply rail for switcher; externally tied to HSO.
20	FB	Regulated feedback input in non-isolated application.
Note:	* Si3402-A legacy pin only, shown for compatibility and comparison purposes. Legacy components and connections for this pin are harmless and can be either retained or deleted.	

5. Package Outline

Figure 6 illustrates the package details for the Si3402. Table 9 lists the values for the dimensions shown in the illustration.

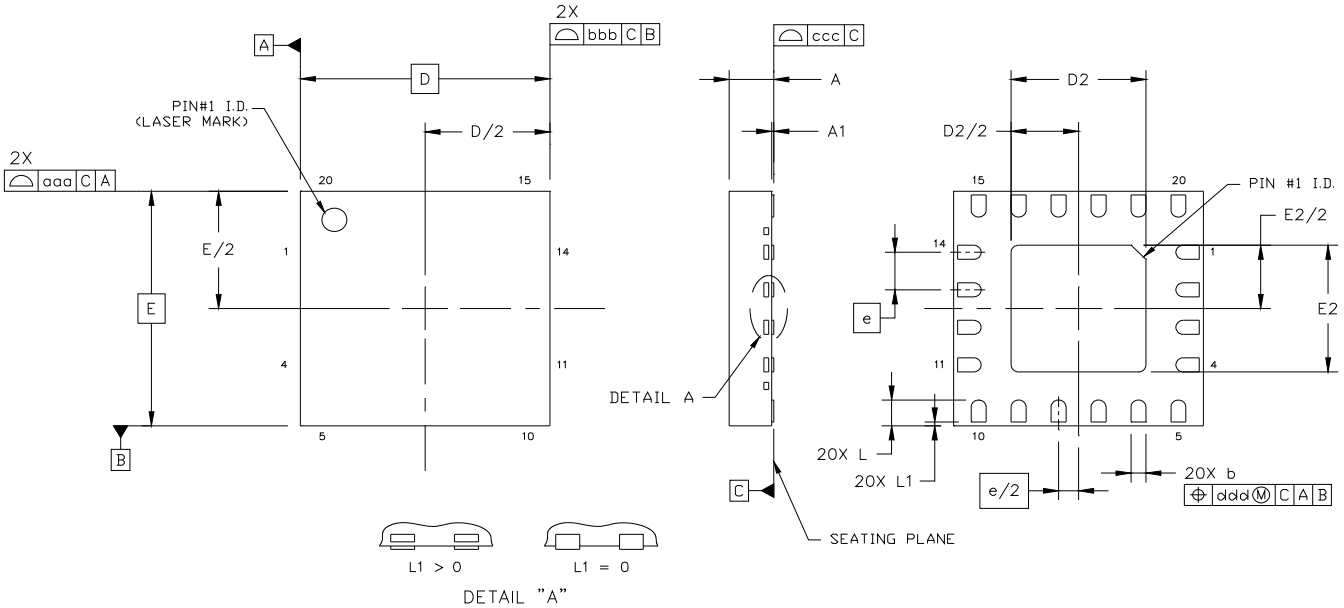


Figure 6. 20-Lead Quad Flat No-Lead Package (QFN)

Table 9. Package Dimensions

Dimension	Min	Nom	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
b	0.25	0.30	0.35
D		5.00 BSC.	
D2	2.60	2.70	2.80
e		0.80 BSC.	
E		5.00 BSC.	
E2	2.60	2.70	2.80
L	0.50	0.55	0.60
L1	0.00	—	0.10
aaa	—	—	0.10
bbb	—	—	0.10
ccc	—	—	0.08
ddd	—	—	0.10

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-220, Variation VHHB-1.

6. Recommended Land Pattern

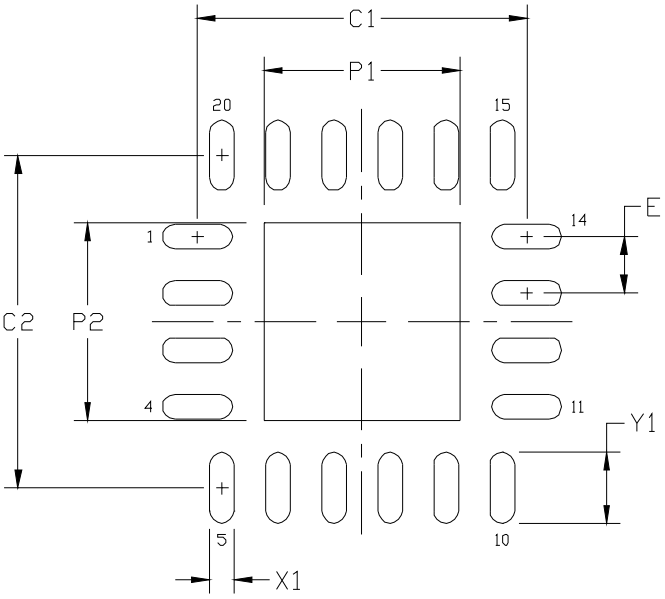


Figure 7. Si3402 Recommended Land Pattern

Table 10. PCB Land Pattern Dimensions

Symbol	Min	Nom	Max
P1	2.70	2.75	2.80
P2	2.70	2.75	2.80
X1	0.25	0.30	0.35
Y1	0.90	0.95	1.00
C1	4.70		
C2	4.70		
E	0.80		

Notes:

General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on the IPC-7351 guidelines.

Solder Mask Design

4. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Stencil Design

5. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
6. The stencil thickness should be 0.125 mm (5 mils).
7. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pins.
8. A 2x2 array of 1.2 mm square openings on 1.4 mm pitch should be used for the center ground pad.

Card Assembly

9. A No-Clean, Type-3 solder paste is recommended.
10. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

7. Ordering Guide

Part Number[1,2]	Package	Temp Range
Si3402-B-GM	20-pin QFN, Pb-free; RoHS compliant	–40 to 85 °C

Notes:
1. "X" denotes product revision.
2. Add an "R" at the end of the part number to denote tape and reel option.

8. Device Marking Diagram

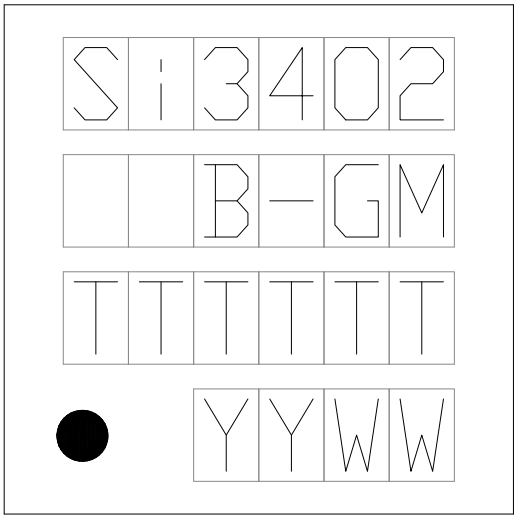


Figure 8. Device Marking Diagram

Table 11. Device Marking Table

Line #	Text Value	Description
1	Si3402	Base part number. This is not the “Ordering Part Number” since it does not contain a specific revision. Refer to "7. Ordering Guide" on page 19 for complete ordering information.
2	B-GM	B = Device Revision B G = Extended temperature range. M = QFN package.
3	TTTTTT	Trace code (assigned by the assembly subcontractor).
4	Circle = 20 mils Diameter (Bottom-Left Justified)	Pin 1 identifier.
	YY	Assembly year.
	WW	Assembly week.

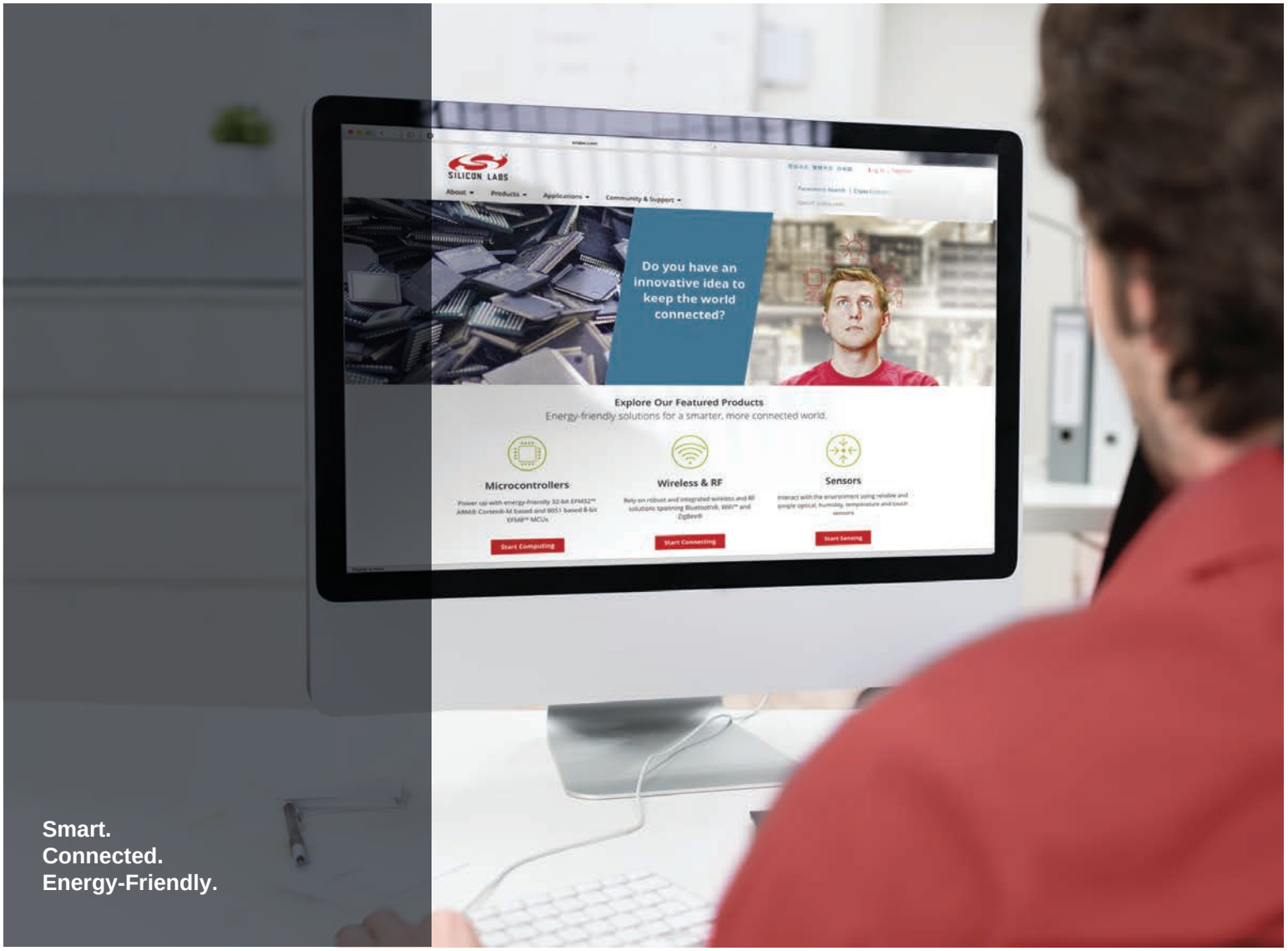
Document Change List

Revision 0.4 to Revision 1.0

- Updated Table 2 on page 4 to reflect improvements and clarifications for several parameters.
- Updated Table 3 on page 5 to reflect detailed Si3402-B behaviors, while retaining system-level compatibility with Si3402-A.
- Updated Table 7, “Component Listing—Class 0 with 5 V Output,” on page 8 and Table 8, “Components—Class 1 with Isolated 5.0 V Output,” on page 9 to reflect component values that must be changed at the board level to maintain Si3402–A compatibility when using Si3402-B.
- Updated Table 8, “Si3402 Pin Descriptions (Top View),” on page 16 and related diagrams to indicate 4 pins that are not internally connected on Si3402-B (SSFT, ISOSSFT, VPOSS, VSS1) vs. Si3402-A.

Revision 1.0 to Revision 1.1

- Deleted Surge Immunity Ratings table. This data is now contained in the Qualification Summary and “AN956: Si3402-B POE PD Controller Design Guide”.
- Updated "2. Typical Application Schematics*" on page 7.
- Added new section, "3.5. Output Voltage and Thermal Considerations" on page 15.
- Deleted references to Class 4 operation.
- Updated Figure 3, “Input Lineside and Hotswap Block Diagram,” on page 9
- Added Figure 4, “UVLO Behavior and Threshold Voltages,” on page 11.
- Updated Figure 5, “Switching Regulator Block Diagram,” on page 14 (formerly Figure 4).



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