

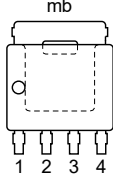
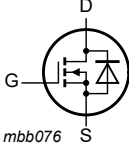
N-channel 40 V, 1.4 mΩ, 240 A logic level MOSFET in LPAK56 using NextPower-S3 technology

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Q_{GD}	gate-drain charge	$I_D = 25\text{ A}$; $V_{DS} = 20\text{ V}$; $V_{GS} = 4.5\text{ V}$; Fig. 12 ; Fig. 13	-	13	26	nC
$Q_{G(tot)}$	total gate charge		-	45	65	nC

- [1] 240A continuous current has been successfully demonstrated during application test. Practically, the current will be limited by PCB, thermal design and operating temperature.

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 <p>LPAK56; Power-SO8 (SOT669)</p>	 <p>mbb076</p>
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN1R4-40YLD	LPAK56; Power-SO8	Plastic single-ended surface-mounted package (LPAK56; Power-SO8); 4 leads	SOT669

7. Marking

Table 4. Marking codes

Type number	Marking code
PSMN1R4-40YLD	1D440L

8. Limiting values

Table 5. Limiting values

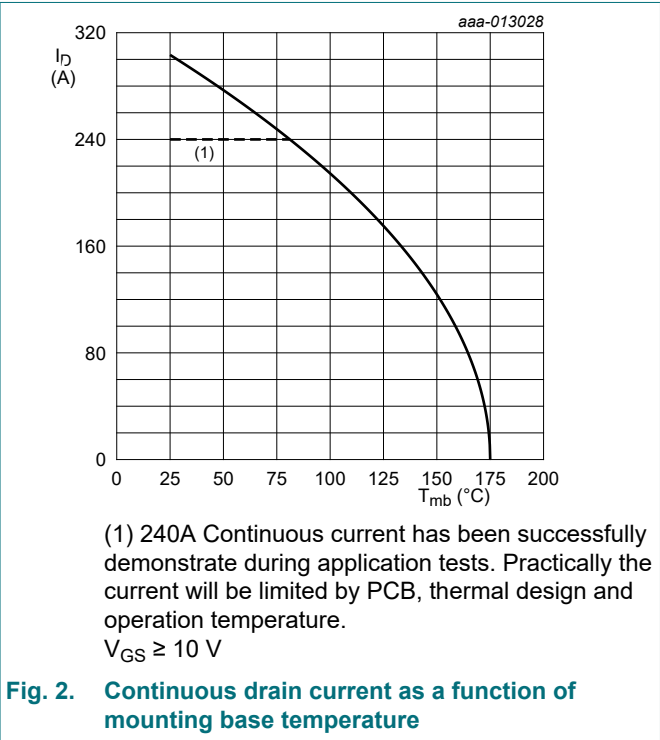
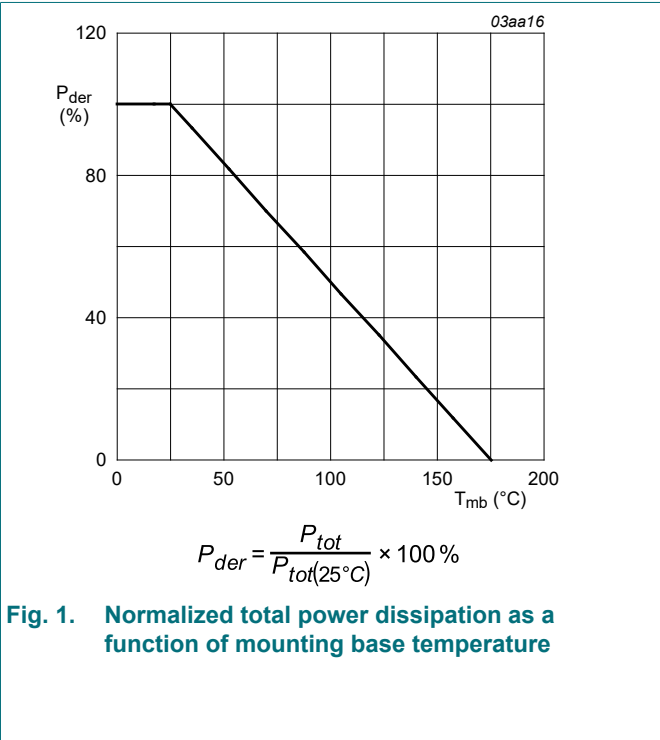
In accordance with the Absolute Maximum Rating System (IEC 60134).

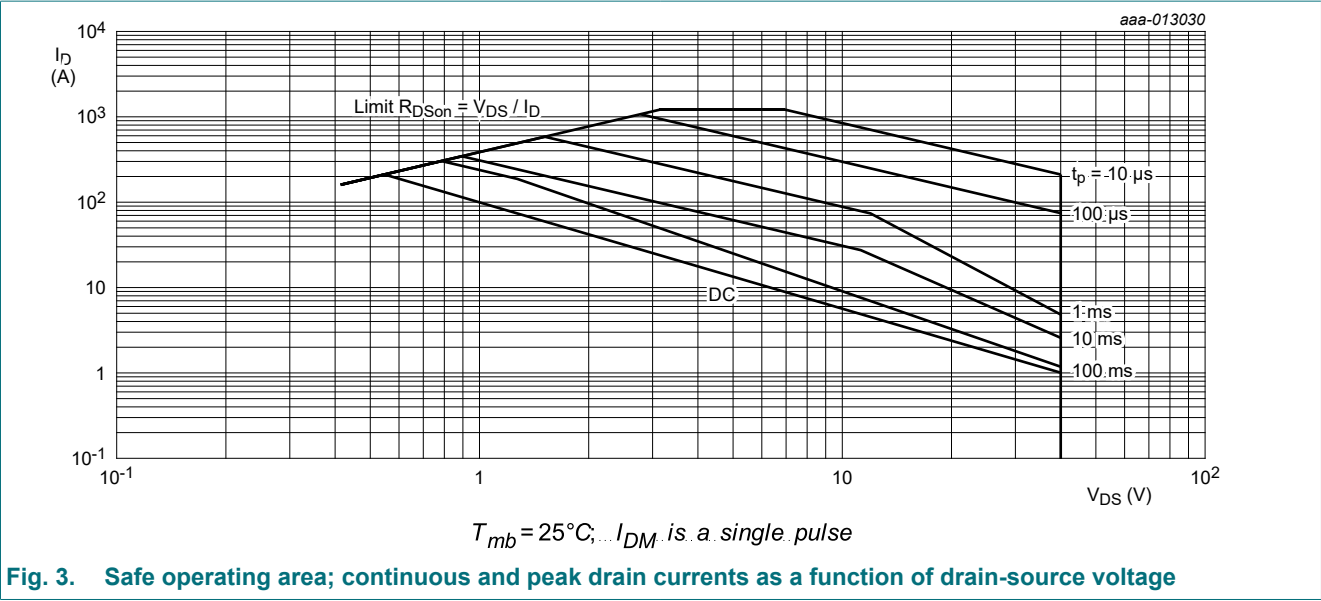
Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	40	V
V_{DSM}	peak drain-source voltage	$t_p \leq 20\text{ ns}$; $f \leq 500\text{ kHz}$; $E_{DS(AL)} \leq 200\text{ nJ}$; pulsed	-	45	V
V_{DGR}	drain-gate voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$; $R_{GS} = 20\text{ k}\Omega$	-	40	V
V_{GS}	gate-source voltage		-20	20	V
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 1	-	238	W
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$; Fig. 2	[1]	240	A
		$V_{GS} = 10\text{ V}$; $T_{mb} = 100\text{ °C}$; Fig. 2	-	214	A
I_{DM}	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ °C}$; Fig. 3	-	1201	A
T_{stg}	storage temperature		-55	175	°C

N-channel 40 V, 1.4 mΩ, 240 A logic level MOSFET in LPAK56 using NextPower-S3 technology

Symbol	Parameter	Conditions		Min	Max	Unit
T _j	junction temperature			-55	175	°C
T _{sld(M)}	peak soldering temperature			-	260	°C
V _{ESD}	electrostatic discharge voltage	HBM		2	-	kV
Source-drain diode						
I _S	source current	T _{mb} = 25 °C		-	198.6	A
I _{SM}	peak source current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C		-	1201	A
Avalanche ruggedness						
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	I _D = 74 A; V _{sup} ≤ 40 V; R _{GS} = 50 Ω; V _{GS} = 10 V; T _{j(init)} = 25 °C; unclamped; t _p = 0.23 ms	[2]	-	446	mJ
		I _D = 25 A; V _{sup} ≤ 40 V; R _{GS} = 50 Ω; V _{GS} = 10 V; T _{j(init)} = 25 °C; unclamped; t _p = 2.52 ms	[2]	-	1641	mJ
I _{AS}	non-repetitive avalanche current	V _{sup} ≤ 40 V; V _{GS} = 10 V; T _{j(init)} = 25 °C; R _{GS} = 50 Ω	[2]	-	190	A

- [1] 240A continuous current has been successfully demonstrated during application test. Practically, the current will be limited by PCB, thermal design and operating temperature.
- [2] Protected by 100% test

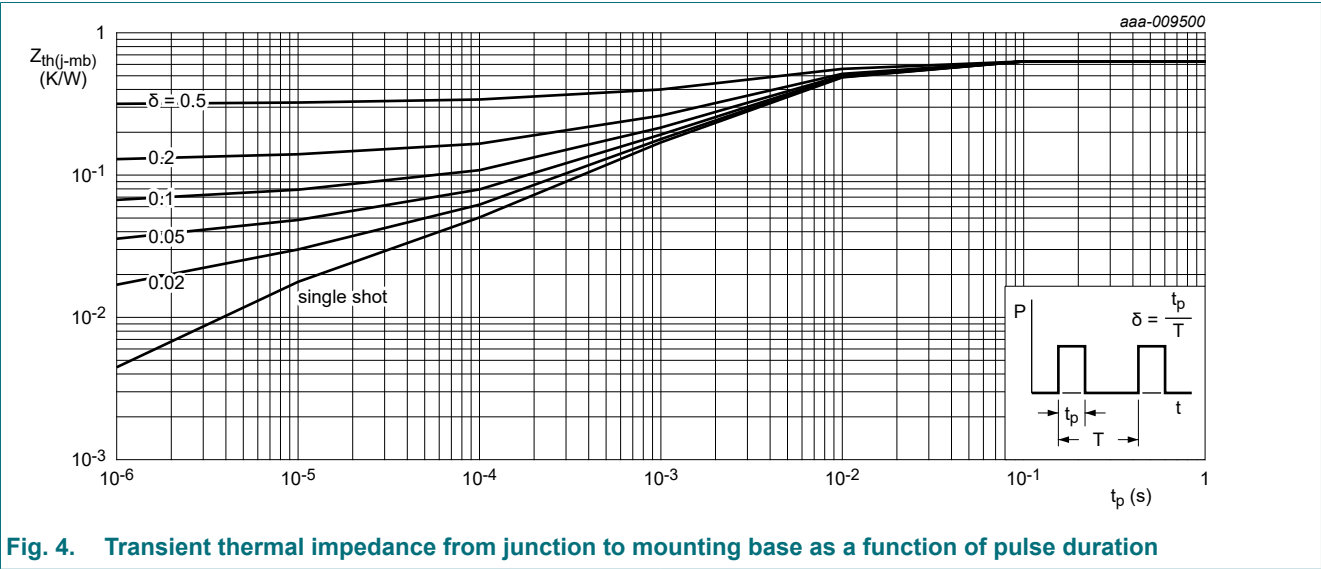




9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 4	-	0.56	0.63	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	Fig. 5	-	50	-	K/W
		Fig. 6	-	125	-	K/W



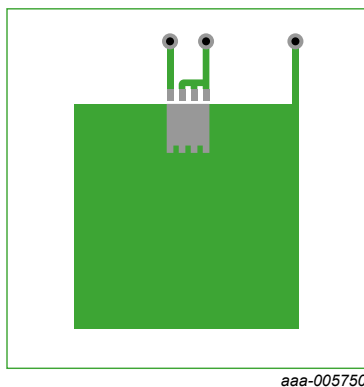


Fig. 5. PCB layout for thermal resistance junction to ambient 1" square pad; FR4 Board; 2oz copper

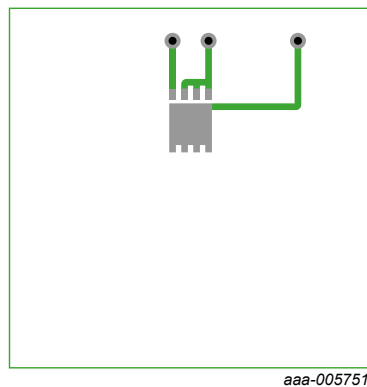


Fig. 6. PCB layout for thermal resistance junction to ambient minimum footprint; FR4 board; 2oz copper

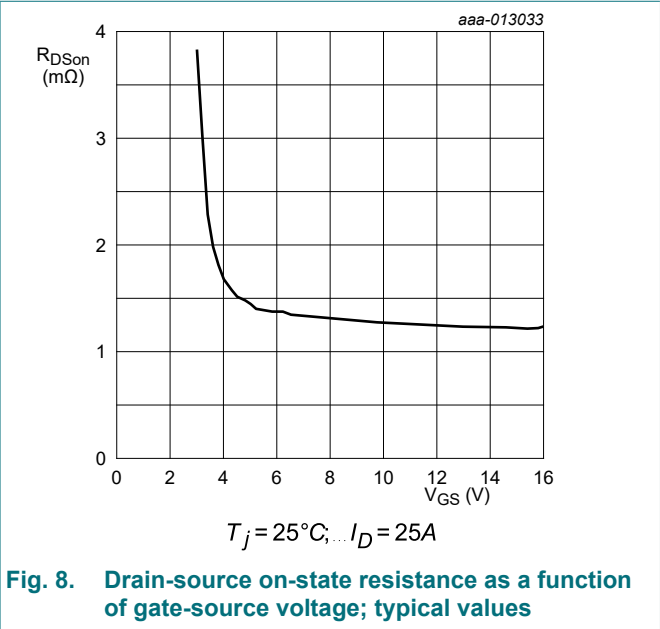
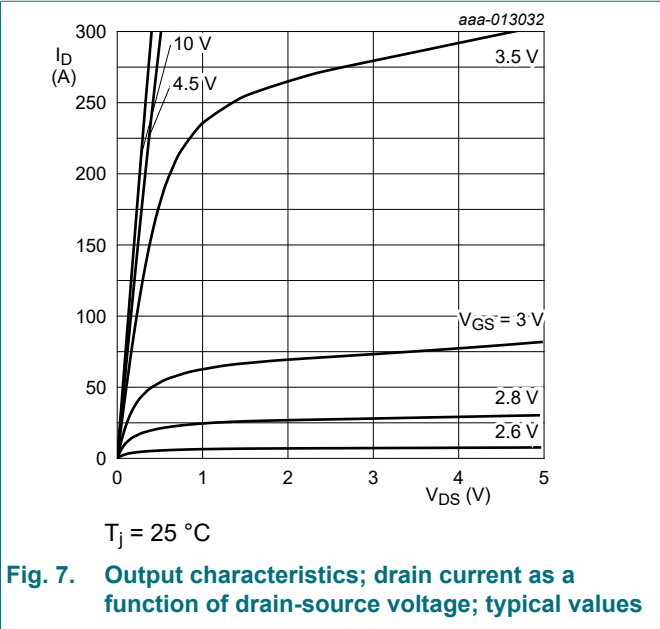
10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_J = 25 ^\circ C$	40	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_J = -55 ^\circ C$	36	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 mA; V_{DS} = V_{GS}; T_J = 25 ^\circ C$	1.05	1.7	2.2	V
$\Delta V_{GS(th)}/\Delta T$	gate-source threshold voltage variation with temperature	$25 ^\circ C \leq T_J \leq 150 ^\circ C$	-	-4.8	-	mV/K
I_{DSS}	drain leakage current	$V_{DS} = 32 V; V_{GS} = 0 V; T_J = 25 ^\circ C$	-	-	1	μA
		$V_{DS} = 32 V; V_{GS} = 0 V; T_J = 125 ^\circ C$	-	12	-	μA
I_{GSS}	gate leakage current	$V_{GS} = 16 V; V_{DS} = 0 V; T_J = 25 ^\circ C$	-	-	100	nA
		$V_{GS} = -16 V; V_{DS} = 0 V; T_J = 25 ^\circ C$	-	-	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10 V; I_D = 25 A; T_J = 25 ^\circ C;$ Fig. 10	-	1.12	1.4	mΩ
		$V_{GS} = 10 V; I_D = 25 A; T_J = 175 ^\circ C;$ Fig. 10; Fig. 11	-	-	2.65	mΩ
		$V_{GS} = 4.5 V; I_D = 25 A; T_J = 25 ^\circ C;$ Fig. 10	-	1.38	1.85	mΩ
		$V_{GS} = 4.5 V; I_D = 25 A; T_J = 175 ^\circ C;$ Fig. 10; Fig. 11	-	-	3.4	mΩ
R_G	gate resistance	$f = 1 MHz$	-	1.1	3.43	Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$I_D = 25 A; V_{DS} = 20 V; V_{GS} = 10 V;$ Fig. 12; Fig. 13	-	96	143	nC
		$I_D = 25 A; V_{DS} = 20 V; V_{GS} = 4.5 V;$ Fig. 12; Fig. 13	-	45	65	nC
		$I_D = 0 A; V_{DS} = 0 V; V_{GS} = 10 V$	-	85	-	nC
Q_{GS}	gate-source charge	$I_D = 25 A; V_{DS} = 20 V; V_{GS} = 4.5 V;$ Fig. 12; Fig. 13	-	15	25	nC
$Q_{GS(th)}$	pre-threshold gate-source charge		-	9	-	nC

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$Q_{GS(th-pl)}$	post-threshold gate-source charge			-	6	-	nC
Q_{GD}	gate-drain charge			-	13	26	nC
$V_{GS(pl)}$	gate-source plateau voltage	$I_D = 25\text{ A}$; $V_{DS} = 20\text{ V}$; Fig. 12; Fig. 13		-	2.7	-	V
C_{iss}	input capacitance	$V_{DS} = 20\text{ V}$; $V_{GS} = 0\text{ V}$; $f = 1\text{ MHz}$;		-	6661	10413	pF
C_{oss}	output capacitance	$T_j = 25\text{ }^{\circ}\text{C}$; Fig. 14		-	1543	2309	pF
C_{rss}	reverse transfer capacitance			-	299	658	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 20\text{ V}$; $R_L = 0.8\text{ }\Omega$; $V_{GS} = 4.5\text{ V}$; $R_{G(ext)} = 5\text{ }\Omega$		-	39	-	ns
t_r	rise time			-	49	-	ns
$t_{d(off)}$	turn-off delay time			-	47	-	ns
t_f	fall time			-	30	-	ns
Q_{oss}	output charge	$V_{GS} = 0\text{ V}$; $V_{DS} = 20\text{ V}$; $f = 1\text{ MHz}$; $T_j = 25\text{ }^{\circ}\text{C}$		-	50	-	nC
Source-drain diode							
V_{SD}	source-drain voltage	$I_S = 25\text{ A}$; $V_{GS} = 0\text{ V}$; $T_j = 25\text{ }^{\circ}\text{C}$; Fig. 15		-	0.78	1.2	V
t_{rr}	reverse recovery time	$I_S = 25\text{ A}$; $dI_S/dt = -100\text{ A}/\mu\text{s}$; $V_{GS} = 0\text{ V}$; $V_{DS} = 20\text{ V}$; Fig. 16		-	47	-	ns
Q_r	recovered charge		[1]	-	61	-	nC
t_a	reverse recovery rise time			-	25.4	-	ns
t_b	reverse recovery fall time			-	21.7	-	ns

[1] includes capacitive recovery



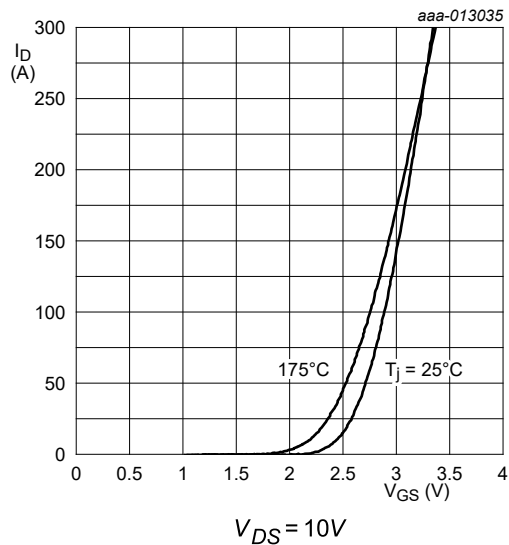


Fig. 9. Transfer characteristics; drain current as a function of gate-source voltage; typical values

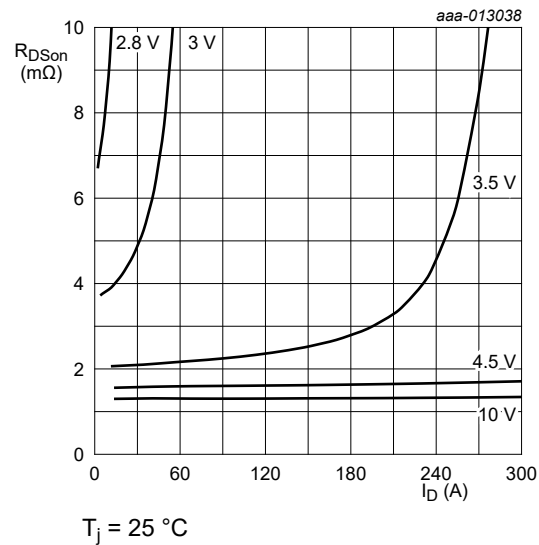
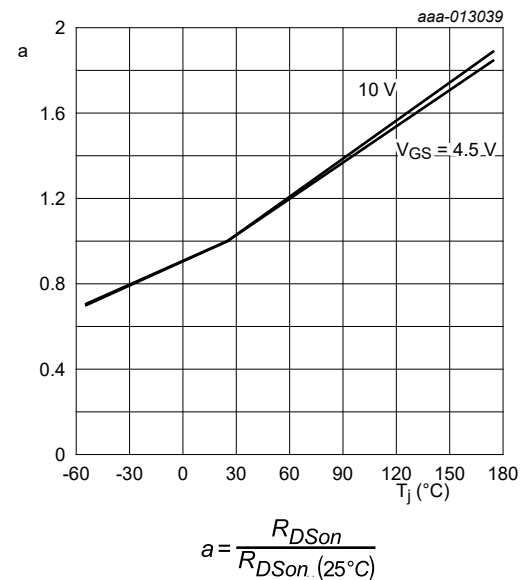


Fig. 10. Drain-source on-state resistance as a function of drain current; typical values



$$a = \frac{R_{DSon}}{R_{DSon}(25^\circ C)}$$

Fig. 11. Normalized drain-source on-state resistance factor as a function of junction temperature

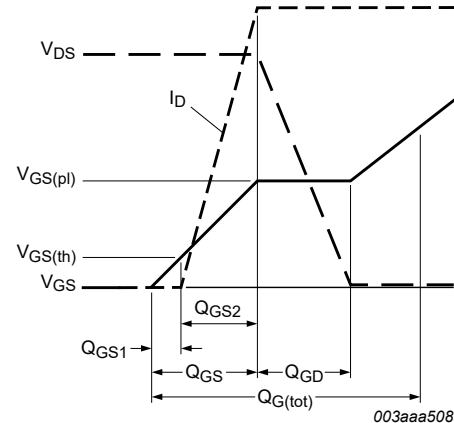


Fig. 12. Gate charge waveform definitions

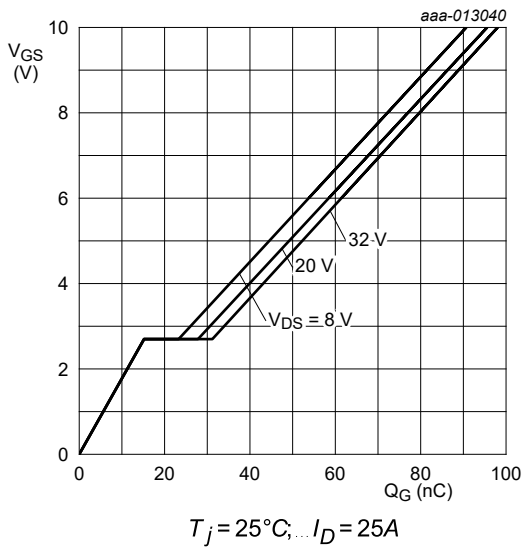


Fig. 13. Gate-source voltage as a function of gate charge; typical values

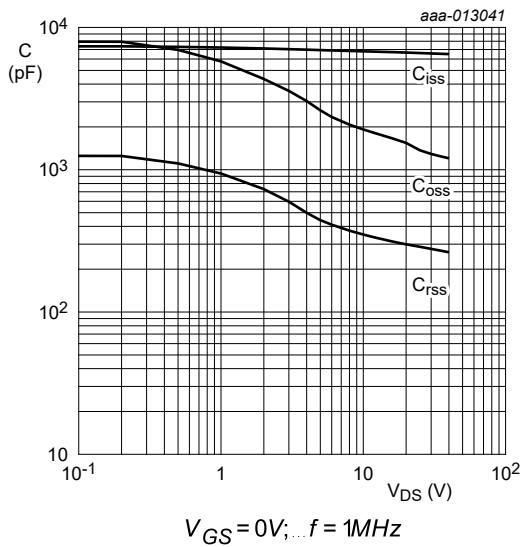


Fig. 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

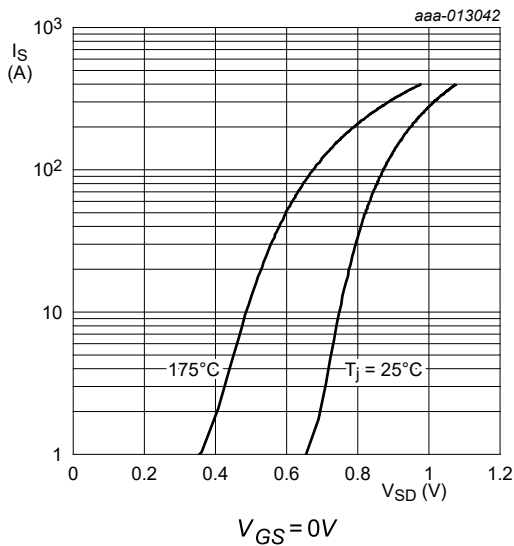


Fig. 15. Source current as a function of source-drain voltage; typical values

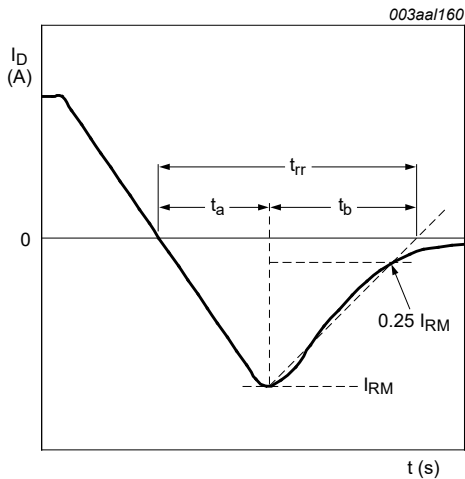


Fig. 16. Reverse recovery timing definition

11. Package outline

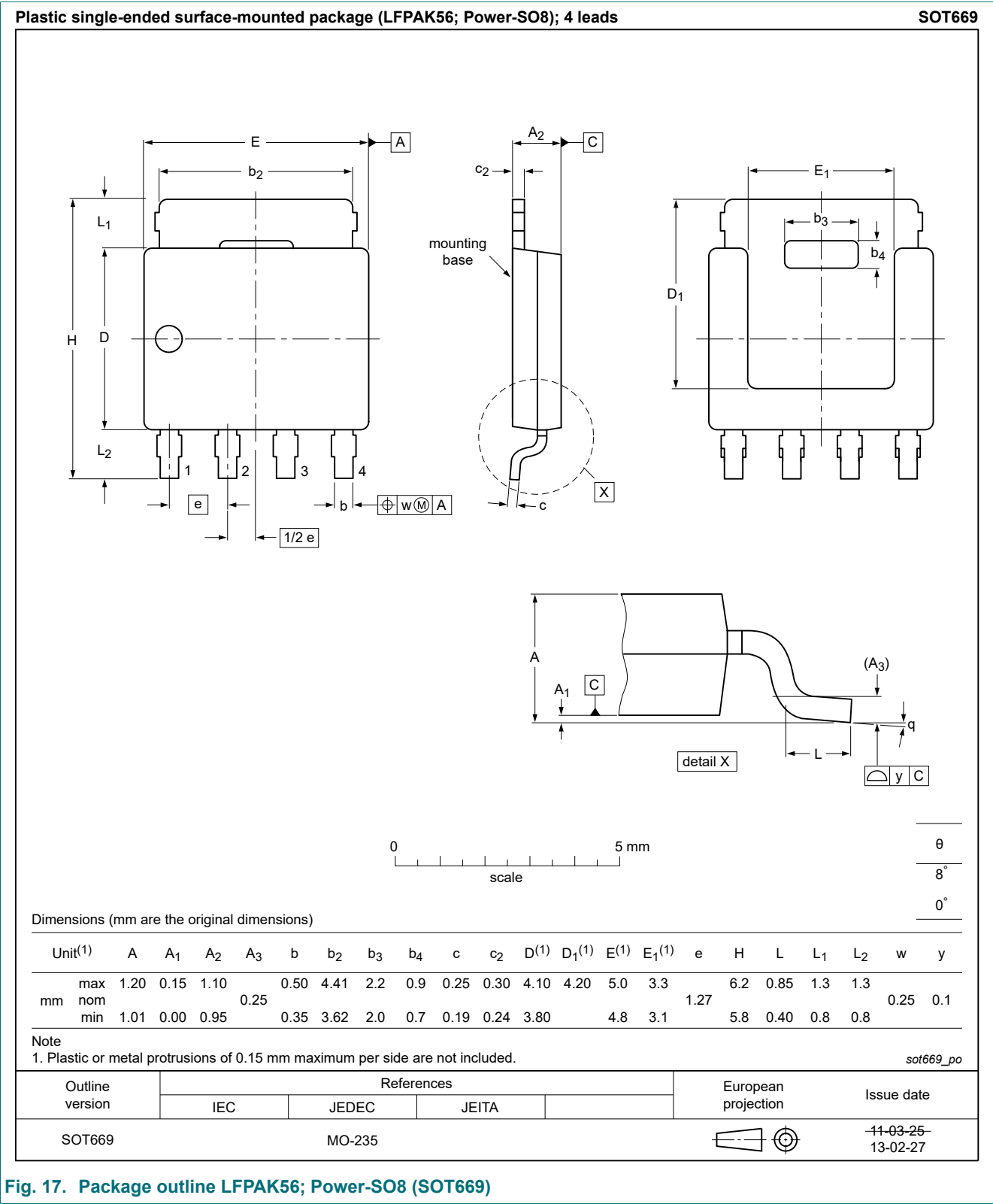


Fig. 17. Package outline LPAK56; Power-SO8 (SOT669)

12. Soldering

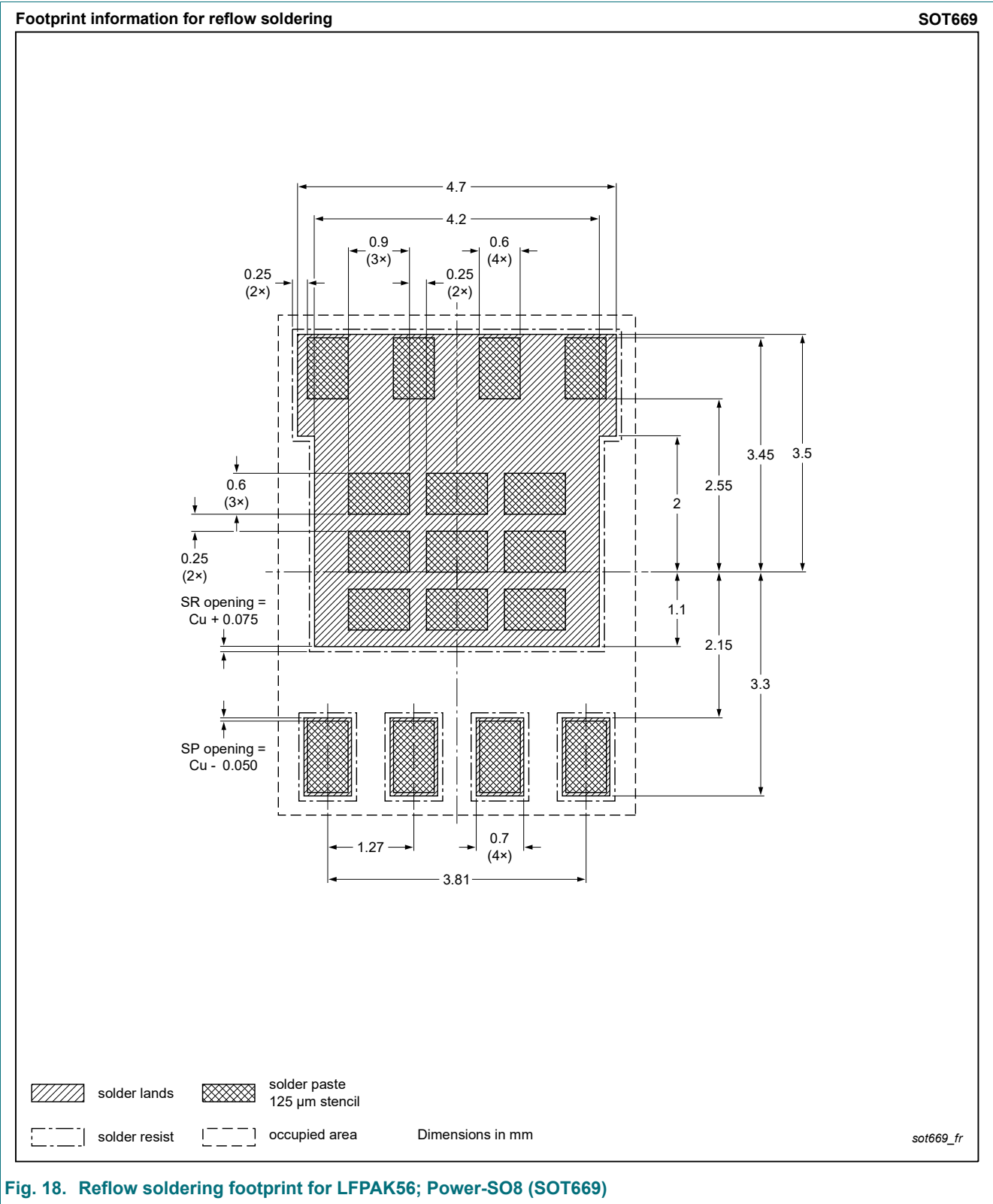


Fig. 18. Reflow soldering footprint for LPAK56; Power-SO8 (SOT669)

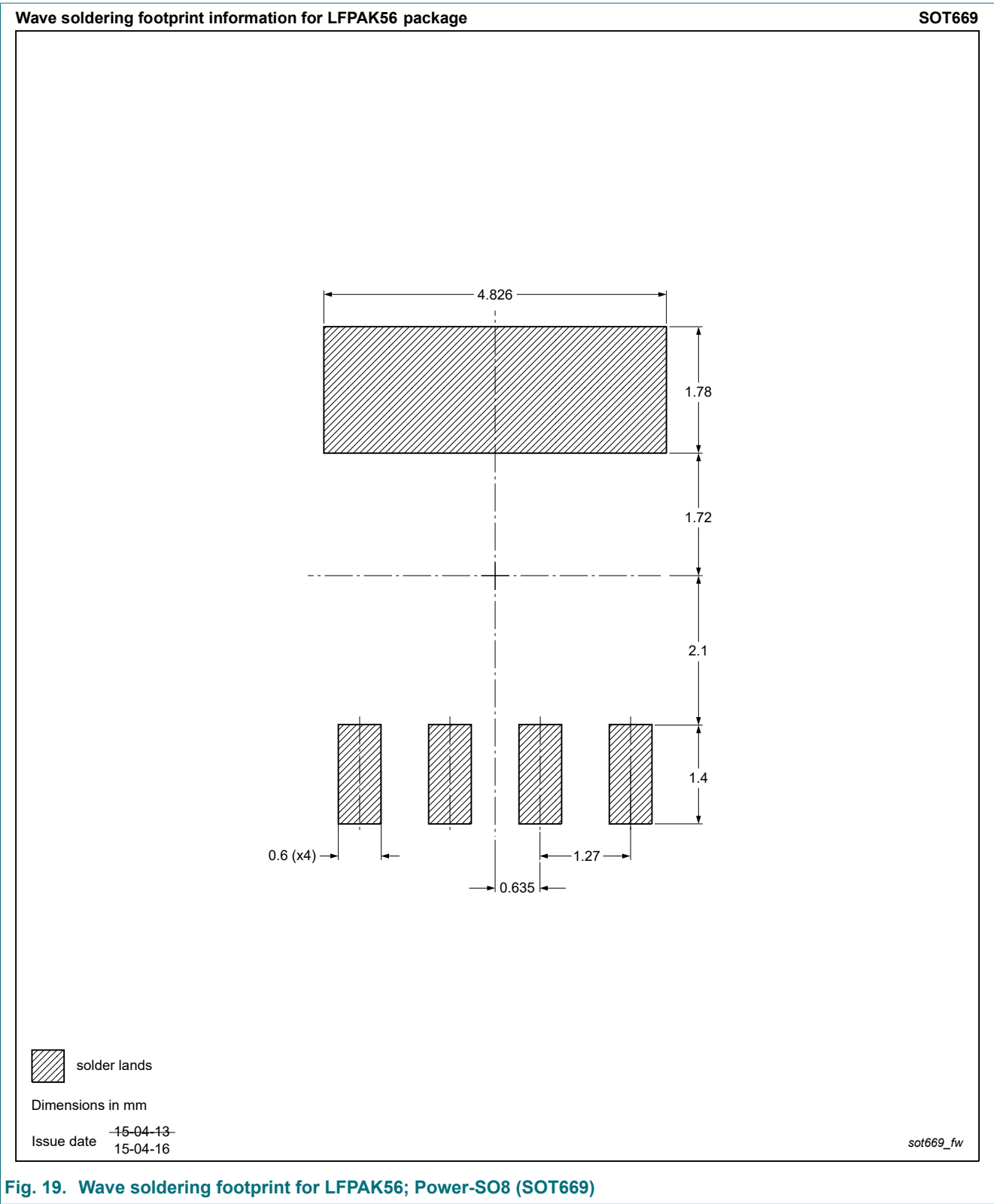


Fig. 19. Wave soldering footprint for LPAK56; Power-SO8 (SOT669)

13. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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