

Figure 1. 8-Lead Pinout (Top View) and Logic Diagram

## **Table 1. PIN DESCRIPTION**

Pin	Function
$\overline{D}$ , $\overline{\overline{D}}$	ECL Differential Inputs
Q	TTL Output
$V_{BB}$	Reference Voltage Output
V <sub>CC</sub>	Positive Supply
V <sub>EE</sub>	Negative Supply
GND	Ground
NC	No Connect
EP	(DFN8 only) Thermal exposed pad must be connected to a sufficient thermal conduit. Electrically connect to the most negative supply (GND) or leave unconnected, floating open.

**Table 2. ATTRIBUTES** 

Character	Va	lue				
Internal Input Pulldown Resistor	75 kΩ					
Internal Input Pullup Resistor		N	/A			
ESD Protection		kV 00 V				
Moisture Sensitivity, Indefinite Tim	ne Out of Drypack (Note 1)	Pb Pkg	Pb-Free Pkg			
	SOIC-8 TSSOP-8 DFN8	Level 1 Level 1 Level 1	Level 1 Level 3 Level 1			
Flammability Rating	UL 94 V-0	@ 0.125 in				
Transistor Count	38 De	evices				
Meets or exceeds JEDEC Spec E	Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test					

<sup>1.</sup> For additional information, see Application Note AND8003/D.

## **Table 3. MAXIMUM RATINGS**

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V <sub>CC</sub>	Positive Power Supply	GND = 0 V	V <sub>EE</sub> = −5.0 V	7	V
V <sub>EE</sub>	Negative Power Supply	GND = 0 V	V <sub>CC</sub> = +5.0 V	-8	V
V <sub>IN</sub>	Input Voltage	GND = 0 V		0 to V <sub>EE</sub>	V
I <sub>BB</sub>	V <sub>BB</sub> Sink/Source			± 0.5	mA
T <sub>A</sub>	Operating Temperature Range			-40 to +85	°C
T <sub>stg</sub>	Storage Temperature Range			-65 to +150	°C
$\theta_{JA}$	Thermal Resistance (Junction-to-Ambient)	0 lfpm 500 lfpm	SOIC-8 SOIC-8	190 130	°C/W °C/W
$\theta_{\sf JC}$	Thermal Resistance (Junction-to-Case)	Standard Board	SOIC-8	41 to 44	°C/W
$\theta_{JA}$	Thermal Resistance (Junction-to-Ambient)	0 lfpm 500 lfpm	TSSOP-8 TSSOP-8	185 140	°C/W °C/W
$\theta_{\sf JC}$	Thermal Resistance (Junction-to-Case)	Standard Board	TSSOP-8	41 to 44 ± 5%	°C/W
$\theta_{JA}$	Thermal Resistance (Junction-to-Ambient)	0 lfpm 500 lfpm	DFN8 DFN8	129 84	°C/W °C/W
T <sub>sol</sub>	Wave Solder Pb Pb-Free	<2 to 3 sec @ 248°C <2 to 3 sec @ 260°C		265 265	°C
$\theta_{\sf JC}$	Thermal Resistance (Junction-to-Case)	(Note 2)	DFN8	35 to 40	°C/W

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

<sup>2.</sup> JEDEC standard multilayer board - 2S2P (2 signal, 2 power)

Table 4. 10ELT SERIES NECL INPUT DC CHARACTERISTICS V<sub>CC</sub> = 5.0 V; V<sub>EE</sub> = -5.0 V; GND = 0 V (Note 3)

			-40°C			25°C			85°C		
Symbol	Characteristic	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Unit
V <sub>IH</sub>	Input HIGH Voltage (Single-Ended) (Note 4)	-1230		-890	-1130		-810	-1060		-720	mV
V <sub>IL</sub>	Input LOW Voltage (Single-Ended) (Note 4)	-1950		-1500	-1950		-1480	-1950		-1445	mV
V <sub>BB</sub>	Output Voltage Reference	-1.43		-1.30	-1.35		-1.25	-1.31		-1.19	V
V <sub>IHCMR</sub>	Input HIGH Voltage Common Mode Range (Differential) (Notes 4 and 5)	-2.8		0.0	-2.8		0.0	-2.8		0.0	V
I <sub>IH</sub>	Input HIGH Current			255			175			175	μΑ
I <sub>IL</sub>	Input LOW Current	0.5			0.5			0.3			μΑ

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

- 3. Input parameters vary 1:1 with GND.  $V_{EE}$  can vary +0.06 V to -0.5 V.
- 4. TTL output  $R_L = 500 \Omega$  to GND
- 5.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ ,  $V_{IHCMR}$  max varies 1:1 with GND.

Table 5. 100ELT SERIES NECL INPUT DC CHARACTERISTICS  $V_{CC} = 5.0 \text{ V}$ ;  $V_{EE} = -5.0 \text{ V}$ ;  $V_{EE} = -5.0$ 

			-40°C			25°C			85°C		
Symbol	Characteristic	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Unit
V <sub>IH</sub>	Input HIGH Voltage (Single-Ended) (Note 7)	-1165		-880	-1165		-880	-1165		-880	mV
V <sub>IL</sub>	Input LOW Voltage (Single-Ended) (Note 7)	-1810		-1475	-1810		-1475	-1810		-1475	mV
V <sub>BB</sub>	Output Voltage Reference	-1.38		-1.26	-1.38		-1.26	-1.38		-1.26	V
V <sub>IHCMR</sub>	Input HIGH Voltage Common Mode Range (Differential) (Notes 7 and 8)	-2.8		0.0	-2.8		0.0	-2.8		0.0	٧
I <sub>IH</sub>	Input HIGH Current			255			175			175	μΑ
I <sub>IL</sub>	Input LOW Current	0.5			0.5			0.5			μΑ

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

- 6. Input parameters vary 1:1 with GND.  $V_{EE}$  can vary +0.8 V to -0.5 V.
- 7. TTL output R<sub>L</sub> = 500  $\Omega$  to GND
- 8.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ ,  $V_{IHCMR}$  max varies 1:1 with GND.

Table 6. TTL OUTPUT DC CHARACTERISTICS  $V_{CC}$  = 4.5 V to 5.5 V;  $T_A$  = -40°C to +85°C

Symbol	Characteristic	Condition	Min	Тур	Max	Unit
V <sub>OH</sub>	Output HIGH Voltage	I <sub>OH</sub> = -3.0 mA	2.4			V
V <sub>OL</sub>	Output LOW Voltage	I <sub>OL</sub> = 24 mA			0.5	V
I <sub>CCH</sub>	Power Supply Current			11	16	mA
I <sub>CCL</sub>	Power Supply Current			13	18	mA
I <sub>EE</sub>	Negative Power Supply Current			15	21	mA
los	Output Short Circuit Current		-150		-60	mA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

Table 7. AC CHARACTERISTICS  $V_{CC}$ = 5.0 V;  $V_{EE}$ = -5.0 V; GND= 0 V (Note 9 and Note 10)

			-40°C			25°C			85°C		
Symbol	Characteristic	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Unit
f <sub>max</sub>	Maximum Toggle Frequency					100					MHz
t <sub>PLH</sub>	Propagation Delay @ 1.5 V	1.7		3.6	1.7		3.6	1.7		3.6	ns
t <sub>PHL</sub>	Propagation Delay @ 1.5 V	2.6		4.1	2.6		4.1	2.6		4.1	ns
t <sub>JITTER</sub>	Random Clock Jitter (RMS)					35					ps
t <sub>r</sub> t <sub>f</sub>	Output Rise/Fall Times QTTL 10% - 90%					1.9 2.3					ns
$V_{PP}$	Input Swing (Note 11)	200		1000	200		1000	200		1000	mV

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

9.  $V_{CC}$  can vary  $\pm$  0.25 V.

 $V_{EE}$  can vary +0.06 V to -0.5 V for 10ELT;  $V_{EE}$  can vary +0.8 V to -0.5 V for 100ELT. 10.  $R_L$  = 500  $\Omega$  to GND and  $C_L$  = 20 pF to GND. Refer to Figure 2.

11. V<sub>PP</sub>(min) is the minimum input swing for which AC parameters are guaranteed. The device has a DC gain of ≈ 40.

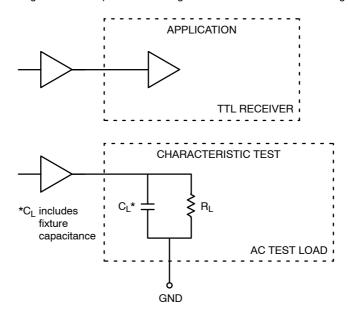


Figure 2. TTL Output Loading Used for Device Evaluation

### **ORDERING INFORMATION**

Device	Package	Shipping <sup>†</sup>
MC10ELT25D	SOIC-8	98 Units / Rail
MC10ELT25DG	SOIC-8 (Pb-Free)	98 Units / Rail
MC10ELT25DR2	SOIC-8	2500 / Tape & Reel
MC10ELT25DR2G	SOIC-8 (Pb-Free)	2500 / Tape & Reel
MC10ELT25DT	TSSOP-8	100 Units / Rail
MC10ELT25DTG	TSSOP-8 (Pb-Free)	100 Units / Rail
MC10ELT25DTR2	TSSOP-8	2500 / Tape & Reel
MC10ELT25DTR2G	TSSOP-8 (Pb-Free)	2500 / Tape & Reel
MC10ELT25MNR4	DFN8	1000 / Tape & Reel
MC10ELT25MNR4G	DFN8 (Pb-Free)	1000 / Tape & Reel
MC100ELT25D	SOIC-8	98 Units / Rail
MC100ELT25DG	SOIC-8 (Pb-Free)	98 Units / Rail
MC100ELT25DR2	SOIC-8	2500 / Tape & Reel
MC100ELT25DR2G	SOIC-8 (Pb-Free)	2500 / Tape & Reel
MC100ELT25DT	TSSOP-8	100 Units / Rail
MC100ELT25DTG	TSSOP-8 (Pb-Free)	100 Units / Rail
MC100ELT25DTR2	TSSOP-8	2500 / Tape & Reel
MC100ELT25DTR2G	TSSOP-8 (Pb-Free)	2500 / Tape & Reel
MC100ELT25MNR4	DFN8	1000 / Tape & Reel
MC100ELT25MNR4G	DFN8 (Pb-Free)	1000 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

## **Resource Reference of Application Notes**

AN1405/D - ECL Clock Distribution Techniques

AN1406/D - Designing with PECL (ECL at +5.0 V)

AN1503/D - ECLinPS™ I/O SPICE Modeling Kit

AN1504/D - Metastability and the ECLinPS Family

AN1568/D - Interfacing Between LVDS and ECL

AND8001/D - The ECL Translator Guide

AND8001/D - Odd Number Counters Design

AND8002/D - Marking and Date Codes

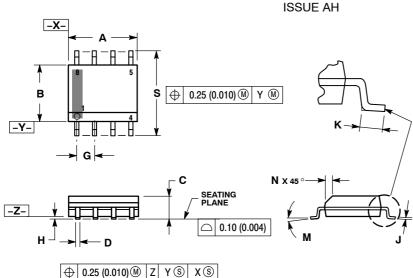
AND8020/D - Termination of ECL Logic Devices

AND8066/D - Interfacing with ECLinPS

AND8090/D - AC Characteristics of ECL Devices

#### PACKAGE DIMENSIONS

# SOIC-8 NB CASE 751-07

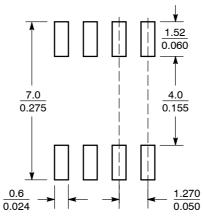


#### NOTES:

- 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982. 2. CONTROLLING DIMENSION: MILLIMETER. 3. DIMENSION A AND B DO NOT INCLUDE
- MOLD PROTRUSION.
  MAXIMUM MOLD PROTRUSION 0.15 (0.006)
- 4. MAXIMUM MOLD PROTRUSION 0.15 (0.006)
  PER SIDE.
  5. DIMENSION D DOES NOT INCLUDE DAMBAR
  PROTRUSION. ALLOWABLE DAMBAR
  PROTRUSION SHALL BE 0.127 (0.005) TOTAL
  IN EXCESS OF THE D DIMENSION AT
  MAXIMUM MATERIAL CONDITION.
  6. 751-01 THRU 751-06 ARE OBSOLETE. NEW
  STANDARD IS 751-07.

	MILLIN	IETERS	INC	HES	
DIM	MIN	MAX	MIN	MAX	
Α	4.80	5.00	0.189	0.197	
В	3.80	4.00	0.150	0.157	
C	1.35	1.75	0.053	0.069	
D	0.33	0.51	0.013	0.020	
G	1.27	7 BSC	0.050 BSC		
Н	0.10	0.25	0.004	0.010	
J	0.19	0.25	0.007	0.010	
K	0.40	1.27	0.016	0.050	
M	0 °	8 °	0 °	8 °	
N	0.25	0.50	0.010	0.020	
S	5.80	6.20	0.228	0.244	

## **SOLDERING FOOTPRINT\***

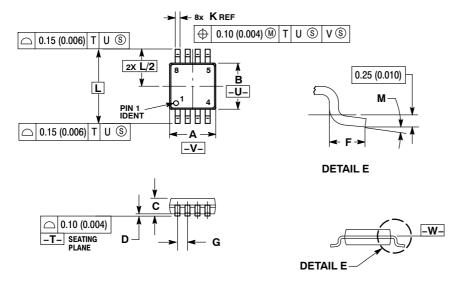


SCALE 6:1

<sup>\*</sup>For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## PACKAGE DIMENSIONS

## TSSOP-8 **DT SUFFIX** PLASTIC TSSOP PACKAGE CASE 948R-02 **ISSUE A**



#### NOTES:

- NOTES:

  1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

  2. CONTROLLING DIMENSION: MILLIMETER.

  3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS, MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
- (0.006) PER SIDE.

  4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.

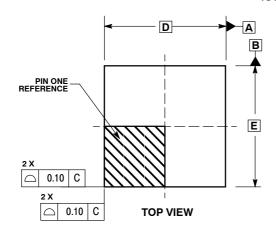
  5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.

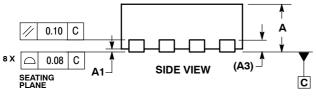
  6. DIMENSION A AND B ARE TO BE DETERMINED.
- 6. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

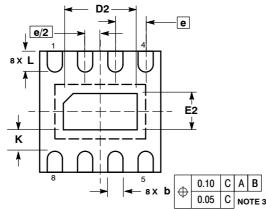
	MILLIN	IETERS	INC	HES
DIM	MIN	MAX	MIN	MAX
Α	2.90	3.10	0.114	0.122
В	2.90	3.10	0.114	0.122
С	0.80	1.10	0.031	0.043
D	0.05	0.15	0.002	0.006
F	0.40	0.70	0.016	0.028
G	0.65	BSC	0.026	BSC
K	0.25	0.40	0.010	0.016
L	4.90	BSC	0.193	BSC
M	0°	6 °	0°	6°

#### PACKAGE DIMENSIONS

## DFN8 CASE 506AA-01 ISSUE D







## NOTES:

- 1. DIMENSIONING AND TOLERANCING PER
- ASME Y14.5M, 1994 .
  CONTROLLING DIMENSION: MILLIMETERS.
- DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN
  0.25 AND 0.30 MM FROM TERMINAL.
  COPLANARITY APPLIES TO THE EXPOSED
  PAD AS WELL AS THE TERMINALS.

	MILLIMETERS					
DIM	MIN	MAX				
Α	0.80	1.00				
A1	0.00	0.05				
АЗ	0.20	REF				
b	0.20	0.30				
D	2.00	BSC				
D2	1.10	1.30				
Е	2.00	BSC				
E2	0.70	0.90				
е	0.50	BSC				
K	0.20					
L	0.25	0.35				

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