Push-Pull FET Driver with Integrated Oscillator and Clock Output

ABSOLUTE MAXIMUM RATINGS

V_{CC} to DGND, PGND .....-0.3V to +18V
CLK, RT to DGND.....-0.3V to +6V
NDRV1, NDRV2 to PGND.....-0.3V to (V_{CC} + 0.3V)
DGND to PGND.....-0.3V to +0.3V
CLK Current.....±20mA
NDRV1, NDRV2 Peak Current (200ns).....±5A
NDRV1, NDRV2 Reverse Current (Latchup Current).....±500mA

Continuous Power Dissipation (T_A = +70°C)
8-Pin µMAX (derate 10.3mW/°C above +70°C).....825mW
Operating Temperature Range .....-40°C to +125°C
Maximum Junction Temperature .....+150°C
Storage Temperature Range .....-60°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +12V, R_{RT} = 124kΩ, NDRV1 = NDRV2 = open, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are measured at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SUPPLY							
Input Voltage Supply Range	V_{CC}			4.5		15.0	V
Switching Supply Current	I_{CCSW}	f_{OSC} = 250kHz			1	3	mA
Undervoltage Lockout	V_{UVLO}	V_{CC} rising		3	3.5	4	V
UVLO Hysteresis					300		mV
OSCILLATOR							
Frequency Range	f_{OSC}	(Note 2)		50		1500	kHz
Accuracy		f_{OSC} = 250kHz , 6V ≤ V_{CC} ≤ 15V (Note 3)		-8		+10	%
Oscillator Jitter					±0.6		%
CLK Output High Voltage		I_{CLK} = 1mA	7V ≤ V_{CC} ≤ 15V	3.9		5.0	V
			4.5V ≤ V_{CC} ≤ 7V	3.35		5.0	
CLK Output Low Voltage		I_{CLK} = -1mA				50	mV
CLK Output Rise Time		C_{CLK} = 30pF			35		ns
CLK Output Fall Time		C_{CLK} = 30pF			10		ns
GATE DRIVERS (NDRV1, NDRV2)							
Output High Voltage	V_{OH}	I_{NDRV1} = I_{NDRV2} = 100mA		V_{CC} - 0.3			V
Output Low Voltage	V_{OL}	I_{NDRV1} = I_{NDRV2} = -100mA				0.3	V
Output Peak Current	I_P	Sourcing and sinking			3		A
Driver Output Impedance		NDRV_ sourcing 100mA			1.8	3	Ω
		NDRV_ sinking 100mA			1.6	2.6	
Latchup Current Protection		Reverse current at NDRV1/NDRV2			400		mA
Rise Time	t_R	C_{LOAD} = 2nF			10		ns
Fall Time	t_F	C_{LOAD} = 2nF			10		ns

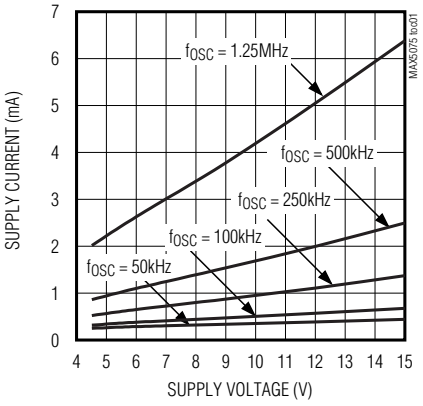
Note 1: The MAX5075 is 100% tested at T_A = T_J = +125°C. All limits over temperature are guaranteed by design.
Note 2: Use the following formula to calculate the MAX5075 oscillator frequency: $f_{OSC} = 10^{12}/(32 \times R_{RT})$.
Note 3: The accuracy of the oscillator's frequency is lower at frequencies greater than 1MHz.

Push-Pull FET Driver with Integrated Oscillator and Clock Output

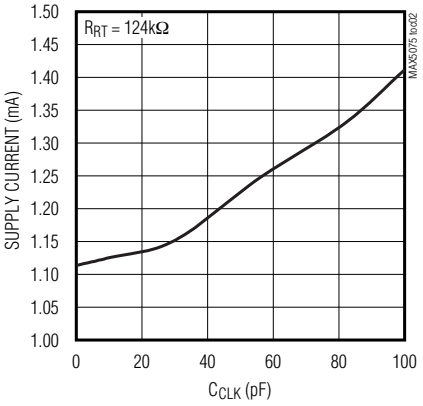
Typical Operating Characteristics

(V_{CC} = +12V, R_{RT} = 124kΩ, NDRV_ = open, CLK = open.)

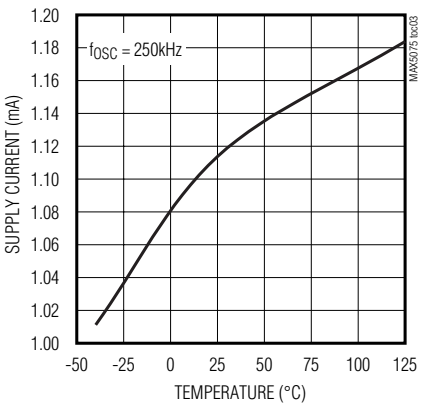
SUPPLY CURRENT vs. SUPPLY VOLTAGE



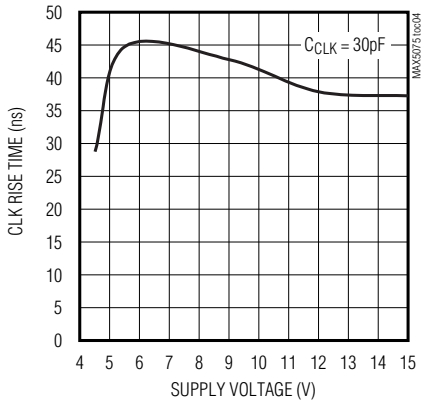
SUPPLY CURRENT vs. C_{CLK}



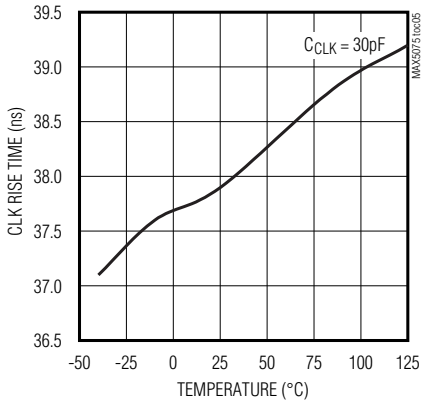
SUPPLY CURRENT vs. TEMPERATURE



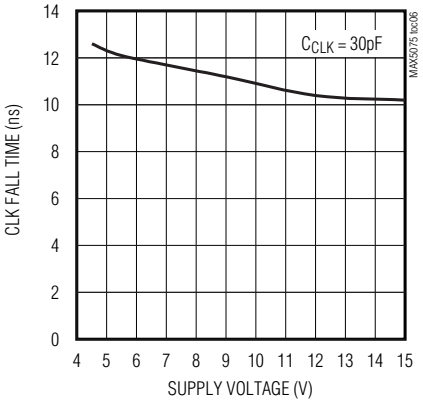
CLK RISE TIME vs. SUPPLY VOLTAGE



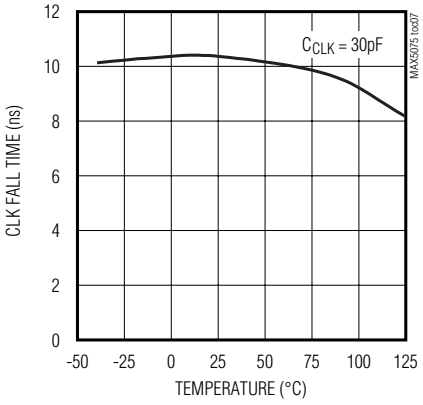
CLK RISE TIME vs. TEMPERATURE



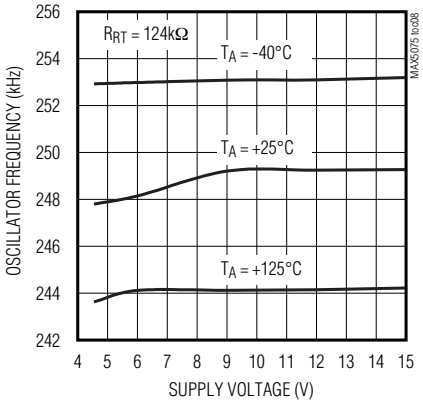
CLK FALL TIME vs. SUPPLY VOLTAGE



CLK FALL TIME vs. TEMPERATURE



OSCILLATOR FREQUENCY vs. SUPPLY VOLTAGE

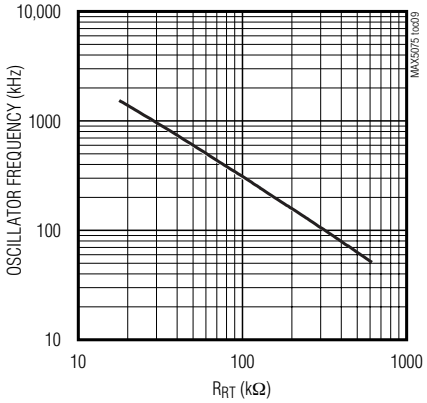


Push-Pull FET Driver with Integrated Oscillator and Clock Output

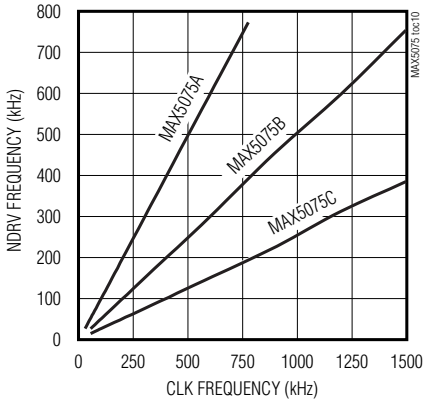
Typical Operating Characteristics (continued)

(V_{CC} = +12V, R_{RT} = 124kΩ, NDRV_ = open, CLK = open.)

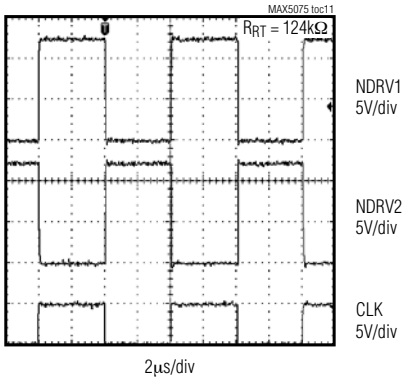
OSCILLATOR FREQUENCY vs. R_{RT}



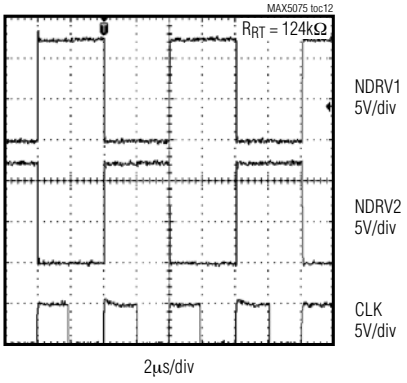
NDRV FREQUENCY vs. CLK FREQUENCY



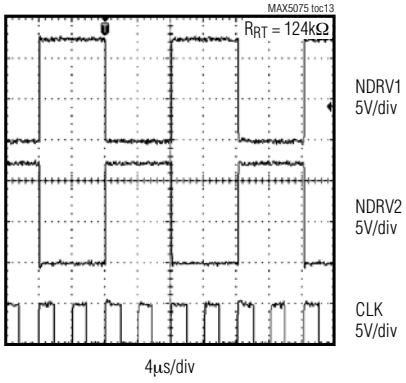
MAX5075A WAVEFORM



MAX5075B WAVEFORM



MAX5075C WAVEFORM



Pin Description

PIN	NAME	FUNCTION
1	CLK	Synchronizing Clock Output. Clock output with a ±10mA peak current drive that can be used to synchronize an external PWM regulator. CLK/NDRV1 frequency has a 1x, 2x, or 4x ratio. See the *Synchronizing Clock Output* section.
2	I.C.	Internal Connection. Connect to ground. Internal function.
3	RT	Oscillator Timing Resistor Connection. Bypass RT with a series combination of a 4.7kΩ resistor and a 1nF capacitor to DGND. Connect a resistor from RT to DGND to set the internal oscillator.
4	DGND	Digital Ground. Connect DGND to ground plane.
5	PGND	Power Ground. Connect PGND to ground plane.
6	NDRV1	Gate Driver 1. Connect NDRV1 to the gate of the external n-channel FET.
7	NDRV2	Gate Driver 2. Connect NDRV2 to the gate of the external n-channel FET.
8	V_{CC}	Power-Supply Input. Bypass V_{CC} to PGND with 0.1µF‖1µF ceramic capacitors.
EP	EP	Exposed Pad. Internally connected to DGND. Connect exposed pad to ground plane.

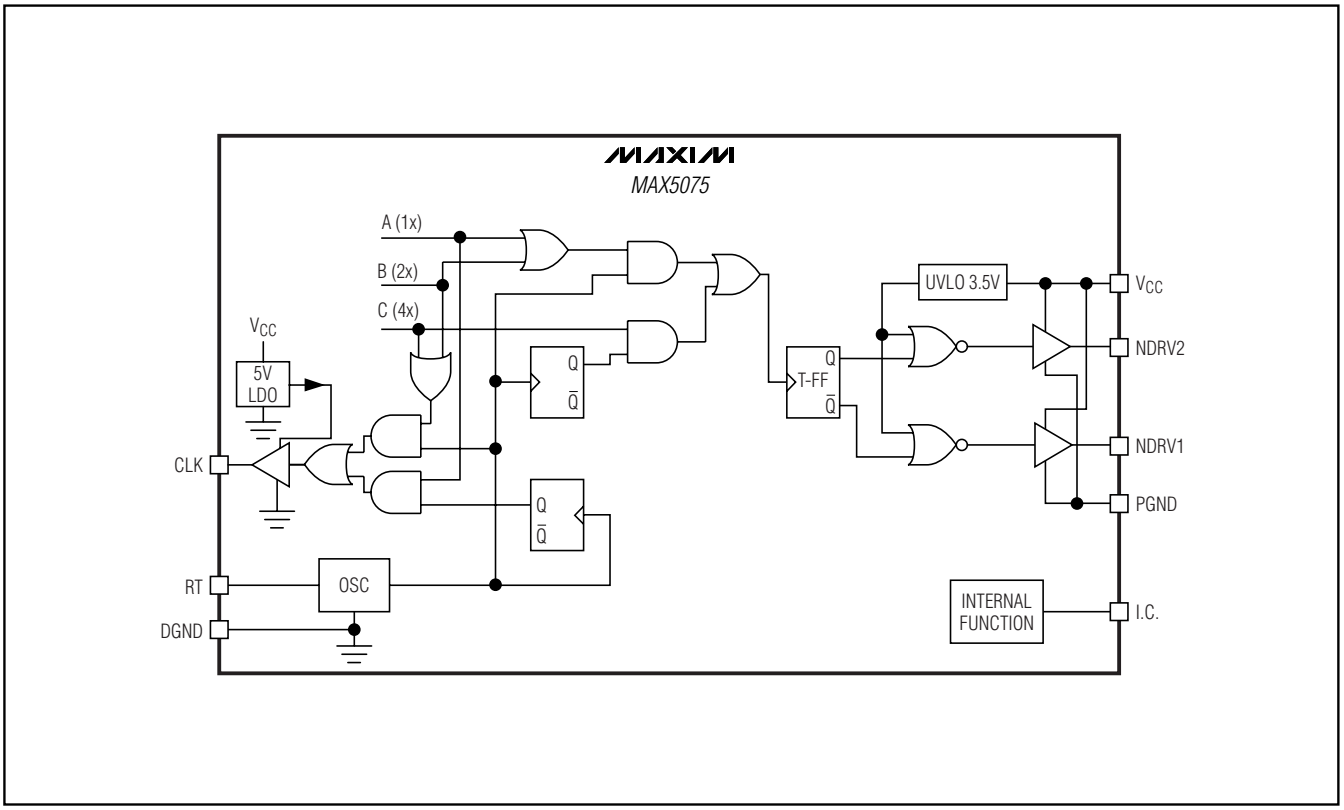


Figure 1. MAX5075 Functional Diagram

Push-Pull FET Driver with Integrated Oscillator and Clock Output

Detailed Description

The MAX5075 is a +4.5V to +15V push-pull, current-fed topology driver subsystem with an integrated oscillator for use in 48V module power supplies.

The MAX5075 features a programmable, accurate integrated oscillator with a synchronizing clock output that can be used to synchronize an external PWM stage. A single external resistor programs the internal oscillator frequency from 50kHz to 1.5MHz.

The MAX5075 incorporates a dual MOSFET driver with ±3A peak drive currents and a 50% duty cycle. The MOSFET driver generates complementary signals to drive external ground-referenced n-channel MOSFETs.

The MAX5075 is available with a clock output frequency to MOSFET driver frequency ratios of 1x , 2x, and 4x.

Internal Oscillator

An external resistor at RT programs the MAX5075 internal oscillator frequency from 50kHz to 1.5MHz. The MAX5075A/B NDRV1 and NDRV2 switching frequencies are one-half the programmed oscillator frequency with a nominal 50% duty cycle. The MAX5075C NDRV1 and NDRV2 switching frequencies are one-fourth the oscillator frequency.

Use the following formula to calculate the internal oscillator frequency:

$$f_{OSC} = \frac{10^{12}}{32 \times R_{RT}}$$

where f_{OSC} is the oscillator frequency and R_{RT} is a resistor connected from RT to DGND in ohms.

Place a series combination of a 4.7kΩ resistor and a 1nF capacitor from RT to DGND for stability and to filter out noise.

Synchronizing Clock Output

The MAX5075 provides a buffered clock output that can be used to synchronize the oscillator input of a PWM controller. CLK is powered from an internal 5V regulator and sources/sinks up to 10mA. The MAX5075 has internal CLK output frequency to NDRV1 and NDRV2 switching frequency ratios set to 1x, 2x, or 4x (Table 1).

The MAX5075A has a CLK frequency to NDRV_ frequency ratio set to 1x. The MAX5075B has a CLK frequency to NDRV_ frequency ratio set to 2x and the MAX5075C has a CLK frequency to NDRV_ frequency ratio set to 4x. There is a typical 30ns delay from CLK to NDRV_ output.

Table 1. MAX5075 CLK Output Frequency

PART	f_{CLK}	f_{NDRV1}	f_{CLK} to f_{SW} RATIO
MAX5075A	f_{OSC} / 2	f_{OSC} / 2	1
MAX5075B	f_{OSC}	f_{OSC} / 2	2
MAX5075C	f_{OSC}	f_{OSC} / 4	4

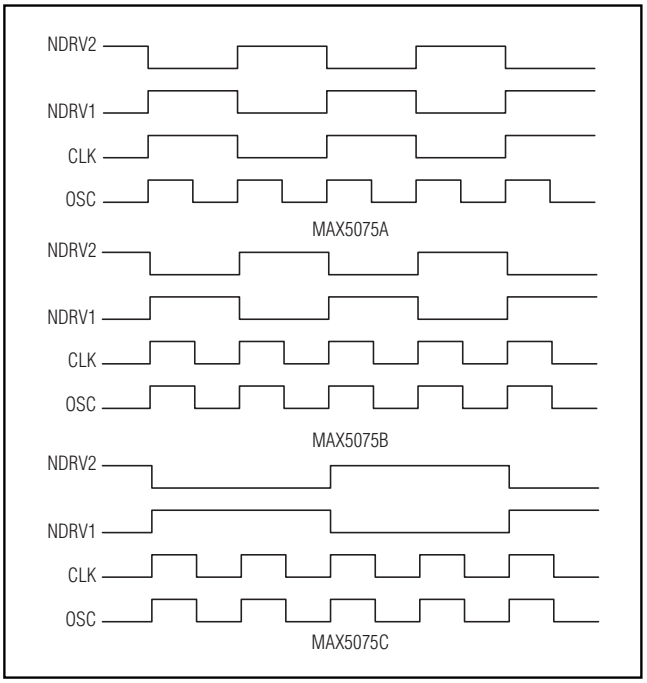


Figure 2. MAX5075 CLK Timing Diagrams

Applications Information

Supply Bypassing

Pay careful attention to bypassing and grounding the MAX5075. Peak supply and output currents may exceed 3A when driving large MOSFETs. Ground shifts due to insufficient device grounding may also disturb other circuits sharing the same ground-return path. Any series inductance in the V_{CC}, NDRV1, NDRV2, and/or GND paths can cause noise due to the very high di/dt when switching the MAX5075 with any capacitive load. Place one or more 0.1µF ceramic capacitors in parallel as close to the device as possible to bypass V_{CC} to PGND. Use a ground plane to minimize ground-return resistance and inductance. Place the external MOSFETs as close as possible to the MAX5075 to further minimize board inductance and AC path impedance.

Power Dissipation

The power dissipation of the MAX5075 is a function of the sum of the quiescent current and the output current (either capacitive or resistive load). Maintain the sum of the currents so the maximum power dissipation limit is not exceeded. The power dissipation (P_{DISS}) due to the quiescent switching supply current (I_{CCSW}) can be calculated as:

$$P_{DISS} = V_{CC} \times I_{CCSW}$$

For capacitive loads, use the following equation to estimate the power dissipation:

$$P_{LOAD} = 2 \times C_{LOAD} \times V_{CC}^2 \times f_{NDRV\_}$$

where C_{LOAD} is the capacitive load at NDRV1 and NDRV2, V_{CC} is the supply voltage, and $f_{NDRV\_}$ is the MAX5075 NDRV_ switching frequency.

Calculate the total power dissipation (P_T) as follows:

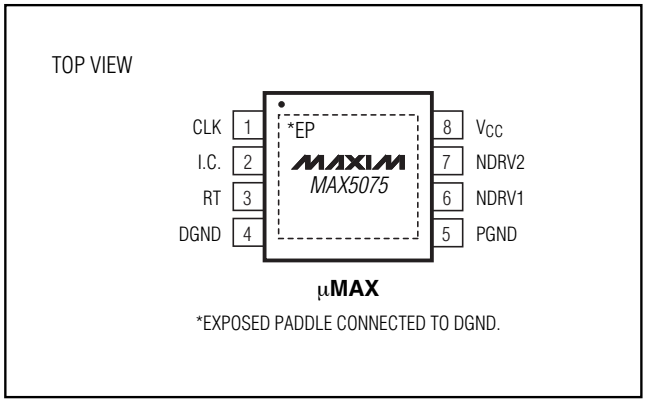
$$P_T = P_{DISS} + P_{LOAD}$$

Layout Recommendations

The MAX5075 sources and sinks large currents that can create very fast rise and fall edges at the gate of the switching MOSFETs. The high di/dt can cause unacceptable ringing if the trace lengths and impedances are not well controlled. Use the following PC board layout guidelines when designing with the MAX5075:

- Place one or more 0.1µF decoupling ceramic capacitors from V_{CC} to PGND as close to the device as possible. Connect V_{CC} and all ground pins to large copper areas. Place one bulk capacitor of 10µF on the PC board with a low-impedance path to the V_{CC} input and PGND of the MAX5075.
- Two AC current loops form between the device and the gate of the driven MOSFETs. The MOSFETs look like a large capacitance from gate to source when the gate pulls low. The current loop is from the MOSFET gate to NDRV1 and NDRV2 of the MAX5075, to PGND, and to the source of the MOSFET. When the gate of the MOSFET pulls high, the current is from the V_{CC} terminal of the decoupling capacitor, to V_{CC} of the MAX5075, to NDRV1 and NDRV2, and to the MOSFET gate and source. Both charging current and discharging current loops are important. Minimize the physical distance and the impedance in these AC current paths.
- Keep the device as close to the MOSFET as possible.

Pin Configuration



Chip Information

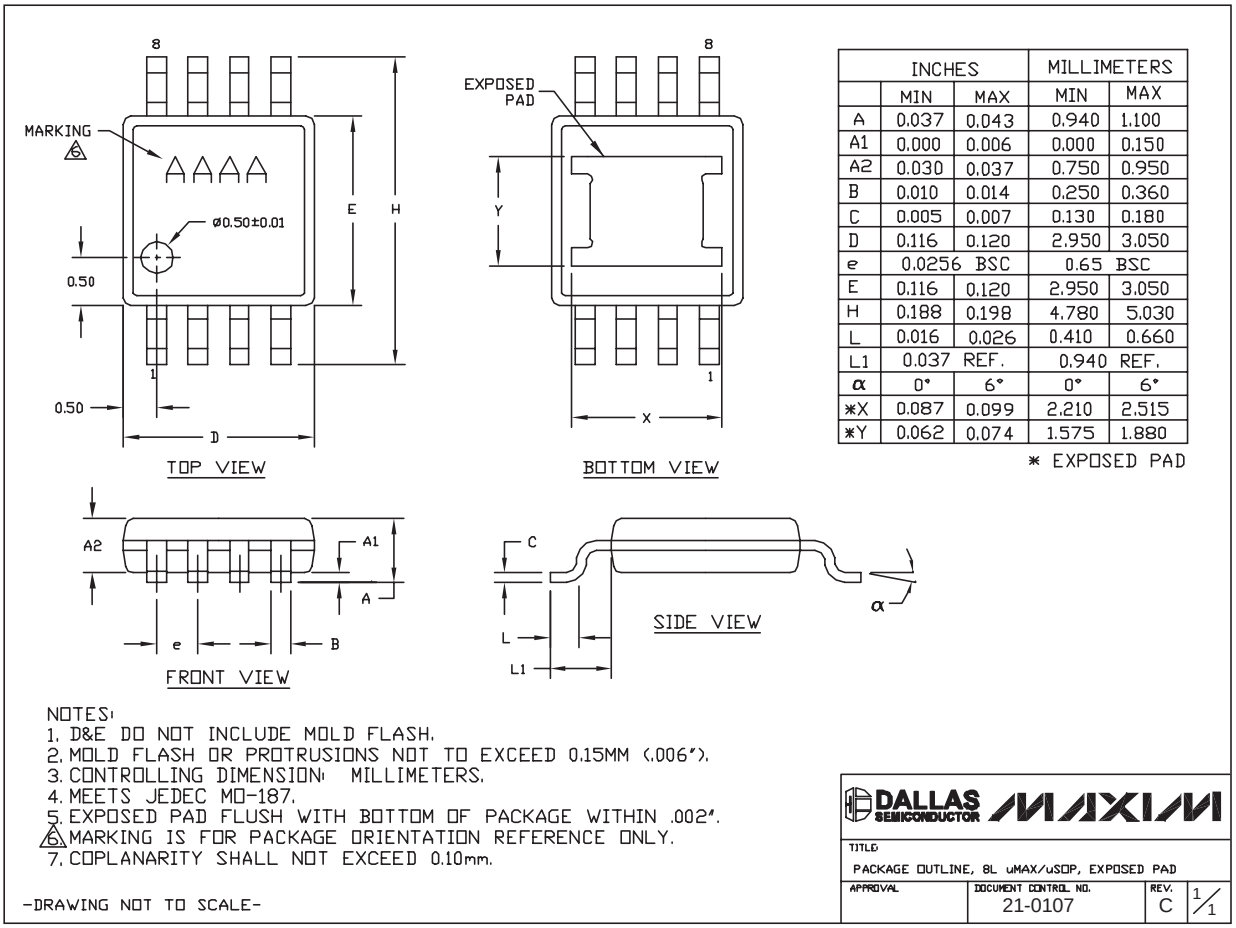
TRANSISTOR COUNT: 1335

PROCESS: BiCMOS

Push-Pull FET Driver with Integrated Oscillator and Clock Output

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)



	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.037	0.043	0.940	1.100
A1	0.000	0.006	0.000	0.150
A2	0.030	0.037	0.750	0.950
B	0.010	0.014	0.250	0.360
C	0.005	0.007	0.130	0.180
D	0.116	0.120	2.950	3.050
e	0.0256 BSC		0.65 BSC	
E	0.116	0.120	2.950	3.050
H	0.188	0.198	4.780	5.030
L	0.016	0.026	0.410	0.660
L1	0.037 REF.		0.940 REF.	
α	0°	6°	0°	6°
*X	0.087	0.099	2.210	2.515
*Y	0.062	0.074	1.575	1.880

* EXPOSED PAD

Revision History

Pages changed at Rev 1: 1, 2, 5, 6, 8

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