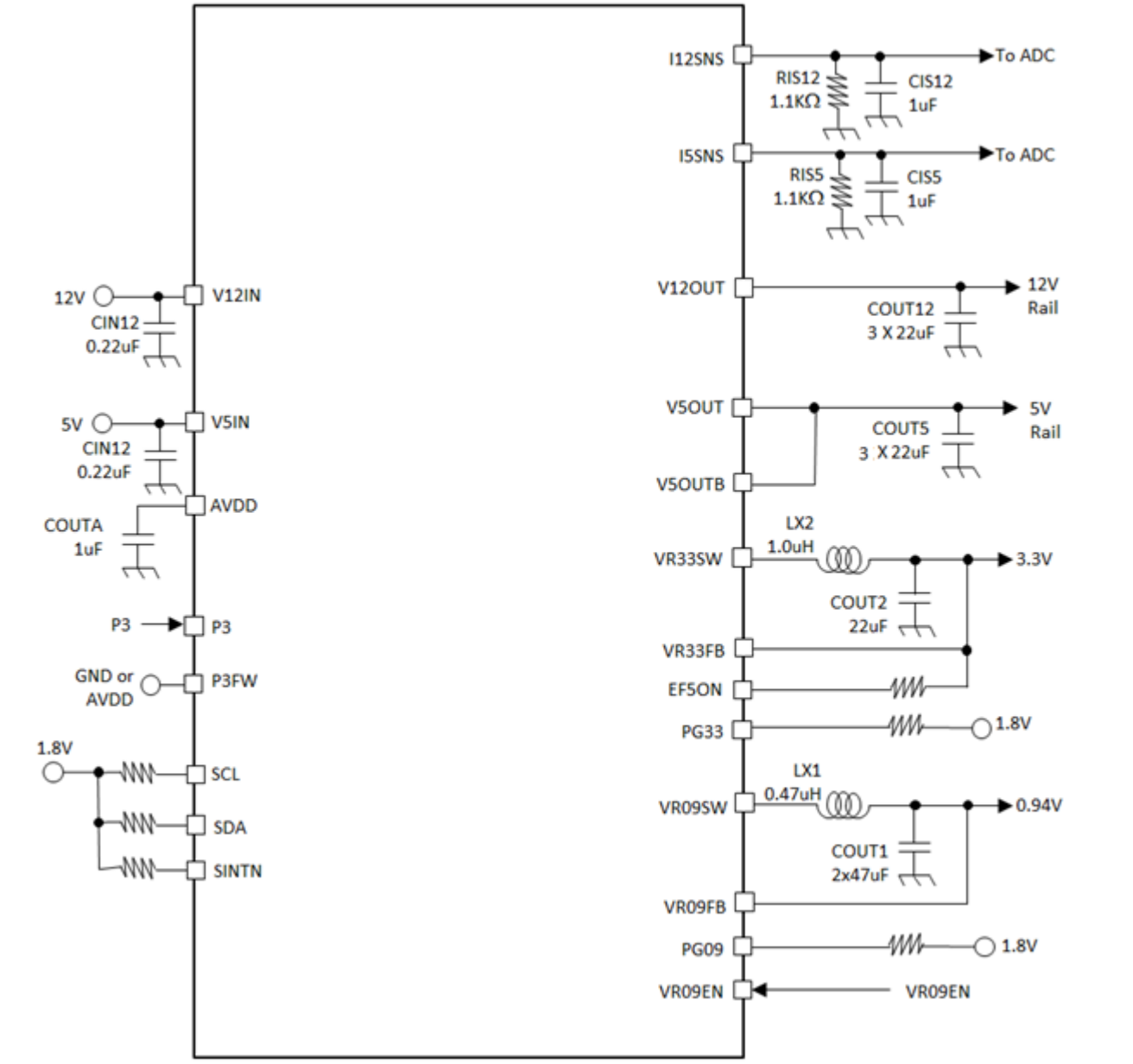


Figure 1 · **Typical Application of LX8237**

Pin Configuration and Pinout

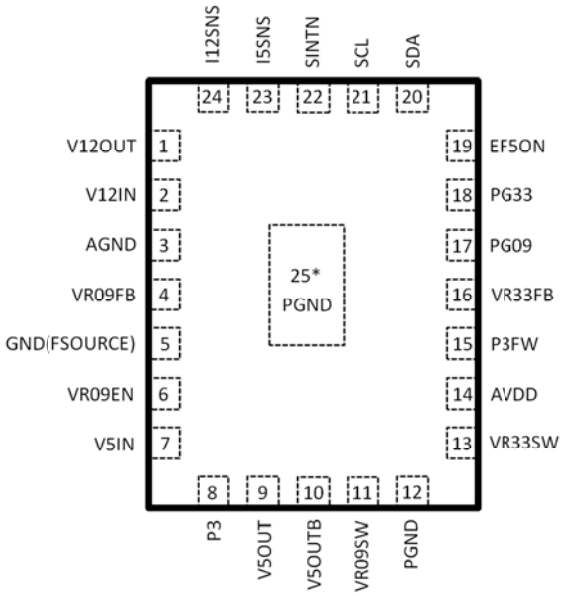


Figure 2 · **Pin out QFN 24L 3.5mm x 4.5mm. (Top View)**

Ordering Information

Ambient Temperature	Type	Package	Part Number	Packaging Type
-40°C to 85°C	RoHS Compliant, Pb-free	QFN 24L 3.5mm x 4.5mm	LX8237ILQ-TR LX8237ILQ-TR-V2R3 LX8237ILQ-TR-V3R2	Tape and Reel

Pin Description

Pin Number	Pin Name	Pin Type	Description
1	V12OUT	Power Output	12V eFuse output. Clamped at 15V when V12IN goes beyond 15V. The initial slew rate at this pin is controlled to limit turn-on surge currents.
2	V12IN	Power Input	12V Input.
3	AGND	Power Input	Analog ground. Connect to the board PGND plane at a single point.
4	VR09FB	Analog Input	0.94V output sense input.
5	GND(FSOURCE)	Power Input	Ground. (Internally Reserved for programming eFUSE. 6V power source pin for programming OTP. After programmed, this pin needs to be grounded.)
6	VR09EN	Digital Input	Input used to enable VR09 to start/stop.
7	V5IN	Power Input	5V input.
8	P3	Digital Input	SAS P3 PowerDisable. 3.3V CMOS input. Force high to initiate PowerDisable sequence. Force low to enter active mode.
9	V5OUT	Power Output	Bi-directionally protected 5V output. Clamped at 6V. The initial slew rate at this pin is controlled to limit turn-on surge currents.
10	V5OUTB	Power Input	5V input after eFuse 5V output for VR33, VR09, and control.
11	VR09SW	Power Output	Drives the 0.94V output L-C filter.
12	PGND	Power Input	Power Ground.
13	VR33SW	Power Output	Drives the 3.3V output L-C filter.
14	AVDD	Power Output	Output of the internal pre-regulator. This housekeeping voltage will be used to generate internal bias currents and voltages. It also represents the voltage that is used for internal IC communication. It will be current limited with an on-chip resistor to limit turn-on surge current. This pin is not to be used by external circuitry. A 1µF bypass cap should be placed between AVDD and AGND.
15	P3FW	Digital Input	Allow firmware to control P3 function when P3FW is connected to AVDD
16	VR33FB	Analog Input	3.3V output sense input. Drives an internal resistive feedback divider.
17	PG09	Digital Output	Power Good pin for 0.9V switching regulator. Open drain output which requires an external pull-up resistor. PG09 will go high a certion delay (1µs: deGlitch=1, 200ns: deGlitch=0) after 0.9V outputs is good, it will be low otherwise. Also used as an internal digital test visibility bus output.
18	PG33	Digital Output	Power Good pin for 3.3V switching regulator. Open drain output which requires an external pull-up resistor. PG33 will go high a certain delay (1µs: deGlitch=1, 200ns: deGlitch=0) after 3.3V outputs is good, it will be low otherwise. Also used as an internal analog test visibility bus output.
19	EF5ON	Digital Output	Open drain ouput. External pull up resistor is required. Logic 1 indicates 5V eFuse FET is closed.
20	SDA	Digital In/Out	I²C data port. External pull up resistor is required. 1.8V CMOS logic levels. The power supply for the external pull up resistors is assumed to be at 1.8V, but the sequencing of this supply can occur at any time before, during or after powering of the LX8237 5V or 12V input. If this power supply drops below 1.8V logic level thresholds tolerance value (+/-10%), then I²C communication may be interrupted. The default register value loading of all I²C registers (customer and test) should be independent on the SDA state.

Pin Number	Pin Name	Pin Type	Description
21	SCL	Digital Input	I²C clock port. External pull up resistor is required. 1.8V CMOS logic levels. The power supply for the external pull up resistors is assumed to be at 1.8V, but the sequencing of this supply can occur at any time before, during or after powering of the LX8237 5V or 12V input. If this power supply drops below 1.8V logic level thresholds tolerance value (+/-10%), then I²C communication may be interrupted. The default register value loading of all I²C registers (customer and test) should be independent on the SCL state.
22	SINTN	Digital Output	General purpose interrupt output. External pull up resistor is required. Logic 0 to indicate interrupt.
23	I5SNS	Analog Output	5V eFuse output current monitor. Connect to an external parallel R-C filter network. These component values will be adjusted when the final gain of the current monitor is determined.
24	I12SNS	Analog Output	12V eFuse output current monitor. Connect to an external parallel R-C filter network. These component values will be adjusted when the final gain of the current monitor is determined.
25*	PGND	Power Ground	Power Ground. Connected to back side thermal pad.

Block Diagram

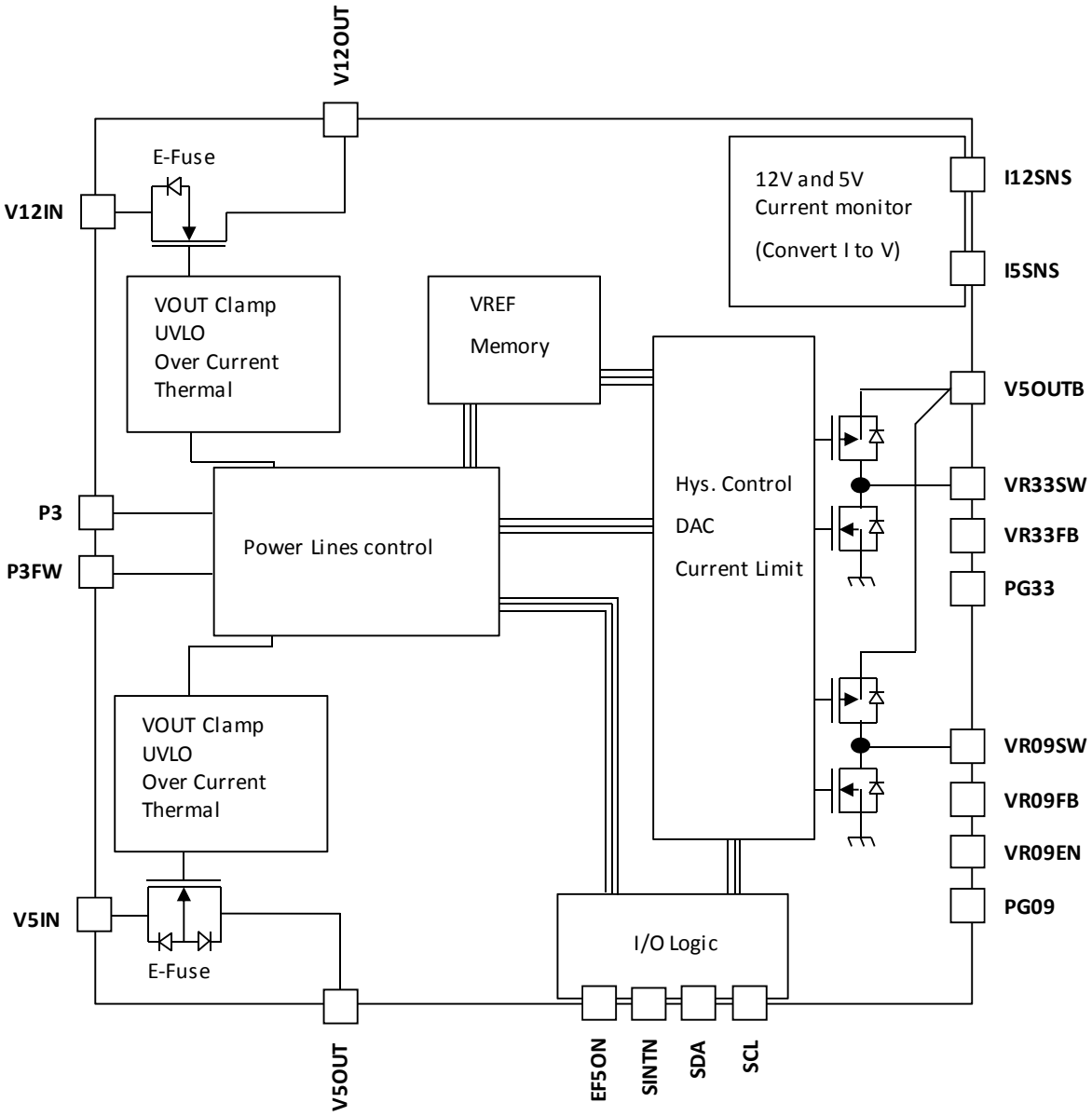


Figure 3 · **Simplified Block Diagram of LX8237**

Absolute Maximum Ratings

Parameter	Min	Max	Units
V12IN	-0.3	25	V
V5IN, V12OUT	-0.3	15	V
V12OUT Current		3.5	A
V5OUT Current		3.5	A
P3, P3FW, V5OUT, SINTN, SDA, SCL, PG09, VR09EN, VR09FB, VR09SW, PG33, VR33FB VR33SW, V5OUTB, I5SNS, I12SNS, AVDD, EF5ON	-0.3	6.5	V
Junction Temperature	-40	150	°C
Storage Temperature	-65	150	°C
Peak Solder Reflow Temperature (40 seconds)		260+0,-5	°C
ESD (Human Body Model)		2000	V
ESD (Charged Device Model)		500	V

Note: Performance is not necessarily guaranteed over this entire range. These are maximum stress ratings only. Exceeding these ratings, even momentarily, can cause immediate damage, or negatively impact long-term operating reliability

Operating Ratings

	Min	Typ	Max	Units
V12IN Voltage	10.8		13.2	V
V12OUT Continous Current			2.5	A
V5IN Voltage	4.3		5.5	V
V5OUT Voltage	3.0		5.5	V
V5OUT Continous Current			2.5	A
Serial I/F Voltage	1.7	1.8	1.95	V
P3 Input Voltage	-0.3	3.3	3.6	V
P3FW Input Voltage	-0.3		1.1*AVDD	V
Junction Temperature	-40		125	°C
Ambient Temperature	-40		85	°C

Note: Performance is generally guaranteed over this range as further detailed below under Electrical Characteristics.

Thermal Properties

Thermal Resistance	Typ	Units
θ_{JA}	50	°C/W

Note: The θ_{JA} numbers assume no forced airflow. Junction Temperature is calculated using $T_J = T_A + (PD \times \theta_{JA})$. In particular, θ_{JA} is a function of the PCB construction. The stated number above is for a four-layer board in accordance with JESD-51 (JEDEC).

Electrical Characteristics

Note: Unless otherwise specified, the following specifications apply over the operating ambient temperature of -40°C ≤ T_A ≤ 85°C. Except where otherwise noted, the following test conditions apply: V12IN=12V, V5IN=5V, LX1=1 µH, COUT1=22µF, LX2=0.47µH, COUT2=44µF, COUT12=3*22µF, COUT5 = 3*22µF. Typical parameters refers to T_A=25°C

Symbol	Parameters	Test Conditions/Comments	Min	Typ	Max	Units
Device						
Ibias1	Biasing current 1	V5IN CURRENT, P3 LOW, VR09EN HIGH, VR33FB=5V @ V12IN=12V, V5IN=5V		0.4	1	mA
Ibias2	Biasing current 2	V5IN CURRENT, P3 LOW, VR09EN LOW, VR33FB=5V @ V12IN=12V, V5IN=5V		0.4	1	mA
Ibias3	Biasing current 3	V5IN CURRENT, P3 HIGH, VR09EN LOW, VR33FB=5V @ V12IN=12V, V5IN=5V		0.4	1	mA
Ibias4	Biasing current 4	V12IN CURRENT, P3 LOW, VR09EN HIGH, VR33FB=5V @ V12IN=12V, V5IN=5V		0.4	1	mA
Ibias5	Biasing current 5	V12IN CURRENT P3 HIGH @ V12IN=12V, V5IN=5V		0.4	1	mA
12V eFuse FET						
I_inrush_12	Inrush Current	Inrush current during the hot-swap condition. Measure the input current into V12IN in the transient of VCC from 0V to 12V at the slewrate of 12V/20ns.			1.5	A
Rdson_12	On Resistance	T_J=25°C, 200mA through V12IN to V12OUT(Note 2)		50		mΩ
		T_J=125°C, 200mA through V12IN to V12OUT(Note 1)			95	
	Off state leakage current				4	µA
Idc_12	Continuous Current	T_A=25°C(Note 1)		2.5		A
Trise_12	Vout ramp time	Measure 10% to 90% rise time at V12OUT Initiate the ramp by setting P3 low.		10		ms
Tdly_12	Turn on delay	Measure delay from the falling edge of P3 to the 10% point at V12OUT.		1.3		ms
Vclamp_12	Output Clamping Voltage	V12IN=18V, dc test, no load. Measure V12OUT.	13.8		14.98	V
	Maximum overshoot in the transient	Increase V12IN from 12V to 24V in 12V/100ns. Monitor the maximum excursion at V12OUT with no load.			15	V
	UVLO falling threshold	Decrease V12IN. Observe when V12OUT with some load falls below V12IN by 100mV.	8.8	9	9.24	V
	UVLO rising hysteresis	Increase V12IN. Observe when V12OUT turns on.	0.6	0.7	0.8	V
Isc_lim_12	Short circuit current limit	V12OUT < 1.5V. Force V12OUT to 0V, measure I(V12OUT).		1	1.5	A

Symbol	Parameters	Test Conditions/Comments	Min	Typ	Max	Units
Iavg_lim_12	Overloading current limit	Force V12OUT to 0.5V less than V12IN,measure I(V12OUT).	3	4	5	A
	Current monitor output current gain	Imon/IeFuse, ImonG=0. Test at 200mA and 300mA.	232.8	240	247.2	uA/A
		Imon/IeFuse, ImonG=1. Test at 200mA and 300mA.	465.6	480	494.4	
	Current monitor error	I(eFuse12) = 200mA, Imon/IeFuse. ImonG=1. Calculate error vs. ideal value.		2	3	%
5V eFuse FET						
I_inrush_5	Inrush Current	Inrush current during the hot-swap condition. Measure the input current into V5IN in the transient of VCC from 0V to 5V at the slewrate of 5V/10ns.			1.5	A
Rdson_5	On Resistance	T_J=25°C, 200mA through V5IN to V5OUT(Note 2)		50		mΩ
		T_J=125°C, 200mA through V5IN to V5OUT(Note 1)			95	
	Off state leakage current				9	µA
Idc_5	Continuous Current	T_A=25°C(Note 1)		2.5		A
Trise_5	Vout ramp time	Measure 10% to 90% rise time at V5OUT Initiate the ramp by setting P3 low.		10		ms
Tdly_5	Turn on delay	Measure delay from the falling edge of P3 to the 10% point at V5OUT.		2.2		ms
Vclamp_5	Output Clamping Voltage	V5IN=10V, dc test, no load. Measure V5OUT.	5.7	6	6.3	V
	Maximum overshoot in the transient	Increase V5IN from 5V to 12V in 70nS (5V/µS). Monitor the maximum excursion at V5OUT with no load.			6.5	V
	UVLO falling threshold	Decrease V5IN. Observe when V5OUT with some load begins to fall.	4.0	4.1	4.2	V
	UVLO rising threshold	Increase V5IN. Observe when V5OUT turns on.	4.25	4.35	4.45	V
Isc_lim_5	Short circuit current limit	V5OUT < 1.5V. Force 0V at V5OUT measure I(V5OUT).		1	1.5	A
Iavg_lim_5	Overloading current limit	Force V5OUT to 0.5V less than V5IN, measure I(V5OUT)	3	4	5	A
	AVDD UVLO rising	This is the point that the 12v E-fuse turns on when 5voutb is rising	2.79		3.2	V
	AVDD UVLO falling	This is the point that the 12V E-fuse turns off when 5OUT5B is lowered	2.17		2.35	V
	V5OUTB UVLO rising	This is where the 3.3V and 0.94 regulators turn on. The SINT pins also in disabled (see the fault condition table)	3.85		4.13	V

Symbol	Parameters	Test Conditions/Comments	Min	Typ	Max	Units
	V5OUTB UVLO faling	This is where the 3.3V and 0.94V regulators turn off. The SINT pins also in disabled (see the fault condition table)	1.92		3.38	V
	Current monitor output current gain	Imon/IeFuse, ImonG=0. Test at 200mA and 300mA.	242.5	250	257.5	µA/A
		Imon/IeFuse, ImonG=1. Test at 200mA and 300mA.	485	500	515	
	Current monitor error	I(eFuse5) = 200mA, Imon/IeFuse		2	3	%
	Reverse current voltage threshold	Force V5OUT above V5IN. Monitor the comparator output. Determine the rising and falling thresholds.		-35		mV
	Reverse current voltage hysteresis	See test above.		15		mV
0.94V Switching Regulator						
	0.94V regulator Input Range	The core blocks of 0.94V Switching Regulator needs to be operational in this condition. The 0.94V regulator will not be enabled until VDD5 has cleared its UVLO threshold and V5OUT has finished rising. (Note 1)	3.0		5.5	V
HSrdson_9	PFET resistance	T_J=25°C, sink -0.5A at VR09SW at V5OUTB=5V(Note 2)		65		mΩ
		T_J=125°C, sink -0.5A at VR09SW at V5OUTB=5V(Note 1)		90		
		T_J=125°C, sink -0.5A at VR09SW at V5OUTB=3V(Note 1)		135		
LSrdson_9	NFET resistance	T_J=25°C, source 0.5A at VR09SW at V5OUTB=5V(Note 2)		18.5		mΩ
		T_J=125°C, source 0.5A at VR09SW at V5OUTB=5V(Note 1)		31		
		T_J=125°C, source 0.5A at VR09SW at V5OUTB=3V(Note 1)		41.2		
Idc_9	Continuous DC out current	T_A=25°C		3.5		A
	Peak Current Limit		6.4	7.1	7.8	A
	Overcurrent –Limit Toff Time				605	ns
	DC output voltage	PWM only, no load. Code 000000		770		mV
		PWM only, no load. Code 111111		1085		
	Output voltage accuracy	PWM only, no load. Measure at 0.94V output.		+/-1	+/-1.5	%
	DC output voltage step size	(Note 1)		5		mV
Tsoftstart_	Soft start time	Measure 10% to 90% rise time at 0.94V output		1		ms

Symbol	Parameters	Test Conditions/Comments	Min	Typ	Max	Units
9		Initiate the ramp by enabling the regulator via VR09EN.				
	VR09EN rising threshold	Increase voltage at VR09EN.	0.6		1	V
	VR09EN falling threshold Hysterisis			100		mV
	VR09EN input bias current	Force 1.8V at VR09EN.			1	uA
	PG09 active voltage	Force the FB pin in open loop. Measure when the PG09 pin pulls low.	-17	-10	-8	%
	PG09 deglitch filter	Register DEGLITCH=0		300		ns
		Register DEGLITCH=1		1.2		µs
	PG09 logic 0 active output voltage	I_{SINK}=1mA			400	mV
Tpgdelay_9	PG09 logic 1 in-active output voltage delay			1		ms
	Hiccup time	FBUVLO hiccup time. Force FB to 60%, monitor the SW pin for high and Hi-Z conditions		8.5		ms
	Voltage output transient due to step transient current	I_{LOAD} Slew-rate: 1.6A/1µs from 0.8A to 2.4A			47	mV
	Switching Frequency	PWM only, no load.	1.6	2	2.4	MHz
	Efficiency	3V < V5OUTB < 5.5V, Iload = 0.5A to 2A		90		%
	CCM to DCM Change Point	Sweep the load current. 0A -> 1500mA -> 0A.		600		mA
	DCM to CCM Change Point			1000		
3.3V Switching Regulator						
	3.3V regulator Input Range	(Note 1)	3.4		5.5	V
HSrdson_3	PFET resistance	T_J=25°C, V5OUTB=5V, sink -0.2A at VR33SW(Note 2)		290		mΩ
		T_J=125°C, V5OUTB=5V, sink -0.2A at VR33SW(Note 1)		350		
		T_J=125°C, V5OUTB=3V, sink -0.2A at VR33SW(Note 1)		500		
LSrdson_3	NFET resistance	T_J=25°C, V5OUTB=5V, source 0.2A at VR33SW(Note 2)		440		mΩ
		T_J=125°C, V5OUTB=5V, source 0.2A at VR33SW(Note 1)		640		
		T_J=125°C, V5OUTB=3V, source 0.2A at		900		

Symbol	Parameters	Test Conditions/Comments	Min	Typ	Max	Units
		VR33SW(Note 1)				
Idc_3	Continuous DC current	T_A=25°C(Note 1)		300		mA
	Peak Current Limit		0.75	1.25	1.75	A
	DC output voltage	PWM only, no load. Code 000000		2540		mV
		PWM only, no load. Code 111111		3780		
	Output voltage accuracy	PWM only, no load. Measure at 3.3V output.		+/-1	+/-1.5	%
	DC output voltage step size	(Note 1)		40		mV
	VR33FB voltage range	(Note 1)			V5OUTB	V
	V5OUTB to enable VR33 to start-up	Increase V5OUTB, measure when VR33 starts up.		4		V
Tsoftstart_3	Soft start time	Measure 10% to 90% rise time at 3.3V output Initiate the ramp by forcing V5OUTB to 5V.		1		ms
	PG33 active voltage	Force the FB pin in open loop. Measure when the PG09 pin pulls low.	-14	-10	-8	%
	PG33 deglitch filter	Register DEGLITCH=0		230		ns
		Register DEGLITCH=1		1.4		µs
	PG33 logic 0 active output voltage	Isink=1mA			400	mV
Tpgdelay_3	PG33 logic 1 in-active output voltage delay			1		ms
	Voltage output transient due to step transient current	I_{LOAD} Slew-rate: 1.6A/1µs from 0.15A to 0.35A			165	mV
	Switching Frequency	PWM only.		6		MHz
	Efficiency	3V < V5OUTB < 5.5V, Iload = 0.1A to 0.3A		90		%
	DCM to CCM Change Point	Sweep the load current. 0A -> 300mA -> 0A.		100		mA
	CCM to DCM Change Point			95		
	Cooling Time	FBUVLO hiccup time. Force FB to 60%, monitor the SW pin for high and Hi-Z conditions. Will probably need a pull down resistor at SW.		10		ms
Temperature Monitor						
EOTW	Early over temperature		140	155	170	°C

Symbol	Parameters	Test Conditions/Comments	Min	Typ	Max	Units
	warning					
OTth	Over Temperature Threshold	Sweep temperature. 5V and 12V eFuse have their own thermal shutdown circuit. They should be separately characterized.	160	175	190	°C
OThy	Over temperature hysteresis	EN/FAULT pin is driven by the other eFuse. Thermal Fault, Output Disabled,		50		°C
Tdelta	Temperature difference from EOTW to OTth	Output Enabled	15	20	25	°C
P3 and P3FW						
VP3th	P3 logic rising threshold	V(P3) < VP3th: Power Enable V(P3) > VP3th: Power Disable Use the digital XOR test mode output	1.2	1.6	2.0	V
	P3 logic falling threshold hystresys		200	300	400	mV
	P3 pull-down resistor		60	100	140	kΩ
VP3FWth	P3FW logic rising threshold	V(P3FW) < VP3FWth: P3EN Register Bit Control throughI2C is disabled. V(P3FW) > VP3FWth: P3EN Register Bit Control throughI2C is enabled. Use the digital XOR test mode output.	1.2	1.6	2.0	V
	P3FW logic threshold hystresys		200	300	400	mV
SINTN						
	Output Low Voltage	ISINK(SINTN)=1mA			0.4	V
	Output High Leakage Current	Set SINTN off, force 1.8V at SINTN, measure the leakage current.			2	µA
EF5ON						
	Output Low Voltage	ISINK(EF5ON)=1mA			0.4	V
	Output High Leakage Current	Set EF5ON off, force 1.8V at EF5ON, measure the leakage current.			2	uA
	EF5ON max output voltage	EF5ON is pulled up to VR33FB through a external resistor. (Note 1)			VR33FB	V
	EF5ON logic 0 output voltage	Isink = 1mA	-300		400	mV
	EF5ON max output voltage			3	VR33FB	V
	EF5ON comparator deglitch filter			500		ns
I²C						
I_{Q_OP}	Vol-SDA	I=4mA(Note 1)			0.4	V
V_{MIN}	VDD for I²C interface	Input condition(Note 1)	1.7	1.8	1.95	V

Symbol	Parameters	Test Conditions/Comments	Min	Typ	Max	Units
	Vil	Logic0 input voltage(Note 1)	-0.5		0.3*VDD	V
	Vih	Logic1 input voltage(Note 1)	0.7*VDD		VDD+0.5	V
	Vihyst	Input hysteresis(Note 1)	0.1*VDD			V
	Iin	Input current, Vi=0.1*VDD to 0.9*VDD (Note 1)	-10		10	µA
	Vol	Logic0 output voltage, Isink=2mA(Note 1)	0		0.2*VDD	V
	Iol	Vol=0.4V(Note 1)	3			mA
	Input voltage deglitch	(Note 1)	0		10	ns
	SCL clock frequency	(Note 1)	0		3.4	MHz
	tsu, start/stop	Setup time(Note 1)	160			ns
	thold, start/stop	Hold time(Note 1)	160			ns
	tlow, SCL	low pulse time(Note 1)	160			ns
	thi, SCL	high pulse time(Note 1)	60			ns
	tsu, SDA	data setup time(Note 1)	10			ns
	thold, SDA	data hold time(Note 1)	0		70	ns
	trise, tfall, SCL	clock rise/fall time(Note 1,3,4)	10		1000	ns
	trise, tfall, SDA	data rise/fall time(Note 1,3,4)	10		1000	ns

Note: 1. Guaranteed by Design

Note: 2. Pulse test: Pulse width = 300µs, Duty cycle = 2%.

Note: 3. The signal must be compliant to the characteristic of standard I2C bus. LX8237 is compatible with “Normal/Fast/Fast Plus/High Speed” mode

Note: 4. To achieve the faster rising time, users may need to adjust the pull up resistor value.

Theory of Operation / Application Information

12V eFuse

The 12V eFuse block functions as follows: The 12V eFuse is initially on its off state. The ON/OFF control of the eFuse is base on the input pins V12IN, P3, P3FW, P3En bit and fault conditions. See application details section for the complete control functions. After the eFuse is allowed to turn on, it then ramps the output voltage to its final value while at the same time limit the max current to the current limit value. If the input continues to rise above the OV12 threshold, the eFuse will limit the output to the OV12limit and set the OV12 bit in the serial port. The 12V eFuse will operate in this state until it hits its OT limit and shuts down. The eFuse will restart after temperature is below the OT hystereis value.The 12V eFuse block also has an output current monitor. The current monitor output current is proportional to the current of the 12V eFuse from input to output.
The 12v E-Fuse will limit current to the current limit level. If the output voltage drops low enough, a short is detected and the current limit is reduced even further. If the short circuit is removed before an over temperature event occurs, the current limit level will remain at the short circuit current limit level until all the faults in the I2C registers are cleared by writing to the status register. This will ensure that the output voltage rise rate is limited to the short circuit current level.

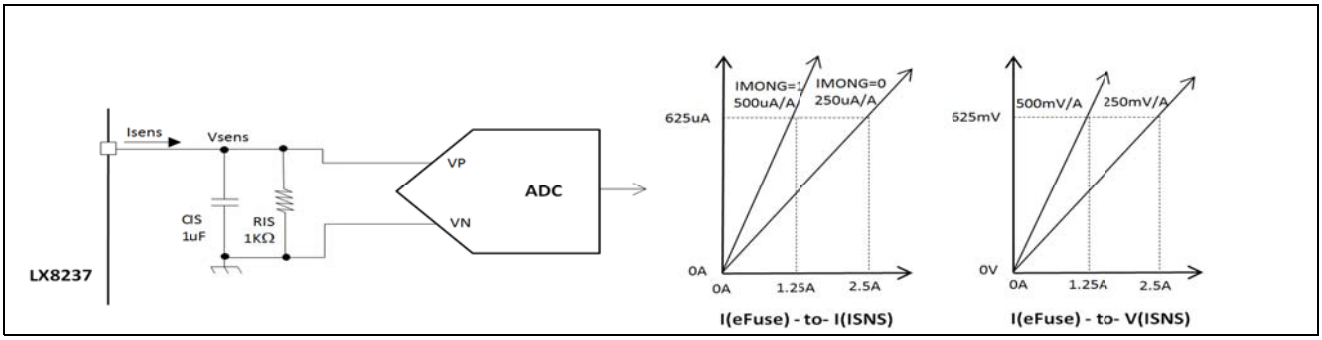
5V eFuse

The 5V eFuse block functions as follows: The 5V eFuse is initially on its off state. The ON/OFF control of the eFuse is base on the input pins V5IN, P3, P3FW, P3En bit and fault conditions. See application details section for the complete control functions. After the eFuse is allowed to turn on, it then ramps the output voltage to its final value while at the same time limit the max current to the current limit value. If the input continues to rise above the OV5 threshold, the chip will limit the output to the OV5limit and set the OV5 bit in the serial port. The 5V eFuse will operate in this state until it hits its OT limit and shuts down. The eFuse will restart after temperature is below the OT hystereis value. When the current goes in the reverse direction above the threshold, the eFuse will open and isolate the output from the input. The eFuse will restart with current limit once the reverse current goes to zero AND the input has satisfied the normal startup criteria. The 5V eFuse block has an output current monitor. The current monitor output current is proportional to the current of the 5V eFuse from input to output. The 5V Efuse block has a logic output at EF5on open drain pin to indicate when the eFuse is in its open protective state.
The 5v E-Fuse will limit current to the current limit level. If the output voltage drops low enough, a short is detected and the current limit is reduced even further. If the short circuit is removed before an over temperature event occurs, the current limit level will remain at the short circuit current limit level until the 3.3v Power Good is OK. This will ensure that the output voltage rise rate is limited to the short circuit current level.

eFuse Current Monitor Function

The average current being supplied by each eFuse output can be monitored at I5SNS and I12SNS. A current proportional to the average eFuse output current will be sourced out of the sense pins. This current will be converted to a voltage and filtered by a parallel R-C network connect at I5SNS and I12SNS pins.

By default, the current monitors are disabled. They are enabled via the serial port. Any fault that turns off either the eFuses or the regulators will turn off the current monitor by reseting IMON bits as well. The current monitors have two different gain selections to allow for better resolution at different current ranges.



094V Switching Regulator

The VR09 regulator is a fully integrated switching regulator. This regulator features adjustable output voltage with power monitor and over current protection. Whenever the output is 10% below the programmed target output voltage, the PG09 pin is pulled low to indicate a fault. The regulator starts when VR09En goes high and turns off when VR09En goes low. When VR09En is low, the VR09Dis and VR09MonDis bits are automatically reset.

Firmware can disable VR09 when VR09En is high as follows:

1. Set the VR09Key bit to allow the VR09Dis/VR09MonDis bits to be programmed.
2. Set VR09MonDis and VR09Dis as desired. When VR09MonDis is set, the state of the PG09 pin is held steady at the previous value, independent of the actual VR09 output voltage. When VR09Dis is set, VR09 is shut off.
3. VR09Key will automatically reset when any register other than 03H is written. This two step programming approach prevents accidentally disabling VR09 through firmware since the VR09MonDis and VR09Dis bits cannot be changed when VR09Key is reset.
4. Setting VR09Key and then resetting VR09Dis will restart VR09. At the end of the soft start period (rising edge-sensitive), VR09MonDis will automatically reset to re-enable PG09. This allows VR09 to be shut off without disturbing the PG09 pin.

These tables specify the functionality of the VR09Key, VR09Dis, and VR09MonDis bits:

0V9KEY	Function
0	0V9Dis and 0V9MonDis bits cannot be changed via the serial interface. This bit is automatically reset when any register other than 03H is written.
1	0V9Dis and 0V9MonDis bits can be changed via the serial interface.

0V9Dis	Function
0	VR09 is controlled by the VR09En pin.
1	Shut off VR09. This bit is automatically reset whenever VR09En (pin) is set low.

0V9MonDis	Function
0	Allows the PG09 pin to monitor the status of the VR09 output.
1	Hold the PG09 state at whatever value it was at when this bit was set. This bit is automatically reset whenever VR09En (pin) is set low. It is also reset at the end of the soft start ramp up period.

This table shows how the VR09 output is controlled by the 0V9SEL bits. The default setting of 100010 gives an output of 0.94V.

0V9SEL	VR09 (V)	0V9SEL	VR09 (V)	0V9SEL	VR09 (V)	0V9SEL	VR09 (V)
000 000	0.770	010 000	0.850	100 000	0.930	110 000	1.010
000 001	0.775	010 001	0.855	100 001	0.935	110 001	1.015
000 010	0.780	010 010	0.860	100 010	0.940	110 010	1.020
000 011	0.785	010 011	0.865	100 011	0.945	110 011	1.025
000 100	0.790	010 100	0.870	100 100	0.950	110 100	1.030
000 101	0.795	010 101	0.875	100 101	0.955	110 101	1.035
000 110	0.800	010 110	0.880	100 110	0.960	110 110	1.040
000 111	0.805	010 111	0.885	100 111	0.965	110 111	1.045
001 000	0.810	011 000	0.890	101 000	0.970	111 000	1.050
001 001	0.815	011 001	0.895	101 001	0.975	111 001	1.055
001 010	0.820	011 010	0.900	101 010	0.980	111 010	1.060
001 011	0.825	011 011	0.905	101 011	0.985	111 011	1.065
001 100	0.830	011 100	0.910	101 100	0.990	111 100	1.070
001 101	0.835	011 101	0.915	101 101	0.995	111 101	1.075
001 110	0.840	011 110	0.920	101 110	1.000	111 110	1.080
001 111	0.845	011 111	0.925	101 111	1.005	111 111	1.085

The safe operating area (SOA) of the device covers the maximum current limit and maximum operating voltage as specified in the electrical characteristics table.

3.3V Switching Regulator

The VR33 regulator is a fully integrated switching regulator. This regulator features adjustable output voltage with power monitor and over current protection. Whenever the output is 10% below the programmed target output voltage, the PG is triggered and the VR33FLT bit is set along with the PG33 pin pulled low to indicate a
failure.This regulator starts when 5VoutB is crosses the start regulator threshold. It will stop when 5VoutB is below its min supply for proper operation. The start/stop thresholds are different.

This table shows how the VR33 output is controlled by the 3V3SEL bits. The default setting of 10011 gives an output of 3.3V.

3V3SEL	VR33 (V)	3V3SEL	VR33 (V)	3V3SEL	VR33 (V)	3V3SEL	VR33 (V)
00 000	2.54	01 000	2.86	10 000	3.18	11 000	3.50
00 001	2.58	01 001	2.90	10 001	3.22	11 001	3.54
00 010	2.62	01 010	2.94	10 010	3.26	11 010	3.58
00 011	2.66	01 011	2.98	10 011	3.30	11 011	3.62
00 100	2.70	01 100	3.02	10 100	3.34	11 100	3.66
00 101	2.74	01 101	3.06	10 101	3.38	11 101	3.70
00 110	2.78	01 110	3.10	10 110	3.42	11 110	3.74
00 111	2.82	01 111	3.14	10 111	3.46	11 111	3.78

I²C Serial Interface

The chip supports a high speed (3.4MHz) serial interface with the I²C serial protocol. This interface is bi-directional allowing the microprocessor to set functions and read status. Status0/1 register bits are latched once the first fault happens. In this case, the following fault cannot write the register anymore. Cleared by write action to the status register.

I²C Port Functional Description

- Simple two wire, bidirectional, serial communication port.
- Multiple devices on same bus speeds from 400Kbps (FS-Mode) to 3.4Mbps (HS-Mode).
- SOC Master controls bus.
- Device listens for the unique address that precedes data.

General I²C Port Description

The LX8237 includes an I²C compatible serial interface, using two dedicated pins: SCL and SDA for I²C clock and data respectively. Each line is externally pulled up to a logic voltage when they are not being controlled by a device on the bus. The LX8237 interface acts as a I²C slave that is clocked by the incoming SCL clock. The LX8237 I²C port will support both the Fast mode (400kHz max) and typically the High Speed mode(3.4MHz max). The data on the SDA line must be stable during the HIGH period of the clock signal (SCL). The state of the SDA line can only be changed when SCL is LOW (except for start, stop, and restart).

START and STOP Commands

When the bus is idle, both SCL and SDA must be high except in the power up case where they may be held high or low during the system power up sequence.

The SOC (bus master) signals START and STOP bits signify the beginning and the end of the I²C transfer. The START condition is defined as the SDA signal transitioning from HIGH to LOW while the SCL line is HIGH. The STOP condition is defined as the SDA transitioning from LOW to HIGH while the SCL is HIGH. The SOC acts as the I²C master and always generates the START and STOP bits. The I²C bus is considered to be busy after START condition and free after STOP condition. During data transfer, SOC master can generate repeated START conditions. The START and the repeated START conditions are functionally equivalent.

Data Transfers

Data is transferred in 8 bit bytes by SDA with the MSB transferred first. Each byte of data has to be followed by an acknowledge (ACK) bit. The acknowledged related clock pulse is generated by the master. The acknowledge occurs when the transmitter master releases the SDA line to a high state during the acknowledge clock. The SDA line must be pulled down by the receiver slave during the 9th clock pulse to signify acknowledgment. A receiver slave which has been addressed must generate an acknowledgement ("ACK") after each byte has been received. After the START condition, the SOC (I^2C) master sends a chip address. The standard I^2C address is seven bits long. Making the eighth bit a data direction bit (R/W). For the eighth bit (LSB), a "0" indicates a WRITE and a "1" indicates a READ. (For clarification, communications are broken up into 9-bit segments, one byte followed by one bit for acknowledging.) The second byte selects the register to which the data will be written. The third byte contains data to write to the selected register.

When a receiver slave doesn't acknowledge the slave address, the data line must be left HIGH by the slave. The master can then generate a STOP command to abort the transfer. If a slave receiver does acknowledge the slave address but, sometime later in the transfer cannot receive any more data bytes, the master must again abort the transfer. This is indicated by the slave generating the not acknowledge on the first byte to follow.

The slave leaves the data line HIGH and the master generates the STOP command. The data line is also left high by the slave and master after a slave has transmitted a byte of data to the master in a read operation, but this is a not acknowledge that indicates that the data transfer is successful.

I2C Slave Address:

The Slave Address for the LX8237 is 01101110 or 6EH.

Serial Bus Register Definition and Map

Address										
Dec	Hex		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		ID1	DEV[1]	DEV[0]	MID[2]	MID[1]	MID[0]	NID[2]	NID[1]	NID[0]
0	00H	Read-Only	0	1	0	1	1	0	0	1
		ID2	VID[3]	VID[2]	VID[1]	VID[0]	FAB[1]	FAB[0]	SID[1]	SID[0]
1	01H	Read-Only	0	0	0	0	0	1	0	0
		0V9VSEL	N/A	N/A	0V9SEL[5]	0V9SEL[4]	0V9SEL[3]	0V9SEL[2]	0V9SEL[1]	0V9SEL[0]
2	02H	Read/Write	0	0	1	0	0	0	1	0
		3V3VSEL	N/A	N/A	0V9KEY	3V3SEL[4]	3V3SEL[3]	3V3SEL[2]	3V3SEL[1]	3V3SEL[0]
3	03H	Read/Write	0	0	0	1	0	0	1	1
		CONTROL0	P3EN	IMONG	VR33PWM	VR09PWM	DEGLITCH	IMONEN	0V9MONDIS	0V9DIS
4	04H	Read/Write	0	0	0	0	0	0	0	0
		STATUS0	UV12	UV5	UV33	UV09	OT12	OT5	EOTW12	EOTW5
5	05H	Read/Write	0	0	0	0	0	0	0	0
		STATUS1	OC12	OC5	OC33	OC09	P3STATE	N/A	OV12	OV5
6	06H	Read/Write	0	0	0	0	0	0	0	0

ID1: DEV = Device [01]
MID= major ID [011]
NID= minor ID [001]
ID2: VID= Device [0000]:
FAB= Fab [01] : Default FAB value is 01.
SID= VendorID [00]

Device	ID1	ID2
LX8237ILQ-TR	X59[01011001]	X04 [0000 0100]
LX8237ILQ-TR-V2R3	X59[01011001]	X04 [0000 0100]
LX8237ILQ-TR-V3R2	X59[01011001]	X04 [0000 0100]

0V9VSEL: 0V9Sel = VR09 output voltage select

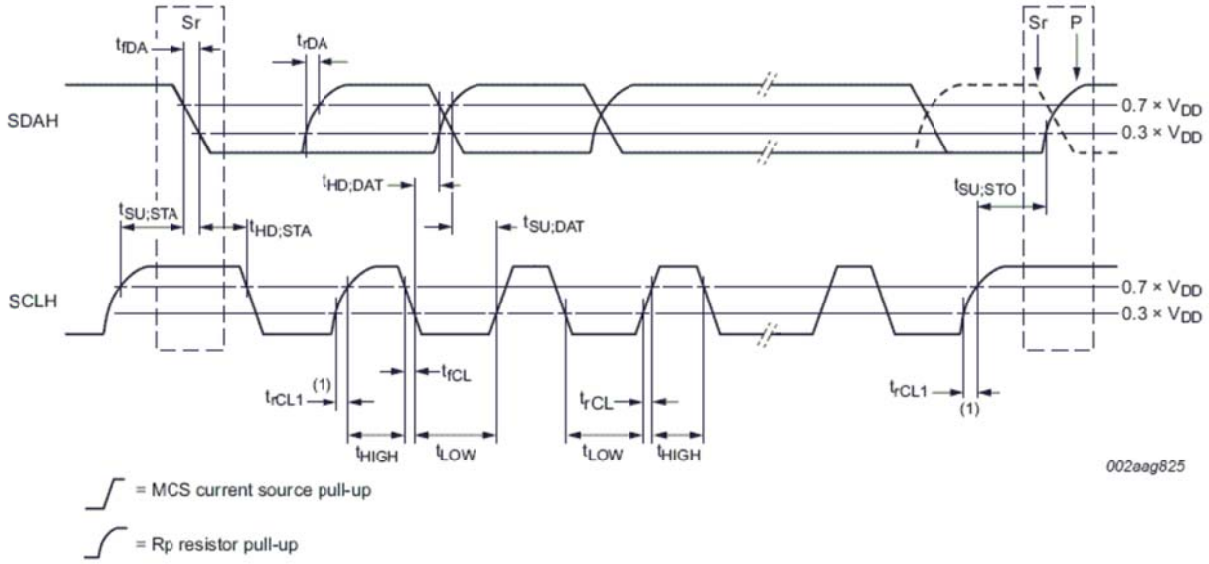
3V3VSEL: 0V9KEY= key to enable 0.94V moniotor & regulator disable.
3V3Sel= VR33 output voltage select

CONTROL0: P3EN= P3 PowerDisable feature enable.
IMONG= Current Monitor Gain
VR33PWM= Force VR33 to operate in PWM mode only
VR09PWM= ForceVR09 to operate in PWM mode only
DEGLITCH= deglitch time selection for Fault/POR detection.
IMONEN= eFuse current monitor Enable.
0V9MONDIS= VR09 regulator monitoring Disable (OFF).
0V9DIS= VR09 regulator Disable (OFF).

STATUS0: UV12 = 12V input voltage under voltage
UV5= 5V input voltage under voltage
UV33= VR33 output voltage under voltage.
UV09= VR09 output voltage under voltage.
OT12= eFuse12 over temperature
OT5= eFuse5 over temperature
EOTW12= eFuse12 early temperature warning
EOTW5= eFuse5 early temperature warning

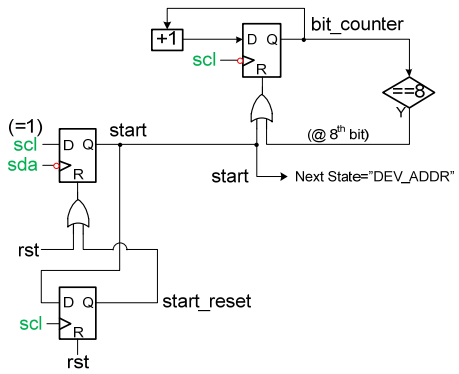
STATUS1:

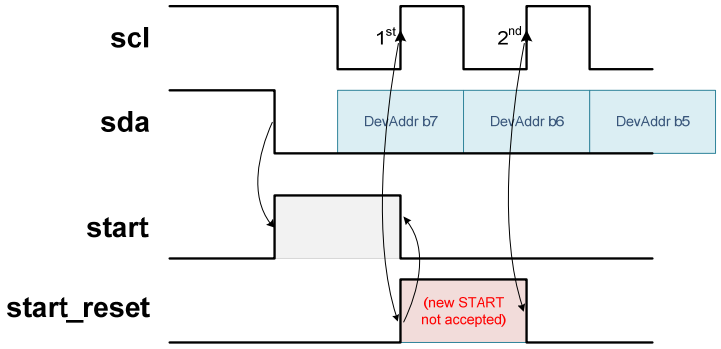
OC12 = eFuse12 over current
OC5 = 3Fuse5 over current
OC33 = VR33 output over current
OC09 = VR09 output over current
P3State = P3 pin state
OV12 = eFuse12 input over voltage
OV5= eFuse5 input over voltage

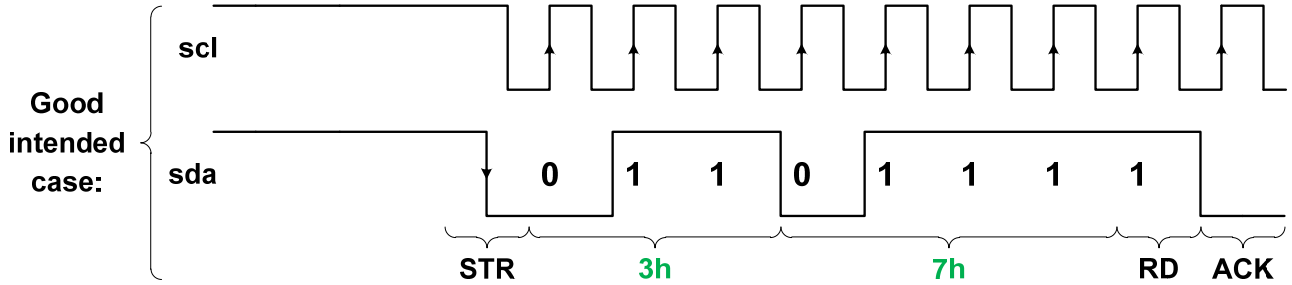


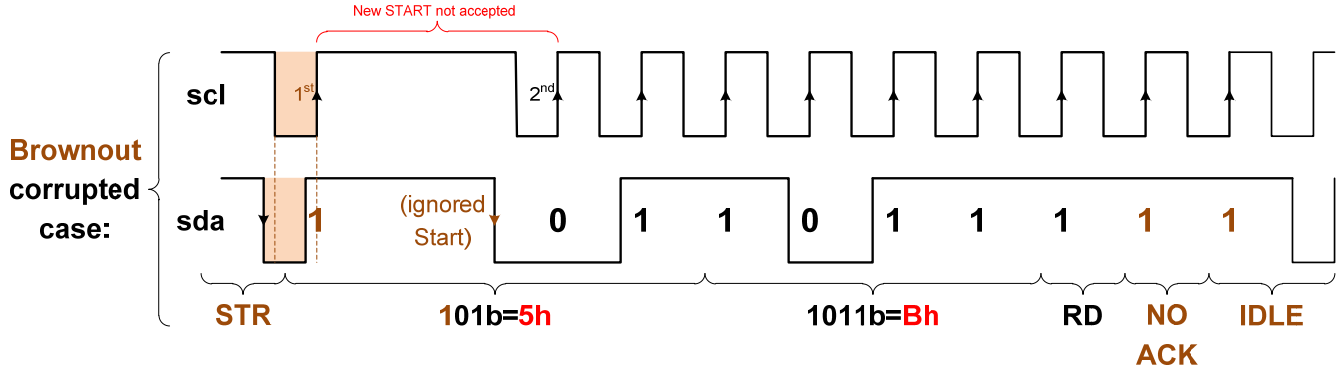
(1) First rising edge of the SCLH signal after Sr and after each acknowledge bit.

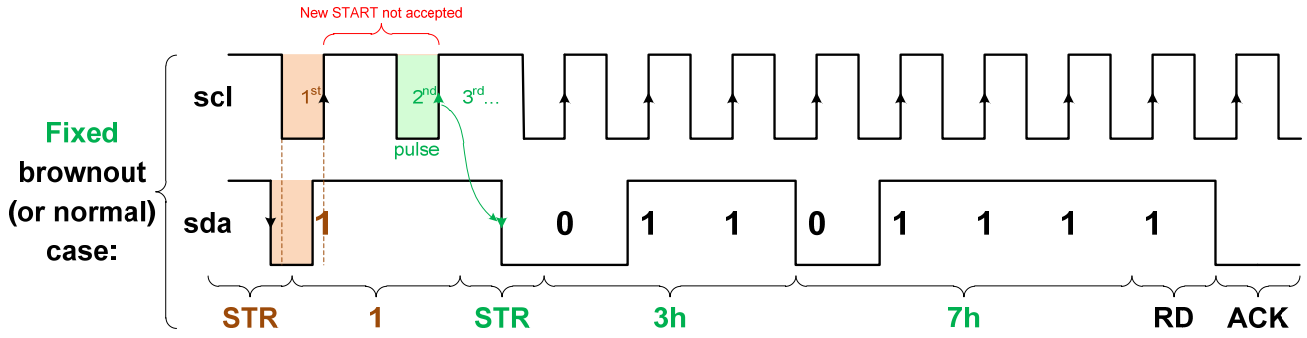
I2C START:



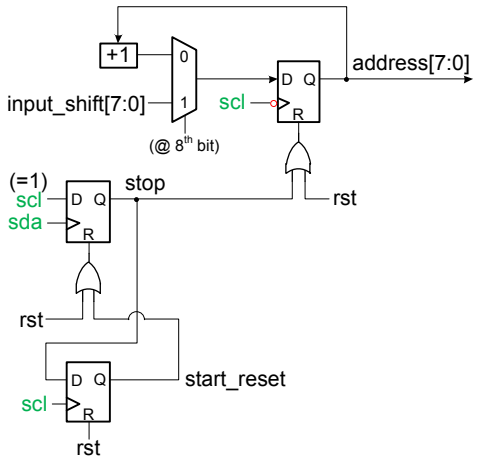


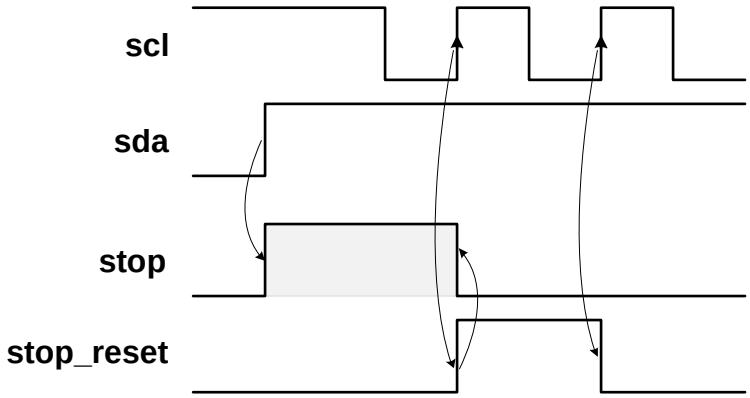






I2C STOP:





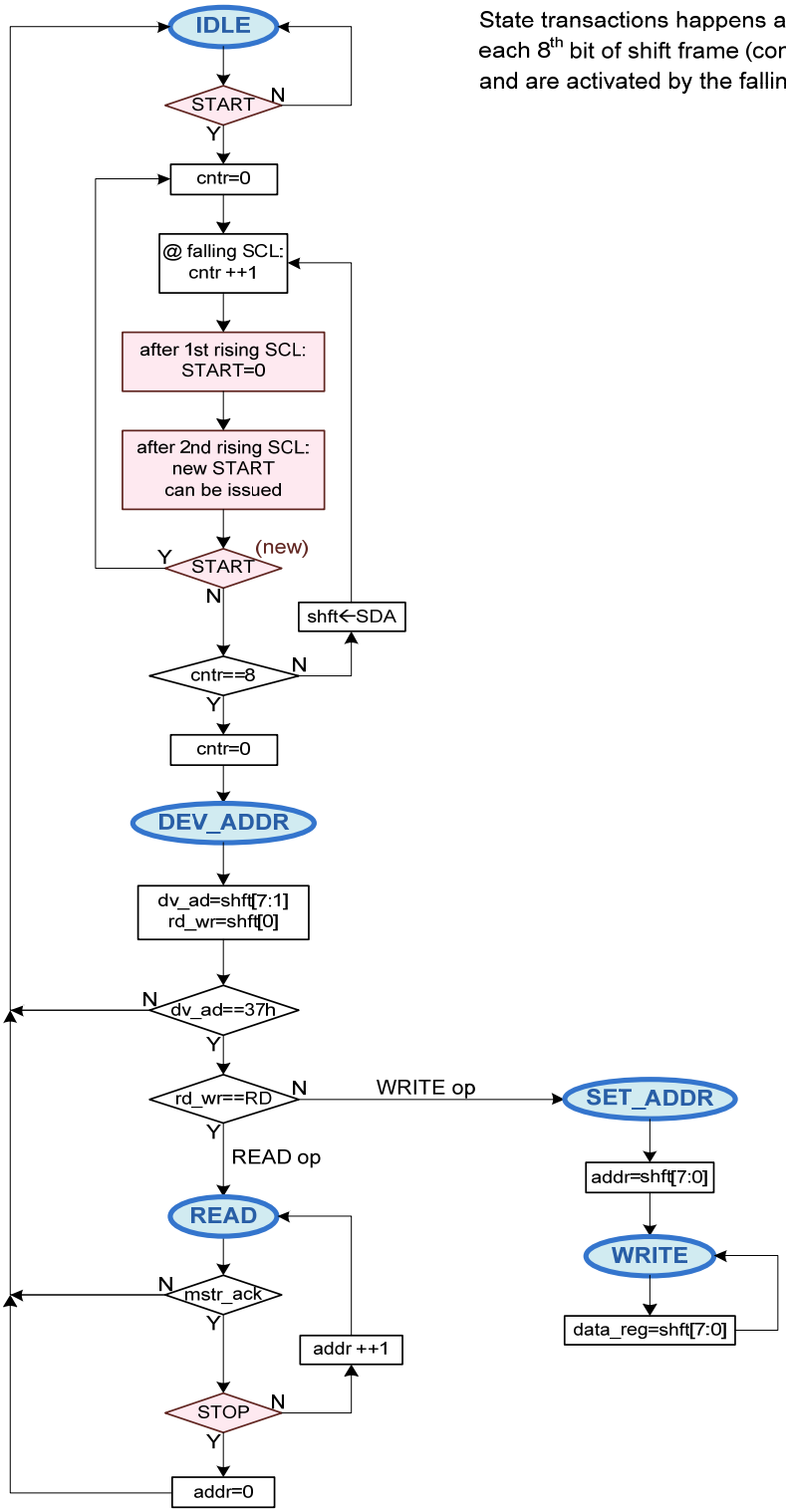
STOP only serves to reset the address pointer. It doesn't reset the I2C circuit since once STOP is issued, I2C gives up the request for SDA line, and does nothing. It may remain in IDLE state for a long period of time.

It's the role of the START signal that resets I2C circuit for a fresh start and kick start the circuit for all the transactions.

It is also the START signal that will clean up and re-sync the communication in case channel is disrupted by noise and/or brownout, etc. The only requirement is a two clock pulses of SCL while maintain SDA high which leading the START. This guarantees the removal of start_reset signal, and a new START will take effect.

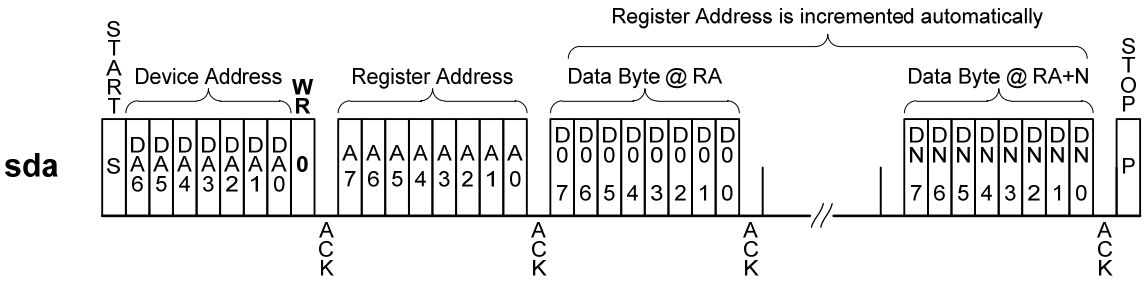
The key components of the double clock pulses are those two rising edges that clears a way for brand new START signal to be accepted by the I2C circuit, as can be seen from the I2C START circuit diagram.

I2C State Machine

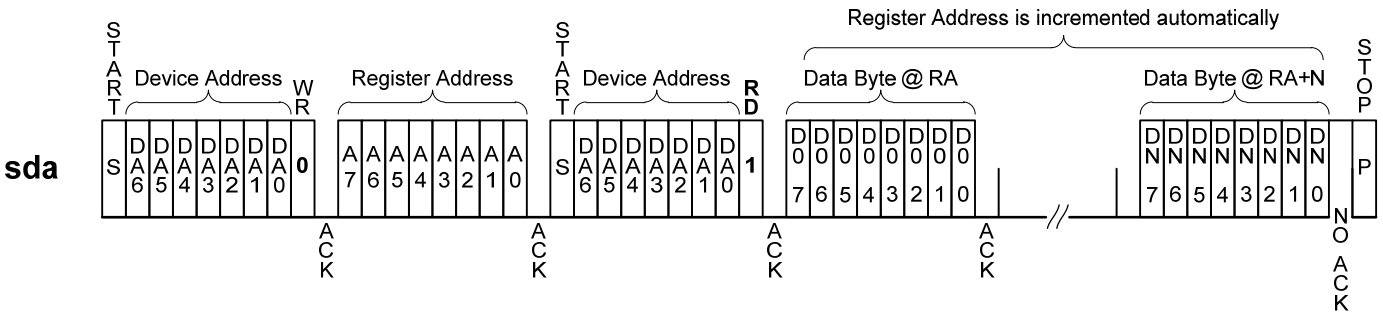


State transactions happens at the completion of each 8th bit of shift frame (condition permitted) and are activated by the falling edges of SCL.

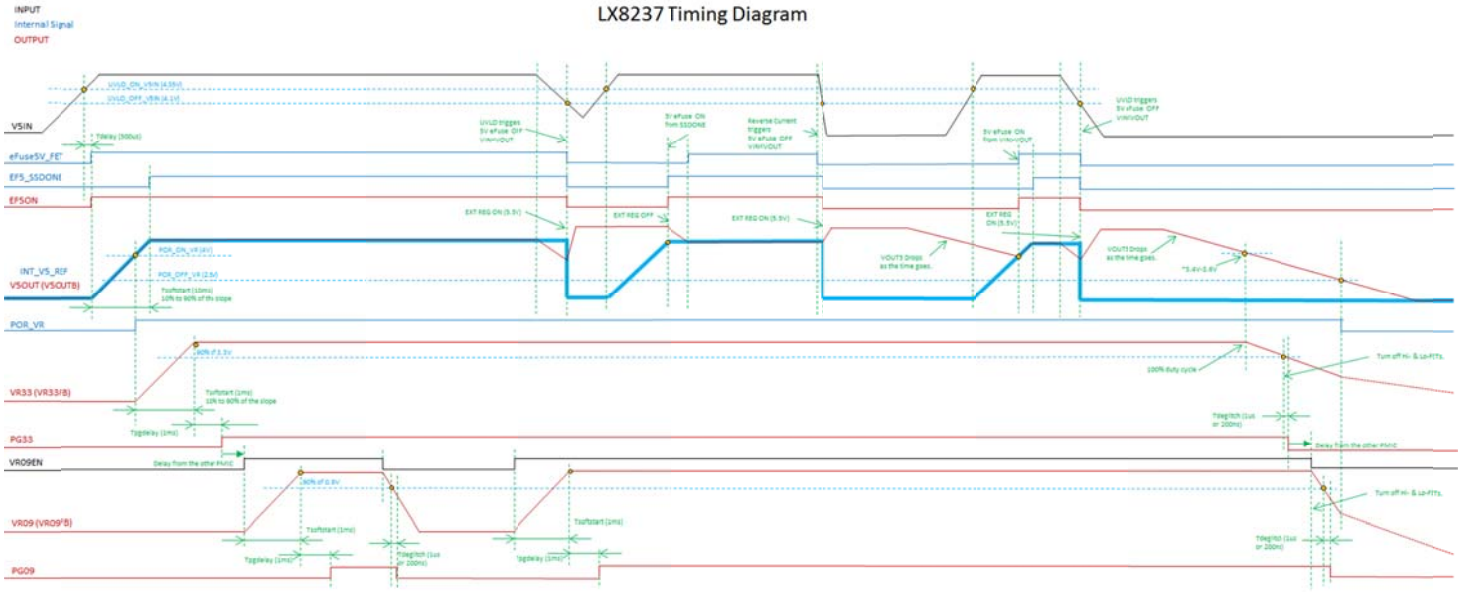
1. Page WRITE (writing multiple bytes)



2. Sequential READ (reading multiple bytes)



Power On and Off Sequence



The Yosemite chip is powered from either the VCC5 input or Vout5 depending on its mode of operation. On startup, eFuse12 will wait for VCC5 to come up before it can close. As long as VCC5 input is present, eFuse12 will close and open with VCC12 input above or below its EF12 close/open threshold. If VCC5in input fails, eFuse12 will open in addition to eFuse5 being open from loss of 5V input.
However, eFuse5 can start up only with VCC5 input present.
The Power on sequence for the system is as follows:

1. VCC5 power up and goes above the required operating voltage for the system.
2. The eFuse5 starts ramping its output.
3. Upon 5Vout crossing the regulator minimum operating voltage for turn ON, the VR33 starts up.
4. After VR33 output crosses PG detection threshold, VR33PG signal goes to logic1 1ms after the last time that VR33 is above its target have stabilized.
5. VR09 starts up after VR09EN pin is at logic1 state
6. VR09 output crosses VR09PGth and outputs V09PG signal to logic1 1ms after the last time VR09 output is above its target.
7. Efuse12 starts to ramp AFTER both VCC5 AND VCC12 are good. If either input fails, its respective EF5/EF12 is open.

Reverse Current Control of 5V eFuse

The simplest protection against to the reverse current is a diode in series connection to the load. However, the power loss is significant at the forward current mode. At the worst, the supply rail of the load is not regulated. In order to solve this problem, the body gating technique is implemented for LX8237. The basic concept on this method is to detect the polarity of voltage drop through the pass N-type FET. Once the negative voltage drop is detected, an active switch connects the body of the pass FET from the source to drain. It generates the opposite polarity of body diode to block the reverse current.

Microsemi's approach to protect the discharging from the output capacitor is to utilize the combination of two methods. One method is to detect the voltage drop over the Rdson of an eFuse FET. The othere is to use the accurate input UVLO circuit.

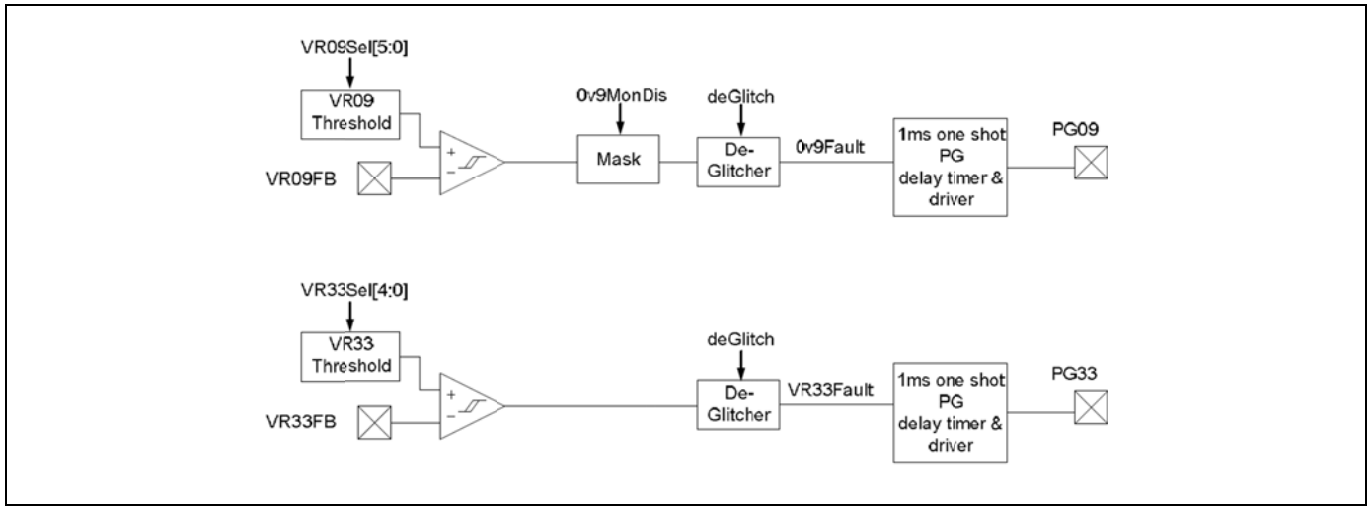
The Rdson sensing is responsible for the high dv/dt input drop like crawbar response (max -5V/µs). 33mV threshold is assigned to detect the reverse voltage from VCC to VOUT through 50mΩ. It represents 660mA reverse current to discharge the output capacitor through eFuse. Any reverse current higher than 660mA by the high dv/dt will be shut off by Rdson sensing circuit.

The slow dv/dt input won't be detected by Rdson sensing circuit since the reverse current is lower than 660mA. The input with slow dv/dt will rely on UVLO detection. Once V5IN goes lower than the UVLO threshold, UVLO circuit will open an eFuse. It requires the accurate threshold(<5%) and fast response time(<2µs).

Power Monitor Functions

The power monitor function has separate functions for each block.

The VR33/VR09 monitor monitors the 3v3/0v9 regulator ouputs respectively and drives PG pin low when either output is 10% below the targeted voltage setting. Upon activation when the input is below the threshold, the power monitor will drive the PG pin to logic0 immediately. Upon deactivation when either of the monitored outputs is above their respective PG thresholds, a 1ms one-shot delay timer is triggered and upon timer timeout, PG is allowed to go to logic1 state..



SINTn Control

The SINTn pin will set to logic0 whenever any on the fault is set in the fault registers. This include the change of state for the P3 pin. Whenever a fault status bit is set, the SINTn output is logic0 until all the faults are cleared by FW by writing to the status register.

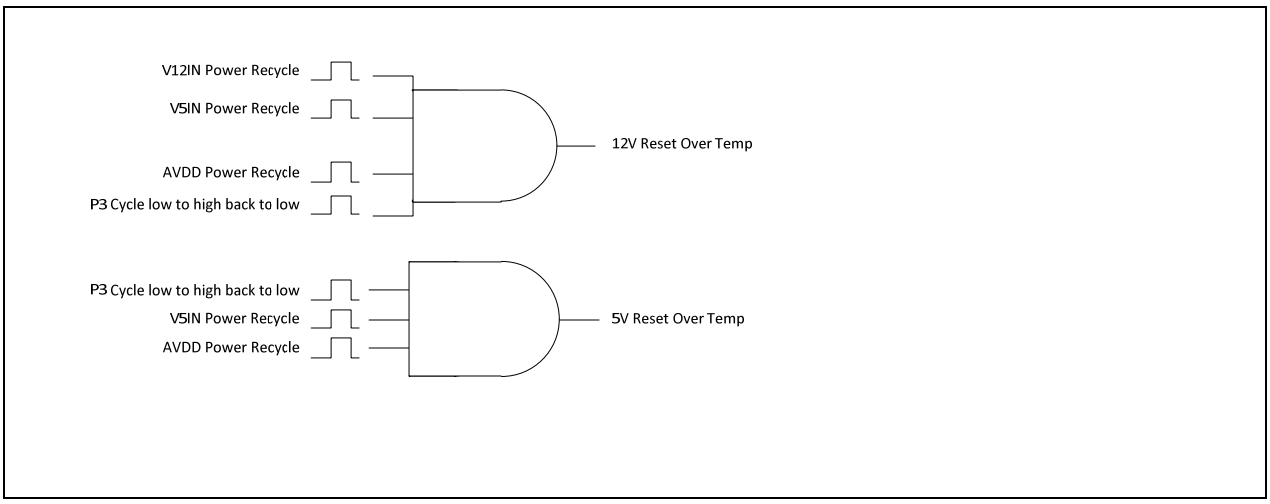
Temperature Monitoring

The chip has on die temperature sensor for thermal protection as well as system warning of impending over temperature. Upon hitting the EOTW threshold, the chip will set the EOTW bit and pull the SINTn pin low to alert the processor. If the temperature continues to rise above the OT threshold, the chip will shut the block that causes the OT off to allow for cool down. Other blocks will remain in its previous state.

Thermal Protection

If the 12V efuse hits 175degC, that efuse will be latched off. It will remain latched off until (V12IN is cycled high to low and back) OR (P3 is cycled low to high and back) OR (V5IN is cycled high to low and back) OR (AVDD somehow cycles high to low and back).

If the 5V efuse hits 175°C, that efuse as well as the 0.9V switching regulator and the 3.3V switching regulator will be latched off. They will remain latched off until (V5IN is cycled high to low and back) OR (P3 is cycled low to high and back) OR (AVDD somehow cycles high to low and back).

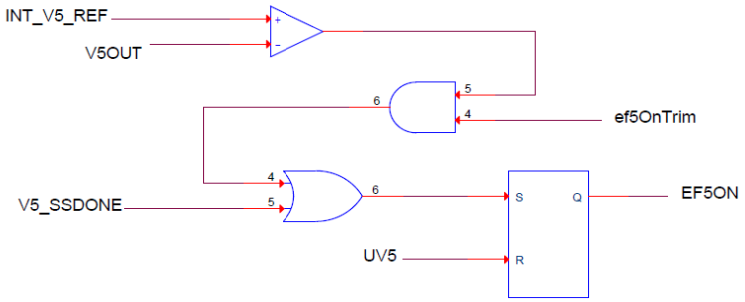


EF5ON Control

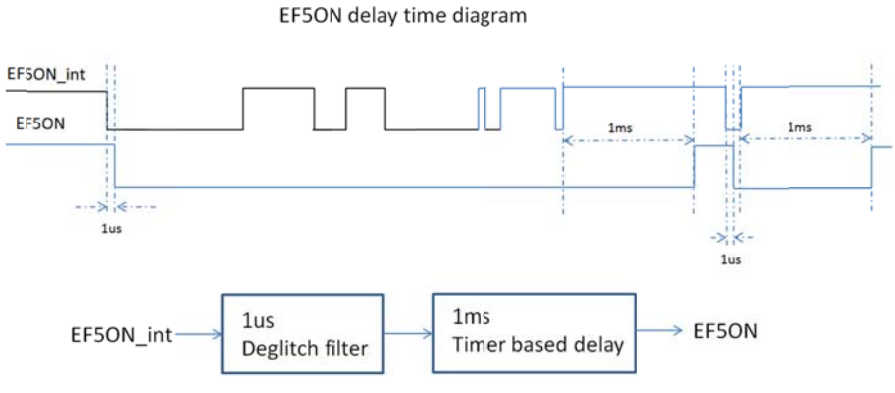
V5OUTB is regulated by an external linear regulator (PMOS pass transistor) when the system in the backup mode. The external regulator shouldn't try to regulate V5OUTB when 5V eFuse is on. For such case, the switch regulator to the V5IN will directly connected to the external linear regulator for V5OUTB. EF5ON signal is used to turn on/off the external linear regulator.

The external regulator won't be turned on unless VR33 soft start done signal is high. Also it shouldn't be turned on in the case 12VOUT is already settled but 5VIN comes later.

EF5ON has 1ms deglitch one shot delay filter to prevent fast transient from toggling the EF5ON.



Modified EF5ON Control Logic



P3 PowerDisable Control

The PowerDisable feature is HW configurable to be allow FW control or not depending on the state of the P3FW pin. of state for the P3 pin. Whenever a fault status bit is set, the SINTn output is logic0 until all the faults are cleared by FW by writing to the status register. When P3FW bit is at logic1 state, FW can enable P3 to control the eFuses.

P3FW	P3EN	P3	12V 5V eFuses
0	0	0	Close
0	0	1	Open
0	1	0	Close
0	1	1	Open
1	0	0	Close
1	0	1	close
1	1	0	close
1	1	1	Open

Fault Condition Management

Signals (which are latched)	Condition / Comment	PG09	PG33	SINTn pin	5V eFuse	12V eFuse	0.94V SR	3.3V SR	Status Bit Set
V12IN under voltage	This fault asserts when the falling V12IN crosses the falling threshold of UVLO of V12IN.	H	H	H => L	Closed	Open	Enable	Enable	UV12
V5IN under voltage	This fault asserts when the falling V5IN crosses the falling threshold of UVLO of V5IN.	H	H	H => L	Open	Closed	Enable	Enable	UV5
V12IN over voltage	This fault asserts when V12OUT clamping occurs.	H	H	H => L	Closed	Closed (V12OUT Clamp)	Enable	Enable	OV12
V5IN over voltage	This fault asserts when V5OUT clamping occurs.	H	H	H => L	Closed (V5OUT Clamp)	Closed	Enable	Enable	OV5
V12OUT Over Current (delay filter ~1.024ms)	This fault asserts when current limit occurs at 12V eFuse FET.	H	H	H => L	Closed	Enable (I12OUT Limit)	Enable	Enable	OC12
V5OUT Over Current (delay filter ~1.024ms)	This fault asserts when current limit occurs at 5V eFuse FET.	H	H	H => L	Enable (I5OUT Limit)	Closed	Enable	Enable	OC5
0.9V Reg under voltage	This fault asserts when V09OUT is lower than 90% of the target voltage.	H => L	H	H => L	Closed	Closed	Enable (Recovery)	Enable	UV09
3.3V Reg under voltage	This fault asserts when V33OUT is lower than 90% of the target voltage.	H	H =>L	H => L	Closed	Closed	Enable	Enable (Recovery)	UV33
0.9V Reg Output Short	This fault VR09OUT is lower than 70% and current limit occurs.	H => L	H	H => L	Closed	Closed	Enable (Hiccup)	Enable	UV09
3.3V Reg Output Short	This fault VR33OUT is lower than 70% and current limit occurs.	H	H => L	H => L	Closed	Closed	Enable	Enable (Hiccup)	UV33
0.9V Reg Over current	This fault asserts when the measure current peak hits the current limit. This fault pulls SINTn low but allow the other fault condition to write the fault register	H	H	H => L	Closed	Closed	Enable (Iout Limit)	Enable	0V90C

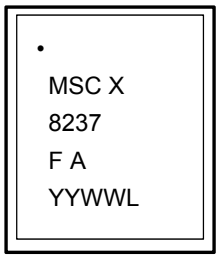
(delay ~32us)	instead of locking up the register not to allow since this fault often occurs at the transient.								
3.3V Reg Over current (delay ~32µs)	This fault asserts when the measure current peak hits the current limit. This fault pulls SINTn low but allow the other fault condition to write the fault register instead of locking up the register not to allow since this fault often occurs at the transient	H	H	H => L	Closed	Closed	Enable	Enable (Iout Limit)	3V3OC
5V Early Over Temperature Warning (delay ~32µs)	This fault asserts when 5V eFuse temperature cross the EOTW threshold.	H	H	H => L	Closed	Closed	Enable	Enable	EOTW 5
12V Early Over Temperature Warning (delay ~32µs)	This fault asserts when 12V eFuse temperature cross the EOTW threshold.	H	H	H => L	Closed	Closed	Enable	Enable	EOTW 12
5V Over Temperature	This fault asserts when temperature cross the OT threshold.	H	H	H => L	Open	Closed	Enable	Enable	OT5
12V Over Temperature	This fault asserts when temperature cross the OT threshold	H	H	H => L	Closed	Open	Enable	Enable	OT12
V5OUTB Under Voltage		-	-	H => L	Open	Open	Disable	Disable	-
VR09EN input voltage low		-	-	H	Closed	Closed	Disable	Enable	-
P3 Pin Logic 1 (feature enabled)		-	-	H => L	Open	Open	-	-	P3STATE

I²C SCL and SDA pin requirements

Ideal Specification:

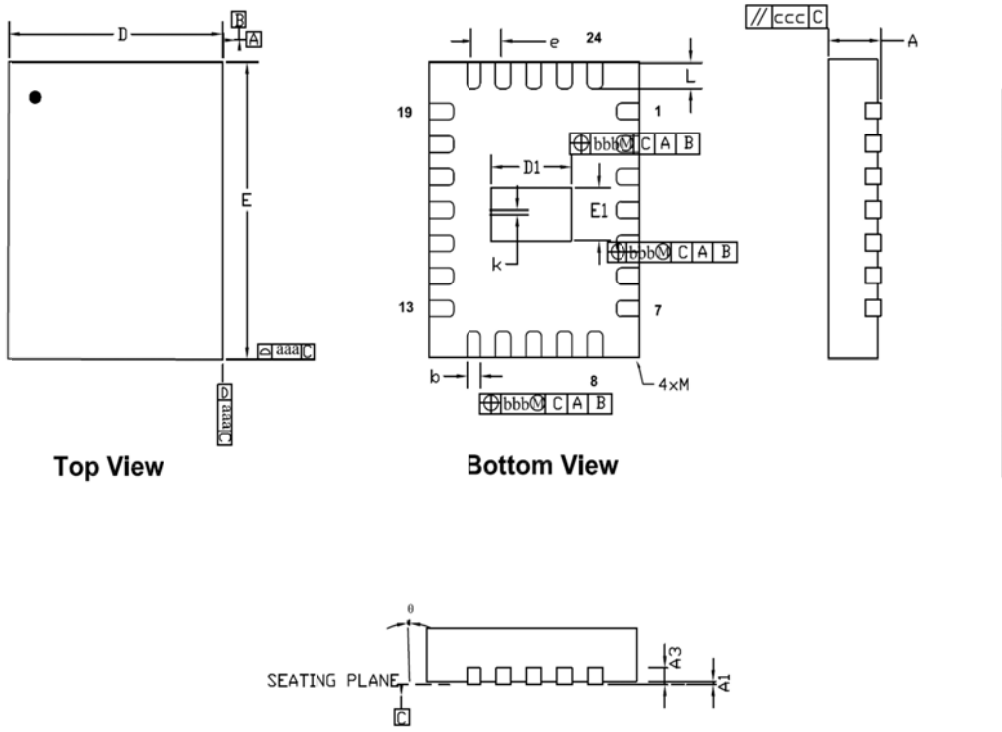
The power supply for the external pull up resistors attached to the SCL and SDA pins is assumed to be at 1.8 us, but the sequencing relative to the internal digital block power supply can occur at any time before or during startup or power down or any time in between. If the power supply drops below 1.8v logic level thresholds tolerance value (-10%), then I²C communication can be interrupted. The default register value loading of all I²C registers (customer and test) should be independent on the SCL/SDA state since this is not known.

Package Marking Description



Device Marking	Description
•	Pin 1 Indicator
MSC	Microsemi Corporation
X	For production parts, X=" P" . All other values of X represent pre-production parts.
8237	Supplier Part Number
F	Wafer Fab Location
A	Assembly Location
YY	Year
WW	Work Week
L	Lot Trace Code

Package Outline Dimensions



SYMBOLS	DIMENSIONS IN MILLIMETERS		
	MIN	NOM	MAX
A	0.80	0.90	1.00
A1	0	0.02	0.05
A3	—	0.203REF.	—
b	0.18	0.25	0.30
D	3.35	3.50	3.65
D1	1.25	1.30	1.35
E	4.35	4.50	4.65
E1	0.75	0.80	0.85
k	—	0.065BSC	—
e	—	0.50BSC	—
L	0.30	0.40	0.50
θ	0	—	12
aaa	—	0.25	—
bbb	—	0.10	—
ccc	—	0.10	—
M	—	—	0.05

Figure 4 · **24-Pin QFN Package Dimensions**

Land Pattern Recommendation

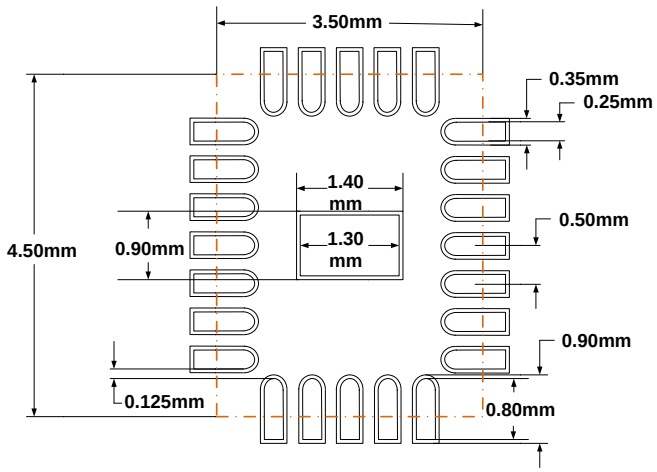


Figure 5 · **24-Pin QFN Package Land Pattern**

Disclaimer:
This PCB land pattern recommendation is based on information available to Microsemi by its suppliers. The actual land pattern to be used could be different depending on the materials and processes used in the PCB assembly, end user must account for this in their final layout. Microsemi makes no warranty or representation of performance based on this recommended land patter

Revision	Date	Comment
Rev 1.4d	23 May	- Adjusted the Fab to 01 from 00 - Added the LX8237ILQ-TR-V3R1 part number -
Rev 1.4e	1 June 2016	- Added the LX8237ILQ-TR-V3R2 part number - Defined ID2 = x04 - Cleaned up Register definitions
Rev 1.4f	6 June 2016	- Removed some text next to MID
Rev 1.4g	31 Agust 2016	- updated with the three final part numbers described LX8237ILQ-TR LX8237ILQ-TR-V2R3 LX8237ILQ-TR-V3R2 - Updated the part numbers in the Device ID table on page 19 accordingly