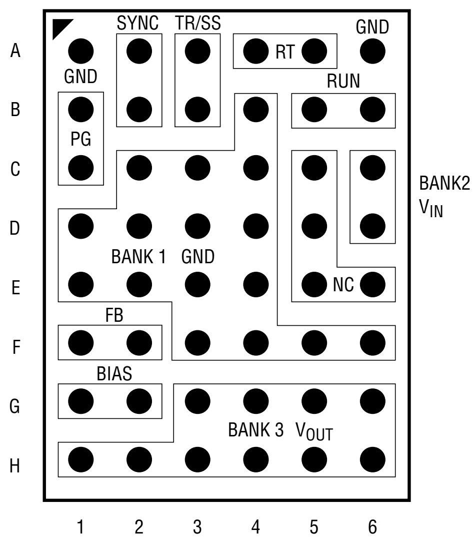
ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

V_{IN}, RUN, PG Voltage 42V
V_{OUT}, BIAS Voltage 19V
FB, TR/SS Voltage 4V
SYNC Voltage 6V
Maximum Internal Temperature (I-Grade) .... 125°C
Maximum Internal Temperature (H-Grade) .... 150°C
Storage Temperature (I-Grade) .... 125°C
Storage Temperature (H-Grade) .... –50°C to 150°C
Peak Reflow Solder Body Temperature .... 250°C

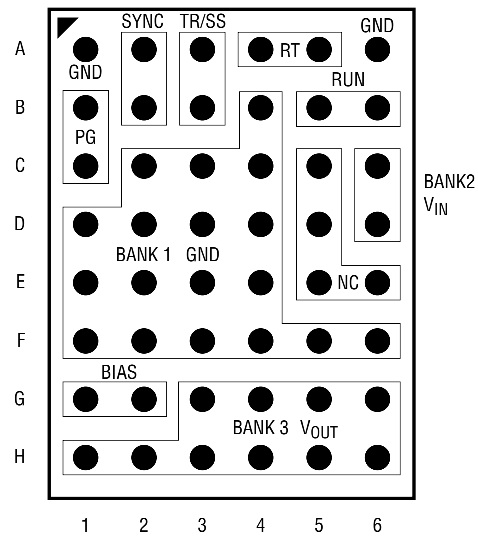
PIN CONFIGURATION

TOP VIEW
ADJUSTABLE VERSION



BGA PACKAGE
48-LEAD (9mm × 6.25mm × 3.32mm) BGA PACKAGE
T_{JMAX} = 150°C, θ_{JA} = 24.7°C/W, $\theta_{JCbottom}$ = 4.5°C/W
θ_{JCtop} = 22.3°C/W, θ_{JB} = 4.2°C/W, WEIGHT = 0.5g
θ VALUES DETERMINED PER JEDEC51-9, 51-12

TOP VIEW
FIXED OUTPUT VERSION



BGA PACKAGE
48-LEAD (9mm × 6.25mm × 3.32mm) BGA PACKAGE
T_{JMAX} = 150°C, θ_{JA} = 24.7°C/W, $\theta_{JCbottom}$ = 4.5°C/W
θ_{JCtop} = 22.3°C/W, θ_{JB} = 4.2°C/W, WEIGHT = 0.5g
θ VALUES DETERMINED PER JEDEC51-9, 51-12

ORDER INFORMATION

PART NUMBER	TERMINAL FINISH	PART MARKING*		PACKAGE TYPE	MSL RATING	TEMPERATURE RANGE
		DEVICE	FINISH CODE			
LTM8003IY#PBF	SAC305 (RoHS)	LTM8003	e1	BGA	3	–40°C to 125°C
LTM8003HY#PBF	SAC305 (RoHS)	LTM8003	e1	BGA	3	–40°C to 150°C
LTM8003IY	SnPb (63/37)	LTM8003	e0	BGA	3	–40°C to 125°C
LTM8003HY	SnPb (63/37)	LTM8003	e0	BGA	3	–40°C to 150°C
LTM8003IY-3.3#PBF	SAC305 (RoHS)	LTM8003-3.3	e1	BGA	3	–40°C to 125°C
LTM8003HY-3.3#PBF	SAC305 (RoHS)	LTM8003-3.3	e1	BGA	3	–40°C to 150°C

- Device temperature grade is indicated by a label on the shipping container.
- Pad or ball finish code is per IPC/JEDEC J-STD-609.
- BGA Package and Tray Drawings
- This product is not recommended for second side reflow.
  This product is moisture sensitive. For more information, go to Recommended BGA PCB Assembly and Manufacturing Procedures.

Rev E

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating temperature range, otherwise specifications are at T_J = 25°C. V_{IN} = 12V, RUN = 2V, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Minimum Input Voltage	V_{IN} Rising	●			3.4	V
Output DC Voltage	LTM8003, R_{FB} Open LTM8003, R_{FB} = 5.62kΩ, V_{IN} = 40V LTM8003-3.3			0.97 18 3.3		V
Peak Output DC Current	V_{OUT} = 3.3V, f_{SW} = 1MHz		6			A
Quiescent Current into V_{IN}	RUN = 0V BIAS = 0V, No Load, SYNC = 0V, Not Switching				3 8	µA µA
Quiescent Current into BIAS	BIAS = 5V, RUN = 0V BIAS = 5V, No Load, SYNC = 0V, Not Switching BIAS = 5V, V_{OUT} = 3.3V, I_{OUT} = 3.5A, f_{SW} = 1MHz				1 5 12	µA µA mA
Line Regulation	5.5V < V_{IN} < 36V, I_{OUT} = 1A			0.5		%
Load Regulation	0.1A < I_{OUT} < 3.5A			0.5		%
Output Voltage Ripple	I_{OUT} = 3.5A			10		mV
Switching Frequency	R_T = 232kΩ R_T = 41.2kΩ R_T = 10.7kΩ			200 0.95 3		kHz MHz MHz
Voltage at FB	LTM8003	●	950	970	980	mV
Minimum BIAS Voltage	(Note 5)				3.2	V
RUN Threshold Voltage			0.9		1.06	V
RUN Current					1	µA
TR/SS Current	TR/SS = 0V			2		µA
TR/SS Pull Down	TR/SS = 0.1V			200		Ω
PG Threshold Voltage at FB (Upper)	FB Falling (Note 6, LTM8003)			1.05		V
PG Threshold Voltage at FB (Lower)	FB Rising (Note 6, LTM8003)			0.89		V
PG Threshold Voltage at V_{OUT} (Upper)	V_{OUT} Falling (Note 6, LTM8003-3.3)			3.57		V
PG Threshold Voltage at V_{OUT} (Lower)	V_{OUT} Rising (Note 6, LTM8003-3.3)			3.03		V
PG Leakage Current	PG = 42V				1	µA
PG Sink Current	PG = 0.1V			150		µA
SYNC Threshold Voltage	Synchronization		0.4		1.5	V
SYNC Voltage	To Enable Spread Spectrum		2.9		4.2	V
SYNC Current	SYNC = 0V				35	µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Unless otherwise noted, the absolute minimum voltage is zero.

Note 3: The LTM8003I is guaranteed to meet specifications over the full –40°C to 125°C internal operating temperature range. The LTM8003H is guaranteed to meet specifications over the full –40°C to 150°C internal operating temperature range. Note that the maximum internal temperature is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance and other environmental factors. High junction temperatures degrade operating lifetimes. Operating lifetime is derated at junction temperatures greater than 125°C.

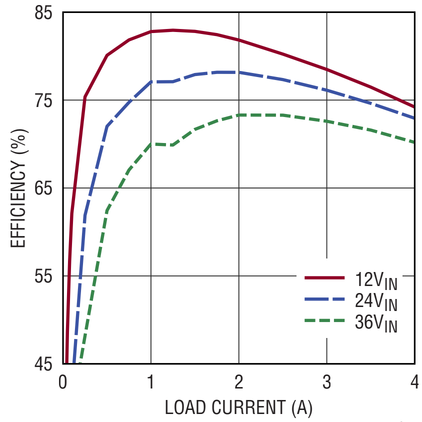
Note 4: The LTM8003 contains overtemperature protection that is intended to protect the device during momentary overload conditions. The internal temperature exceeds the maximum operating junction temperature when the overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

Note 5: Below this specified voltage, internal circuitry will draw power from V_{IN}.

Note 6: PG transitions from low to high.

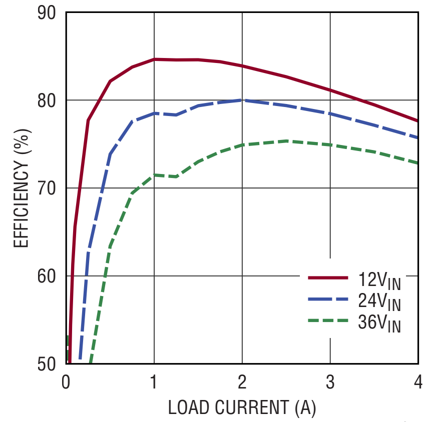
TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

Efficiency vs Load Current, V_{OUT} = 0.97V, BIAS = 5V



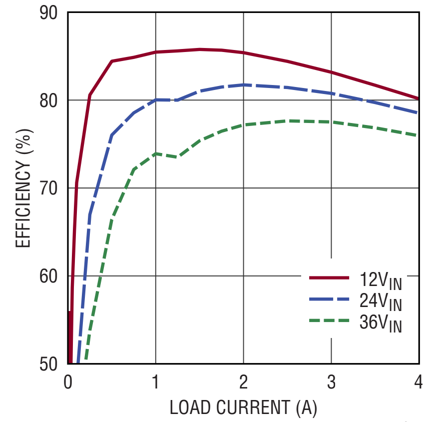
8003 G01

Efficiency vs Load Current, V_{OUT} = 1.2V, BIAS = 5V



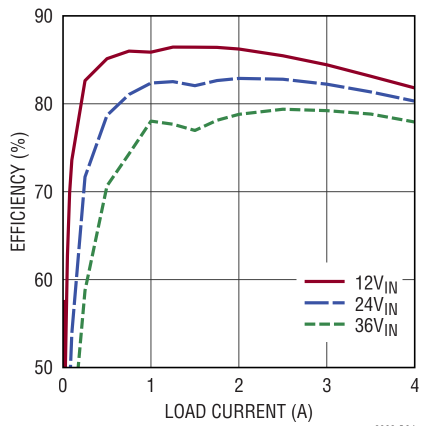
8003 G02

Efficiency vs Load Current, V_{OUT} = 1.5V, BIAS = 5V



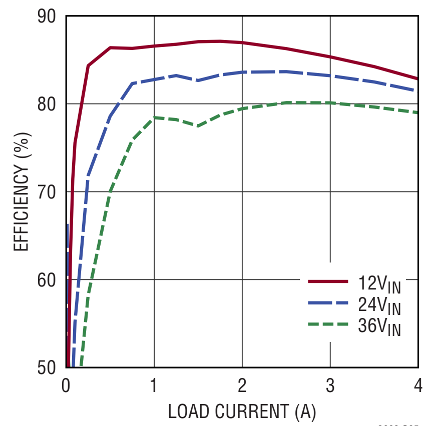
8003 G03

Efficiency vs Load Current, V_{OUT} = 1.8V, BIAS = 5V



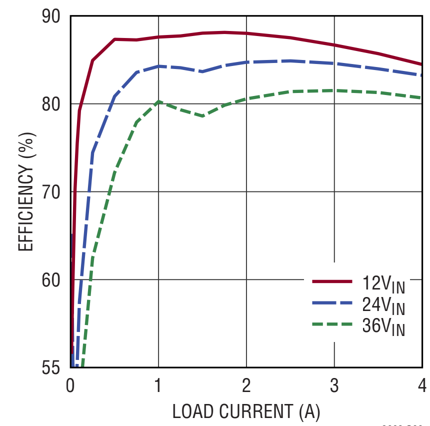
8003 G04

Efficiency vs Load Current, V_{OUT} = 2V, BIAS = 5V



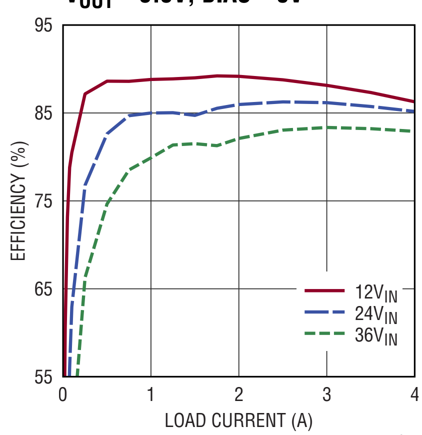
8003 G05

Efficiency vs Load Current, V_{OUT} = 2.5V, BIAS = 5V



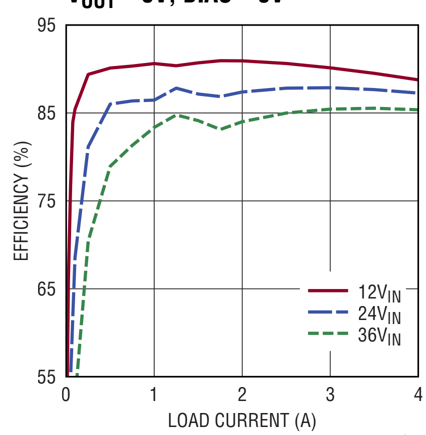
8003 G06

Efficiency vs Load Current, V_{OUT} = 3.3V, BIAS = 5V



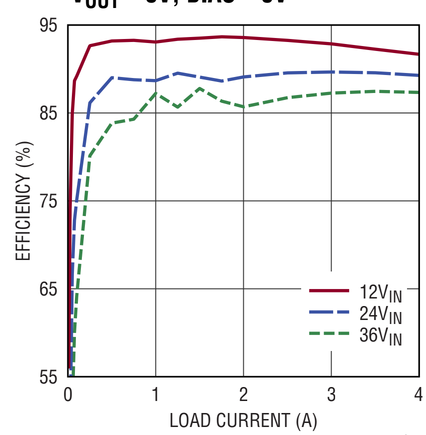
8003 G07

Efficiency vs Load Current, V_{OUT} = 5V, BIAS = 5V



8003 G08

Efficiency vs Load Current, V_{OUT} = 8V, BIAS = 5V

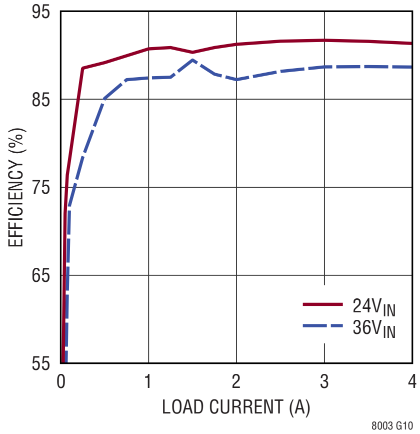


8003 G09

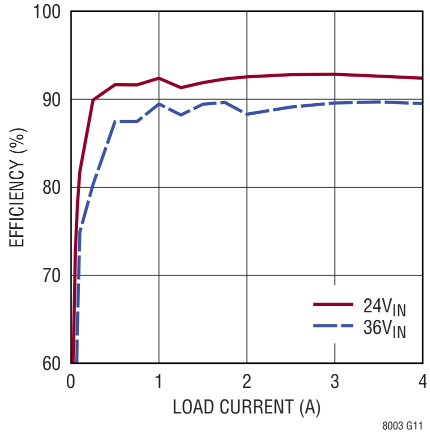
Rev E

TYPICAL PERFORMANCE CHARACTERISTICS $T_A = 25°C$, unless otherwise noted.

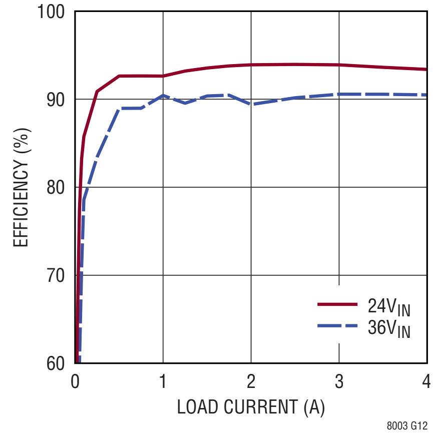
Efficiency vs Load Current, V_{OUT} = 12V, BIAS = 5V



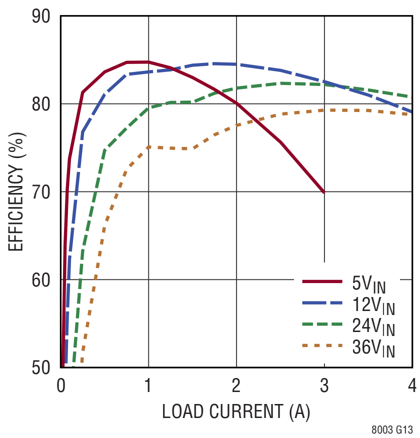
Efficiency vs Load Current, V_{OUT} = 15V, BIAS = 5V



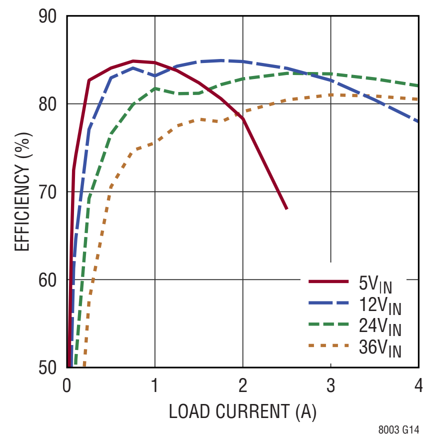
Efficiency vs Load Current, V_{OUT} = 18V, BIAS = 5V



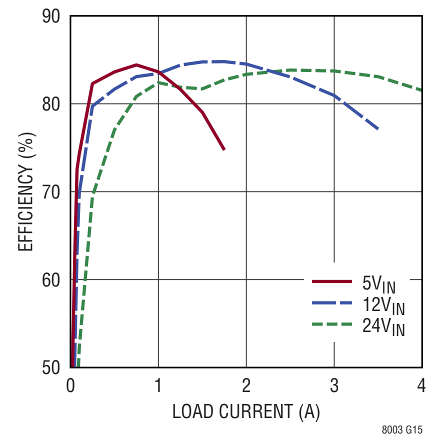
Efficiency vs Load Current, V_{OUT} = –3.3V, BIAS Tied to LTM8003 GND



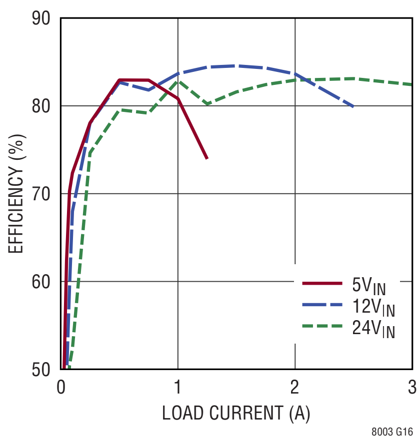
Efficiency vs Load Current, V_{OUT} = –5V, BIAS Tied to LTM8003 GND



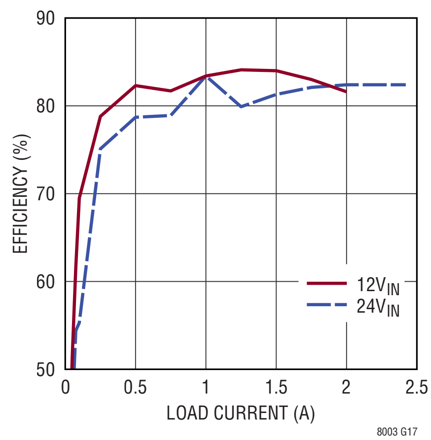
Efficiency vs Load Current, V_{OUT} = –8V, BIAS Tied to LTM8003 GND



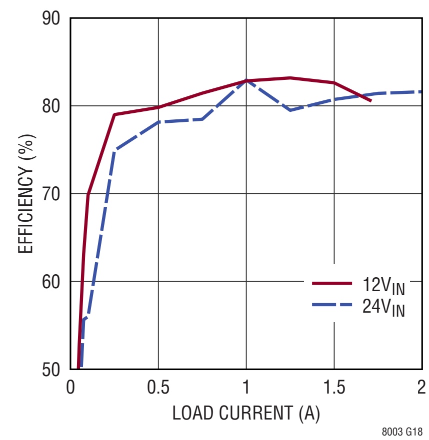
Efficiency vs Load Current, V_{OUT} = –12V, BIAS Tied to LTM8003 GND



Efficiency vs Load Current, V_{OUT} = –15V, BIAS Tied to LTM8003 GND

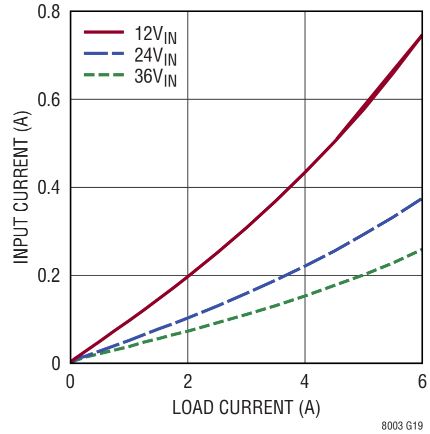


Efficiency vs Load Current, V_{OUT} = –18V, BIAS Tied to LTM8003 GND

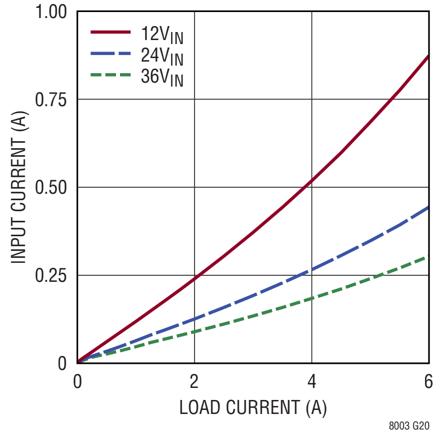


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

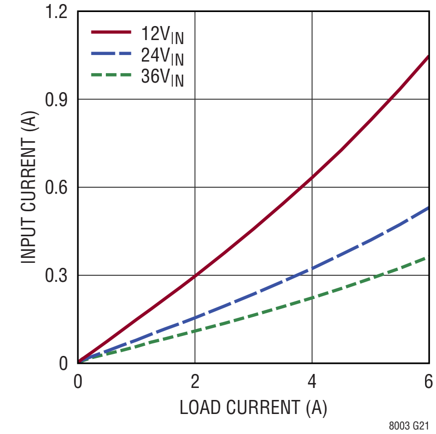
Input vs Load Current V_{OUT} = 0.97V, BIAS = 5V



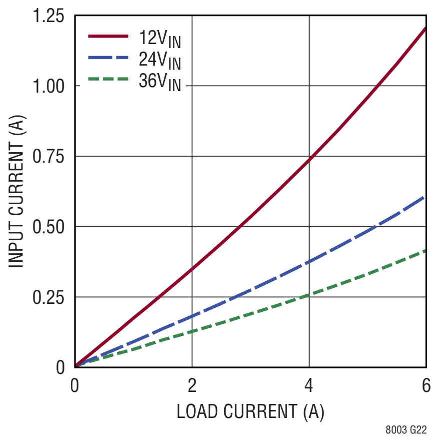
Input vs Load Current V_{OUT} = 1.2V, BIAS = 5V



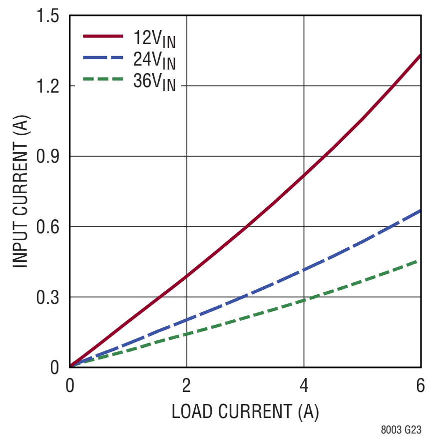
Input vs Load Current V_{OUT} = 1.5V, BIAS = 5V



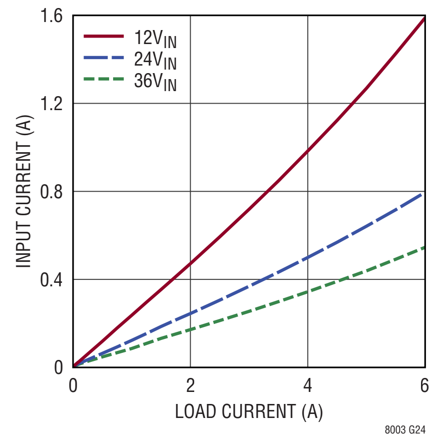
Input vs Load Current V_{OUT} = 1.8V, BIAS = 5V



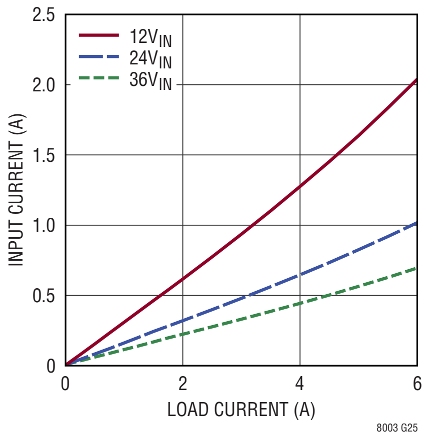
Input vs Load Current V_{OUT} = 2V, BIAS = 5V



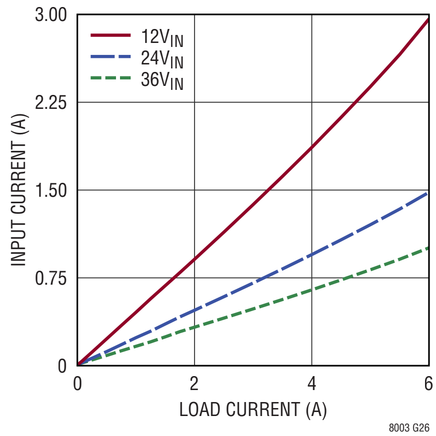
Input vs Load Current V_{OUT} = 2.5V, BIAS = 5V



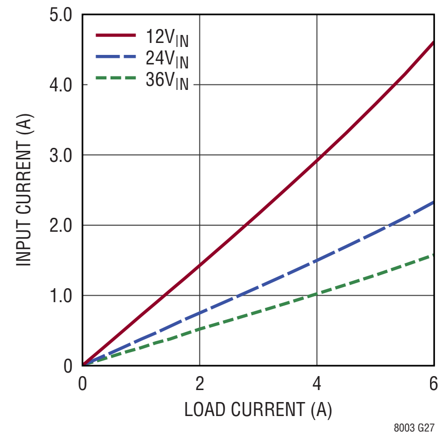
Input vs Load Current V_{OUT} = 3.3V, BIAS = 5V



Input vs Load Current V_{OUT} = 5V, BIAS = 5V

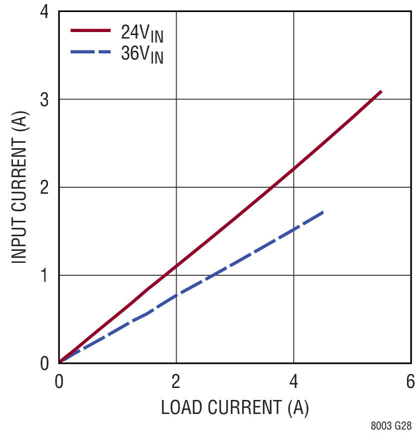


Input vs Load Current V_{OUT} = 8V, BIAS = 5V

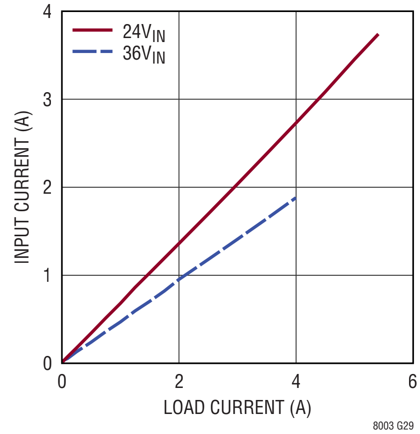


TYPICAL PERFORMANCE CHARACTERISTICS $T_A = 25°C$, unless otherwise noted.

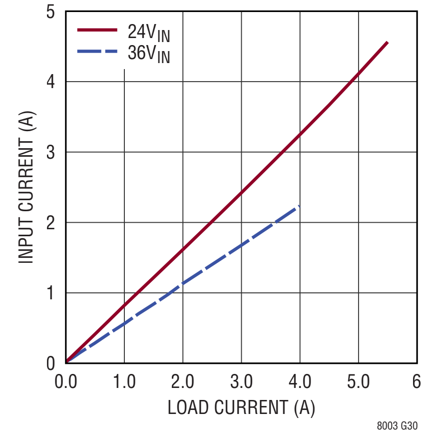
Input vs Load Current
V_{OUT} = 12V, BIAS = 5V



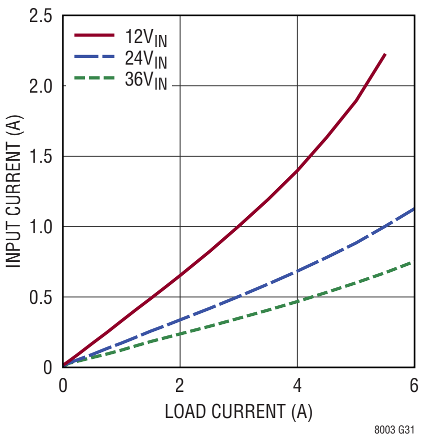
Input vs Load Current
V_{OUT} = 15V, BIAS = 5V



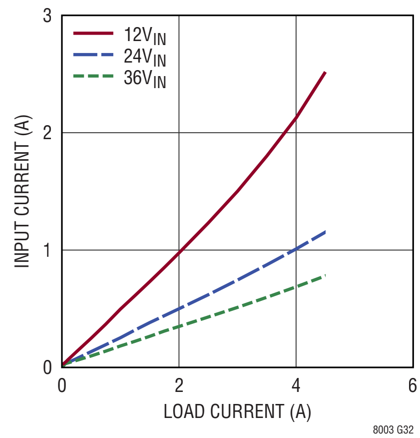
Input vs Load Current
V_{OUT} = 18V, BIAS = 5V



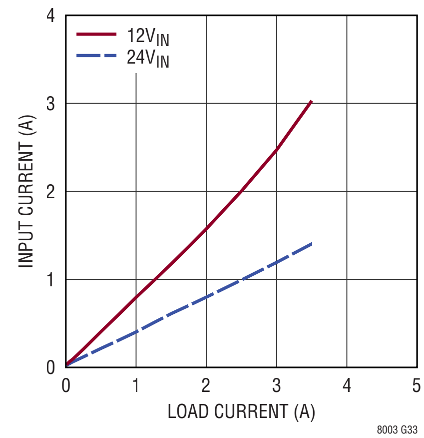
Input vs Load Current
V_{OUT} = –3.3V, BIAS Tied to LTM8003 GND



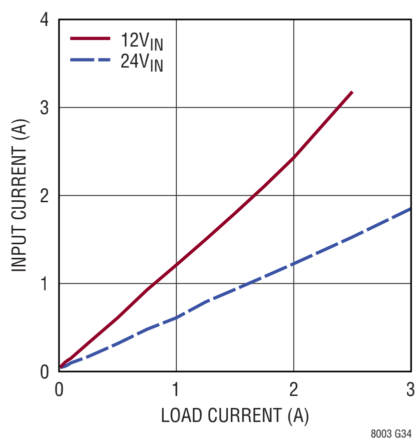
Input vs Load Current
V_{OUT} = –5V, BIAS Tied to LTM8003 GND



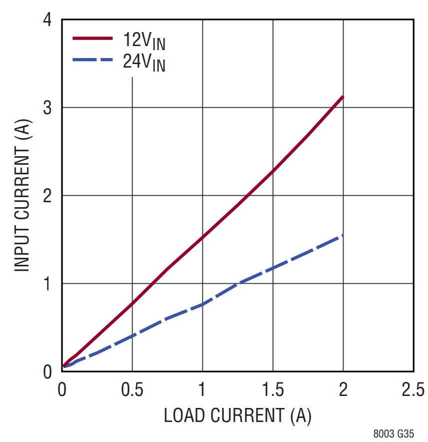
Input vs Load Current
V_{OUT} = –8V, BIAS Tied to LTM8003 GND



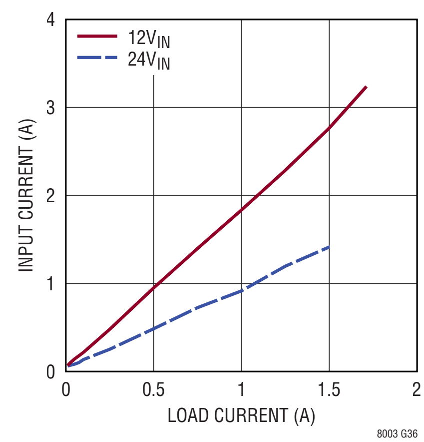
Input vs Load Current
V_{OUT} = –12V, BIAS Tied to LTM8003 GND



Input vs Load Current
V_{OUT} = –15V, BIAS Tied to LTM8003 GND

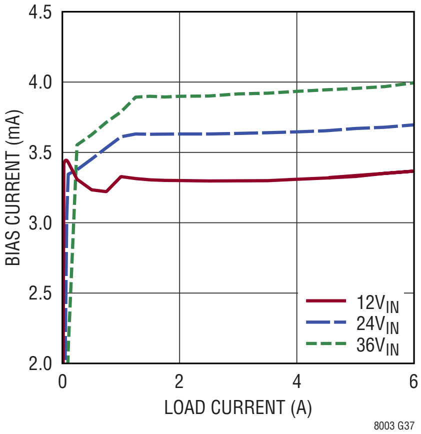


Input vs Load Current
V_{OUT} = –18V, BIAS Tied to LTM8003 GND

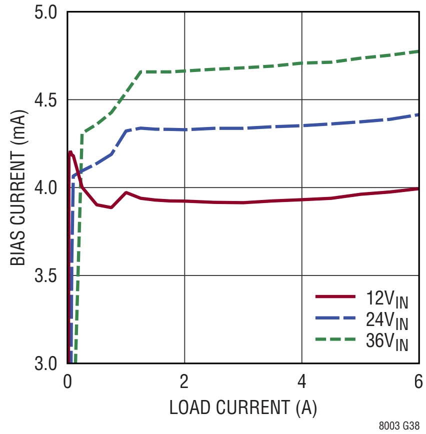


TYPICAL PERFORMANCE CHARACTERISTICS $T_A = 25°C$, unless otherwise noted.

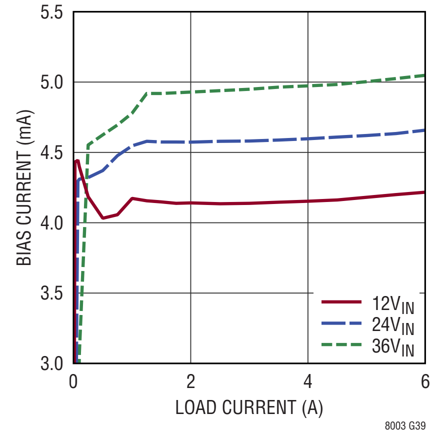
BIAS Current vs Load Current $V_{OUT} = 0.97V$, BIAS = 5V



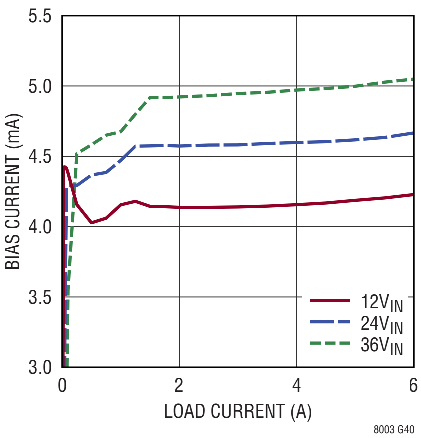
BIAS Current vs Load Current $V_{OUT} = 1.2V$, BIAS = 5V



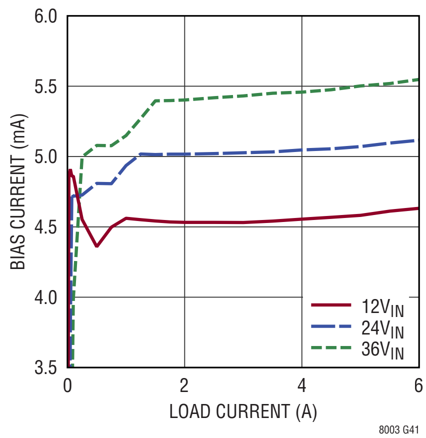
BIAS Current vs Load Current $V_{OUT} = 1.5V$, BIAS = 5V



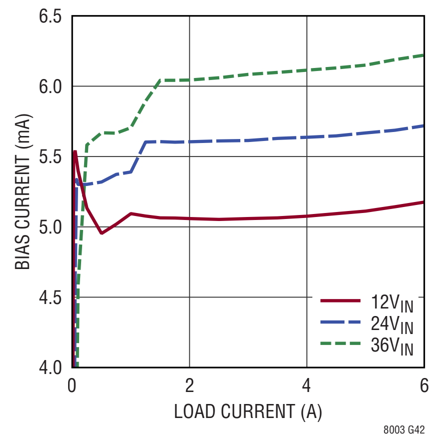
BIAS Current vs Load Current $V_{OUT} = 1.8V$, BIAS = 5V



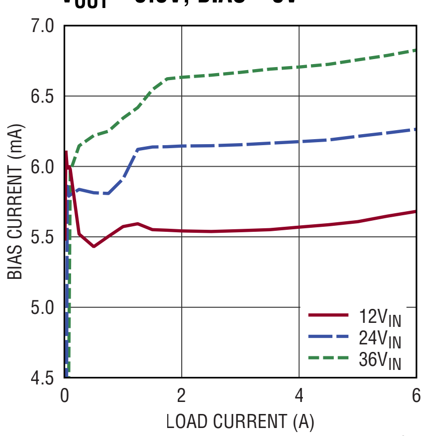
BIAS Current vs Load Current $V_{OUT} = 2V$, BIAS = 5V



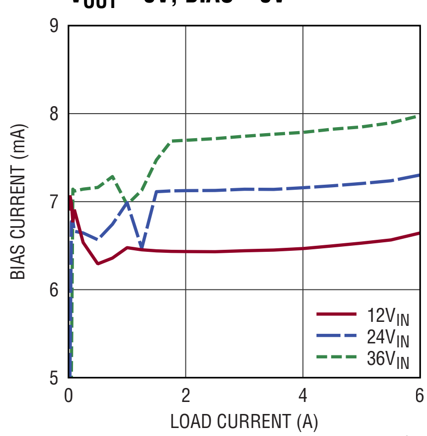
BIAS Current vs Load Current $V_{OUT} = 2.5V$, BIAS = 5V



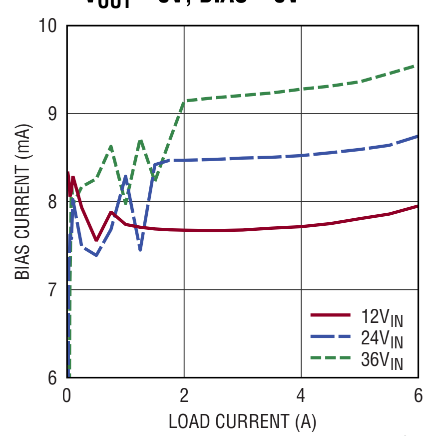
BIAS Current vs Load Current $V_{OUT} = 3.3V$, BIAS = 5V



BIAS Current vs Load Current $V_{OUT} = 5V$, BIAS = 5V

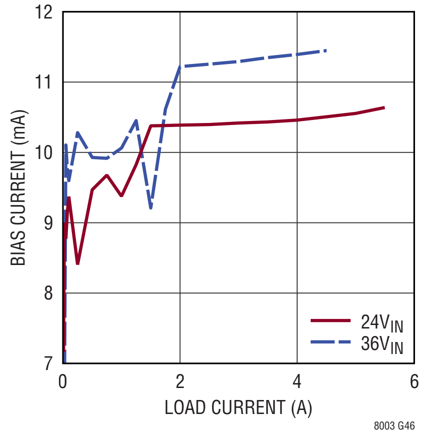


BIAS Current vs Load Current $V_{OUT} = 8V$, BIAS = 5V

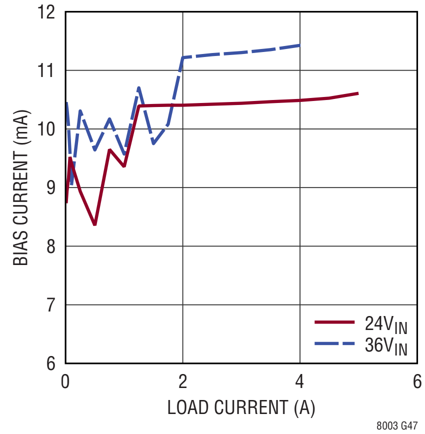


TYPICAL PERFORMANCE CHARACTERISTICS $T_A = 25°C$, unless otherwise noted.

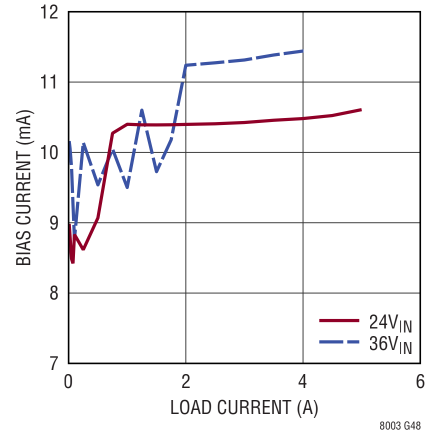
BIAS Current vs Load Current V_{OUT} = 12V, BIAS = 5V



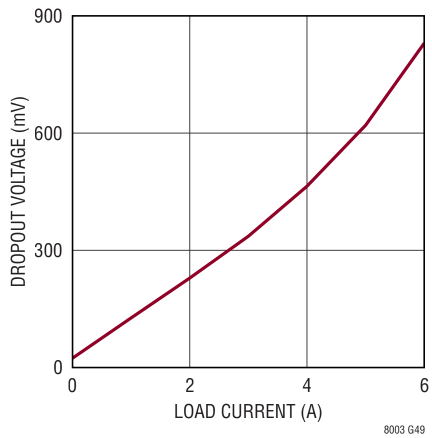
BIAS Current vs Load Current V_{OUT} = 15V, BIAS = 5V



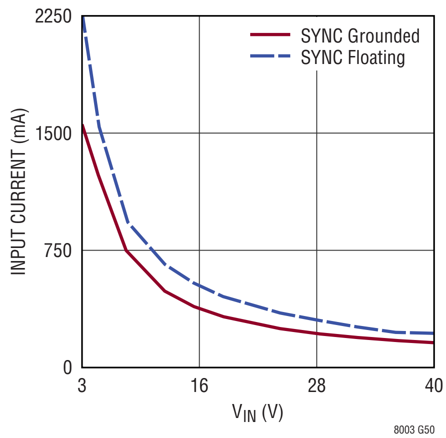
BIAS Current vs Load Current V_{OUT} = 18V, BIAS = 5V



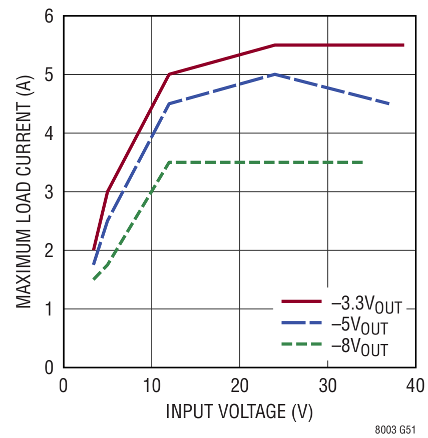
Dropout Voltage vs Load Current, V_{OUT} = 5V, BIAS = 5V



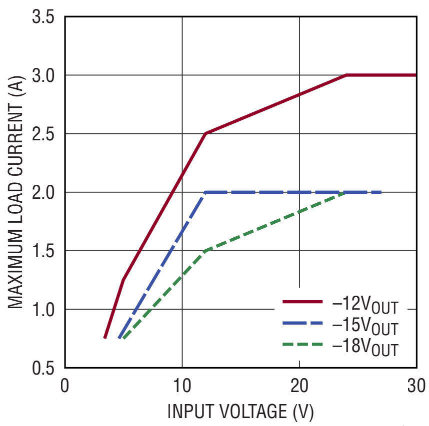
Input Current vs V_{IN} V_{OUT} Short Circuited



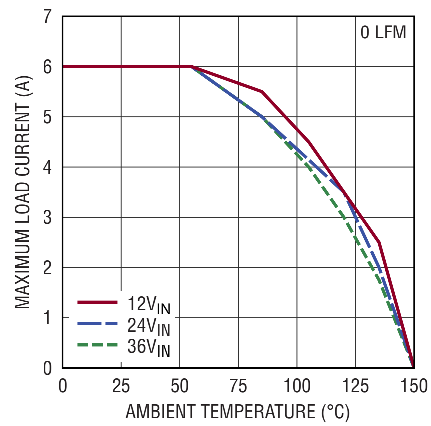
Maximum Load Current vs V_{IN} BIAS Open



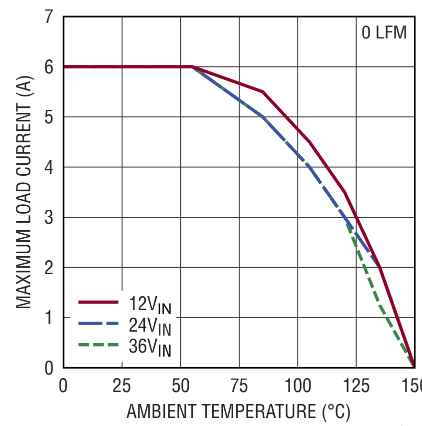
Maximum Load Current vs V_{IN} BIAS Open



Derating, H-Grade, V_{OUT} = 0.97V, BIAS = 5V, DC2416A Demo Board



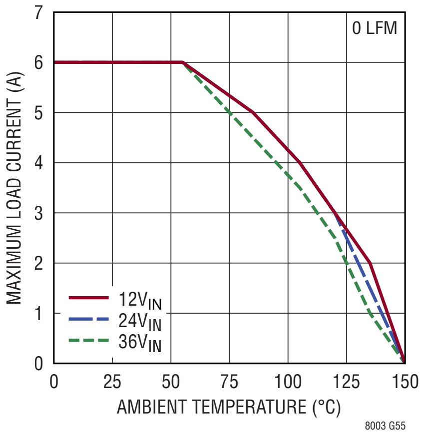
Derating, H-Grade, V_{OUT} = 1.2V, BIAS = 5V, DC2416A Demo Board



Rev E

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

Derating, H-Grade, V_{OUT} = 1.5V, BIAS = 5V, DC2416A Demo Board



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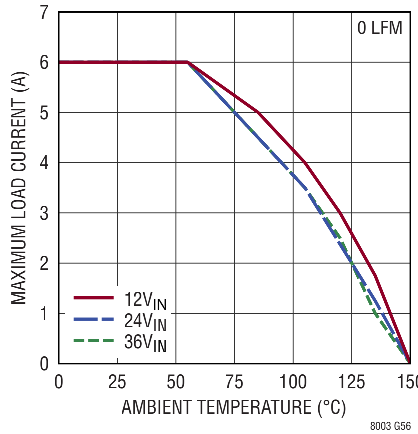
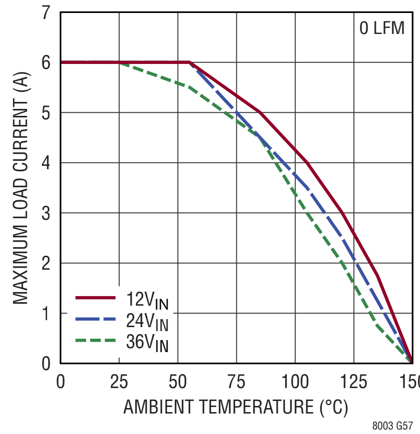


Derating, H-Grade, V_{OUT} = 2V, BIAS = 5V, DC2416A Demo Board



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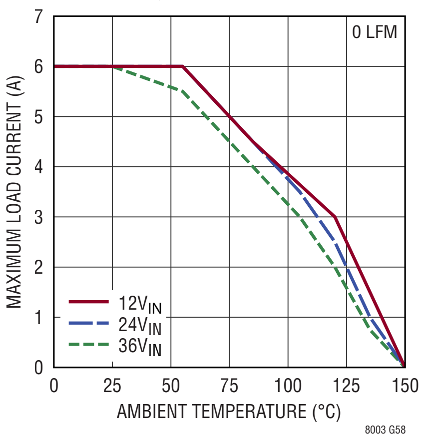
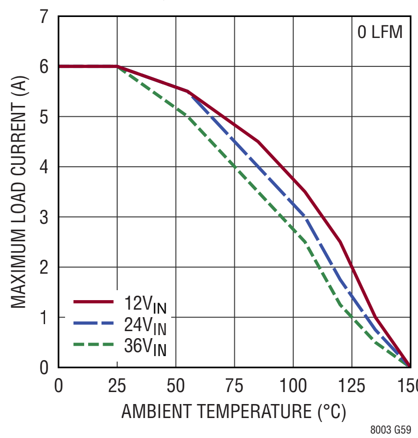
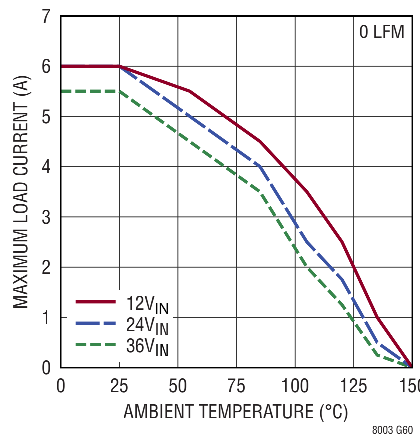


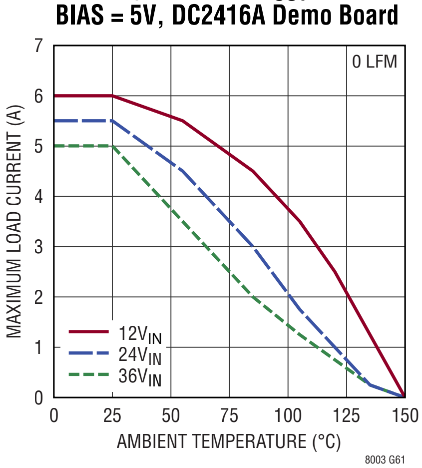
Derating, H-Grade, V_{OUT} = 3.3V, BIAS = 5V, DC2416A Demo Board



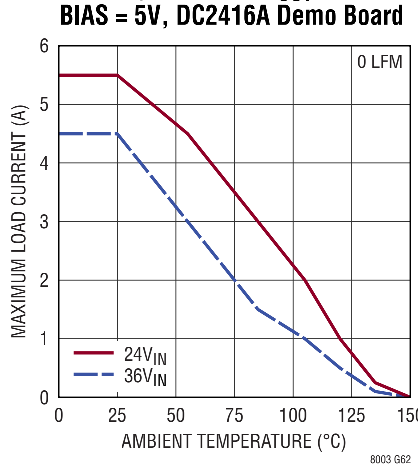
Derating, H-Grade, V_{OUT} = 5V, BIAS = 5V, DC2416A Demo Board



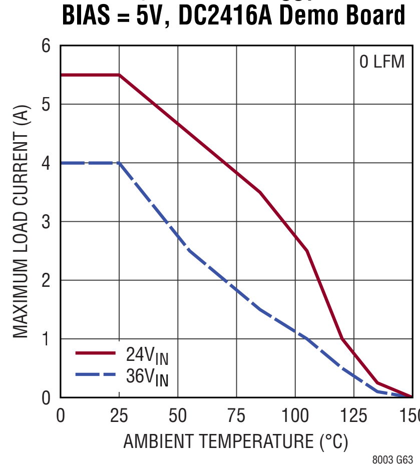
Derating, H-Grade, V_{OUT} = 8V, BIAS = 5V, DC2416A Demo Board



Derating, H-Grade, V_{OUT} = 12V, BIAS = 5V, DC2416A Demo Board



Derating, H-Grade, V_{OUT} = 15V, BIAS = 5V, DC2416A Demo Board



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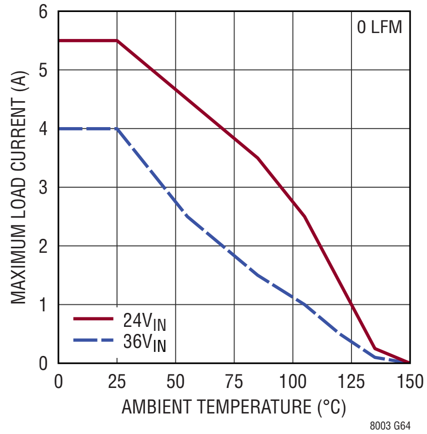
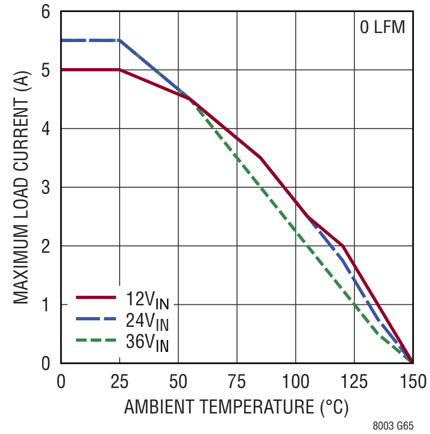
TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

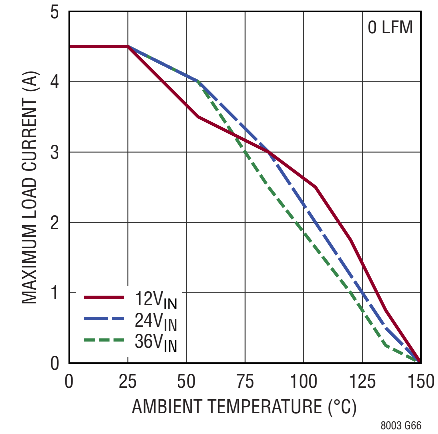
Derating, H-Grade, V_{OUT} = 18V, BIAS = 5V, DC2416A Demo Board



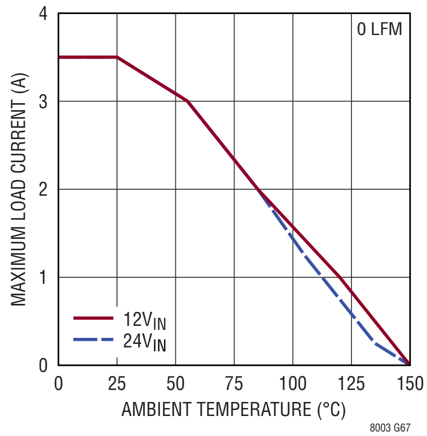
Derating, H-Grade, V_{OUT} = –3.3V, BIAS Tied to LTM8003 GND, DC2416A Demo Board



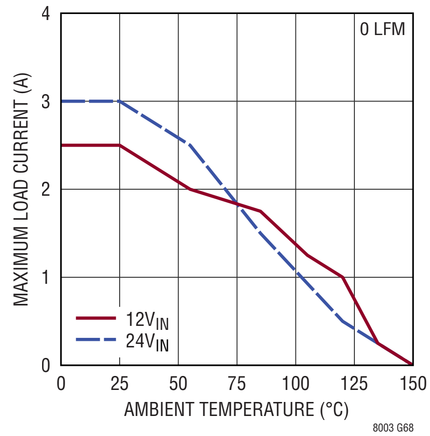
Derating, H-Grade, V_{OUT} = –5V, BIAS Tied to LTM8003 GND, DC2416A Demo Board



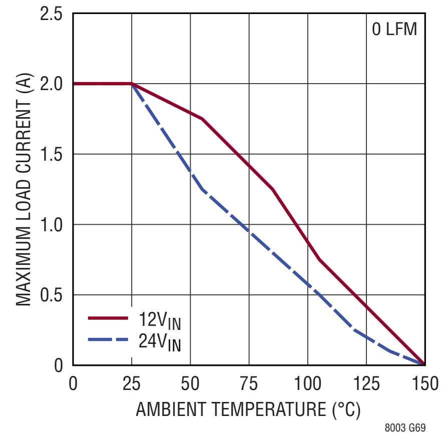
Derating, H-Grade, V_{OUT} = –8V, BIAS Tied to LTM8003 GND, DC2416A Demo Board



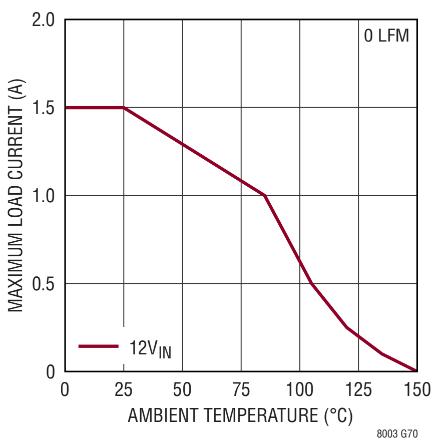
Derating, H-Grade, V_{OUT} = –12V, BIAS Tied to LTM8003 GND, DC2416A Demo Board



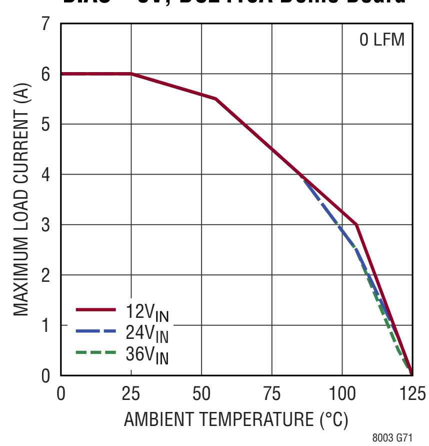
Derating, H-Grade, V_{OUT} = –15V, BIAS Tied to LTM8003 GND, DC2416A Demo Board



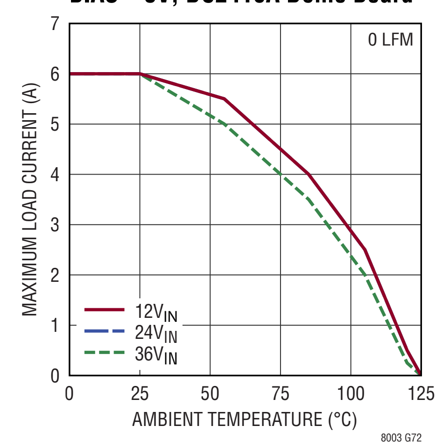
Derating, H-Grade, V_{OUT} = –18V, BIAS Tied to LTM8003 GND, DC2416A Demo Board



Derating, I-Grade, V_{OUT} = 0.97V, BIAS = 5V, DC2416A Demo Board

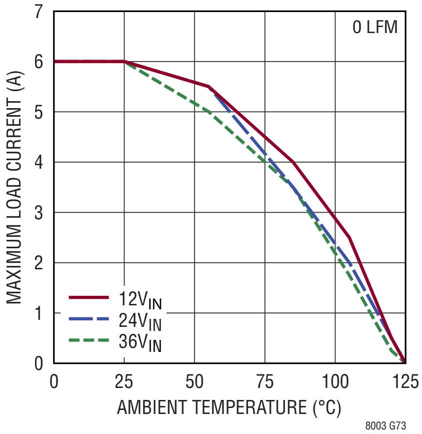


Derating, I-Grade, V_{OUT} = 1.2V, BIAS = 5V, DC2416A Demo Board

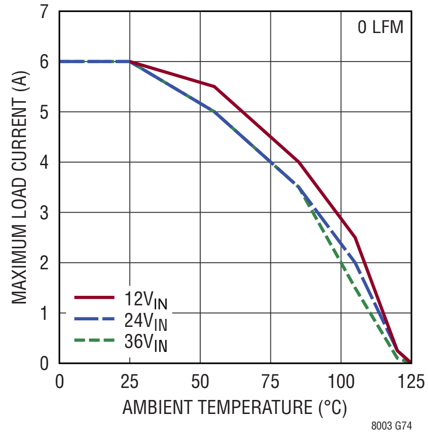


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

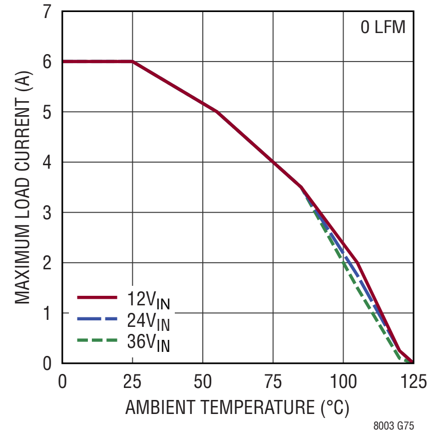
Derating, I-Grade, V_{OUT} = 1.5V, BIAS = 5V, DC2416A Demo Board



Derating, I-Grade, V_{OUT} = 1.8V, BIAS = 5V, DC2416A Demo Board



Derating, I-Grade, V_{OUT} = 2V, BIAS = 5V, DC2416A Demo Board



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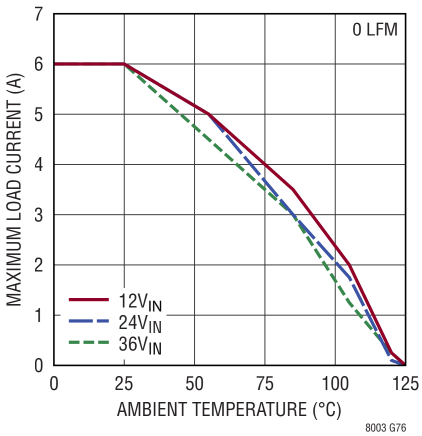
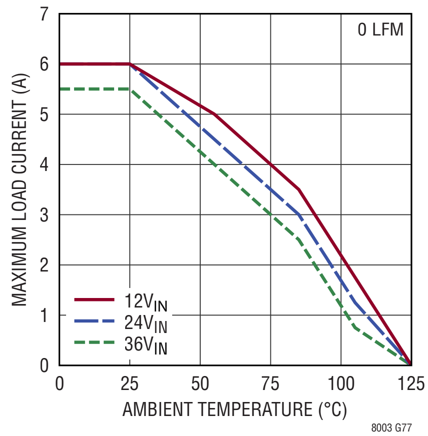
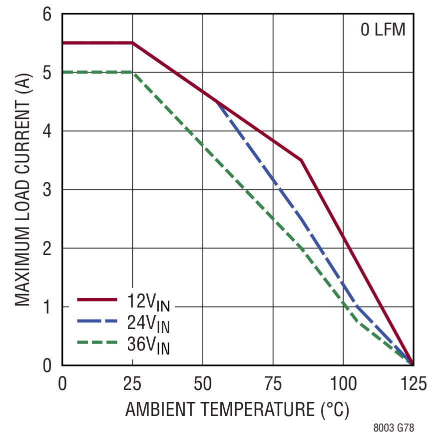


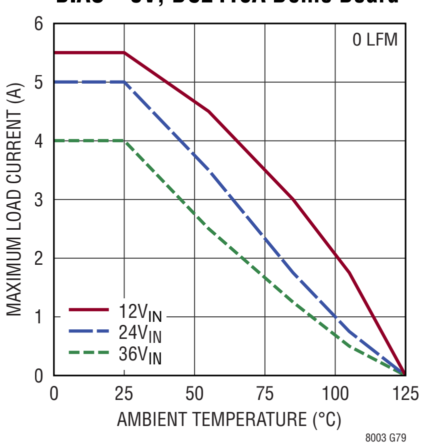
Derating, I-Grade, V_{OUT} = 3.3V, BIAS = 5V, DC2416A Demo Board



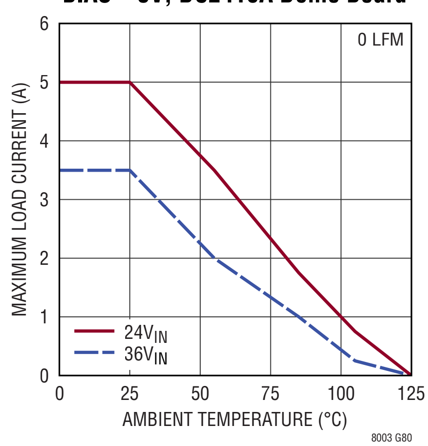
Derating, I-Grade, V_{OUT} = 5V, BIAS = 5V, DC2416A Demo Board



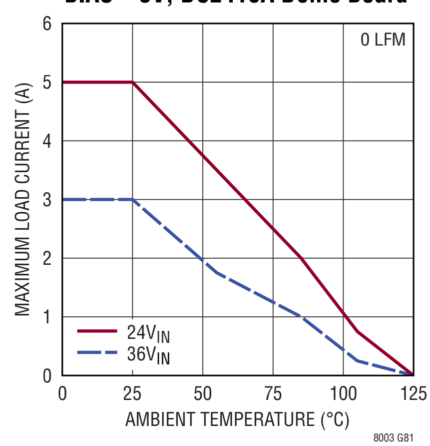
Derating, I-Grade, V_{OUT} = 8V, BIAS = 5V, DC2416A Demo Board



Derating, I-Grade, V_{OUT} = 12V, BIAS = 5V, DC2416A Demo Board



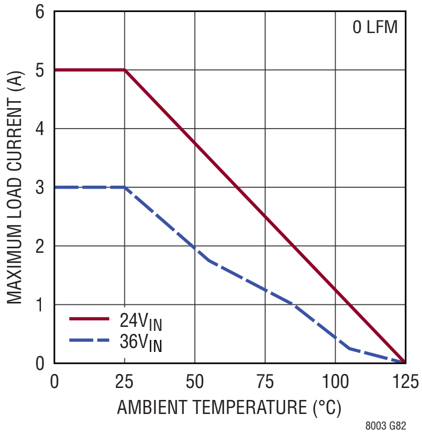
Derating, I-Grade, V_{OUT} = 15V, BIAS = 5V, DC2416A Demo Board



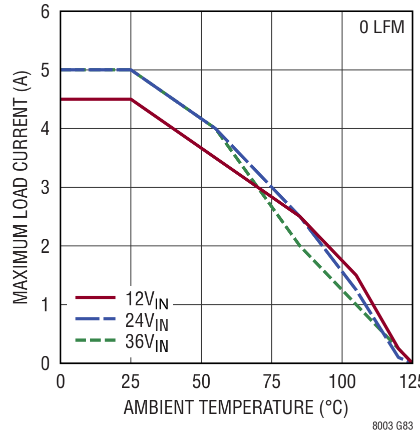
Rev E

TYPICAL PERFORMANCE CHARACTERISTICS $T_A = 25°C$, unless otherwise noted.

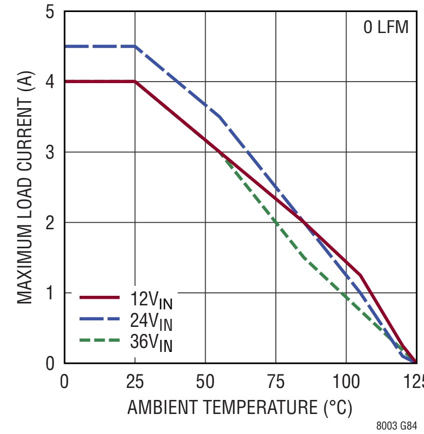
Derating, I-Grade, V_{OUT} = 18V, BIAS = 5V, DC2416A Demo Board



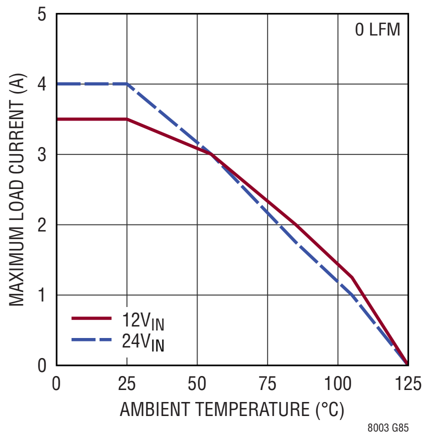
Derating, I-Grade, V_{OUT} = –3.3V, BIAS Tied to LTM8003 GND, DC2416A Demo Board



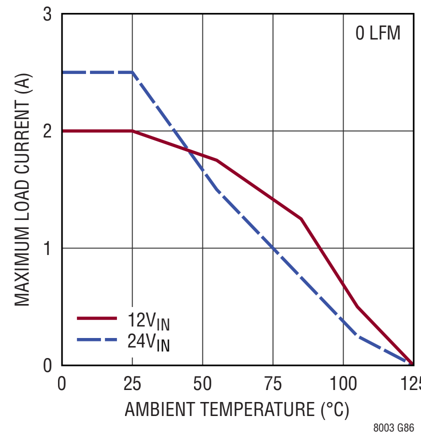
Derating, I-Grade, V_{OUT} = –5V, BIAS Tied to LTM8003 GND, DC2416A Demo Board



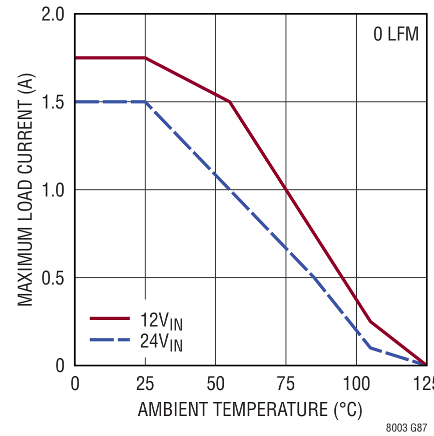
Derating, I-Grade, V_{OUT} = –8V, BIAS Tied to LTM8003 GND, DC2416A Demo Board



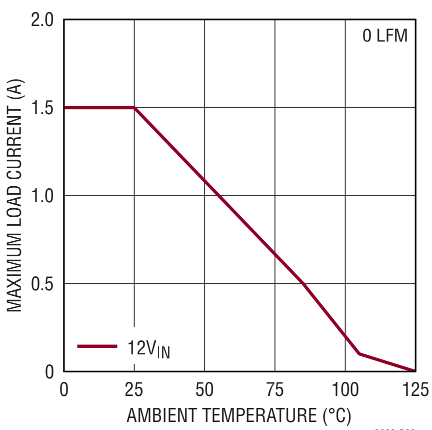
Derating, I-Grade, V_{OUT} = –12V, BIAS Tied to LTM8003 GND, DC2416A Demo Board



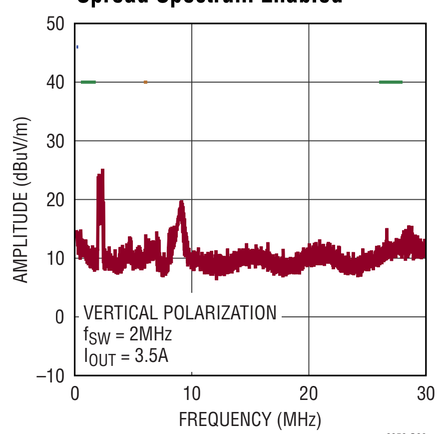
Derating, I-Grade, V_{OUT} = –15V, BIAS Tied to LTM8003 GND, DC2416A Demo Board



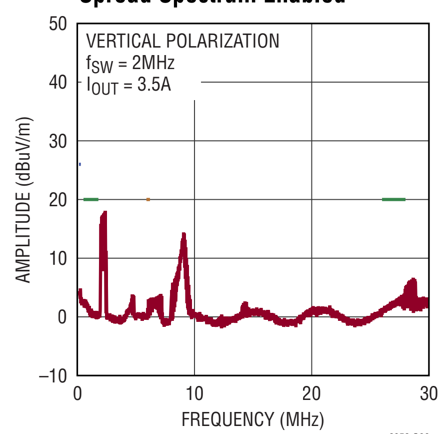
Derating, I-Grade, V_{OUT} = –18V, BIAS Tied to LTM8003 GND, DC2416A Demo Board



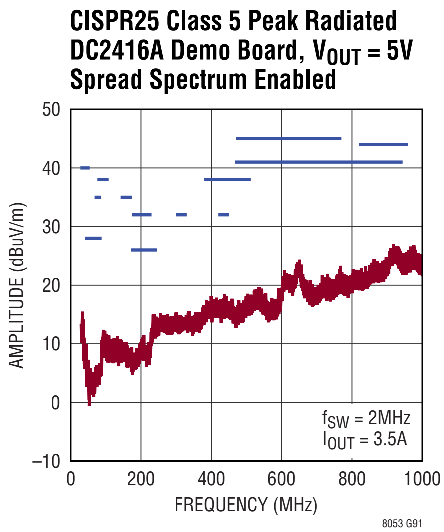
CISPR25 Class 5 Peak Radiated DC2416A Demo Board, V_{OUT} = 5V Spread Spectrum Enabled

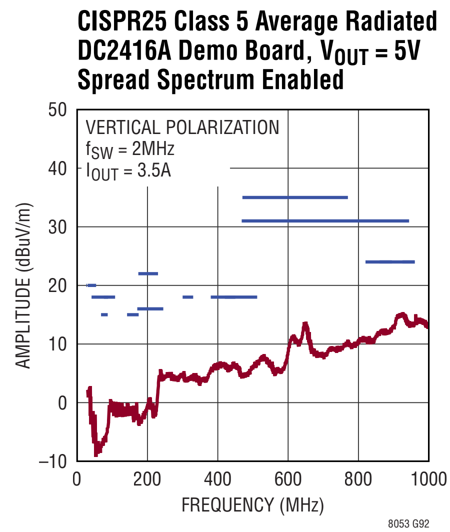


CISPR25 Class 5 Average Radiated DC2416A Demo Board, V_{OUT} = 5V Spread Spectrum Enabled



TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.





PIN FUNCTIONS

GND (Bank 1, A1, A6): Tie these GND pins to a local ground plane below the LTM8003 and the circuit components. In most applications, the bulk of the heat flow out of the LTM8003 is through these pads, so the printed circuit design has a large impact on the thermal performance of the part. See the PCB Layout and Thermal Considerations sections for more details.

V_{IN} (Bank 2): V_{IN} supplies current to the LTM8003's internal regulator and to the internal power switch. These pins must be locally bypassed with an external, low ESR capacitor; see Table 1 for recommended values.

V_{OUT} (Bank 3): Power Output Pins. Apply the output filter capacitor and the output load between these pins and GND pins.

BIAS (Pins G1, G2): The BIAS pin connects to the internal power bus. Connect to a power source greater than 3.2V and less than 18V. If V_{OUT} is greater than 3.2V, connect this pin there. If the output voltage is less, connect this to a voltage source above 3.2V. Decouple this pin with at least 1µF if the voltage source for BIAS is remote. If unused or generating a negative output, tie BIAS to LTM8003 GND.

RUN (Pins B5, B6): Pull the RUN pin below 0.9V to shut down the LTM8003. Tie to 1.06V or more for normal operation. If the shutdown feature is not used, tie this pin to the V_{IN} pin.

RT (Pins A4, A5): The RT pin is used to program the switching frequency of the LTM8003 by connecting a resistor from this pin to ground. The Applications Information section of the data sheet includes a table to determine the resistance value based on the desired switching frequency. Minimize capacitance at this pin. Do not drive this pin.

SYNC (Pins A2, B2): External clock synchronization input and operational mode. This pin programs four different operating modes:

1. Burst Mode®. Tie this pin to ground for Burst Mode operation at low output loads—this will result in ultralow quiescent current.
2. Pulse-skipping mode. Float this pin for pulse-skipping mode. This mode offers full frequency operation down to low output loads before pulse skipping occurs.
3. Spread spectrum mode. Tie this pin high (between 2.9V and 4.2V) for pulse-skipping mode with spread spectrum modulation.
4. Synchronization mode. Drive this pin with a clock source to synchronize to an external frequency. During synchronization the part will operate in pulse-skipping mode.

PG (Pin B1, C1): The PG pin is the open-collector output of an internal comparator. PG remains low until the FB pin voltage is within about 10% of the final regulation

PIN FUNCTIONS

voltage. The PG signal is valid when V_{IN} is above 3.4V. If V_{IN} is above 3.4V and RUN is low, PG will drive low. If this function is not used, leave this pin floating.

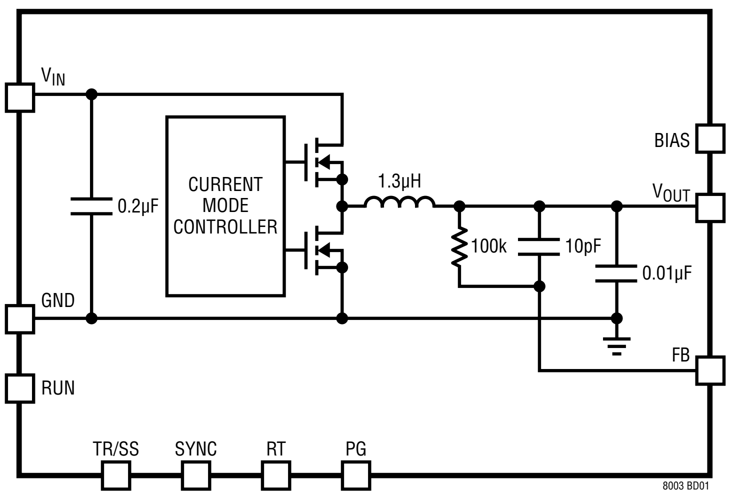
FB (Pin F1, F2): The LTM8003 regulates its FB pin to 0.97V. Connect the adjust resistor from this pin to ground. The value of R_{FB} is given by the equation $R_{FB} = 97/(V_{OUT} – 0.97)$, where R_{FB} is in kΩ.

TR/SS (Pin A3, B3): The TR/SS pin is used to provide a soft-start or tracking function. The internal 2µA pull-up current in combination with an external capacitor tied to this pin creates a voltage ramp. If TR/SS is less than 0.97V, the output voltage tracks to this value. For tracking, tie a resistor divider to this pin from the tracked output. This pin is pulled to ground with an internal MOSFET during shutdown and fault conditions; use a series resistor if driving from a low impedance output. This pin may be left floating if the tracking function is not needed.

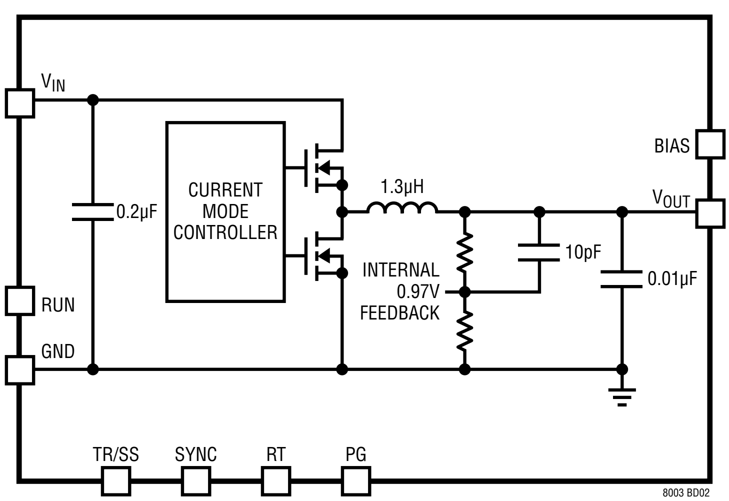
NC (Pins C5, D5, E5, E6): These pins are not connected, either to any other net or each other.

BLOCK DIAGRAM

LTM8003 Block Diagram



LTM8003-3.3 Block Diagram



Rev E

OPERATION

The LTM8003 is a stand-alone non-isolated step-down switching DC/DC power supply that can deliver up to 6A. The continuous current is determined by the internal operating temperature. It provides a precisely regulated output voltage programmable via one external resistor from 0.97V to 18V. The input voltage range is 3.4V to 40V. Given that the LTM8003 is a step-down converter, make sure that the input voltage is high enough to support the desired output voltage and load current. Simplified Block Diagrams are given on the previous page.

The LTM8003 contains a current mode controller, power switching elements, power inductor and a modest amount of input and output capacitance. The LTM8003 is a fixed frequency PWM regulator. The switching frequency is set by simply connecting the appropriate resistor value from the RT pin to GND.

An internal regulator provides power to the control circuitry. This bias regulator normally draws power from the V_{IN} pin, but if the BIAS pin is connected to an external voltage higher than 3.2V, bias power is drawn from the external source (typically the regulated output voltage). This improves efficiency. The RUN pin is used to place the LTM8003 in shutdown, disconnecting the output and reducing the input current to a few µA.

To enhance efficiency, the LTM8003 automatically switches to Burst Mode operation in light or no load situations. Between bursts, all circuitry associated with controlling the output switch is shut down reducing the input supply current to just a few µA.

The oscillator reduces the LTM8003's operating frequency when the voltage at the FB pin is low. This frequency foldback helps to control the output current during start-up and overload.

The TR/SS node acts as an auxiliary input to the error amplifier. The voltage at FB servos to the TR/SS voltage until TR/SS goes above about 0.97V. Soft-start is implemented by generating a voltage ramp at the TR/SS pin using an external capacitor which is charged by an internal constant current. Alternatively, driving the TR/SS pin with a signal source or resistive network provides a tracking function. Do not drive the TR/SS pin with a low impedance voltage source. See the Applications Information section for more details.

The LTM8003 contains a power good comparator which trips when the FB pin is at about 90% to 110% of its regulated value. The PG output is an open-drain transistor that is off when the output is in regulation, allowing an external resistor to pull the PG pin high. The PG signal is valid when V_{IN} is above 3.4V. If V_{IN} is above 3.4V and RUN is low, PG will drive low.

The LTM8003 is equipped with a thermal shutdown that inhibits power switching at high junction temperatures. The activation threshold of this function is above the maximum temperature rating to avoid interfering with normal operation, so prolonged or repetitive operation under a condition in which the thermal shutdown activates may damage or impair the reliability of the device.

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For most applications, the design process is straightforward, summarized as follows:

1. Look at Table 1 and find the row that has the desired input range and output voltage.
2. Apply the recommended C_{FF}, C_{IN}, C_{OUT}, R_{FB} and R_T values.
3. Apply the C_{FF} (from V_{OUT} to F_B) as required.
4. Connect BIAS as indicated.

While these component combinations have been tested for proper operation, it is incumbent upon the user to verify proper operation over the intended system's line, load and environmental conditions. Bear in mind that the maximum output current is limited by junction temperature, the relationship between the input and output voltage magnitude and polarity and other factors. Please refer to the graphs in the Typical Performance Characteristics section for guidance.

The maximum frequency (and attendant R_T value) at which the LTM8003 should be allowed to switch is given in Table 1 in the Maximum f_{SW} column, while the recommended frequency (and R_T value) for optimal efficiency over the given input condition is given in the f_{SW} column. There are additional conditions that must be satisfied if the synchronization function is used. Please refer to the Synchronization section for details.

Table 1. Recommended Component Values and Configuration (T_A = 25°C)

V_{IN}	V_{OUT} (V)	R_{FB} (kΩ)	C_{IN}[2]	C_{OUT}	C_{FF} (pF)	BIAS (V)	f_{SW}	R_T (kΩ)	Maximum f_{SW}	Minimum R_T (kΩ)
3.4V to 40V	0.97	Open	4.7µF 50V 1206 X5R	2x 100µF 6.3V 1210 X5R	47	3.2 to 19	450kHz	97.6	675kHz	63.4
3.4V to 40V	1.2	402	4.7µF 50V 1206 X5R	2x 100µF 6.3V 1210 X5R	47	3.2 to 19	550kHz	78.7	850kHz	49.9
3.4V to 40V	1.5	174	4.7µF 50V 1206 X5R	100µF 6.3V 1210 X5R	27	3.2 to 19	600kHz	71.5	1.1MHz	36.5
3.4V to 40V	1.8	115	4.7µF 50V 1206 X5R	100µF 6.3V 1210 X5R	10	3.2 to 19	600kHz	71.5	1.3MHz	30.9
3.4V to 40V	2.0	90.9	4.7µF 50V 1206 X5R	100µF 0805 4V X5R		3.2 to 19	650kHz	64.9	1.4MHz	28.0
4V to 40V[1]	2.5	63.4	4.7µF 50V 1206 X5R	100µF 0805 4V X5R		3.2 to 19	750kHz	56.2	1.8MHz	20.5
5V to 40V[1]	3.3	41.2	4.7µF 50V 1206 X5R	100µF 0805 4V X5R		3.2 to 19	850kHz	48.7	2.3MHz	14.7
7V to 40V[1]	5	24.3	4.7µF 50V 1206 X5R	47µF 6.3V 0805 X5R		3.2 to 19	1MHz	40.2	3MHz	10.7
11V to 40V[1]	8	13.7	4.7µF 50V 1206 X5R	22µF 1206 10V X7R		3.2 to 19	1.2MHz	33.2	3MHz	10.7
16V to 40V[1]	12	8.66	4.7µF 50V 1206 X5R	10µF 0805 16V X7S		3.2 to 19	1.5MHz	25.5	3MHz	10.7
19.5 to 40V[1]	15	6.81	4.7µF 50V 1206 X5R	10µF 0805 16V X7S		3.2 to 19	1.5MHz	25.5	3MHz	10.7
23.5V to 40V[1]	18	5.62	4.7µF 50V 1206 X5R	10µF 1206 25V X5R		3.2 to 19	1.5MHz	25.5	3MHz	10.7
5V to 22V[1]	–18	5.62	4.7µF 50V 1206 X5R	10µF 1206 25V X5R		LTM8003 GND	1.5MHz	25.5	3MHz	10.7
4.5V to 25V[1]	–15	6.81	4.7µF 50V 1206 X5R	10µF 0805 16V X7S		LTM8003 GND	1.5MHz	25.5	3MHz	10.7
3.4V to 28V[1]	–12	8.66	4.7µF 50V 1206 X5R	10µF 0805 16V X7S		LTM8003 GND	1.5MHz	25.5	3MHz	10.7
3.4V to 32V[1]	–8	13.7	4.7µF 50V 1206 X5R	22µF 1206 10V X7R		LTM8003 GND	1.2MHz	33.2	3MHz	10.7
3.4V to 35[1]	–5	24.3	4.7µF 50V 1206 X5R	47µF 6.3V 0805 X5R		LTM8003 GND	1MHz	40.2	3MHz	10.7
3.4V to 36V[1]	–3.3	41.2	4.7µF 50V 1206 X5R	100µF 0805 4V X5R		LTM8003 GND	850kHz	48.7	2.3MHz	14.7

1. The LTM8003 may be capable of lower input voltages but may skip switching cycles.
2. An input bulk capacitor is required

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Capacitor Selection Considerations

The C_{IN} and C_{OUT} capacitor values in Table 1 are the minimum recommended values for the associated operating conditions. Applying capacitor values below those indicated in Table 1 is not recommended and may result in undesirable operation. Using larger values is generally acceptable, and can yield improved dynamic response, if it is necessary. Again, it is incumbent upon the user to verify proper operation over the intended system's line, load and environmental conditions.

Ceramic capacitors are small, robust and have very low ESR. However, not all ceramic capacitors are suitable. X5R and X7R types are stable over temperature and applied voltage and give dependable service. Other types, including Y5V and Z5U have very large temperature and voltage coefficients of capacitance. In an application circuit they may have only a small fraction of their nominal capacitance resulting in much higher output voltage ripple than expected.

Ceramic capacitors are also piezoelectric. In Burst Mode operation, the LTM8003's switching frequency depends on the load current, and can excite a ceramic capacitor at audio frequencies, generating audible noise. Since the LTM8003 operates at a lower current limit during Burst Mode operation, the noise is typically very quiet to a casual ear.

If this audible noise is unacceptable, use a high performance electrolytic capacitor at the output. It may also be a parallel combination of a ceramic capacitor and a low cost electrolytic capacitor.

A final precaution regarding ceramic capacitors concerns the maximum input voltage rating of the LTM8003. A ceramic input capacitor combined with trace or cable inductance forms a high-Q (underdamped) tank circuit. If the LTM8003 circuit is plugged into a live supply, the input voltage can ring to twice its nominal value, possibly exceeding the device's rating. This situation is easily avoided; see the Hot-Plugging Safely section.

Frequency Selection

The LTM8003 uses a constant frequency PWM architecture that can be programmed to switch from 200kHz to 3MHz by using a resistor tied from the RT pin to ground. Table 2 provides a list of R_T resistor values and their resultant frequencies.

Table 2. SW Frequency vs R_T Value

f_{SW} (MHz)	R_T (kΩ)
0.2	232
0.3	150
0.4	110
0.5	88.7
0.6	71.5
0.7	60.4
0.8	52.3
1.0	40.2
1.2	33.2
1.4	28.0
1.6	23.7
1.8	20.5
2.0	18.2
2.2	15.8
3.0	10.7

Operating Frequency Trade-Offs

It is recommended that the user apply the optimal R_T value given in Table 1 for the input and output operating condition. System level or other considerations, however, may necessitate another operating frequency. While the LTM8003 is flexible enough to accommodate a wide range of operating frequencies, a haphazardly chosen one may result in undesirable operation under certain operating or fault conditions. A frequency that is too high can reduce efficiency, generate excessive heat or even damage the LTM8003 if the output is overloaded or short-circuited. A frequency that is too low can result in a final design that has too much output ripple or too large of an output capacitor.

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BIAS Pin Considerations

The BIAS pin is used to provide drive power for the internal power switching stage and operate other internal circuitry. For proper operation, it must be powered by at least 3.2V. If the output voltage is programmed to 3.2V or higher, BIAS may be simply tied to V_{OUT}. If V_{OUT} is less than 3.2V, BIAS can be tied to V_{IN} or some other voltage source. If the BIAS pin voltage is too high, the efficiency of the LTM8003 may suffer. The optimum BIAS voltage is dependent upon many factors, such as load current, input voltage, output voltage and switching frequency. In all cases, ensure that the maximum voltage at the BIAS pin is less than 19V. If BIAS power is applied from a remote or noisy voltage source, it may be necessary to apply a decoupling capacitor locally to the pin. A 1µF ceramic capacitor works well. The BIAS pin may also be left open at the cost of a small degradation in efficiency. If unused or generating a negative output, tie BIAS to LTM8003 GND.

Maximum Load

The maximum practical continuous load that the LTM8003 can drive, while rated at 3.5A, actually depends upon both the internal current limit and the internal temperature. The internal current limit is designed to prevent damage to the LTM8003 in the case of overload or short-circuit. The internal temperature of the LTM8003 depends upon operating conditions such as the ambient temperature, the power delivered, and the heat sinking capability of the system. For example, if the LTM8003H is configured to regulate at 1.2V, it may continuously deliver 6A from $12V_{IN}$ if the ambient temperature is controlled to less than 50°C. This is quite a bit higher than the 3.5A continuous rating. Please see the "Derating, H-Grade, V_{OUT} = 1.2V" curve in the Typical Performance Characteristics section. Similarly, if the output voltage is 18V and the ambient temperature is 100°C, the LTM8003H will deliver at most 2.7A from $24V_{IN}$, which is less than the 3.5A continuous rating.

Load Sharing

Neither the LTM8003 nor LTM8003-3.3 are designed to load share.

Burst Mode Operation

To enhance efficiency at light loads, the LTM8003 automatically switches to Burst Mode operation which keeps the output capacitor charged to the proper voltage while minimizing the input quiescent current. During Burst Mode operation, the LTM8003 delivers single cycle bursts of current to the output capacitor followed by sleep periods where most of the internal circuitry is powered off and energy is delivered to the load by the output capacitor. During the sleep time, V_{IN} and BIAS quiescent currents are greatly reduced, so, as the load current decreases towards a no load condition, the percentage of time that the LTM8003 operates in sleep mode increases and the average input current is greatly reduced, resulting in higher light load efficiency.

Burst Mode operation is enabled by tying SYNC to GND.

Minimum Input Voltage

The LTM8003 is a step-down converter, so a minimum amount of headroom is required to keep the output in regulation. Keep the input above 3.4V to ensure proper operation. Voltage transients or ripple valleys that cause the input to fall below 3.4V may turn off the LTM8003.

Output Voltage Tracking and Soft-Start

The LTM8003 allows the user to adjust its output voltage ramp rate by means of the TR/SS pin. An internal 2µA pulls up the TR/SS pin to about 2.4V. Putting an external capacitor on TR/SS enables soft starting the output to reduce current surges on the input supply. During the soft-start ramp the output voltage will proportionally track the TR/SS pin voltage. For output tracking applications, TR/SS can be externally driven by another voltage source. From 0V to 0.97V, the TR/SS voltage will override the internal 0.97V reference input to the error amplifier, thus regulating the FB pin voltage to that of the TR/SS pin. When TR/SS is above 0.97V, tracking is disabled and the feedback voltage will regulate to the internal reference voltage. The TR/SS pin may be left floating if the function is not needed.

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An active pull-down circuit is connected to the TR/SS pin which will discharge the external soft-start capacitor in the case of fault conditions and restart the ramp when the faults are cleared. Fault conditions that clear the soft-start capacitor are the RUN pin transitioning low, V_{IN} voltage falling too low, or thermal shutdown.

Pre-Biased Output

As discussed in the Output Voltage Tracking and Soft-Start section, the LTM8003 regulates the output to the FB voltage determined by the TR/SS pin whenever TR/SS is less than 0.97V. If the LTM8003 output is higher than the target output voltage, the LTM8003 will attempt to regulate the output to the target voltage by returning a small amount of energy back to the input supply. If there is nothing loading the input supply, its voltage may rise. Take care that it does not rise so high that the input voltage exceeds the absolute maximum rating of the LTM8003.

Frequency Foldback

The LTM8003 is equipped with frequency foldback which acts to reduce the thermal and energy stress on the internal power elements during a short circuit or output overload condition. If the LTM8003 detects that the output has fallen out of regulation, the switching frequency is reduced as a function of how far the output is below the target voltage. This in turn limits the amount of energy that can be delivered to the load under fault. During the start-up time, frequency foldback is also active to limit the energy delivered to the potentially large output capacitance of the load. When a clock is applied to the SYNC pin, the SYNC pin is floated or held high, the frequency foldback is disabled, and the switching frequency will slow down only during overcurrent conditions.

Synchronization

To select low ripple Burst Mode operation, tie the SYNC pin below about 0.4V (this can be ground or a logic low output). To synchronize the LTM8003 oscillator to an external frequency, connect a square wave (with about 20% to 80% duty cycle) to the SYNC pin. The square wave amplitude should have valleys that are below 0.4V and peaks above 1.5V.

The LTM8003 will not enter Burst Mode operation at low output loads while synchronized to an external clock, but instead will pulse skip to maintain regulation. The LTM8003 may be synchronized over a 200kHz to 3MHz range. The R_T resistor should be chosen to set the switching frequency equal to or below the lowest synchronization input. For example, if the synchronization signal will be 500kHz and higher, the R_T should be selected for 500kHz.

For some applications it is desirable for the LTM8003 to operate in pulse-skipping mode, offering two major differences from Burst Mode operation. The first is that the clock stays awake at all times and all switching cycles are aligned to the clock. The second is that full switching frequency is reached at lower output load than in Burst Mode operation. These two differences come at the expense of increased quiescent current. To enable pulse-skipping mode, the SYNC pin is floated.

The LTM8003 features spread spectrum operation to further reduce EMI/EMC emissions. To enable spread spectrum operation, apply between 2.9V and 4.2V to the SYNC pin. In this mode, triangular frequency modulation is used to vary the switching frequency between the value programmed by R_T to about 20% higher than that value. The modulation frequency is about 3kHz. For example, when the LTM8003 is programmed to 2MHz, the frequency will vary from 2MHz to 2.4MHz at a 3kHz rate. When spread spectrum operation is selected, Burst Mode operation is disabled, and the part will run in pulse-skipping mode.

The LTM8003 does not operate in forced continuous mode regardless of SYNC signal.

Negative Output

The LTM8003 is capable of generating a negative output voltage by connecting its V_{OUT} to system GND and the LTM8003 GND to the negative voltage rail. An example of this is shown in the Typical Applications section. The

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most versatile way to generate a negative output is to use a dedicated regulator that was designed to generate a negative voltage, but using a buck regulator like the LTM8003 to generate a negative voltage is a simple and cost effective solution, as long as certain restrictions are kept in mind.

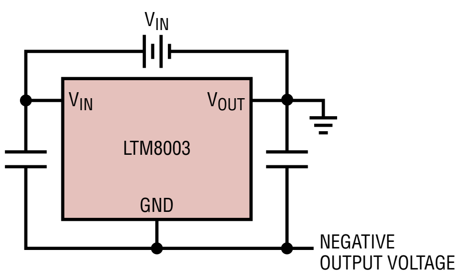

Figure 1. The LTM8003 Can Be Used to Generate a Negative Voltage

Figure 1 shows a typical negative output voltage application. Note that LTM8003 V_{OUT} is tied to system GND and input power is applied from V_{IN} to LTM8003 V_{OUT}. As a result, the LTM8003 is not behaving as a true buck regulator, and the maximum output current depends upon the input voltage. In the example shown in the Typical Applications section, there is an attending graph that shows how much current the LTM8003 can deliver for given input voltages.

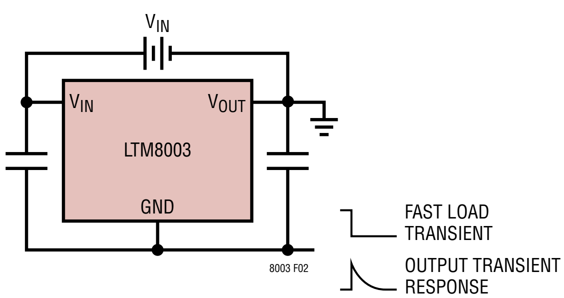

Figure 2. Any Output Voltage Transient Appears on LTM8003 GND

Note that this configuration requires that any load current transient will directly impress the transient voltage onto the LTM8003 GND, as shown in Figure 2, so fast load transients can disrupt the LTM8003's operation or even cause damage.

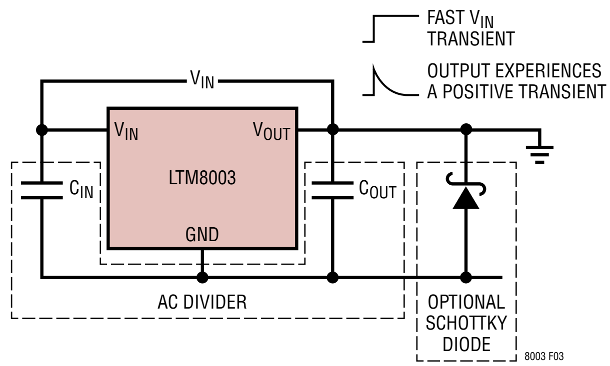

Figure 3. A Schottky Diode Can Limit the Transient Caused by a Fast Rising V_{IN} to Safe Levels

The C_{IN} and C_{OUT} capacitors in Figure 3 form an AC divider at the negative output voltage node. If V_{IN} is hot-plugged or rises quickly, the resultant V_{OUT} will be a positive transient, which may be unhealthy for the application load. An anti-parallel Schottky diode may be able to prevent this positive transient from damaging the load. The location of this Schottky diode is important. For example, in a system where the LTM8003 is far away from the load, placing the Schottky diode closest to the most sensitive load component may be the best design choice. Carefully evaluate whether the negative buck configuration is suitable for the application. When generating a negative output voltage, tie BIAS to LTM8003 GND.

Shorted Input Protection

Care needs to be taken in systems where the output is held high when the input to the LTM8003 is absent. This may occur in battery charging applications or in battery backup systems where a battery or some other supply is diode ORed with the LTM8003's output. If the V_{IN} pin is allowed to float and the RUN pin is held high (either by a logic signal or because it is tied to V_{IN}), then the LTM8003's internal circuitry pulls its quiescent current through its internal power switch. This is fine if your system can tolerate a few milliamps in this state. If you ground the RUN pin, the internal current drops to essentially zero. However, if the V_{IN} pin is grounded while the output is held high, parasitic

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diodes inside the LTM8003 can pull large currents from the output through the V_{IN} pin. Figure 4 shows a circuit that runs only when the input voltage is present and that protects against a shorted or reversed input.

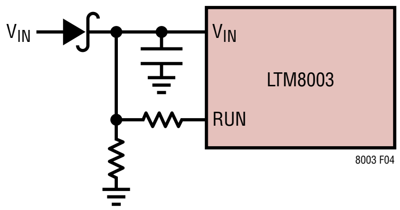

Figure 4. The Input Diode Prevents a Shorted Input from Discharging a Backup Battery Tied to the Output. It Also Protects the Circuit from a Reversed Input. The LTM8003 Runs Only When the Input Is Present

PCB Layout

Most of the headaches associated with PCB layout have been alleviated or even eliminated by the high level of integration of the LTM8003. The LTM8003 is nevertheless a switching power supply, and care must be taken to minimize EMI and ensure proper operation. Even with the high level of integration, you may fail to achieve specified operation with a haphazard or poor layout. See Figure 5 for a suggested layout. Ensure that the grounding and heat sinking are acceptable.

A few rules to keep in mind are:

1. Place C_{FF}, R_{FB} and R_T as close as possible to their respective pins.
2. Place the C_{IN} capacitor as close as possible to the V_{IN} and GND connection of the LTM8003.
3. Place the C_{OUT} capacitor as close as possible to the V_{OUT} and GND connection of the LTM8003.
4. Place the C_{IN} and C_{OUT} capacitors such that their ground current flow directly adjacent to or underneath the LTM8003.
5. Connect all of the GND connections to as large a copper pour or plane area as possible on the top layer. Avoid breaking the ground connection between the external components and the LTM8003.
6. Use vias to connect the GND copper area to the board's internal ground planes. Liberally distribute these GND vias to provide both a good ground connection and thermal path to the internal planes of the printed circuit board. Pay attention to the location and density of the thermal vias in Figure 5. The LTM8003 can benefit from the heat-sinking afforded by vias that connect to internal GND planes at these locations, due to their proximity to internal power handling components. The optimum

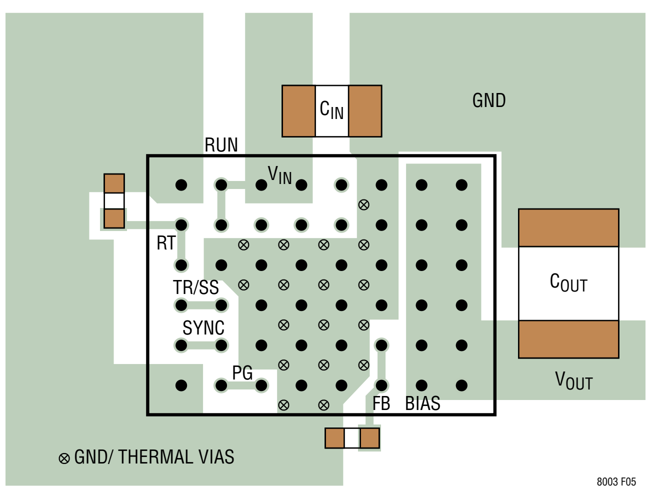

Figure 5. Layout Showing Suggested External Components, GND Plane and Thermal Vias

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number of thermal vias depends upon the printed circuit board design. For example, a board might use very small via holes. It should employ more thermal vias than a board that uses larger holes.

Hot-Plugging Safely

The small size, robustness and low impedance of ceramic capacitors make them an attractive option for the input bypass capacitor of LTM8003. However, these capacitors can cause problems if the LTM8003 is plugged into a live supply (see Linear Technology Application Note 88 for a complete discussion). The low loss ceramic capacitor combined with stray inductance in series with the power source forms an underdamped tank circuit, and the voltage at the V_{IN} pin of the LTM8003 can ring to more than twice the nominal input voltage, possibly exceeding the LTM8003's rating and damaging the part. If the input supply is poorly controlled or the LTM8003 is hot-plugged into an energized supply, the input network should be designed to prevent this overshoot. This can be accomplished by installing a small resistor in series to V_{IN}, but the most popular method of controlling input voltage overshoot is add an electrolytic bulk cap to the V_{IN} net. This capacitor's relatively high equivalent series resistance damps the circuit and eliminates the voltage overshoot. The extra capacitor improves low frequency ripple filtering and can slightly improve the efficiency of the circuit, though it is likely to be the largest component in the circuit.

Thermal Considerations

The LTM8003 output current may need to be derated if it is required to operate in a high ambient temperature. The amount of current derating is dependent upon the input voltage, output power and ambient temperature. The derating curves given in the Typical Performance Characteristics section can be used as a guide. These curves were generated by the LTM8003 mounted to a 58cm^2 4-layer FR4 printed circuit board. Boards of other sizes and layer count can exhibit different thermal behavior, so it is incumbent upon the user to verify proper operation over the intended system's line, load and environmental operating conditions.

For increased accuracy and fidelity to the actual application, many designers use FEA (Finite Element Analysis) to predict thermal performance. To that end, Page 2 of the data sheet typically gives four thermal coefficients:

θ_{JA} – Thermal resistance from junction to ambient

$\theta_{JCbottom}$ – Thermal resistance from junction to the bottom of the product case

θ_{JCtop} – Thermal resistance from junction to top of the product case

θ_{JB} – Thermal resistance from junction to the printed circuit board.

While the meaning of each of these coefficients may seem to be intuitive, JEDEC has defined each to avoid confusion and inconsistency. These definitions are given in JESD 51-12, and are quoted or paraphrased below:

θ_{JA} is the natural convection junction-to-ambient air thermal resistance measured in a one cubic foot sealed enclosure. This environment is sometimes referred to as "still air" although natural convection causes the air to move. This value is determined with the part mounted to a JESD 51-9 defined test board, which does not reflect an actual application or viable operating condition.

$\theta_{JCbottom}$ is the junction-to-board thermal resistance with all of the component power dissipation flowing through the bottom of the package. In the typical µModule regulator, the bulk of the heat flows out the bottom of the package, but there is always heat flow out into the ambient environment. As a result, this thermal resistance value may be useful for comparing packages but the test conditions don't generally match the user's application.

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θ_{JCtop} is determined with nearly all of the component power dissipation flowing through the top of the package. As the electrical connections of the typical µModule regulator are on the bottom of the package, it is rare for an application to operate such that most of the heat flows from the junction to the top of the part. As in the case of $\theta_{JCbottom}$, this value may be useful for comparing packages but the test conditions don't generally match the user's application.

θ_{JB} is the junction-to-board thermal resistance where almost all of the heat flows through the bottom of the µModule regulator and into the board, and is really the sum of the $\theta_{JCbottom}$ and the thermal resistance of the bottom of the part through the solder joints and through a portion of the board. The board temperature is measured a specified distance from the package, using a two sided, two layer board. This board is described in JESD 51-9.

Given these definitions, it should now be apparent that none of these thermal coefficients reflects an actual physical operating condition of a µModule regulator. Thus, none of them can be individually used to accurately predict the thermal performance of the product. Likewise, it would be inappropriate to attempt to use any one coefficient to correlate to the junction temperature vs load graphs given in the product's data sheet. The only appropriate way to use the coefficients is when running a detailed thermal analysis, such as FEA, which considers all of the thermal resistances simultaneously.

A graphical representation of these thermal resistances is given in Figure 6. The blue resistances are contained within the µModule regulator, and the green are outside.

The die temperature of the LTM8003 must be lower than the maximum rating, so care should be taken in the layout of the circuit to ensure good heat sinking of the LTM8003. The bulk of the heat flow out of the LTM8003 is through the bottom of the package and the pads into the printed circuit board. Consequently a poor printed circuit board design can cause excessive heating, resulting in impaired performance or reliability. Please refer to the PCB Layout section for printed circuit board design suggestions.

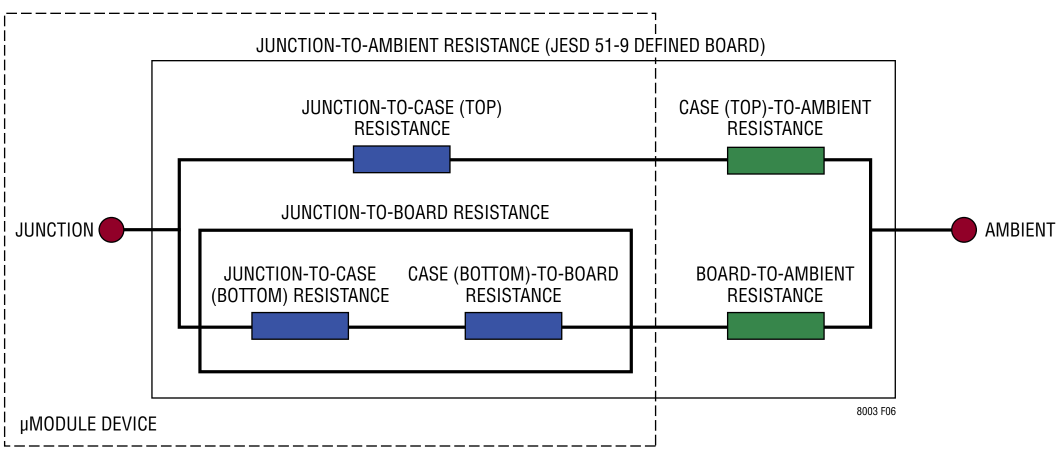

Figure 6. Graphical Representation of the Thermal Resistances Between the Device Junction and Ambient

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Fault Tolerance

The fixed output version of LTM8003 is designed to tolerate a single fault condition. Shorting two adjacent pins together or leaving one single pin floating does not raise V_{OUT} or cause damage to the LTM8003 μModule regulator.

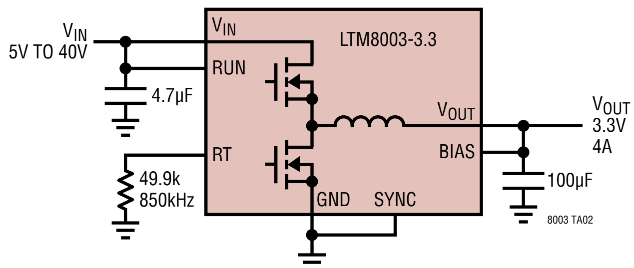
Table 2 describe the effects that result from shorting adjacent pins. Note that, since all pins are redundant, there is no analysis describing what happens when a single pin opens. The NC pins must be left floating to ensure fault tolerance.

Table 3. Table 2. FMEA Analysis — Adjacent Pin Short Test

PIN NAME	HEAT	SMOKE	EFFECT
V_{IN}–NC	NO	NO	Circuit behaves normally.
V_{IN}–RUN	NO	NO	Circuit behaves normally.
RUN–NC	NO	NO	Circuit behaves normally.
RUN–RT	NO	NO	V_{OUT} falls to 0V. Device can be damaged if EN/UV voltage is higher than RT ABS MAX.
RUN–GND	NO	NO	Vout falls to 0V.
RT–GND	NO	NO	SW frequency increases. V_{OUT} may fall below regulation voltage.
RT–GND BANK1	NO	NO	SW frequency increases. V_{OUT} may fall below regulation voltage.
RT–TRSS	NO	NO	V_{OUT} will fall below regulation voltage.
TR/SS–SYNC	NO	NO	V_{OUT} will fall below regulation voltage.
TR/SS–GND BANK1	NO	NO	V_{OUT} will fall below regulation voltage.
SYNC–GND	NO	NO	Circuit behaves normally.
SYNC–PG	NO	NO	Circuit behaves normally.
SYNC–GND BANK1	NO	NO	Circuit behaves normally.
BIAS–GND BANK1	NO	NO	Efficiency may decrease.
BIAS–V_{OUT} BANK3	NO	NO	Efficiency may decrease. If BIAS is tied to a voltage source > V_{OUT}, V_{OUT} may rise. If BIAS is tied to a votlage source < V_{OUT}, V_{OUT} may be reduced.
V_{OUT} BANK3–GND BANK1	NO	NO	V_{OUT} will fall to 0V.

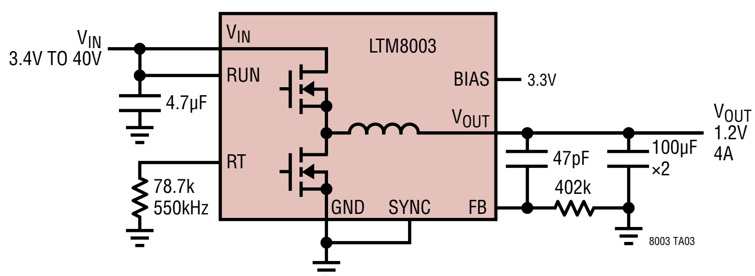
TYPICAL APPLICATIONS

3.3V$_{OUT}$ from 5V$_{IN}$ to 40V$_{IN}$ Step-Down Converter. BIAS Is Tied to V$_{OUT}$



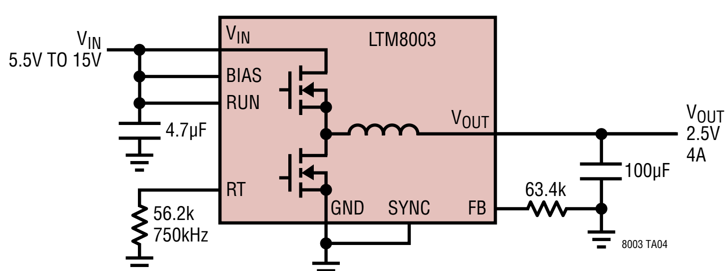
PINS NOT USED IN THIS CIRCUIT: TR/SS, PG

1.2V$_{OUT}$ from 3.4V$_{IN}$ to 40V$_{IN}$ Step-Down Converter. BIAS Is Tied to an External 3.3V Source



PINS NOT USED IN THIS CIRCUIT: TR/SS, PG

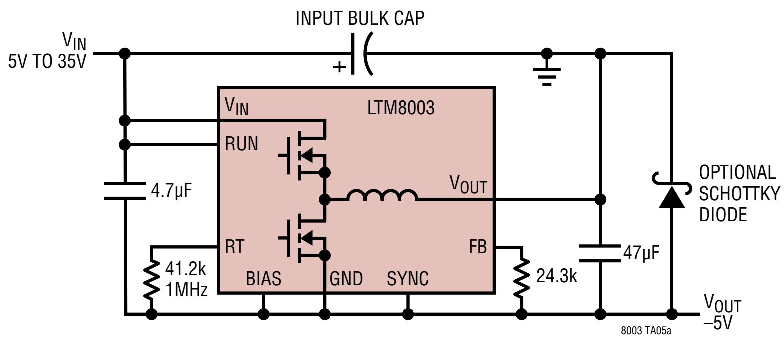
2.5V$_{OUT}$ from 5.5V$_{IN}$ to 15V$_{IN}$ Step-Down Converter. BIAS Is Tied to V$_{IN}$



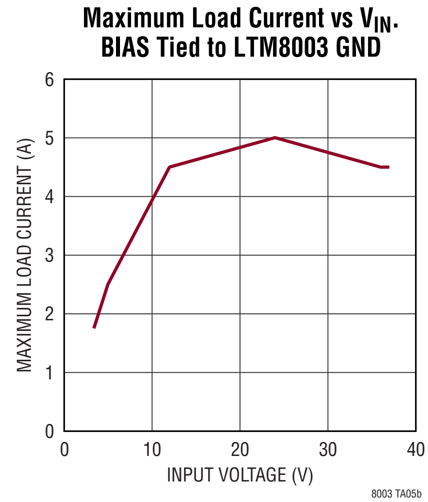
PINS NOT USED IN THIS CIRCUIT: TR/SS, PG

TYPICAL APPLICATIONS

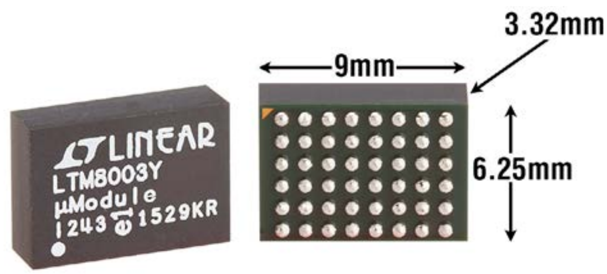
–5V_{OUT} from 5V_{IN} to 35V_{IN} Positive to Negative Converter, BIAS tied to LTM8003 GND



PINS NOT USED IN THIS CIRCUIT: TR/SS, PG



PACKAGE PHOTO



PACKAGE DESCRIPTION

Table 4

LTM8003 Pinout (Adjustable Version, Sorted by Pin Number)

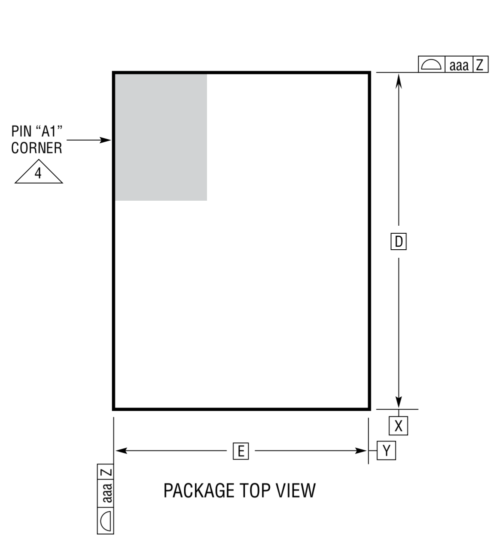
PIN		PIN NAME	PIN		PIN NAME	PIN		PIN NAME	PIN		PIN NAME	PIN		PIN NAME	PIN		PIN NAME	PIN		PIN NAME	PIN		PIN NAME
A	1	GND	B	1	PG	C	1	PG	D	1	GND	E	1	GND	F	1	FB	G	1	BIAS	H	1	V_{OUT}
A	2	SYNC	B	2	SYNC	C	2	GND	D	2	GND	E	2	GND	F	2	FB	G	2	BIAS	H	2	V_{OUT}
A	3	SS	B	3	SS	C	3	GND	D	3	GND	E	3	GND	F	3	GND	G	3	V_{OUT}	H	3	V_{OUT}
A	4	RT	B	4	GND	C	4	GND	D	4	GND	E	4	GND	F	4	GND	G	4	V_{OUT}	H	4	V_{OUT}
A	5	RT	B	5	RUN	C	5	NC	D	5	NC	E	5	NC	F	5	GND	G	5	V_{OUT}	H	5	V_{OUT}
A	6	GND	B	6	RUN	C	6	V_{IN}	D	6	V_{IN}	E	6	NC	F	6	GND	G	6	V_{OUT}	H	6	V_{OUT}

LTM8003 Pinout (Fixed Output Voltage, Sorted by Pin Number)

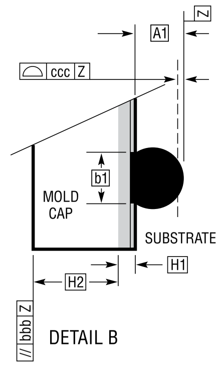
PIN		PIN NAME	PIN		PIN NAME	PIN		PIN NAME	PIN		PIN NAME	PIN		PIN NAME	PIN		PIN NAME	PIN		PIN NAME	PIN		PIN NAME
A	1	GND	B	1	PG	C	1	PG	D	1	GND	E	1	GND	F	1	GND	G	1	BIAS	H	1	V_{OUT}
A	2	SYNC	B	2	SYNC	C	2	GND	D	2	GND	E	2	GND	F	2	GND	G	2	BIAS	H	2	V_{OUT}
A	3	SS	B	3	SS	C	3	GND	D	3	GND	E	3	GND	F	3	GND	G	3	V_{OUT}	H	3	V_{OUT}
A	4	RT	B	4	GND	C	4	GND	D	4	GND	E	4	GND	F	4	GND	G	4	V_{OUT}	H	4	V_{OUT}
A	5	RT	B	5	RUN	C	5	NC	D	5	NC	E	5	NC	F	5	GND	G	5	V_{OUT}	H	5	V_{OUT}
A	6	GND	B	6	RUN	C	6	V_{IN}	D	6	V_{IN}	E	6	NC	F	6	GND	G	6	V_{OUT}	H	6	V_{OUT}

PACKAGE DESCRIPTION

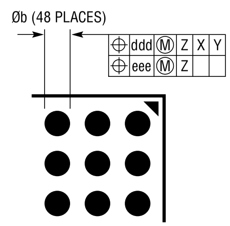
BGA Package
48-Lead (9mm × 6.25mm × 3.32mm)
(Reference LTC DWG # 05-08-1999 Rev B)



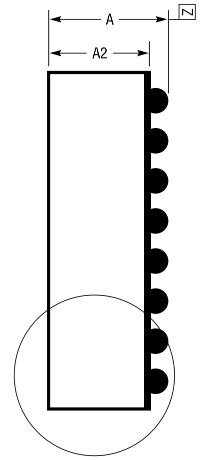
PACKAGE TOP VIEW



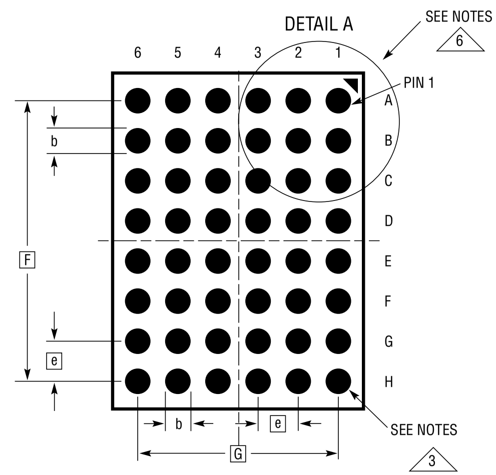
DETAIL B



DETAIL A

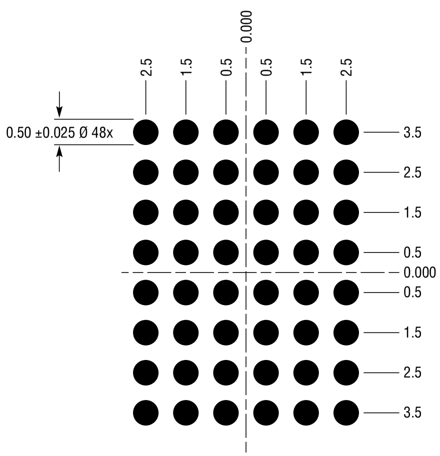


DETAIL B
PACKAGE SIDE VIEW



PACKAGE BOTTOM VIEW

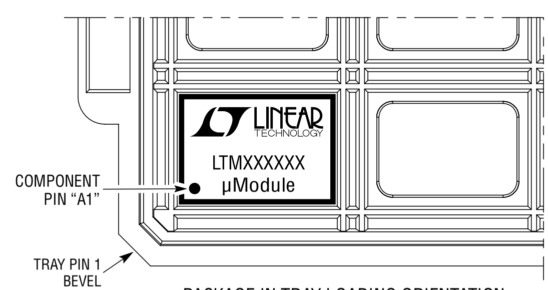
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. BALL DESIGNATION PER JEP95
4. DETAILS OF PIN #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE PIN #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE
5. PRIMARY DATUM -Z- IS SEATING PLANE
6. PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG µModule PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY



SUGGESTED PCB LAYOUT
TOP VIEW

	DIMENSIONS			
SYMBOL	MIN	NOM	MAX	NOTES
A	3.12	3.32	3.52	
A1	0.40	0.50	0.60	BALL HT
A2	2.72	2.82	2.92	
b	0.50	0.60	0.70	BALL DIMENSION
b1	0.47	0.50	0.53	PAD DIMENSION
D		9.00		
E		6.25		
e		1.00		
F		7.00		
G		5.00		
H1	0.27	0.32	0.37	SUBSTRATE THK
H2	2.45	2.50	2.55	MOLD CAP HT
aaa			0.15	
bbb			0.10	
ccc			0.20	
ddd			0.25	
eee			0.10	

TOTAL NUMBER OF BALLS: 48



PACKAGE IN TRAY LOADING ORIENTATION

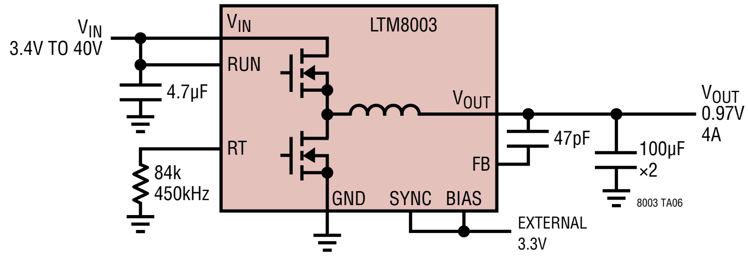
BGA 48 0517 REV B

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	2/17	Added "Silent Switcher" to product description and features.	1
		Added EMI performance graph.	13, 14
		Added Fault Tolerance section and FMEA analysis table.	25
B	5/17	Added LTM8003IY and LTM8003HY.	2
		Changed recommended BIAS pin connection from Open to GND for negative output applications.	5, 7, 11, 13, 14, 17, 19, 21, 27
C	12/17	Changed Peak Reflow Body Temperature from 260°C to 250°C.	2
D	7/18	Corrected graph title on p27 from Bias Open to Bias Tied to LTM8003 GND.	27
E	9/18	Corrected part numbers on the Order Information table: LTM8003-3.3IY#PBF to LTM8003IY-3.3#PBF LTM8003-3.3HY#PBF to LTM8003HY-3.3#PBF	2
		Updated package thermal resistance: θ_{JA} = 23.5°C/W to θ_{JA} = 24.7°C/W, $\theta_{JCbottom}$ = 3.2°C/W to $\theta_{JCbottom}$ = 4.5°C/W θ_{JCtop} = 17.9°C/W to θ_{JCtop} = 22.3°C/W, θ_{JB} = 3.1°C/W to θ_{JB} = 4.2°C/W	2
		Changed recommended BIAS voltage from 5 to, 3.2 to 19 on Table 1	17

TYPICAL APPLICATION

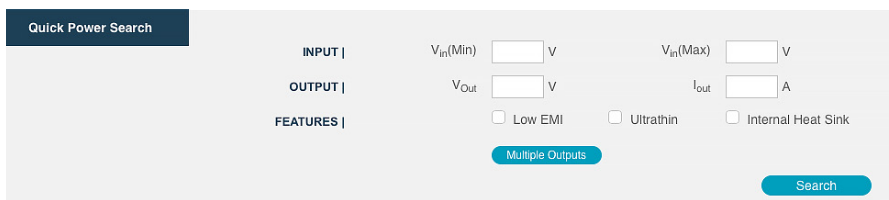
0.97V_{OUT} from 3.4V_{IN} to 40V_{IN} Step Down Converter with Spread Spectrum. BIAS is Tied to an External 3.3V Source



PINS NOT USED IN THIS CIRCUIT: TR/SS, PG

DESIGN RESOURCES

SUBJECT	DESCRIPTION	
µModule Design and Manufacturing Resources	Design: • Selector Guides • Demo Boards and Gerber Files • Free Simulation Tools	Manufacturing: • Quick Start Guide • PCB Design, Assembly and Manufacturing Guidelines • Package and Board Level Reliability
µModule Regulator Products Search	1. Sort table of products by parameters and download the result as a spread sheet. 2. Search using the Quick Power Search parametric table.	
Digital Power System Management	Analog Devices' family of digital power supply management ICs are highly integrated solutions that offer essential functions, including power supply monitoring, supervision, margining and sequencing, and feature EEPROM for storing user configurations and fault logging.	



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTM8002	Lower Current of LTM8003. 40V, 2.5A Step-Down Silent Switcher µModule Regulator with FMEA Compliant Pinout	3.4V ≤ V_{IN} ≤ 40V, 0.97V ≤ V_{OUT} ≤ 18V, 6.25mm × 6.25mm × 2.22mm BGA Package
LTM8053	40V, 3.5A Step-Down Silent Switcher µModule Regulator	3.4V ≤ V_{IN} ≤ 40V, 0.97V ≤ V_{OUT} ≤ 15V, 6.25mm × 9mm × 3.32mm BGA Package
LTM8063	40V, 2A Step-Down Silent Switcher µModule Regulator	3.2V ≤ V_{IN} ≤ 40V, 0.8V ≤ V_{OUT} ≤ 15V, 4mm × 6.25mm × 2.22mm BGA Package
LTM8065	40V, 2.5A Step-Down Silent Switcher µModule Regulator	3.4V ≤ V_{IN} ≤ 40V, 0.97V ≤ V_{OUT} ≤ 18V, 6.25mm × 6.25mm × 2.32mm BGA Package
LTM8032	36V, 2A Low EMI Step-Down µModule Regulator	3.6V ≤ V_{IN} ≤ 36V, 0.8V ≤ V_{OUT} ≤ 10V, EN55022B Compliant
LTM8033	36V, 3A Low EMI Step-Down µModule Regulator	3.6V ≤ V_{IN} ≤ 36V, 0.8V ≤ V_{OUT} ≤ 24V, EN55022B Compliant
LTM8026	36V, 5A CVCC Step-Down µModule Regulator	6V ≤ V_{IN} ≤ 36V, 1.2V ≤ V_{OUT} ≤ 24V, Constant Voltage Constant Current Operation
LTM4613	36V, 8A Low EMI Step-Down µModule Regulator	5V ≤ V_{IN} ≤ 36V, 3.3V ≤ V_{OUT} ≤ 15V, EN55022B Compliant
LTM8073	60V, 3A Step-Down Silent Switcher µModule Regulator	3.4V ≤ V_{IN} ≤ 60V, 0.8V ≤ V_{OUT} ≤ 15V, 6.25mm × 9mm × 3.32mm BGA Package

D17129-0-9/18(E)
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