Continued from preceding page.

- Stepping motor driver integrated in an MCP
  Saturation driven H bridge 4ch
  Built in thermal protection circuit
  Built in low voltage malfunction prevention circuit
  Built in transistor for photo sensor drive
  Two driver power supplies (VM : for motor, V_{CC} : for others)

- Operation Clock
  Clock generated from built in oscillation amplifier
  Clock input directly from CLKIN pin
  Selection with MODE1 pin
  Recommended drive frequency 24MHz, Permission drive frequency 15MHz to 36MHz

- Package
  FLGA49 (4mm × 4mm)
  Pb-Free
  Halogen Free

- Power supply voltage (Typical voltage)
  Logic LSI : Pin 3.3V, Inside 1.8V (External supply required)
  Driver LSI : VM 5.0V, V_{CC} 3.3V

Electrical Characteristics

Absolute Maximum Ratings at V_{SS} = 0V

Parameter	Symbol	Conditions	Ratings	unit
Power supply voltage	$V_{DD}18$ max	Ta ≤25°C	-0.3 to 3.6	V
	$V_{DD}33$ max	Ta ≤25°C	-0.3 to 4.6	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

D.C. Characteristics: Input/output level/V_{SS} = 0V, V_{DD} = 2.7 to 3.6V, Ta = -30 to 85°C

Parameter	Symbol	Conditions	min	typ	max	unit	Applicable pin
High-level input voltage	V_{IH}	CMOS schmidt	1.4			V	(1)
Low-level input voltage	V_{IL}				0.36	V	
High-level input voltage	V_{IH}	CMOS schmidt	1.4			V	(2)
Low-level input voltage	V_{IL}				0.50	V	
High-level input voltage	V_{IH}	CMOS schmidt	1.5			V	(3)
Low-level input voltage	V_{IL}				0.36	V	

*Applicable pin
(1)ZRESET
(2)CLKIN
(3)SCLK, MOSI

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

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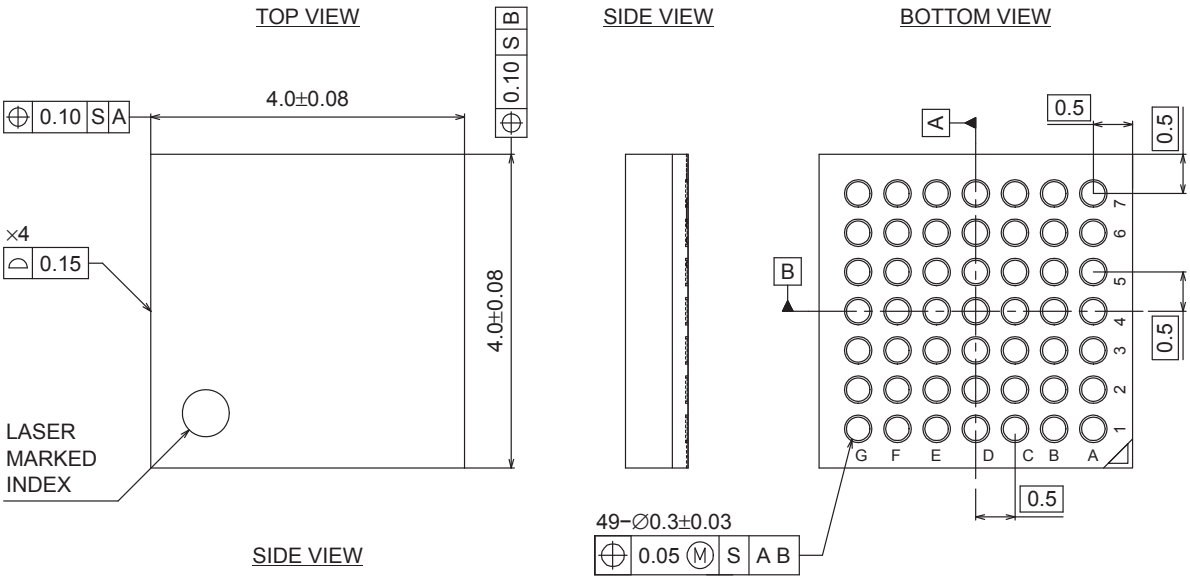
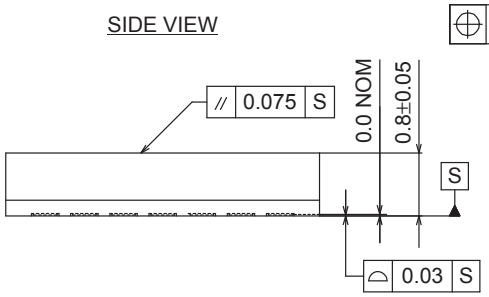
Package Dimensions

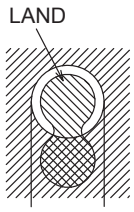
unit : mm

LFLGA49 4x4 / FLGA49
CASE 569AM
ISSUE A





NSMD
Off set Via type

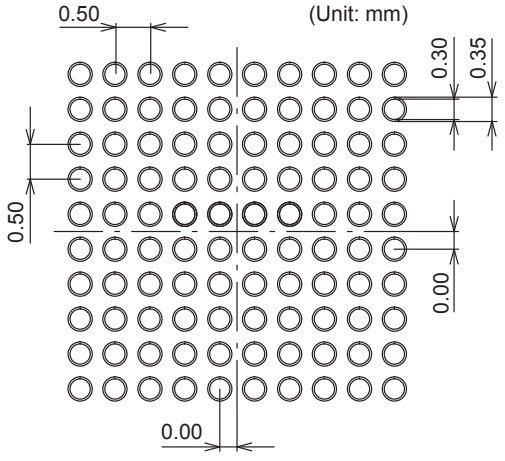


GENERIC MARKING DIAGRAM*

XXXXX = Specific Device Code
Y = Year
M = Month
DDD = Additional Traceability Data

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, “G” or microdot “▪”, may or may not be present.

SOLDERING FOOTPRINT*



NOTE: The measurements are not to guarantee but for reference only.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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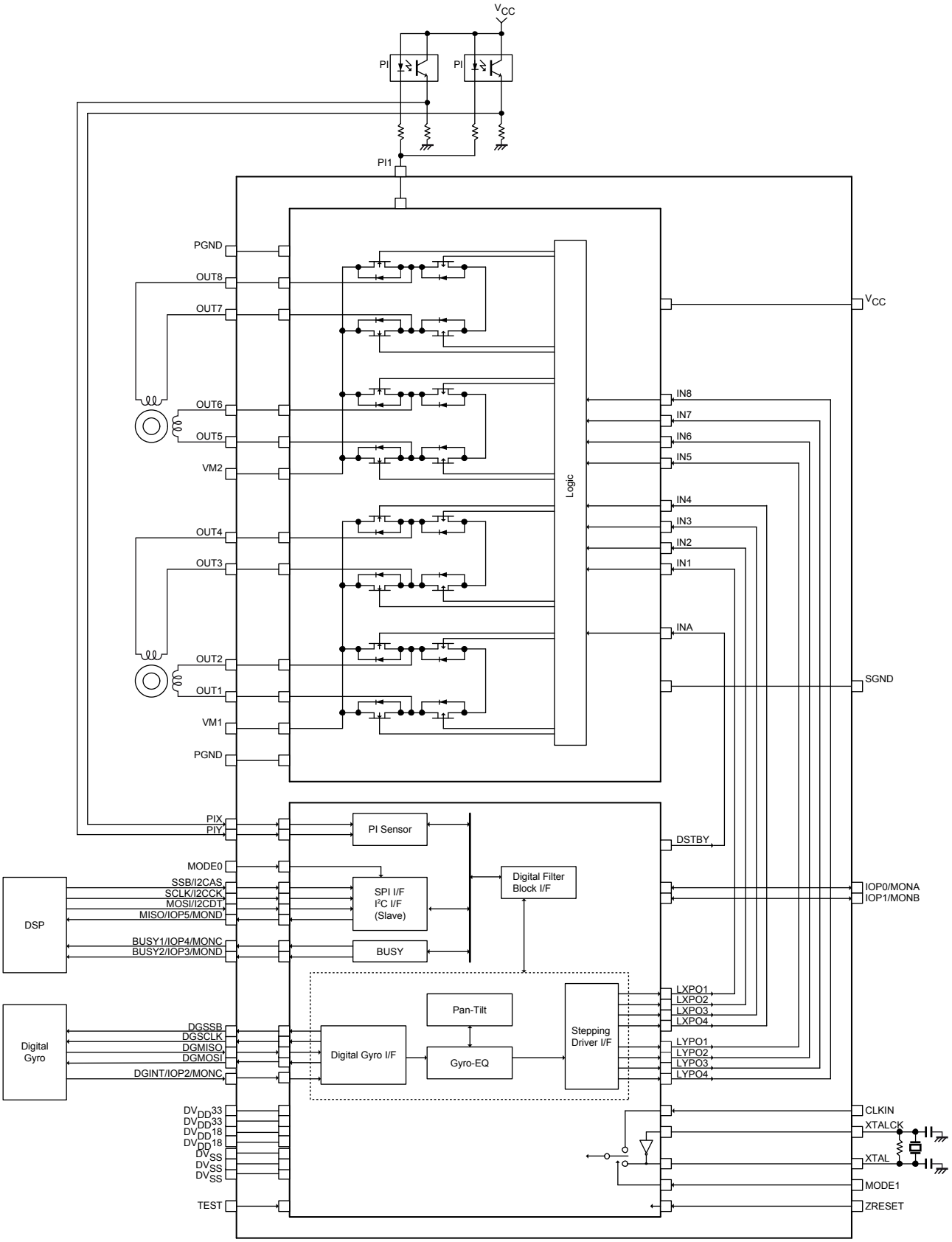
Block Diagram



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Pin Description

TYPE					
I	INPUT	P	Power, GND	NC	NOT CONNECT
O	OUTPUT				
B (I)	BIDIRECTION : INPUT at reset				
B (O)	BIDIRECTION : OUTPUT at reset				

Logic LSI

SPI/I^{2}C interface (Slave)

SSB/I2CSA	I	SPI chip select/ I^{2}C slave address select (L: 0100100, H: 0100101, Please make sure to connect the pin to L level or H level.)
SCLK/I2CCK	B (I)	SPI clock/I^{2}C clock
MOSI/I2CDT	B (I)	SPI received data/I^{2}C data
MISO/IOP5/MOND	B (O)	SPI transmit data/Monitor pin

Sensor output signal input for reference point detection

PIX	B(I)
PIY	B(I)

Digital gyro interface

DGSSB	O	Digital gyro I/F chip select
DGSCLK	O	Digital gyro I/F transfer clock
DGMOSI	O	Digital gyro I/F transmit data
DGMISO	I	Digital gyro I/F received data
DGINT/IOP2/MONC	B (I)	Digital gyro I/F timing signal/General-purpose port/Monitor pin

PIO interface

IOP0/MONA	B (I)	General-purpose port/Monitor pin
IOP1/MONB	B (I)	General-purpose port/Monitor pin

BUSY flag

BUSY1/IOP4/MONC	B (O)	BUSY pin (RAM access BUSY signal when SPI I/F is selected)
BUSY2/IOP3/MOND	B (O)	BUSY pin (Stepping motor force movement busy, measurement busy etc.)

Clock, Reset pin

XTALCK	I	Oscillation amplifier input (recommended drive frequency : 24MHz, permission drive frequency : 15MHz to 36MHz)
XTAL	O	Oscillation amplifier output
CLKIN	I	Clock input (Refer to XTALCK description about both recommended and permission drive frequency)
ZRESET	I	Power-on reset

Mode select pin

MODE0	I	Interface select : L→SPI, H→I^{2}C
MODE1	I	Clock select : L→XTALCK/XTAL use, H→CLKIN use

Test pin

TEST	I	For test mode setting (fixed to L for normal operation)

Power supply pin

$DV_{DD}33$	P	3.3V digital power supply
$DV_{DD}18$	P	1.8V digital power supply
DV_{SS}	P	Digital ground

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***Process when pins are not used**

PIN TYPE "O" —— The pin must be left open.
PIN TYPE "I" —— The pin must not be left open. Please make sure to connect the pin to V_{DD} or V_{SS} even when it is not used. (Please check with us whether to connect to V_{DD} or V_{SS}.)
PIN TYPE "B" —— Please contact us if you are uncertain about a processing method in the pin description in the PIN layout table.

A problem may occur if the processing method is used wrongly for any unused pin.
Please make sure to contact us.

Driver LSI

Saturation-driven H bridge output

OUT1 to OUT8	O	Motor control pulse output

Power supply pin

VM1,VM2	P	Motor power supply
V_{CC}	P	Other power supply
SGND	P	Signal ground
PGND	P	Power ground

Photo sensor pin

PI1	I	Photo sensor connectiong pin

Pin Assignment

Top View

	A	B	C	D	E	F	G
7	OUT7	OUT8	PGND2	VM2	DV_{SS}	IOP1	CLKIN
6	OUT6	NC	NC	$DV_{DD}33$	$DV_{DD}18$	PIX	XTAL
5	OUT5	NC	DGMISO	ZRESET	DV_{SS}	PIY	XTALCK
4	OUT4	DGINT	DGSSB	DGMOSI	BUSY2	BUSY1	MODE1
3	OUT3	NC	DGSCLK	MODE0	SSB	MOSI	SCLK
2	OUT2	IOP0	NC	TEST	$DV_{DD}18$	MISO	$DV_{DD}33$
1	PGND1	OUT1	VM1	V_{CC}	SGND	PI1	DV_{SS}

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ORDERING INFORMATION

Device	Package	Shipping (Qty / Packing)
LC898113-TBM-H	LFLGA49 4x4 / FLGA49 (Pb-Free / Halogen Free)	2000 / Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D. http://www.onsemi.com/pub_link/Collateral/BRD8011-D.PDF

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