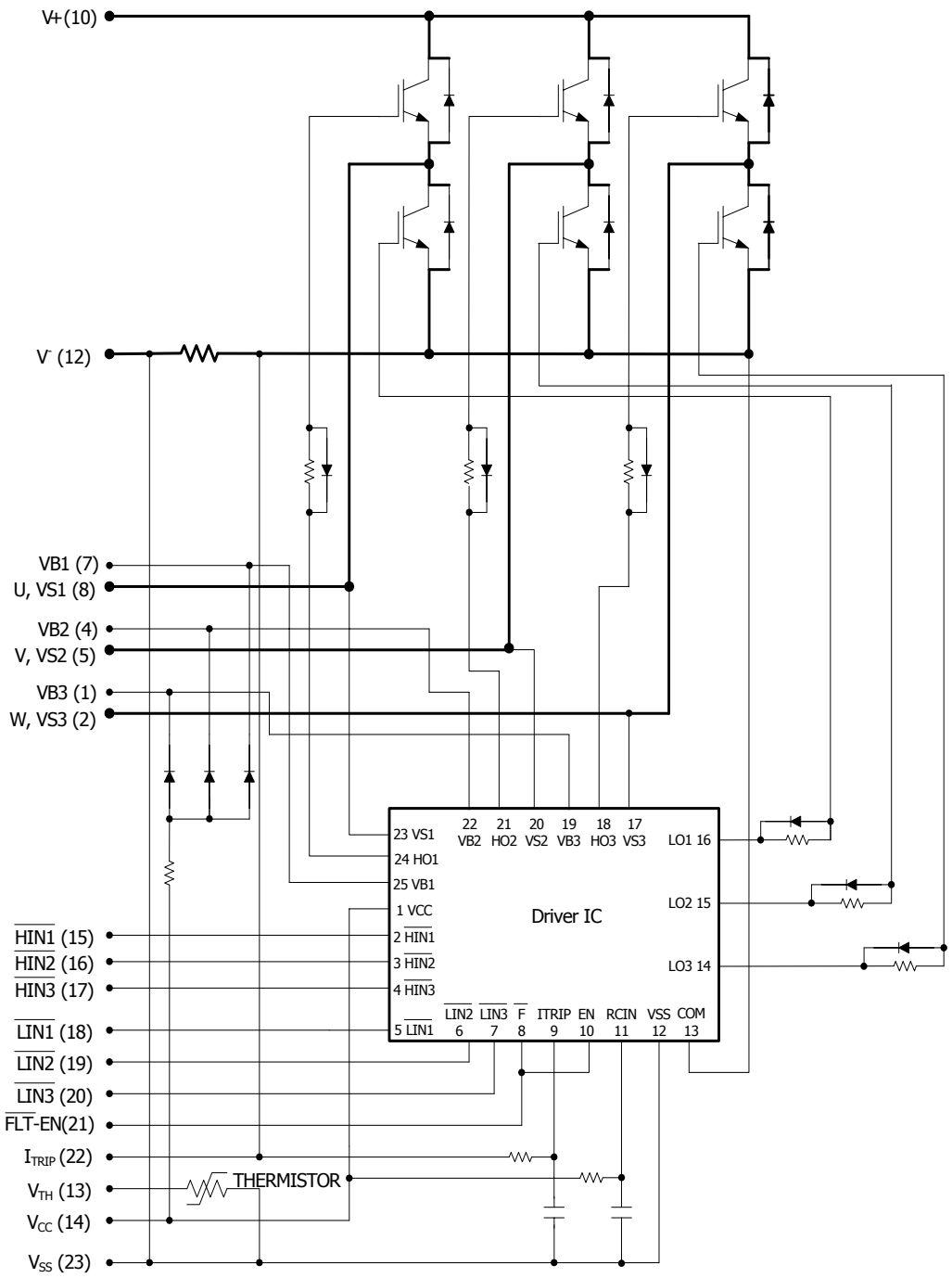
## Internal Electrical Schematic - IRAMS06UP60B



## Inverter Section Electrical Characteristics @ $T_J$ = 25°C

| Symbol | Parameter | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| $V_{(BR)CES}$ | Collector-to-Emitter Breakdown Voltage | 600 | --- | --- | V | $V_{IN}$=5V, $I_C$=250µA |
| $\Delta V_{(BR)CES}$ / $\Delta T$ | Temperature Coeff. Of Breakdown Voltage | --- | 0.3 | --- | V/°C | $V_{IN}$=5V, $I_C$=1.0mA (25°C - 150°C) |
| $V_{CE(ON)}$ | Collector-to-Emitter Saturation Voltage | --- | 1.9 | 2.4 | V | $I_C$=3A, $V_{DD}$=15V |
| | | --- | 2.2 | 2.6 | | $I_C$=3A, $V_{DD}$=15V, $T_J$=150°C |
| $I_{CES}$ | Zero Gate Voltage Collector-to-Emitter Current | --- | 15 | 45 | µA | $V_{IN}$=5V, $V^+$=600V |
| | | --- | 60 | 170 | | $V_{IN}$=5V, $V^+$=600V, $T_J$=150°C |
| $I_{lk\_module}$ | Zero Gate Phase-to-Phase Current | -- | -- | 50 | µA | $V_{IN}$=5V, $V^+$=600V |
| $V_{FM}$ | Diode Forward Voltage Drop | --- | 1.45 | 1.85 | V | $I_C$=3A |
| | | --- | 1.25 | 1.65 | | $I_C$=3A, $T_J$=150°C |
| $I_{BUS\_Trip}$ | Current Protection Threashold (positive going) | 8.5 | --- | 10.5 | A | $T_j$=-40°C to 150°C (Overcurrent duration ≥ 6µs) |

## Inverter Section Switching Characteristics @ $T_J$ = 25°C

| Symbol | Parameter | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| $E_{on}$ | Turn-On Switching Loss | --- | 130 | 235 | µJ | $I_C$=3A, $V^+$=400V |
| $E_{off}$ | Turn-Off Switching Loss | --- | 65 | 120 | | $V_{DD}$=15V, L=1mH |
| $E_{tot}$ | Total Switching Loss | --- | 195 | 355 | | See CT1 $T_J$=25°C |
| $E_{on}$ | Turn-on Swtiching Loss | --- | 200 | 345 | µJ | See CT1 $T_J$=150°C |
| $E_{off}$ | Turn-off Switching Loss | --- | 90 | 150 | | Energy losses include "tail" and |
| $E_{tot}$ | Total Switching Loss | --- | 290 | 495 | | diode reverse recovery |
| $E_{rec}$ | Diode Rev. Recovery energy | --- | 50 | 110 | µJ | $T_J$=150°C, $V^+$ =400V $V_{DD}$=15V, |
| $t_{rr}$ | Diode Reverse Recovery time | --- | 150 | 200 | ns | $I_F$=3A, L=1mH |
| RBSOA | Reverse Bias Safe Operating Area | FULL SQUARE | | | | $T_J$=150°C, $I_C$=3A, $V_P$=600V $V^+$=480V, $V_{DD}$=+15V to 0V See CT3 |
| SCSOA | Short Circuit Safe Operating Area | 10 | --- | --- | µs | $T_J$=150°C, $V_P$=600V, $V^+$=360V, $V_{DD}$=+15V to 0V See CT2 |

## Thermal Resistance

| Symbol | Parameter | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| $R_{th(J-C)}$ | Junction to case thermal resistance, each IGBT under inverter operation. | --- | --- | 6.5 | °C/W | Flat, greased surface. Heatsink compound thermal conductivity - 1W/mK |
| $R_{th(J-C)}$ | Junction to case thermal resistance, each Diode under inverter operation. | --- | --- | 9 | °C/W | |
| $R_{th(C-S)}$ | Case to sink thermal resistance | --- | 0.1 | --- | °C/W | |

## Absolute Maximum Ratings Driver Function

Absolute Maximum Ratings indicate substained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to $V_{SS}$ . (Note 2)

| Symbol | Definition | Min | Max | Units |
|---|---|---|---|---|
| $V_{S1,2,3}$ | High Side offset voltage | -0.3 | 600 | V |
| $V_{B1,2,3}$ | High Side floating supply voltage | -0.3 | 20 | V |
| $V_{DD}$ | Low Side and logic fixed supply voltage | -0.3 | 20 | V |
| $V_{IN}$ | Input voltage LIN, HIN, T/$I_{TRIP}$ | -0.3 | $V_{SS}$+15 | V |
| $T_J$ | Juction Temperature | -40 | 150 | °C |

## Recommended Operating Conditions Driver Function

The Input/Output logic timing diagram is shown in Figure 1. For proper operation the device should be used within the recommended conditions. All voltages are absolute referenced to $V_{SS}$. The $V_S$ offset is tested with all supplies biased at 15V differential (Note 2). All input pin ($V_{IN}$ ) and $I_{TRIP}$ are clamped with a 5.2V zener diode and pull-up resistor to $V_{DD}$.

| Symbol | Definition | Min | Max | Units |
|---|---|---|---|---|
| $V_{B1,2,3}$ | High side floating supply voltage | $V_S$+12 | $V_S$+20 | V |
| $V_{S1,2,3}$ | High side floating supply offset voltage | Note 3 | 450 | |
| $V_{DD}$ | Low side and logic fixed supply voltage | 12 | 20 | V |
| $V_{IN}$ | Logic input voltage LIN, HIN | $V_{SS}$ | $V_{SS}$+5 | V |

## Static Electrical Characteristics Driver Function

$V_{BIAS}$ ($V_{DD}$, $V_{BS1,2,3}$)=15V, unless otherwise specified. The $V_{IN}$ and $I_{IN}$ parameters are referenced to $V_{SS}$ and are applicable to all six channels. (Note 2)

| Symbol | Definition | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| $V_{IN,th+}$ | Positive going input threshold | 3.0 | --- | --- | V |
| $V_{IN,th-}$ | Negative going input threshold | --- | --- | 0.8 | V |
| $V_{CCUV+}$<br>$V_{BSUV+}$ | $V_{CC}$ and $V_{BS}$ supply undervoltage<br>Positive going threshold | 10.6 | 11.1 | 11.6 | V |
| $V_{CCUV-}$<br>$V_{BSUV-}$ | $V_{CC}$ and $V_{BS}$ supply undervoltage<br>Negative going threshold | 10.4 | 10.9 | 11.4 | V |
| $V_{CCUVH}$<br>$V_{BSUVH}$ | $V_{CC}$ and $V_{BS}$ supply undervoltage<br>$I_{lockout}$ hysteresis | --- | 0.2 | --- | V |
| $I_{QBS}$ | Quiescent $V_{BS}$ supply current | --- | 70 | 120 | µA |
| $I_{QCC}$ | Quiscent $V_{CC}$ supply current | --- | 1.6 | 2.3 | mA |
| $I_{LK}$ | Offset Supply Leakage Current | --- | --- | 50 | µA |
| $I_{IN+}$ | Input bias current (OUT=LO) | --- | 100 | 220 | µA |
| $I_{IN+}$ | Input bias current (OUT=HI) | --- | 200 | 300 | µA |
| $V(I_{TRIP})$ | $I_{TRIP}$ threshold Voltage (OUT=HI or OUT=LO) | 0.44 | 0.49 | 0.54 | V |

## Dynamic Electrical Characteristics

$V_{DD}$=$V_{BS}$=$V_{BIAS}$=15V, $PWM_{IN}$=2kHz, $V_{IN\_ON}$=$V_{IN\_th+}$, $V_{IN\_OFF}$=$V_{IN\_th-}$
$T_A$=25°C, unless otherwise specified

| Symbol | Definition | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| $T_{ON}$ | Input to output propagation turn-on delay time (see fig.11) | - | 470 | - | ns |
| $T_{OFF}$ | Input to output propagation turn-off delay time (see fig. 11) | - | 615 | - | ns |
| $D_T$ | Dead Time | - | 290 | - | ns |
| $I/T_{Trip}$ | $T/I_{Trip}$ to six switch to turn-off propagation delay (see fig. 2) | - | 750 | - | ns |
| $T_{FCLTRL}$ | Post $I_{Trip}$ to six switch to turn-off clear time (see fig. 2) | - | 9 | - | ms |

## Internal NTC - Thermistor Characteristics

| Parameter | | Typ | Units | Conditions |
|---|---|---|---|---|
| $R_{25}$ | Resistance | 100 +/- 3% | kΩ | $T_C$ = 25°C |
| $R_{125}$ | Resistance | 2.522 ±10.9% | kΩ | $T_C$ = 125°C |
| B | B-constant (25-50°C) | 4250 +/- 2% | k | $R_2 = R_1 e^{[B(1/T2 - 1/T1)]}$ |
| Temperature Range | | -40 / 125 | °C | |
| Typ. Dissipation constant | | 1 | mW/°C | $T_C$ = 25°C |

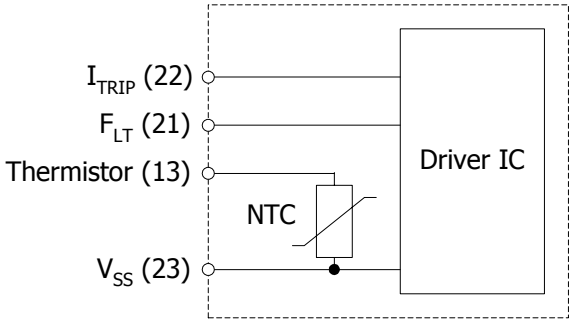
## Internal Current Sensing Resistor - Shunt Characteristics

| Parameter | | Units |
|---|---|---|
| Resistance | 50 ±1% | mΩ |
| Tollerance | ±1% | |
| Max Power Dissipation | 1.5 | W |
| Temperature Range | -40 / 125 | °C |

Note 2: For more details, see IR21363 data sheet

Note 3: Logic operational for $V_S$ from $V^-$ -5V to $V^-$ +600V. Logic state held for $V_S$ from $V^-$ -5V to $V^-$ -$V_{BS}$. (please refer to DT97-3 for more details)

### Thermistor Built-in IRAMS06UP60B




Note 4: The Maximum recommended sense voltage at the $I_{TRIP}$ terminal under normal operating conditions is 3.3V.

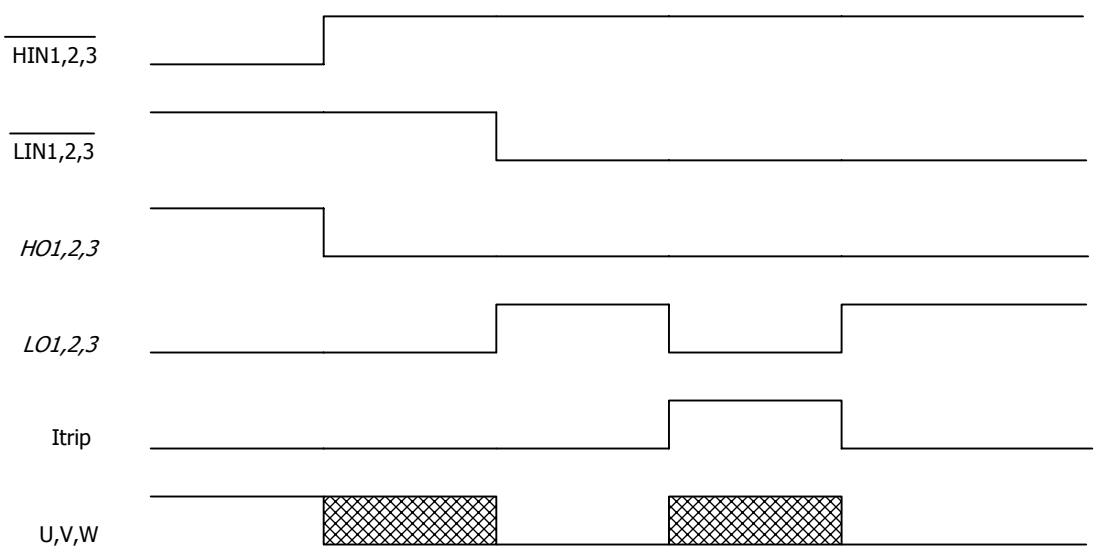
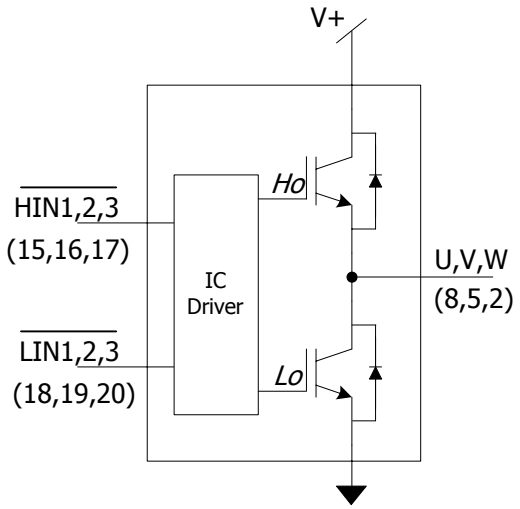
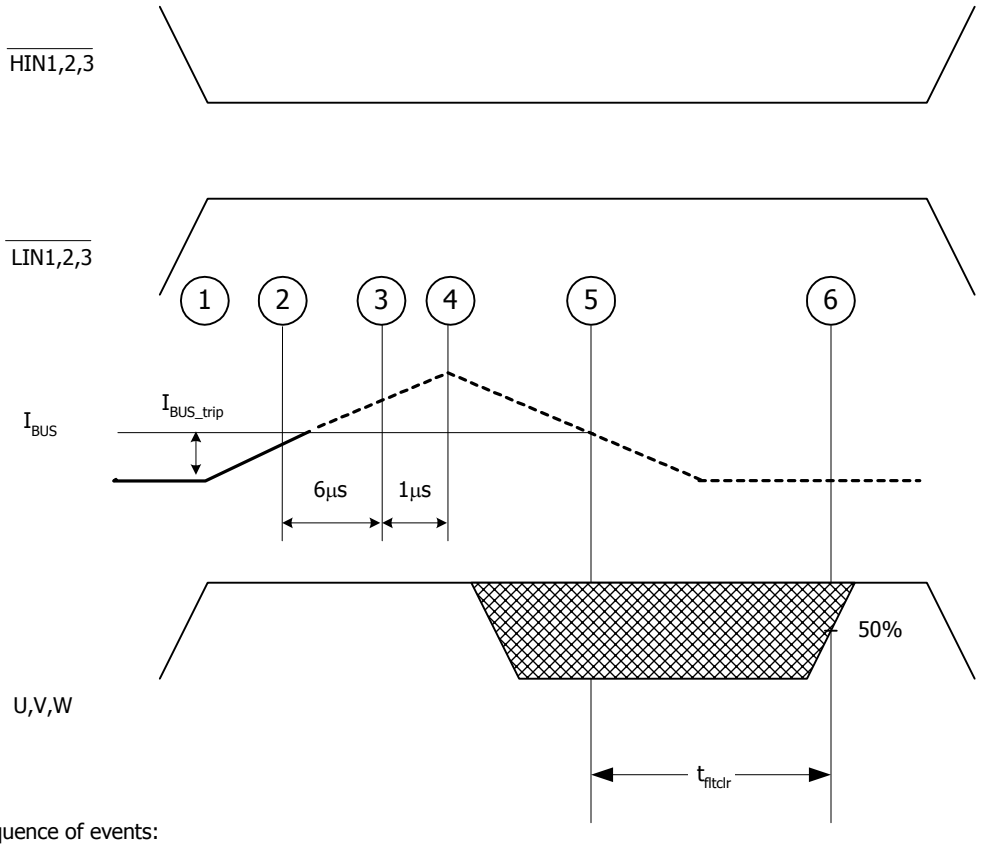



Figure1. Input/Output Timing Diagram

Note 5: The shaded area indicates that both high-side and low-side switches are off and therefore the half-bridge output voltage would be determined by the direction of current flow in the load.




| Itrip | $\overline{HIN1,2,3}$ | $\overline{LIN1,2,3}$ | U,V,W |
|---|---|---|---|
| 0 | 0 | 1 | V+ |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | X |
| 1 | X | X | X |




Sequence of events:
1-2) Current begins to rise
2) Current reaches $I_{BUS\_Trip}$ level
2-3) Current is higher than $I_{BUS\_Trip}$ for at least 6µs. This value is the worst-case condition with very low over-current. In case of high current (short circuit), the actual delay will be smaller.
3-4) Delay between driver identification of over-current condition and disabling of all outputs
4) Current starts decreasing, eventually reaching 0
5) Current goes below $I_{BUS\_trip}$, the driver starts its auto-reset sequence
6) Driver is automatically reset and normal operation can resume (over-current condition must be removed by the time the drivers automatically resets itself)

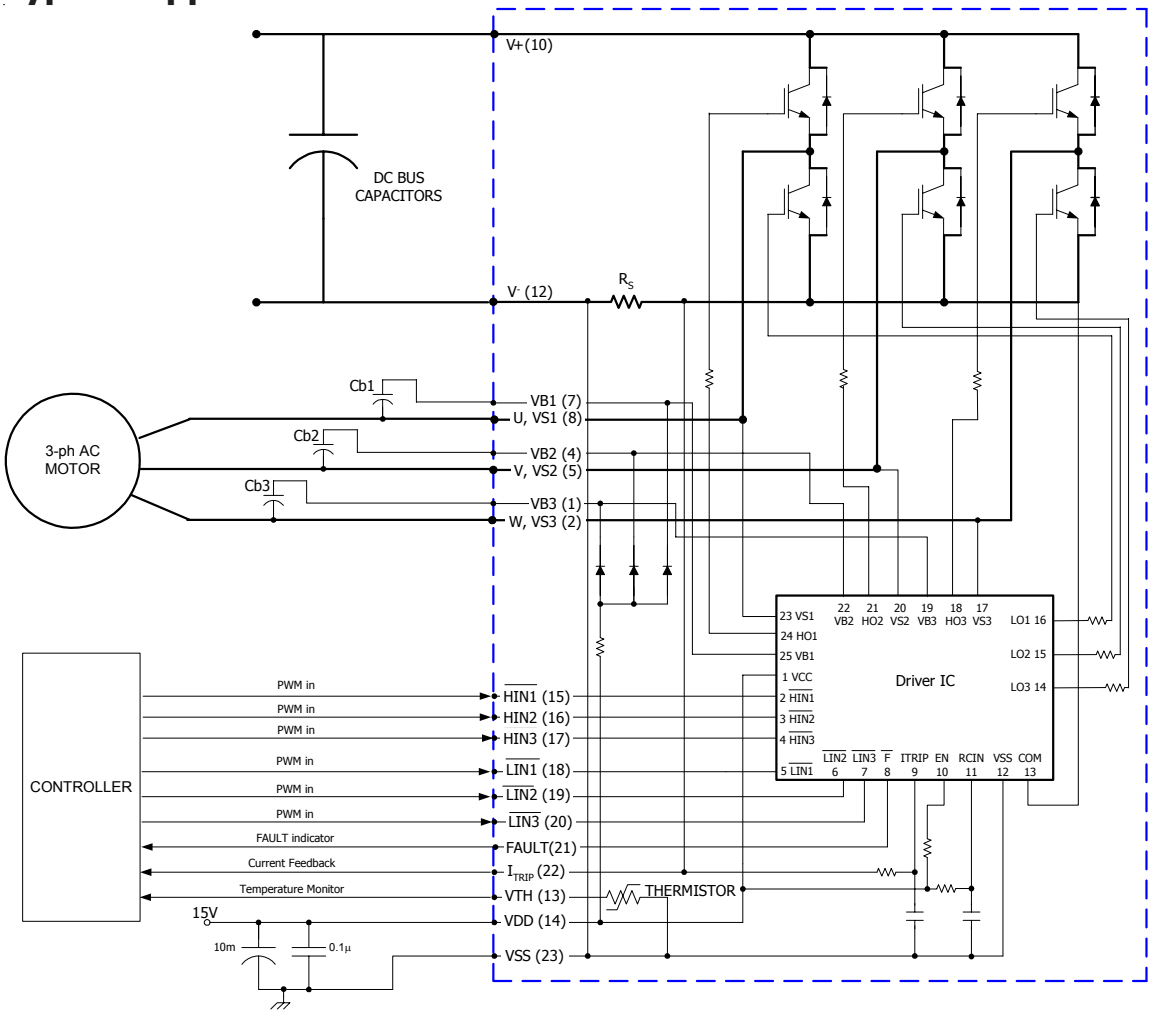
Figure 2. $I_{Trip}$ Timing Waveform

Note 6: The shaded area indicates that both high-side and low-side switches are off and therefore the half-bridge output voltage would be determined by the direction of current flow in the load.

## Module Pin-Out Description

| Pin | Name | Description |
|---|---|---|
| 1 | $V_{B3}$ | High Side Floating Supply Voltage 3 |
| 2 | W,$V_{S3}$ | Output 3 - High Side Floating Supply Offset Voltage |
| 3 | NA | none |
| 4 | $V_{B2}$ | High Side Floating Supply voltage 2 |
| 5 | V,$V_{S2}$ | Output 2 - High Side Floating Supply Offset Voltage |
| 6 | NA | none |
| 7 | $V_{B1}$ | High Side Floating Supply voltage 1 |
| 8 | U, $V_{S1}$ | Output 1 - High Side Floating Supply Offset Voltage |
| 9 | NA | none |
| 10 | $V^+$ | Positive Bus Input Voltage |
| 11 | NA | none |
| 12 | $V^-$ | Negative Bus Input Voltage |
| 13 | $V_{TH}$ | Temperature Feedback |
| 14 | $V_{CC}$ | +15V Main Supply |
| 15 | $\overline{H_{IN1}}$ | Logic Input High Side Gate Driver - Phase 1 |
| 16 | $\overline{H_{IN2}}$ | Logic Input High Side Gate Driver - Phase 2 |
| 17 | $\overline{H_{IN3}}$ | Logic Input High Side Gate Driver - Phase 3 |
| 18 | $\overline{L_{IN1}}$ | Logic Input Low Side Gate Driver - Phase 1 |
| 19 | $\overline{L_{IN2}}$ | Logic Input Low Side Gate Driver - Phase 2 |
| 20 | $\overline{L_{IN3}}$ | Logic Input Low Side Gate Driver - Phase 3 |
| 21 | $\overline{FLT}$/Enable | Fault Output and Enable Pin |
| 22 | $I_{TRIP}$ | Current Sense and Itrip Pin |
| 23 | $V_{SS}$ | Negative Main Supply |

## Typical Application Connection IRAMS06UP60B




1. Electrolytic bus capacitors should be mounted as close to the module bus terminals as possible to reduce ringing and EMI problems. Additional high frequency ceramic capacitor mounted close to the module pins will further improve performance.

2. In order to provide good decoupling between $V_{CC}$-Gnd and $V_B$-$V_{SS}$ terminals, the capacitors shown connected between these terminals should be located very close to the module pins. Additional high frequency capacitors, typically 0.1µF, are strongly recommended.

3. Value of the boot-strap capacitors depends upon the switching frequency. Their selection should be made based on IR design tip DN 98-2a, application note AN-1044 or Figure 9.

4. Current sense signal can be obtained from pin 22 and pin 23

5. After approx. 9 ms the FAULT is reset

6.PWM generator must be disabled within Fault duration to garantee shutdown of the system, overcurrent condition must be cleared before resuming operation

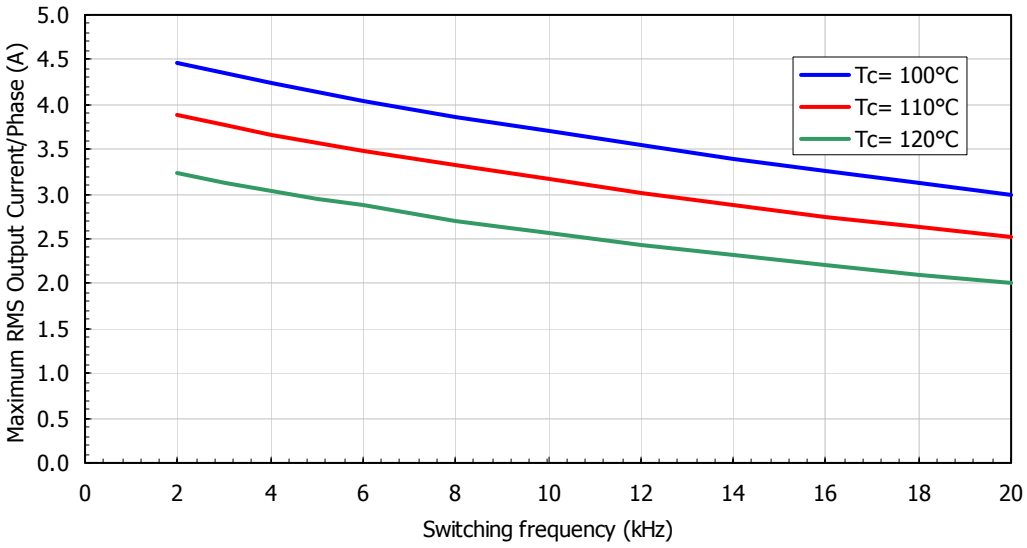



Figure 3. Maximum sinusoidal phase current as function of switching frequency
V+ = 400V, $T_j$=150°C, Modulation Depth=0.8, PF=0.6

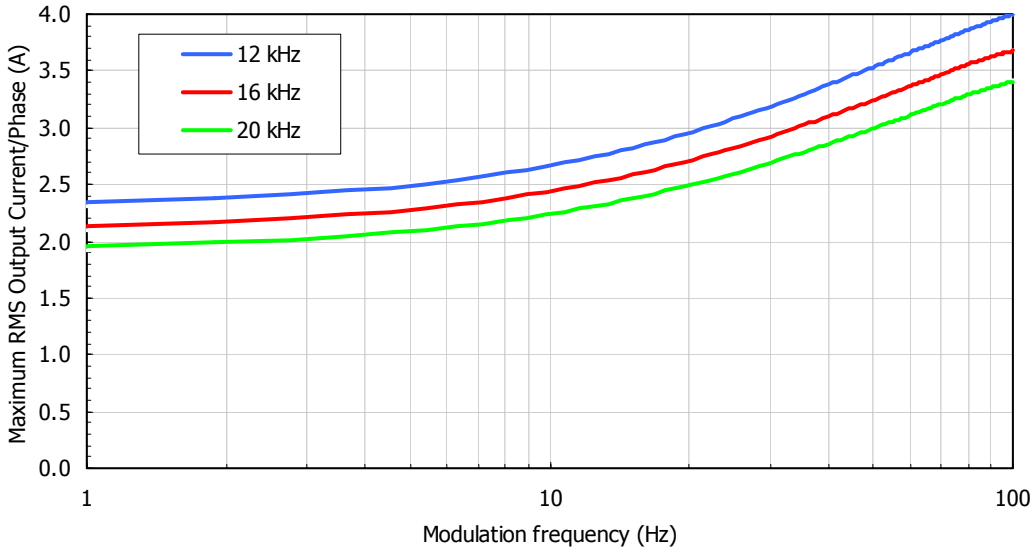



Figure 4. Maximum sinusoidal phase current as function of modulation frequency
V+=400V, $T_j$=150°C, $T_c$=100°C, Modulation Depth=0.8, PF=0.6

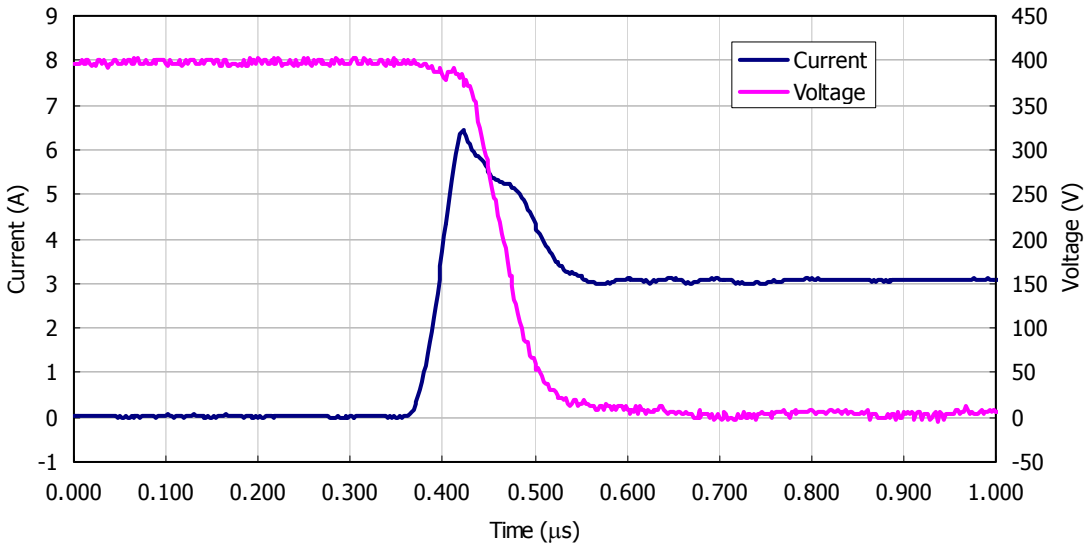



Figure 5. IGBT Turn-on. Typical turn-on waveform @$T_j$=125°C, V+=400V

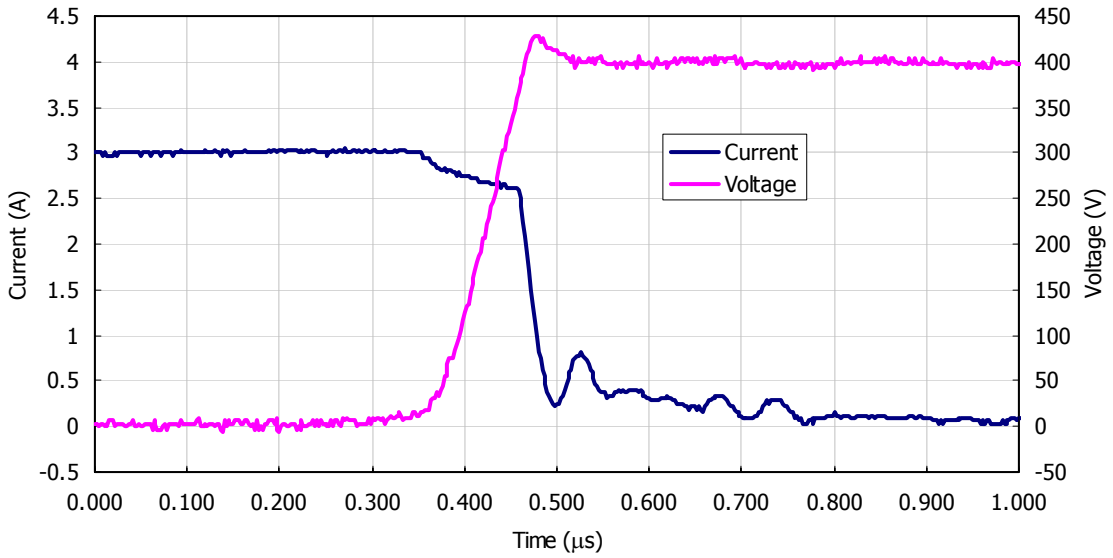



Figure 6. IGBT Turn-off. Typical turn-off waveform @$T_j$=125°C, V+=400V

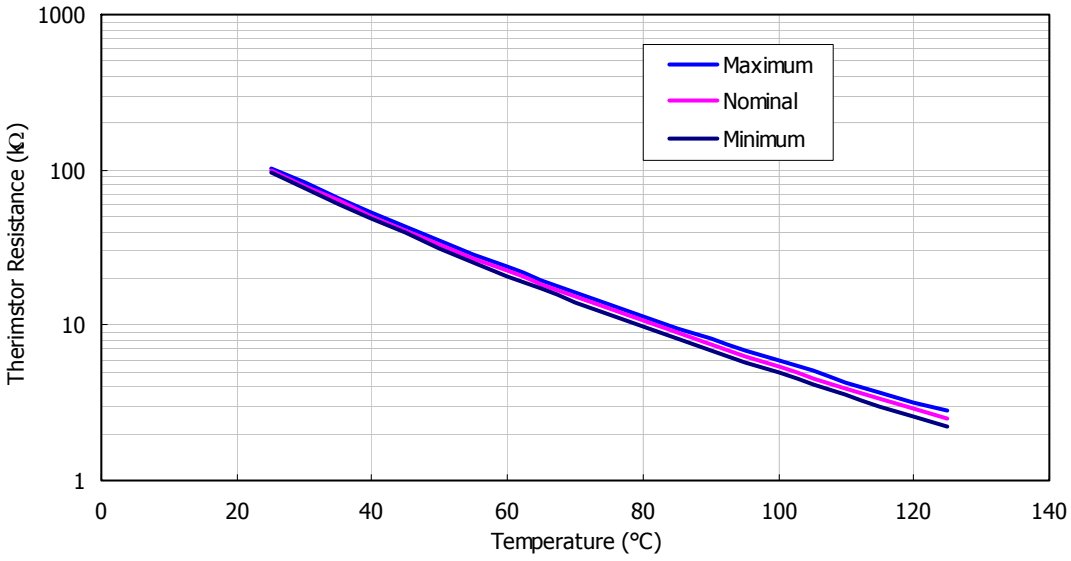



Figure 7. Variation of thermistor resistance with temperature

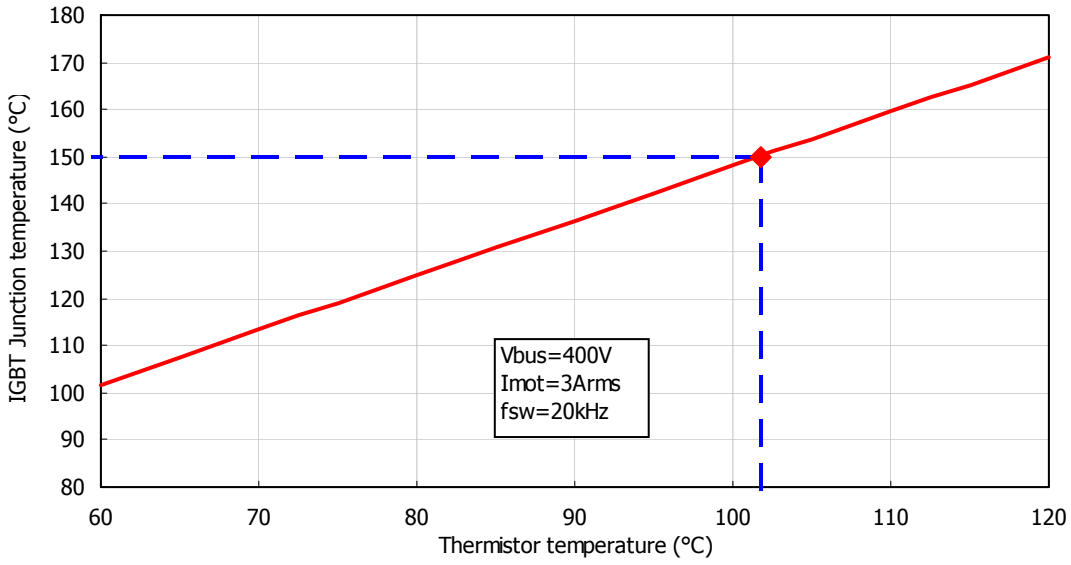



Figure 8. Estimated maximum IGBT junction temperature with thermistor temperature

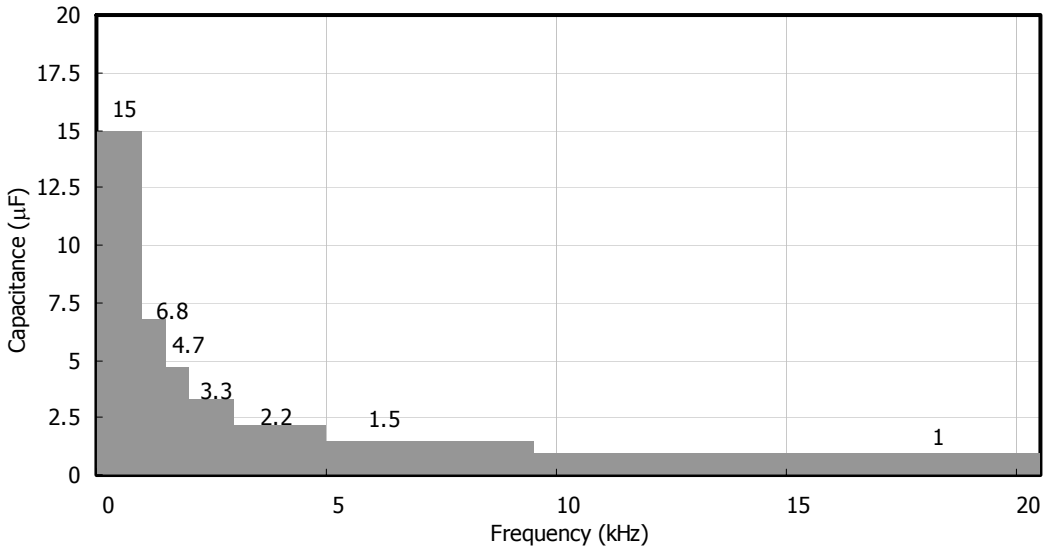



Figure 9. Recommended minimum Bootstrap Capacitor value Vs Switching Frequency

Figure 11. Switching Parameter Definitions

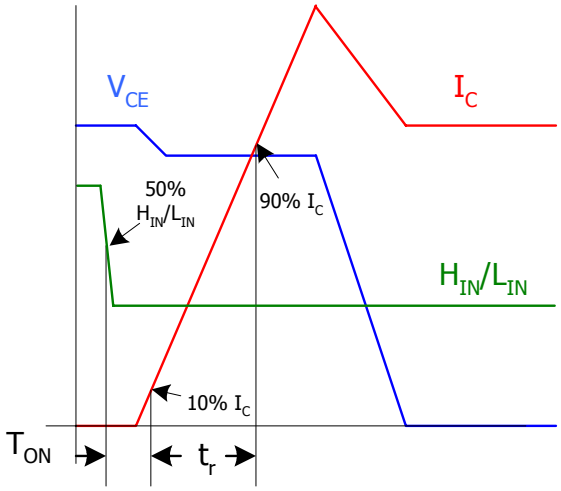



Figure 11a. Input to Output propagation turn-on delay time

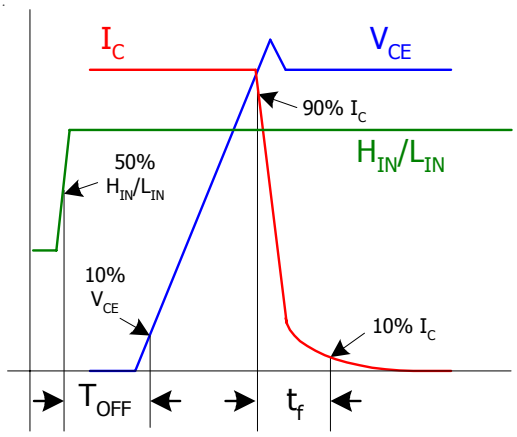



Figure 11b. Input to Output propagation turn-off delay time

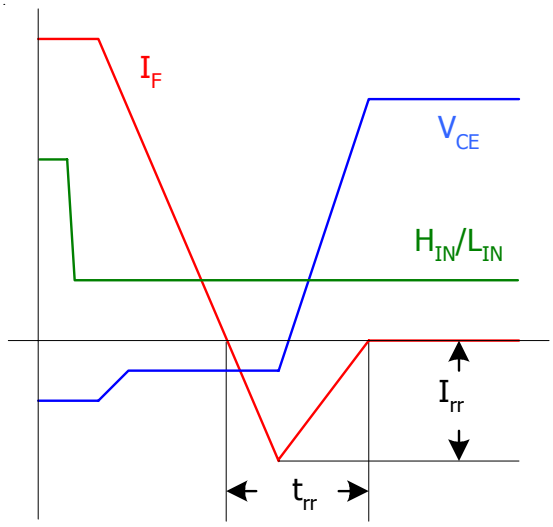



Figure 11c. Diode Reverse Recovery

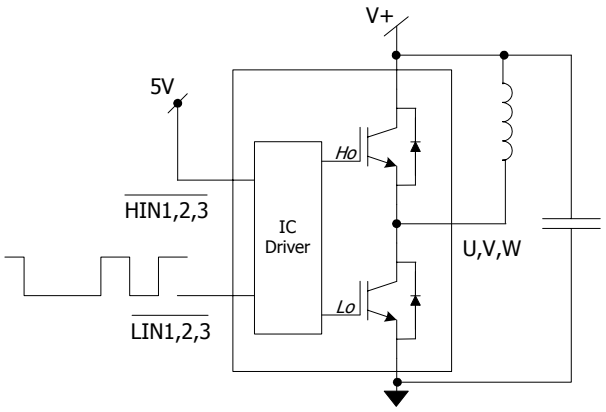
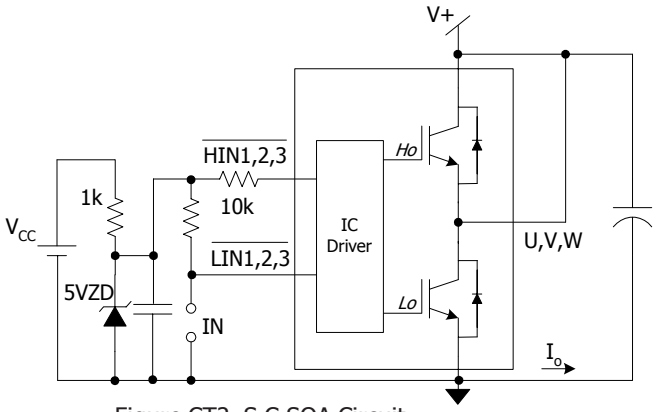
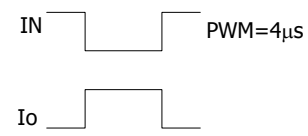


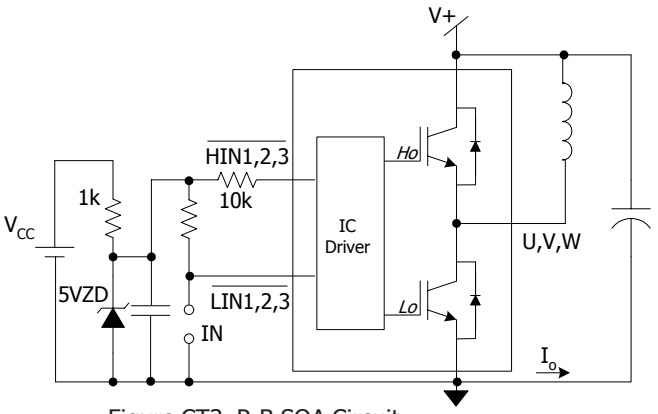

Figure CT1. Switching Loss Circuit

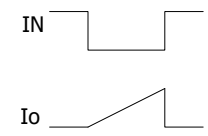



$V_P$=Peak Voltage on the IGBT die

Figure CT2. S.C.SOA Circuit

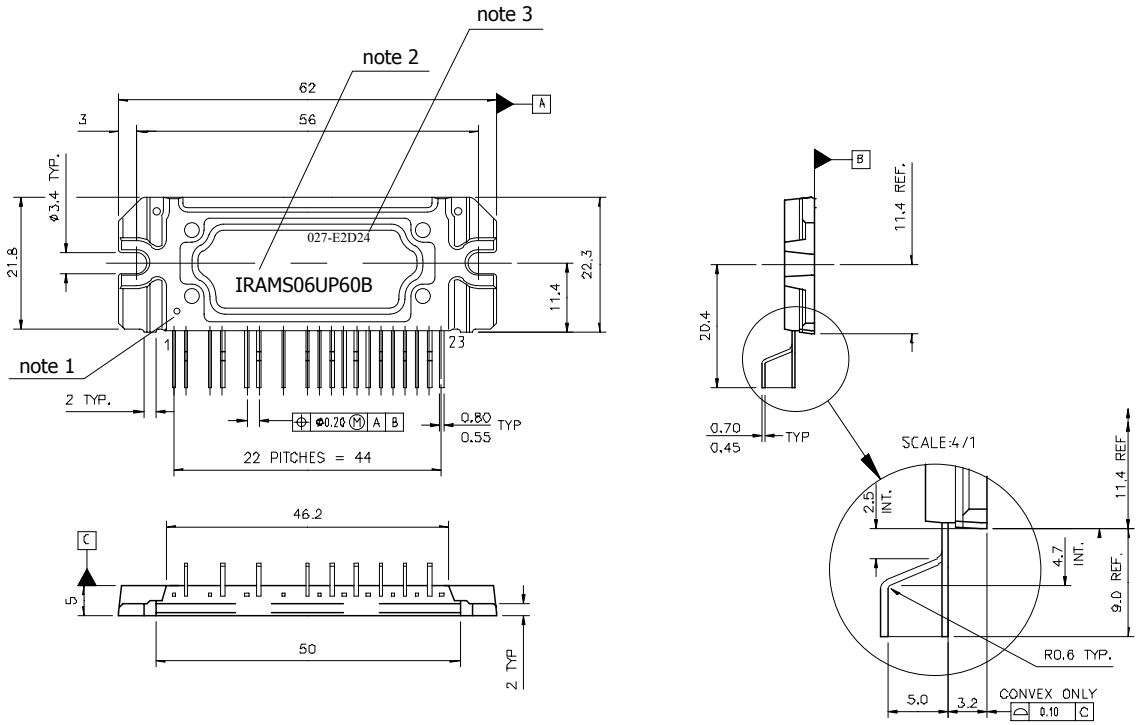



$V_P$=Peak Voltage on the IGBT die

Figure CT3. R.B.SOA Circuit

## Package Outline

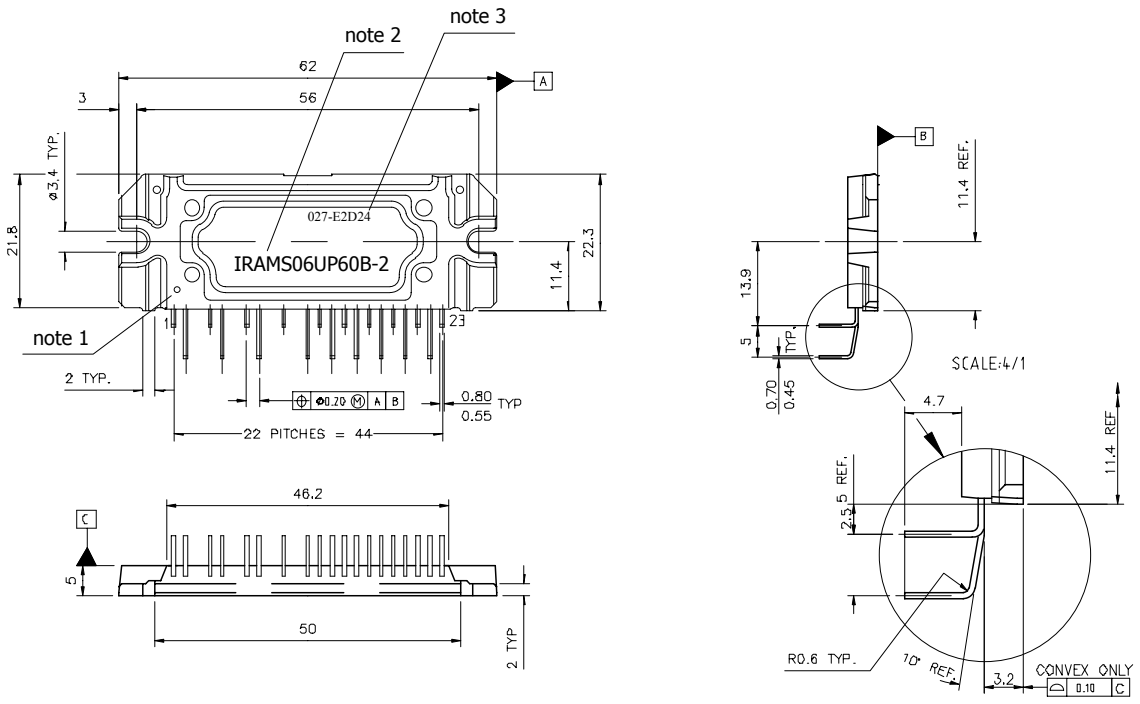



Standard pin leadforming option

Notes:
Dimensions in mm
1- Marking for pin 1 identification
2- Product Part Number
3- Lot and Date code marking

For mounting instruction, see AN1049

## Package Outline




Pin leadforming option -2

Notes:
Dimensions in mm
1- Marking for pin 1 identification
2- Product Part Number
3- Lot and Date code marking

Data and Specifications are subject to change without notice

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