

# DN2530

## 1.0 ELECTRICAL CHARACTERISTICS

### ABSOLUTE MAXIMUM RATINGS†

Drain-to-source voltage.....	$BV_{DSX}$
Drain-to-gate voltage.....	$BV_{DGX}$
Gate-to-source voltage.....	$\pm 20V$
Operating and Storage Temperature.....	-55 to 150 °C

† **Notice:** Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

### DC AND AC CHARACTERISTICS

Electrical Specifications: Unless otherwise specified, for all specifications $T_A = +25^\circ C$						
Parameter	Symbol	Min	Typ	Max	Units	Conditions
<b>DC Parameters (Note 1, unless otherwise stated)</b>						
Drain-to-source breakdown voltage	$BV_{DSX}$	300	-	-	V	$V_{GS} = -5.0V, I_D = 100 \mu A$
Gate-to-source off voltage	$V_{GS(OFF)}$	-1.0	-	-3.5	V	$V_{DS} = 25V, I_D = 10 \mu A$
$V_{GS(OFF)}$ change with temperature	$\Delta V_{GS(OFF)}$	-	-	-4.5	mV/°C	$V_{DS} = 25V, I_D = 10 \mu A$ (Note 2)
Gate body leakage current	$I_{GSS}$	-	-	100	nA	$V_{GS} = \pm 20V, V_{DS} = 0V$
Drain-to-source leakage current	$I_{D(OFF)}$	-	-	10	$\mu A$	$V_{DS} = \text{Max rating}, V_{GS} = -10V$
		-	-	1.0	mA	$V_{DS} = 0.8 \text{ Max Rating}, V_{GS} = -10V, T_A = 125^\circ C$ (Note 2)
Saturated drain-to-source current	$I_{DSS}$	200	-	-	mA	$V_{GS} = 0V, V_{DS} = 25V$
Static drain-to-source on-state resistance	$R_{DS(ON)}$	-	-	12	$\Omega$	$V_{GS} = 0V, I_D = 150 \text{ mA}$
Change in $R_{DS(ON)}$ with temperature	$\Delta R_{DS(ON)}$	-	-	1.1	%/°C	$V_{GS} = 0V, I_D = 150 \text{ mA}$ (Note 2)
<b>AC Parameters (Note 2)</b>						
Forward transconductance	$G_{FS}$	300	-	-	mmho	$V_{DS} = 10V, I_D = 150 \text{ mA}$
Input capacitance	$C_{ISS}$	-	-	300	pF	$V_{GS} = -10V,$ $V_{DS} = 25V,$ $f = 1 \text{ MHz}$
Common source output capacitance	$C_{OSS}$	-	-	30		
Reverse transfer capacitance	$C_{RSS}$	-	-	5		
Turn-on delay time	$t_{d(ON)}$	-	-	10	ns	$V_{DD} = 25V,$ $I_D = 150 \text{ mA},$ $R_{GEN} = 25\Omega,$
Rise time	$t_r$	-	-	15		
Turn-off delay time	$t_{d(OFF)}$	-	-	15		
Fall time	$t_f$	-	-	20		
<b>Diode Parameters</b>						
Diode forward voltage drop	$V_{SD}$	-	-	1.8	V	$V_{GS} = -10V, I_{SD} = 150 \text{ mA}$ (Note 1)
Reverse recovery time	$t_{rr}$	-	600	-	ns	$V_{GS} = -10V, I_{SD} = 1.0A$ (Note 2)

**Note 1:** All DC parameters are 100% tested at 25°C unless otherwise stated. Pulse test: 300  $\mu s$  pulse, 2% duty cycle.

**2:** Specification is obtained by characterization and is not 100% tested.

## TEMPERATURE SPECIFICATIONS

Electrical Specifications: Unless otherwise specified, for all specifications $T_A = T_J = +25^\circ\text{C}$						
Parameter	Symbol	Min	Typ	Max	Units	Conditions
<b>Temperature Ranges</b>						
Operating and Storage Temperature	$T_A$	-55	–	150	$^\circ\text{C}$	
<b>Package Thermal Resistances</b>						
Thermal Resistance, TO-92	$\theta_{ja}$	–	132	–	$^\circ\text{C}/\text{W}$	
Thermal Resistance, TO-243AA	$\theta_{ja}$	–	133	–	$^\circ\text{C}/\text{W}$	

## THERMAL CHARACTERISTICS

Package	$I_D(1)$ continuous (mA)	$I_D$ pulsed (mA)	Power Dissipation @ $T_A = 25^\circ\text{C}$ (W)	$I_{DR}(1)$ (mA)	$I_{DRM}$ (mA)
TO-92	175	500	0.74	175	500
TO-243AA (SOT-89)	200	500	1.6 (2)	200	500

**Note 1:**  $I_D$  continuous is limited by max rated  $T_J$

**2:** Mounted on FR4 board, 25mm x 25mm x 1.57 mm

## 2.0 PIN DESCRIPTION

The locations of the pins are listed in [Package Types](#) and [Packaging Information](#).

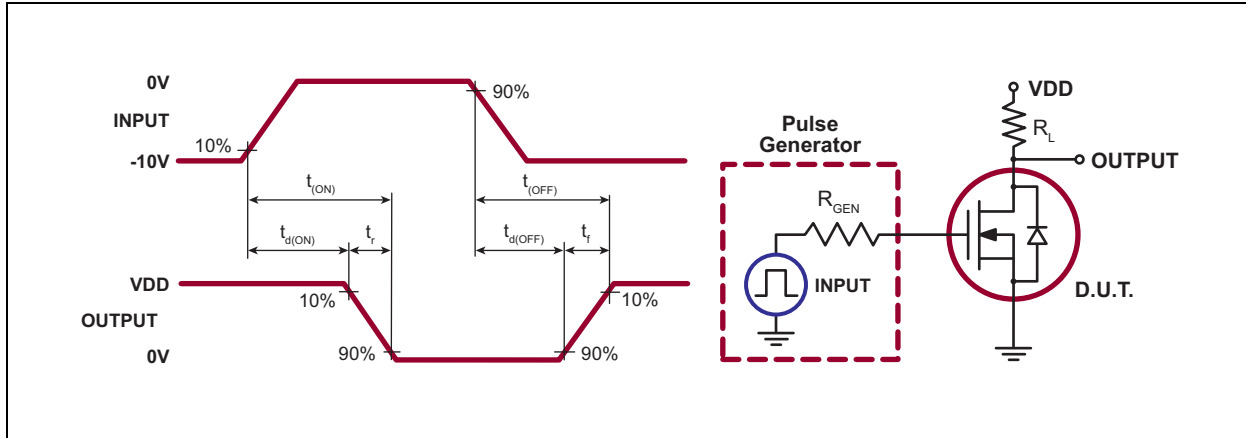
**TABLE 2-1: PIN DESCRIPTION**

Pin # TO-92	Pin # TO-243AA	Function
2	1	GATE
3	2, 4	DRAIN
1	3	SOURCE

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## 3.0 FUNCTIONAL DESCRIPTION

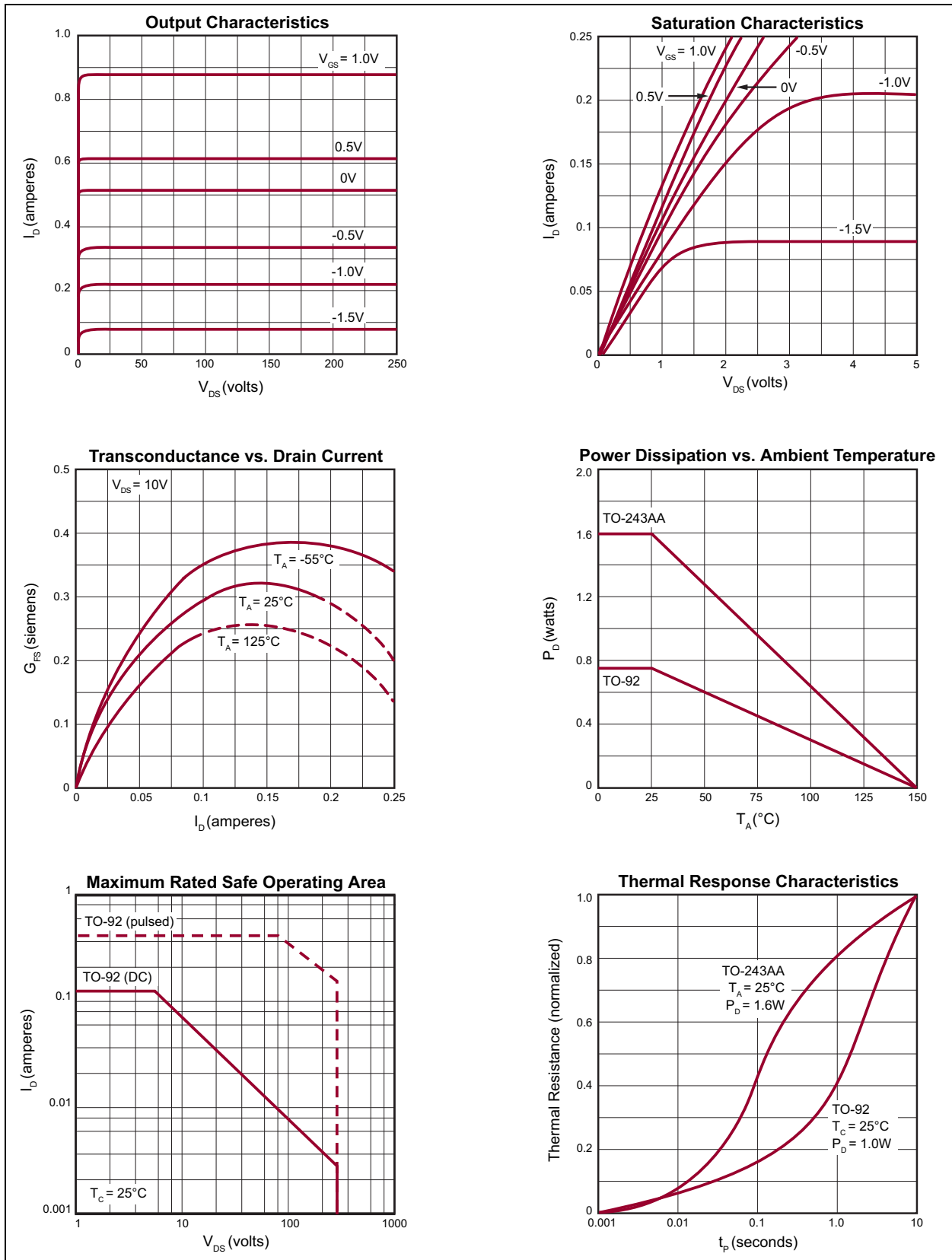
Figure 3-1 shows the switching waveform and test circuit for DN2530. Figure 3-2 and Figure 3-3 provide typical performance curves.



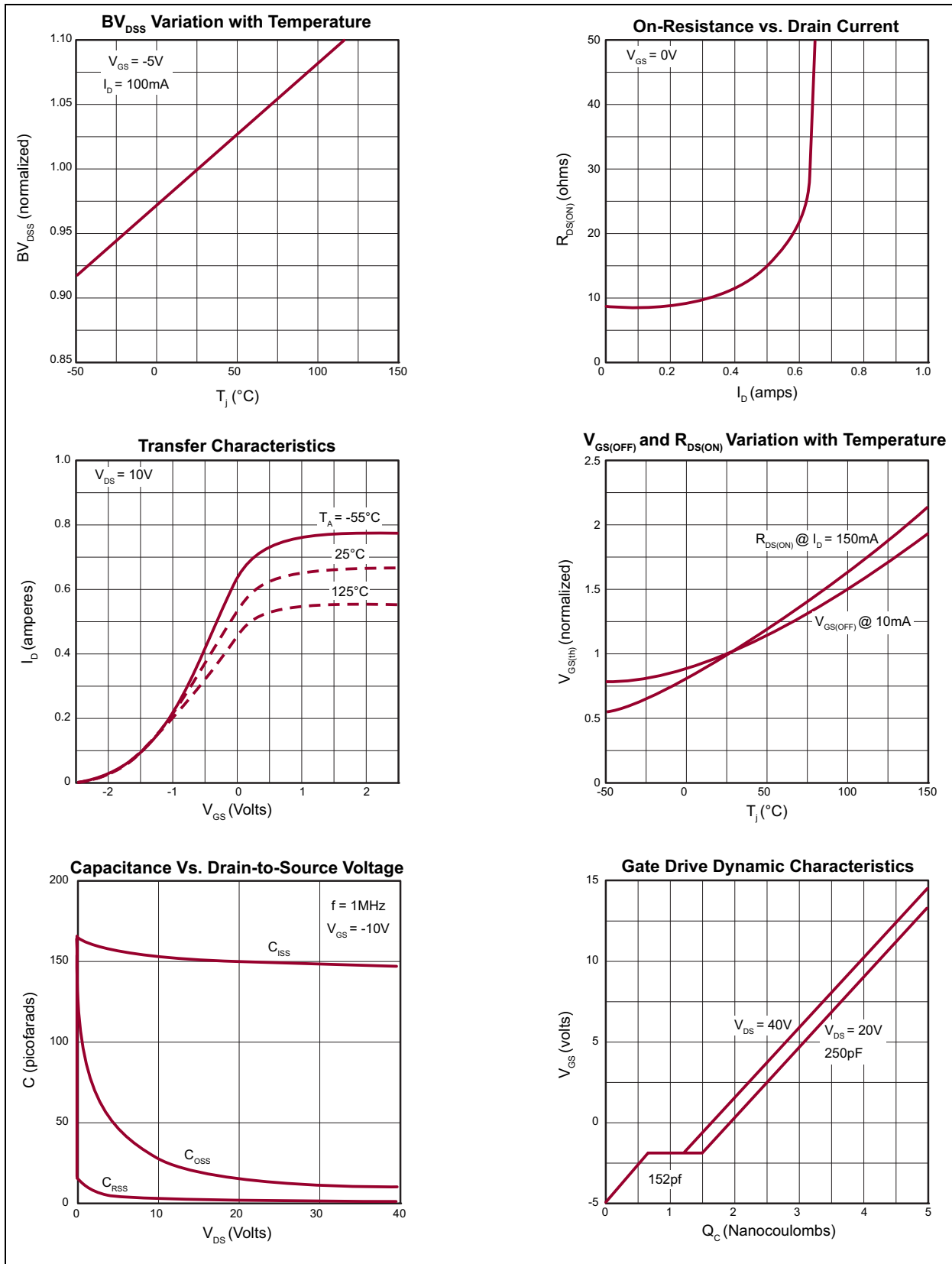
**FIGURE 3-1:** Switching Waveforms and Test Circuit

### Product Summary

$BV_{DSX}/BV_{DGX}$ (V)	$R_{DS(ON)}$ (max) ( $\Omega$ )	$I_{DSS}$ (min) (mA)
300	12	200



**FIGURE 3-2:** Typical Performance Curves

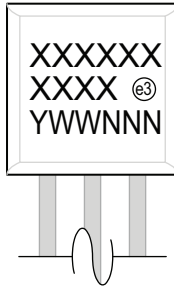


**FIGURE 3-3:** Typical Performance Curves (continued)

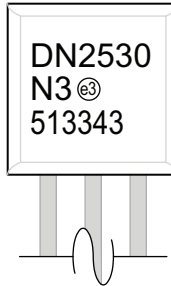
## 4.0 PACKAGING INFORMATION

### 4.1 Package Marking Information

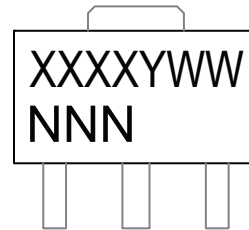
3-lead TO-92



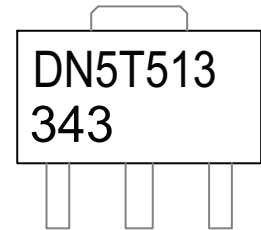
Example



3-lead TO-243AA \*  
(SOT-89)



Example

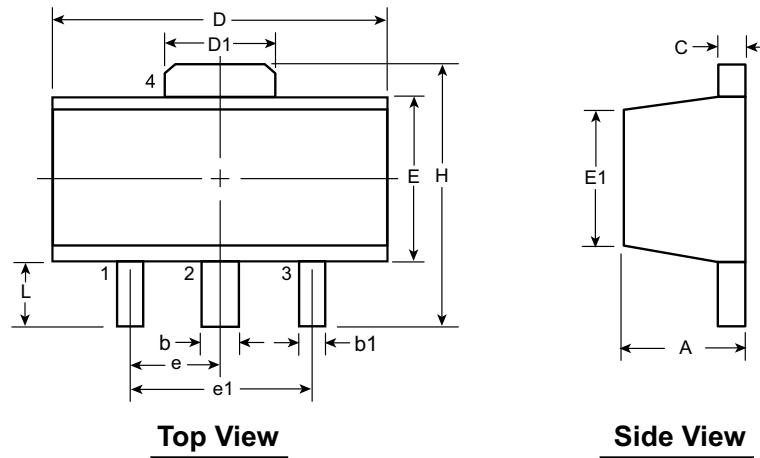


<b>Legend:</b>	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

**Note:** In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or not include the corporate logo.

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## 3-Lead TO-243AA (SOT-89) Package Outline (N8)



Note: For the most current package drawings, see the Microchip Packaging Specification at [www.microchip.com/packaging](http://www.microchip.com/packaging).

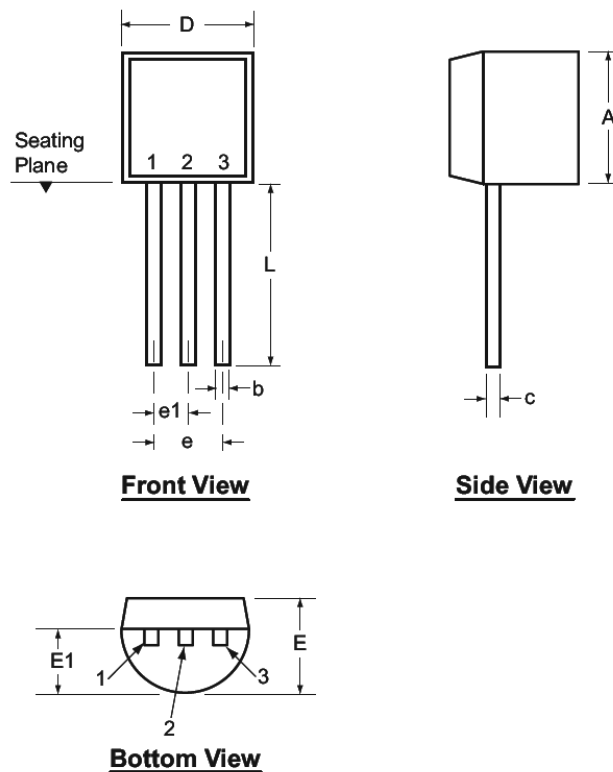
Symbol		A	b	b1	C	D	D1	E	E1	e	e1	H	L		
Dimensions (mm)	MIN	1.40	0.44	0.36	0.35	4.40	1.62	2.29	2.00 <sup>†</sup>	1.50 BSC	3.00 BSC	3.94	0.73 <sup>†</sup>		
	NOM	-	-	-	-	-	-	-	-			-	-	-	-
	MAX	1.60	0.56	0.48	0.44	4.60	1.83	2.60	2.29			-	-	4.25	1.20

JEDEC Registration TO-243, Variation AA, Issue C, July 1986.

<sup>†</sup> This dimension differs from the JEDEC drawing

Drawings not to scale.

## 3-Lead TO-92 Package Outline (L/LL/N3)



Note: For the most current package drawings, see the Microchip Packaging Specification at [www.microchip.com/packaging](http://www.microchip.com/packaging).

Symbol		A	b	c	D	E	E1	e	e1	L
Dimensions (inches)	MIN	.170	.014 <sup>†</sup>	.014 <sup>†</sup>	.175	.125	.080	.095	.045	.500
	NOM	-	-	-	-	-	-	-	-	-
	MAX	.210	.022 <sup>†</sup>	.022 <sup>†</sup>	.205	.165	.105	.105	.055	.610*

JEDEC Registration TO-92.

\* This dimension is not specified in the JEDEC drawing.

† This dimension differs from the JEDEC drawing.

**Drawings not to scale.**



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## APPENDIX A: REVISION HISTORY

### Revision A (January 2016)

- Converted Supertex Doc #DSFP-DN2530 to Microchip DS20005451A.
- Removed 2000/Reel option for TO-92 package.

## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

<u>PART NO.</u>	<u>XX</u>	-	<u>X</u>	-	<u>X</u>
Device	Package Options		Environmental		Media Type
Device:	DN2530	=	N-Channel, Depletion-Mode, Vertical DMOS FET		
Package:	N3	=	TO-92, 3-lead		
	N8	=	TO-243AA (SOT-89), 3-lead		
Environmental	G	=	Lead (Pb)-free/ROHS-compliant package		
Media Type:	(blank)	=	1000/Reel for N3 packages 2000/Reel for N8 packages		

**Examples:**

a) DN2530N3-G      TO-92 package, 1000/reel

b) DN2530N8-G      TO-243AA package, 2000/reel

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