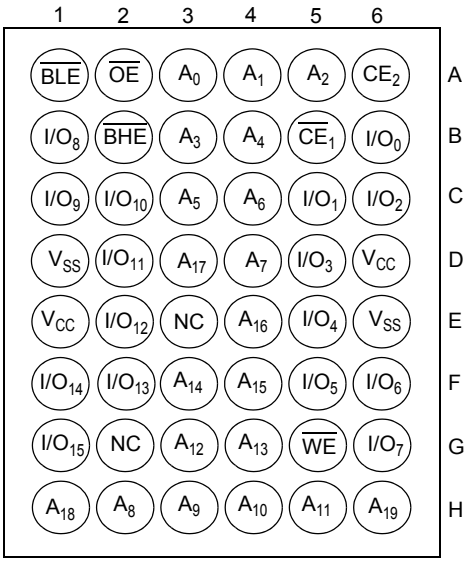
Contents

Selection Guide

Description	-10	Unit
Maximum access time	10	ns
Maximum operating current	110	mA
Maximum CMOS standby current	30	mA

Pin Configurations

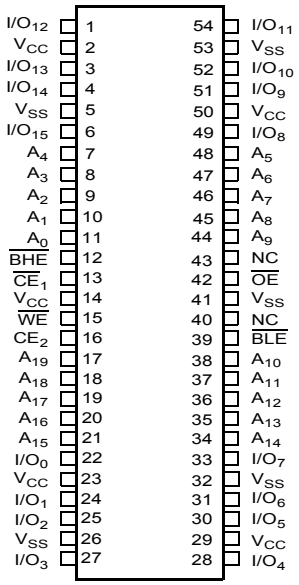
Figure 1. 48-ball VFBGA (8 × 9.5 × 1 mm) Dual Chip Enable pinout (Top View) [1]



Note
1. NC pins are not connected internally to the die.

Pin Configurations (continued)

Figure 2. 54-pin TSOP II (22.4 × 11.84 × 1.0 mm) pinout (Top View) [2]



Note
2. NC pins are not connected internally to the die.

Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage Temperature ..... –65 °C to +150 °C

Ambient Temperature with Power Applied ..... –55 °C to +125 °C

Supply Voltage on V_{CC} relative to GND [3] ..... –0.5 V to V_{CC} + 0.5 V

DC Voltage Applied to Outputs in High Z State [3] ..... –0.5 V to V_{CC} + 0.5 V

DC Input Voltage [3] ..... –0.5 V to V_{CC} + 0.5 V

Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage (MIL-STD-883, Method 3015) ..... >2001 V

Latch Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Industrial	–40 °C to +85 °C	2.2 V to 3.6 V

DC Electrical Characteristics

Over the Operating Range

Parameter	Description		Test Conditions	-10			Unit
				Min	Typ [4]	Max	
V_{OH}	Output HIGH voltage	2.2 V to 2.7 V	V_{CC} = Min, I_{OH} = –0.1 mA	2.0	–	–	V
		2.7 V to 3.6 V	V_{CC} = Min, I_{OH} = –4.0 mA	2.2	–	–	
V_{OL}	Output LOW voltage	2.2 V to 2.7 V	V_{CC} = Min, I_{OL} = 2 mA	–	–	0.4	V
		2.7 V to 3.6 V	V_{CC} = Min, I_{OL} = 8 mA	–	–	0.4	
V_{IH}	Input HIGH voltage [3]	2.2 V to 2.7 V	–	2.0	–	V_{CC} + 0.3	V
		2.7 V to 3.6 V	–	2.0	–	V_{CC} + 0.3	
V_{IL}	Input LOW voltage [3]	2.2 V to 2.7 V	–	–0.3	–	0.6	V
		2.7 V to 3.6 V	–	–0.3	–	0.8	
I_{IX}	Input leakage current		GND ≤ V_I ≤ V_{CC}	–1	–	+1	µA
I_{OZ}	Output leakage current		GND ≤ V_{OUT} ≤ V_{CC}, Output disabled	–1	–	+1	µA
I_{CC}	V_{CC} operating supply current		V_{CC} = Max, f = f_{MAX} = $1/t_{RC}$, I_{OUT} = 0 mA, CMOS levels	–	90	110	mA
I_{SB1}	Automatic CE power down current – TTL inputs		Max V_{CC}, $\overline{CE}_1$ ≥ V_{IH}, CE_2 ≤ V_{IL}, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}	–	–	40	mA
I_{SB2}	Automatic CE power down current – CMOS inputs		Max V_{CC}, $\overline{CE}_1$ ≥ V_{CC} – 0.3 V, CE_2 ≤ 0.3 V, V_{IN} ≥ V_{CC} – 0.3 V or V_{IN} ≤ 0.3 V, f = 0	–	20	30	mA

Note

3. $V_{IL(min)}$ = –2.0 V and $V_{IH(max)}$ = V_{CC} + 2 V for pulse durations of less than 2 ns.
4. Typical values are included only for reference and are not guaranteed or tested. Typical values are measured at V_{CC} = 3 V (for a V_{CC} range of 2.2 V–3.6 V), T_A = 25 °C.

Capacitance

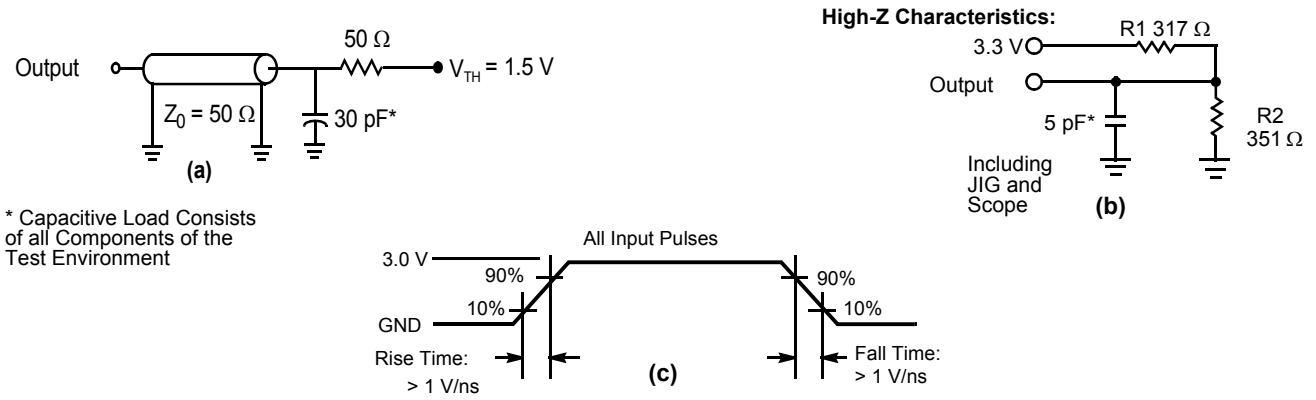
Parameter [5]	Description	Test Conditions	54-pin TSOP II	48-ball VFBGA	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{CC} = 3.3 V	10	10	pF
C_{OUT}	I/O capacitance		10	10	pF

Thermal Resistance

Parameter [5]	Description	Test Conditions	54-pin TSOP II	48-ball VFBGA	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 inch, four layer printed circuit board	93.63	31.50	°C/W
Θ_{JC}	Thermal resistance (junction to case)		21.58	15.75	°C/W

AC Test Loads and Waveforms

Figure 3. AC Test Loads and Waveforms [6]



Notes
5. Tested initially and after any design or process changes that may affect these parameters.
6. Valid SRAM operation does not occur until the power supplies have reached the minimum operating V_{DD} (3.0 V). 100 µs (t_{power}) after reaching the minimum operating V_{DD}, normal SRAM operation begins including reduction in V_{DD} to the data retention (V_{CCDR}, 1.0 V) voltage.

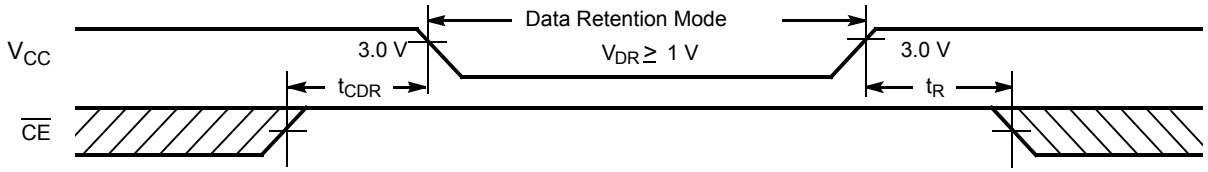
Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions	Min	Max	Unit
V_{DR}	V_{CC} for data retention	–	1	–	V
I_{CCDR}	Data retention current	V_{CC} = 1.2 V, $\overline{CE}_1 \geq V_{CC} - 0.2$ V, $CE_2 \leq 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V	–	30	mA
t_{CDR} [7]	Chip deselect to data retention time	–	0	–	ns
t_R [8]	Operation recovery time	–	10	–	ns

Data Retention Waveform

Figure 4. Data Retention Waveform [9]



Notes

7. Tested initially and after any design or process changes that may affect these parameters.
8. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min.)} \geq 100$ µs or stable at $V_{CC(min.)} \geq 100$ µs.
9. $\overline{CE}$ is the logical combination of $\overline{CE}_1$ and CE_2. When $\overline{CE}_1$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW; when $\overline{CE}_1$ is HIGH or CE_2 is LOW, $\overline{CE}$ is HIGH.

AC Switching Characteristics

Over the Operating Range

Parameter [10]	Description	-10		Unit
		Min	Max	
Read Cycle				
t_{power}	V_{CC}(typical) to the first access [11]	100	–	µs
t_{RC}	Read cycle time	10	–	ns
t_{AA}	Address to data valid	–	10	ns
t_{OHA}	Data hold from address change	3	–	ns
t_{ACE}	$\overline{CE}_1$ LOW/CE_2 HIGH to data valid	–	10	ns
t_{DOE}	$\overline{OE}$ LOW to data valid	–	5	ns
t_{LZOE}	$\overline{OE}$ LOW to low Z [12]	0	–	ns
t_{HZOE}	$\overline{OE}$ HIGH to high Z [12]	–	5	ns
t_{LZCE}	$\overline{CE}_1$ LOW/CE_2 HIGH to low Z [12]	3	–	ns
t_{HZCE}	$\overline{CE}_1$ HIGH/CE_2 LOW to high Z [12]	–	5	ns
t_{PU}	$\overline{CE}_1$ LOW/CE_2 HIGH to power-up [13]	0	–	ns
t_{PD}	$\overline{CE}_1$ HIGH/CE_2 LOW to power-down [13]	–	10	ns
t_{DBE}	Byte enable to data valid	–	5	ns
t_{LZBE}	Byte enable to low Z	0	–	ns
t_{HZBE}	Byte disable to high Z	–	6	ns
Write Cycle [14, 15]				
t_{WC}	Write cycle time	10	–	ns
t_{SCE}	$\overline{CE}_1$ LOW/CE_2 HIGH to write end	7	–	ns
t_{AW}	Address setup to write end	7	–	ns
t_{HA}	Address hold from write end	0	–	ns
t_{SA}	Address setup to write start	0	–	ns
t_{PWE}	$\overline{WE}$ pulse width	7	–	ns
t_{SD}	Data setup to write end	5	–	ns
t_{HD}	Data hold from write end	0	–	ns
t_{LZWE}	$\overline{WE}$ HIGH to low Z [12,13.]	3	–	ns
t_{HZWE}	$\overline{WE}$ LOW to high Z [12,13.]	–	5	ns
t_{BW}	Byte Enable to End of Write	7	–	ns

Notes

10. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, and input pulse levels of 0 to 3.0 V. Test conditions for the read cycle use output loading shown in part (a) of Figure 3 on page 6, unless specified otherwise.
11. t_{POWER} gives the minimum amount of time that the power supply is at typical V_{CC} values until the first memory access is performed.
12. t_{HZOE}, t_{HZCE}, t_{HZWE}, t_{HZBE}, t_{LZOE}, t_{LZCE}, t_{LZWE}, and t_{LZBE} are specified with a load capacitance of 5 pF as in (b) of Figure 3 on page 6. Transition is measured when output goes into high impedance
13. These parameters are guaranteed by design and are not tested.
14. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}_1$ = V_{IL}, and CE_2 = V_{IH}. Chip enables must be active and $\overline{WE}$ and byte enables must be LOW to initiate a write, and the transition of any of these signals can terminate. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
15. The minimum write cycle time for Write Cycle No. 2 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD}.

Switching Waveforms

Figure 5. Read Cycle No. 1 (Address Transition Controlled) [16, 17]

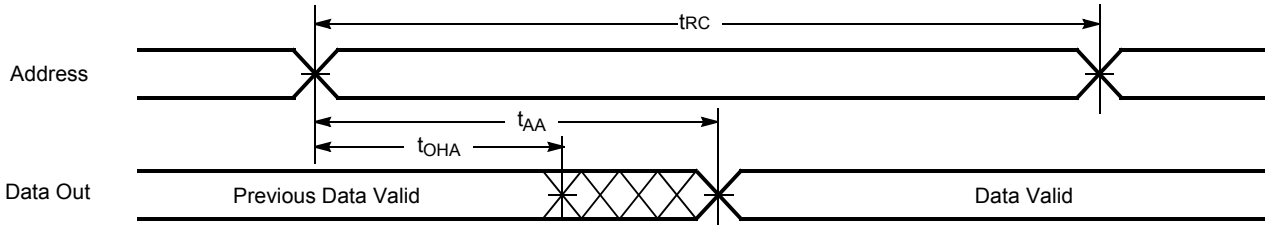
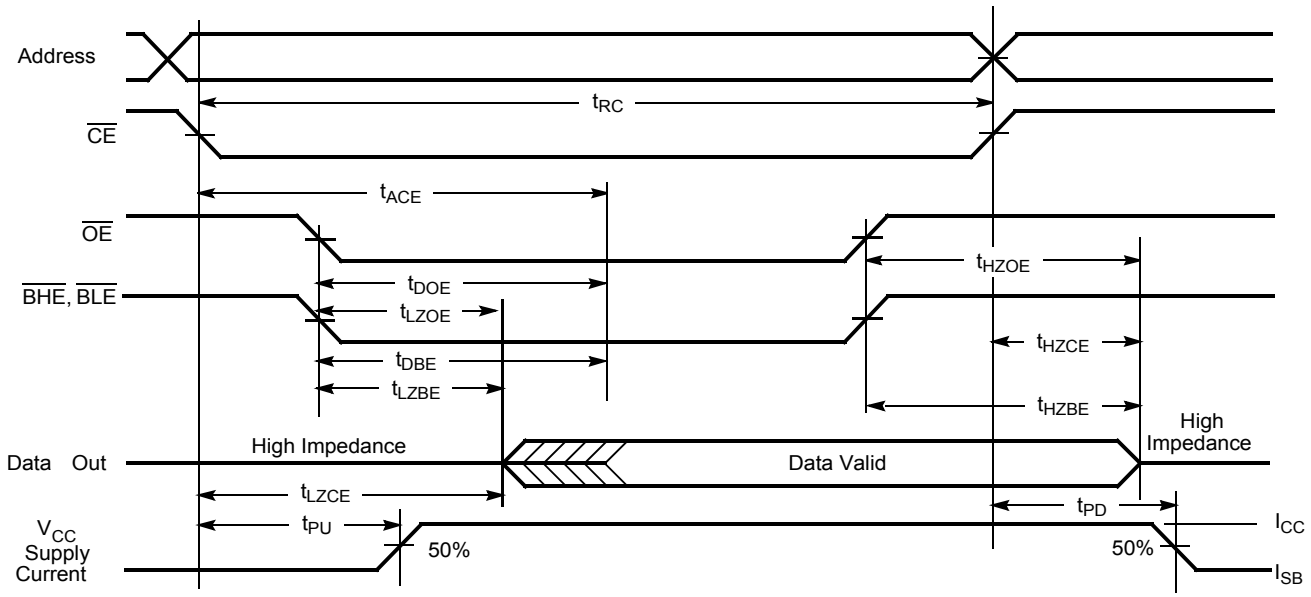


Figure 6. Read Cycle No. 2 ($\overline{OE}$ Controlled) [17, 18, 19]



Notes

16. The device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}, $\overline{BHE}$, $\overline{BLE}$ or both = V_{IL}.
17. $\overline{WE}$ is HIGH for read cycle.
18. $\overline{CE}$ is the logical combination of $\overline{CE}_1$ and CE_2. When $\overline{CE}_1$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW; when $\overline{CE}_1$ is HIGH or CE_2 is LOW, $\overline{CE}$ is HIGH.
19. Address valid before or similar to $\overline{CE}$ transition LOW.

Switching Waveforms (continued)

Figure 7. Write Cycle No. 1 ($\overline{CE}$ Controlled) [20, 21, 22]

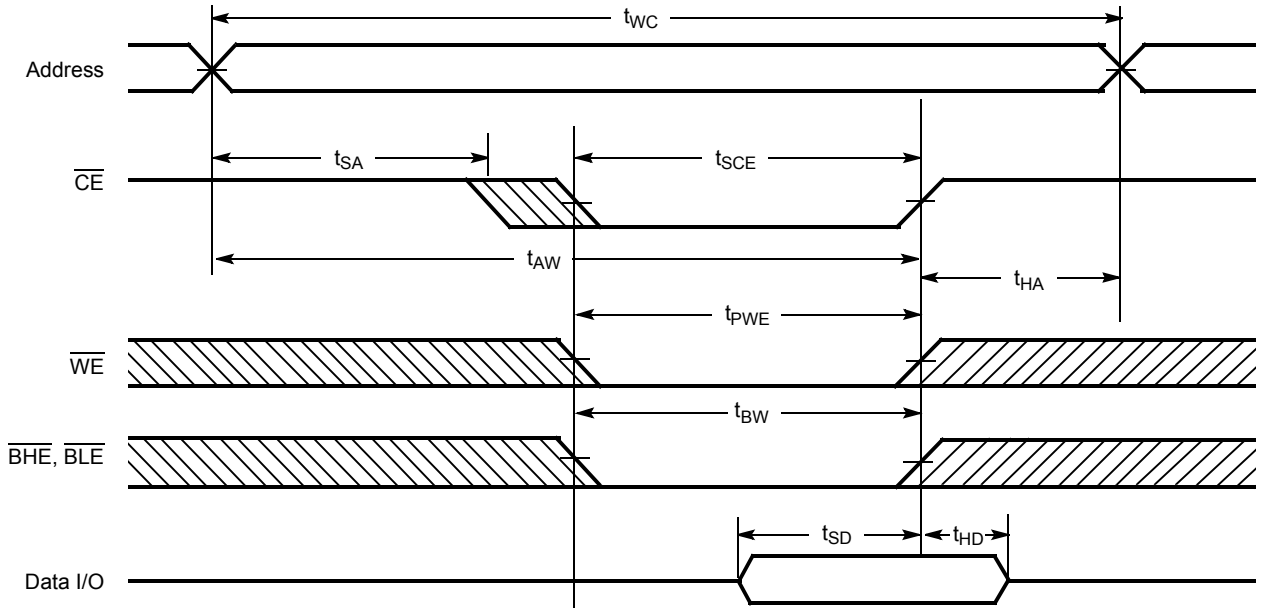
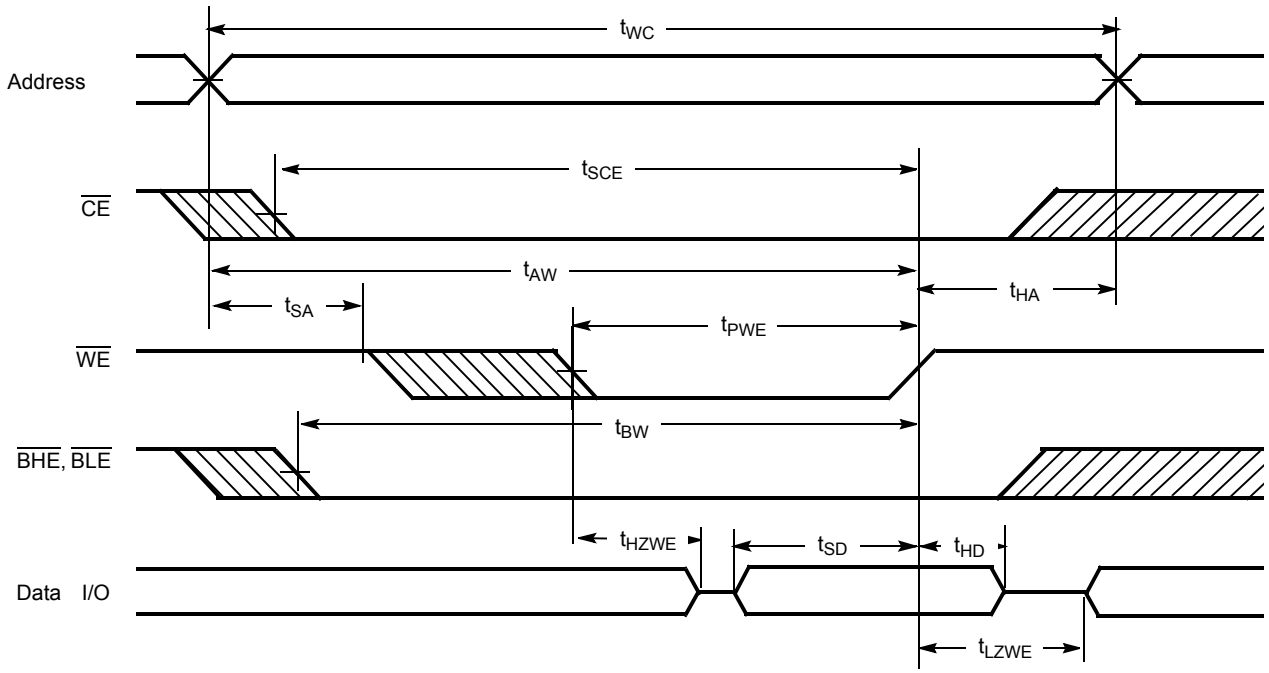


Figure 8. Write Cycle No. 2 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) [20, 21, 22]

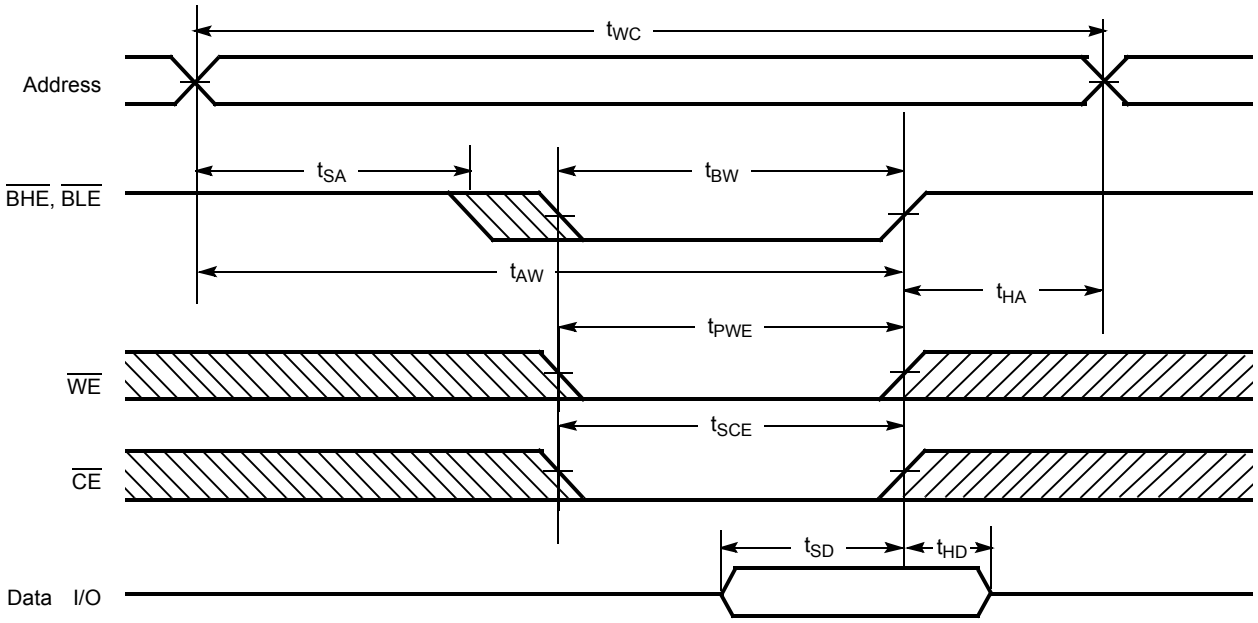


Notes

20. $\overline{CE}$ is the logical combination of $\overline{CE}_1$ and CE_2. When $\overline{CE}_1$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW; when $\overline{CE}_1$ is HIGH or CE_2 is LOW, $\overline{CE}$ is HIGH.
21. Data I/O is high impedance if $\overline{OE}$, $\overline{BHE}$, and/or $\overline{BLE}$ = V_{IH}.
22. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ going HIGH, the output remains in a high-impedance state.

Switching Waveforms (continued)

Figure 9. Write Cycle No. 3 ($\overline{BLE}$ or $\overline{BHE}$ Controlled) [23]



Note
23. $\overline{CE}$ is the logical combination of $\overline{CE}_1$ and CE_2. When $\overline{CE}_1$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW; when $\overline{CE}_1$ is HIGH or CE_2 is LOW, $\overline{CE}$ is HIGH.

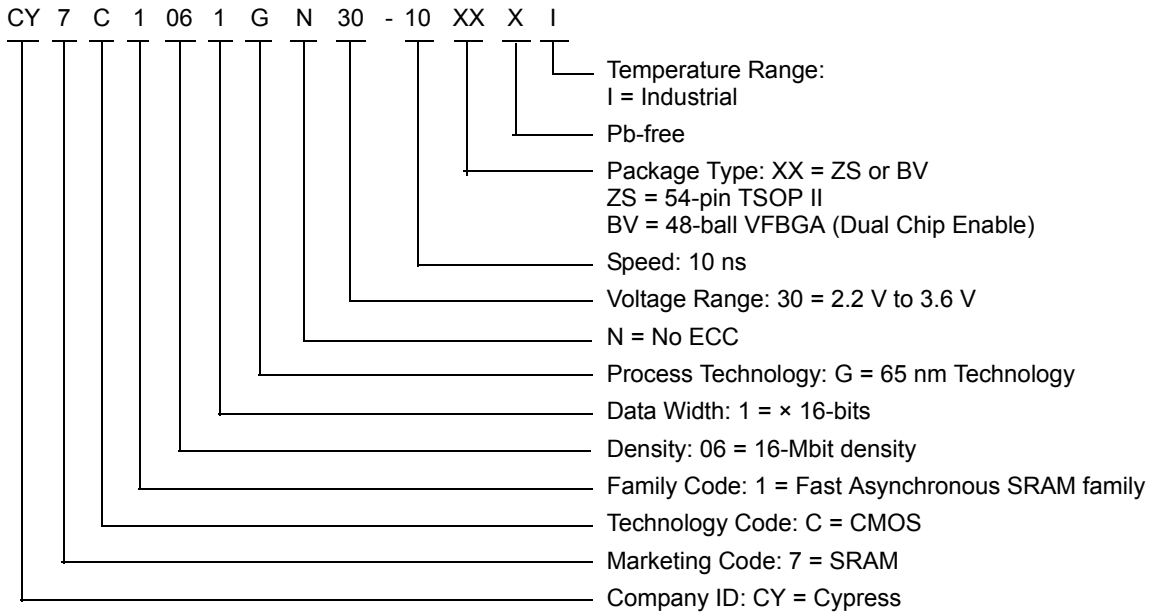
Truth Table

$\overline{CE}_1$	CE_2	$\overline{OE}$	$\overline{WE}$	$\overline{BLE}$	$\overline{BHE}$	I/O_0–I/O_7	I/O_8–I/O_{15}	Mode	Power
H	X	X	X	X	X	High Z	High Z	Power down	Standby (I_{SB})
X	L	X	X	X	X	High Z	High Z	Power down	Standby (I_{SB})
L	H	L	H	L	L	Data out	Data out	Read all bits	Active (I_{CC})
L	H	L	H	L	H	Data out	High Z	Read lower bits only	Active (I_{CC})
L	H	L	H	H	L	High Z	Data out	Read upper bits only	Active (I_{CC})
L	H	X	L	L	L	Data in	Data in	Write all bits	Active (I_{CC})
L	H	X	L	L	H	Data in	High Z	Write lower bits only	Active (I_{CC})
L	H	X	L	H	L	High Z	Data in	Write upper bits only	Active (I_{CC})
L	H	H	H	X	X	High Z	High Z	Selected, outputs disabled	Active (I_{CC})

Ordering Information

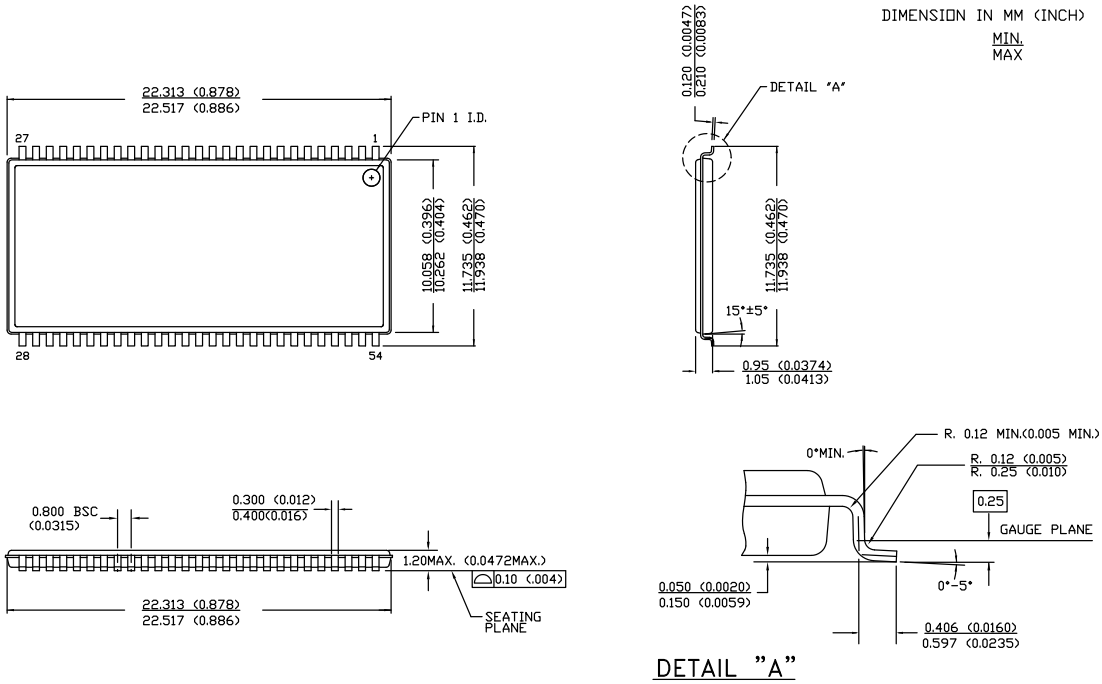
Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
10	CY7C1061GN30-10ZSXI	51-85160	54-pin TSOP II (22.4 × 11.84 × 1.0 mm) (Pb-free)	Industrial
	CY7C1061GN30-10BVXI	51-85150	48-ball VFBGA (6 × 8 × 1.0 mm) (Pb-free) (Dual Chip Enable)	

Ordering Code Definitions



Package Diagrams

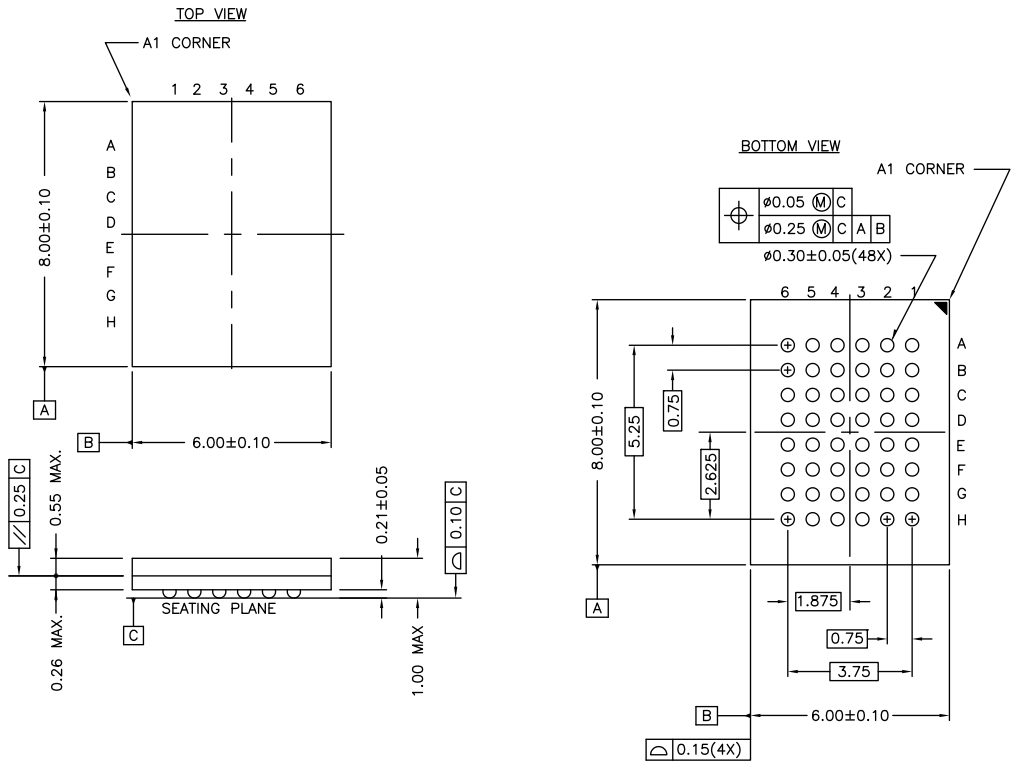
Figure 10. 54-pin TSOP II (22.4 × 11.84 × 1.0 mm) Z54-II Package Outline, 51-85160



51-85160 *E

Package Diagrams (continued)

Figure 11. 48-ball VFBGA (6 × 8 × 1.0 mm) BV48/BZ48 Package Outline, 51-85150



NOTE:
PACKAGE WEIGHT: See Cypress Package Material Declaration Datasheet (PMDD) posted on the Cypress web.

51-85150 *H

Acronyms

Acronym	Description
$\overline{BHE}$	Byte High Enable
$\overline{BLE}$	Byte Low Enable
$\overline{CE}$	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input/Output
$\overline{OE}$	Output Enable
SRAM	Static Random Access Memory
TSOP	Thin Small Outline Package
TTL	Transistor-Transistor Logic
VFBGA	Very Fine-Pitch Ball Grid Array
$\overline{WE}$	Write Enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
µA	microampere
µs	microsecond
mA	milliampere
mm	millimeter
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY7C1061GN30, 16-Mbit (1 M words × 16 bit) Static RAM Document Number: 001-93680				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	4505531	VINI	01/02/2015	New data sheet.
*A	4900408	NILE	09/11/2015	Updated DC Electrical Characteristics: Updated details in “Test Conditions” column of V_{OH} and V_{OL} parameters. Updated Ordering Information: No change in part numbers. Replaced “51-85178” with “51-85150” in “Package Diagram” column. Replaced “8 × 9.5 × 1 mm” with “6 × 8 × 1.0 mm” in “Package Type” column. Updated Package Diagrams: Removed spec 51-85178 *C. Added spec 51-85150 *H. Updated to new template.

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