

**Pin Description**

| Name                                            | Pins                           | Description                                                                                                                                                                                                        |
|-------------------------------------------------|--------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| REF                                             | 56                             | 3.3V 14.318 MHz clock output                                                                                                                                                                                       |
| XTAL_IN                                         | 2                              | 14.318 MHz crystal input                                                                                                                                                                                           |
| XTAL_OUT                                        | 3                              | 14.318 MHz crystal input                                                                                                                                                                                           |
| CPU, CPU [0:3]#                                 | 44, 45, 48, 49, 51, 52, 53, 54 | Differential CPU clock outputs                                                                                                                                                                                     |
| 3V66_0                                          | 33                             | 3.3V 66 MHz clock output                                                                                                                                                                                           |
| 3V66_1/VCH                                      | 35                             | 3.3V selectable through SMBus to be 66 MHz or 48 MHz                                                                                                                                                               |
| 66IN/3V66_5                                     | 24                             | 66 MHz input to buffered 66BUFF and PCI or 66 MHz clock from internal VCO                                                                                                                                          |
| 66BUFF [0:2] /3V66 [2:4]                        | 21, 22, 23                     | 66 MHz buffered outputs from 66Input or 66 MHz clocks from internal VCO                                                                                                                                            |
| PCI_F [0:2]                                     | 5, 6, 7,                       | 33 MHz clocks divided down from 66Input or divided down from 3V66                                                                                                                                                  |
| PCI [0:6]                                       | 10, 11, 12, 13, 16, 17, 18     | PCI clock outputs divided down from 66Input or divided down from 3V66                                                                                                                                              |
| USB                                             | 39                             | Fixed 48 MHz clock output                                                                                                                                                                                          |
| DOT                                             | 38                             | Fixed 48 MHz clock output                                                                                                                                                                                          |
| S2                                              | 40                             | Special 3.3V 3-level input for Mode selection                                                                                                                                                                      |
| S1                                              | 55                             | 3.3V LVTTTL inputs for CPU frequency selection                                                                                                                                                                     |
| IREF                                            | 42                             | A precision resistor is attached to this pin which is connected to the internal current reference                                                                                                                  |
| MULT0                                           | 43                             | 3.3V LVTTTL input for selecting the current multiplier for the CPU outputs                                                                                                                                         |
| PD#                                             | 25                             | 3.3V LVTTTL input for Power_Down# (active LOW). Do not add any decoupling capacitors. Use an external 1.0-KΩ pull-up resistor.                                                                                     |
| PCI_STOP#                                       | 34                             | 3.3V LVTTTL input for PCI_STOP# (active LOW)                                                                                                                                                                       |
| VTPWRGD#                                        | 28                             | 3.3V LVTTTL input is a level-sensitive strobe used to determine when S[1:2] and MULT0 inputs are valid and OK to be sampled (Active LOW). Once VTPWRGD# is sampled LOW, the status of this output will be ignored. |
| SDATA                                           | 29                             | SMBus-compatible SDATA                                                                                                                                                                                             |
| SCLK                                            | 30                             | SMBus-compatible Sclk                                                                                                                                                                                              |
| VDD_REF, VDD_PCI, VDD_3V66, VDD_48 MHz, VDD_CPU | 1, 8, 14, 19, 32, 37, 46, 50   | 3.3V power supply for outputs                                                                                                                                                                                      |
| VDD_CORE                                        | 26                             | 3.3V power supply for PLL                                                                                                                                                                                          |
| GND_REF, GND_PCI, GND_3V66, GND_IREF, VDD_CPU   | 4, 9, 15, 20, 31, 36, 41, 47   | Ground for outputs                                                                                                                                                                                                 |
| GND_CORE                                        | 27                             | Ground for PLL                                                                                                                                                                                                     |

**Function Table<sup>[1]</sup>**

| S2  | S1 | CPU (MHz) | 3V66[0:1] (MHz) | 66BUFF[0:2]/3V66[2:4] (MHz) | 66IN/3V66_5 (MHz) | PCI_F/PCI (MHz) | REF0(MHz)  | USB/DOT (MHz) | Notes   |
|-----|----|-----------|-----------------|-----------------------------|-------------------|-----------------|------------|---------------|---------|
| 1   | 0  | 100 MHz   | 66 MHz          | 66IN                        | 66-MHz Input      | 66IN/2          | 14.318 MHz | 48 MHz        | 2, 3, 4 |
| 1   | 1  | 133 MHz   | 66 MHz          | 66IN                        | 66-MHz Input      | 66IN/2          | 14.318 MHz | 48 MHz        | 2, 3, 4 |
| 0   | 0  | 100 MHz   | 66 MHz          | 66 MHz                      | 66-MHz Input      | 33 MHz          | 14.318 MHz | 48 MHz        | 2, 3, 4 |
| 0   | 1  | 133 MHz   | 66 MHz          | 66 MHz                      | 66-MHz Input      | 33 MHz          | 14.318 MHz | 48 MHz        | 2, 3, 4 |
| Mid | 0  | Hi-Z      | Hi-Z            | Hi-Z                        | Hi-Z              | Hi-Z            | Hi-Z       | Hi-Z          | 5, 6    |
| Mid | 1  | TCLK/2    | TCLK/4          | TCLK/4                      | TCLK/4            | TCLK/8          | TCLK       | TCLK/2        | 1, 6    |

**Swing Select Functions**

| Mult0 | Board Target Trace/Term Z | Reference R, IREF = $V_{DD}/(3 \cdot R_r)$ | Output Current             | $V_{OH}$ @ Z, |
|-------|---------------------------|--------------------------------------------|----------------------------|---------------|
| 0     | 50 ohm                    | $R_r = 221\%$ ,<br>IREF = 5.00 mA          | $I_{OH} = 4 \cdot I_{ref}$ | 1.0V @ 50     |
| 1     | 50 ohm                    | $R_r = 475\%$ ,<br>IREF = 2.32 mA          | $I_{OH} = 6 \cdot I_{ref}$ | 0.7V @ 50     |

**Clock Driver Impedances**

| Buffer Name       | $V_{DD}$ Range | Buffer Type | Impedance  |            |            |
|-------------------|----------------|-------------|------------|------------|------------|
|                   |                |             | Min. (Ohm) | Typ. (Ohm) | Max. (Ohm) |
| CPU, CPU#         |                | Type X1     |            | 50         |            |
| REF               | 3.135–3.465    | Type 3      | 20         | 40         | 60         |
| PCI, 3V66, 66BUFF | 3.135–3.465    | Type 5      | 12         | 30         | 55         |
| USB               | 3.135–3.465    | Type 3A     | 12         | 30         | 55         |
| DOT               | 3.135–3.465    | Type 3B     | 12         | 30         | 55         |

**Clock Enable Configuration**

| PD# | PCI_STOP# | CPU    | CPU#  | 3V66 | 66BUFF | PCI_F | PCI | USB/DOT | VCOS/OSC |
|-----|-----------|--------|-------|------|--------|-------|-----|---------|----------|
| 0   | X         | IREF*2 | FLOAT | LOW  | LOW    | LOW   | LOW | LOW     | OFF      |
| 1   | 0         | ON     | ON    | ON   | ON     | ON    | OFF | ON      | ON       |
| 1   | 1         | ON     | ON    | ON   | ON     | ON    | ON  | ON      | ON       |

**Notes:**

1. TCLK is a test clock driven in on the XTALIN input in test mode.
2. "Normal" mode of operation.
3. Range of reference frequency allowed is min. = 14.316 nominal = 14.31818 MHz, max. = 14.32 MHz.
4. Frequency accuracy of 48 MHz must be +167 PPM to match USB default.
5. Required for board level "bed of nails" testing.
6. Mid is defined a Voltage level between 1.0V and 1.8V for 3 level input functionality. Low is below 0.8V. High is above 2.0V.

## Serial Data Interface (SMBus)

To enhance the flexibility and function of the clock synthesizer, a two-signal SMBus interface is provided according to SMBus specification. Through the Serial Data Interface, various device functions such as individual clock output buffers, etc. can be individually enabled or disabled. CY28329 support both block read and block write operations.

The registers associated with the Serial Data Interface initializes to its default setting upon power-up, and therefore use of this interface is optional. Clock device register changes are normally made upon system initialization, if any are required. The interface can also be used during system operation for power management functions.

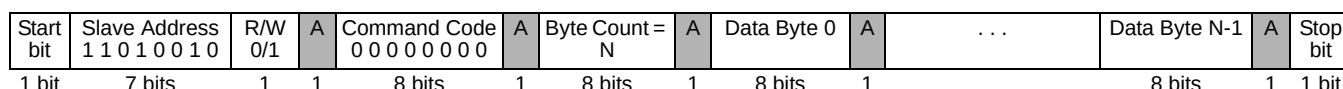
### Data Protocol

The clock driver serial protocol accepts only Block Writes from the controller. The bytes must be accessed in sequential order from lowest to highest byte, (most significant bit first) with the ability to stop after any complete byte has been transferred. Indexed bytes are not allowed.

A Block write begins with a slave address and a WRITE condition. The R/W bit is used by the SMBus controller as a data direction bit. A zero indicates a WRITE condition to the clock device. The slave receiver address is 11010010 (D2h).

A command code of 0000 0000 (00h) and the byte count bytes are required for any transfer. After the command code, the core logic issues a byte count, which describes number of additional bytes required for the transfer, not including the command code and byte count bytes. For example, if the host has 20 data bytes to send, the first byte would be the number 20 (14h), followed by the 20 bytes of data. The byte count byte is required to be a minimum of 1 byte and a maximum of 32 bytes. It may not be 0. *Figure 1* shows an example of a block write.

A transfer is considered valid after the acknowledge bit corresponding to the byte count is read by the controller.



☐ From Master to Slave

☒ From Slave to Master

**Figure 1. An Example of a Block Write**

## Data Byte Configuration Map

**Data Byte 0: Control Register (0 = Enable, 1 = Disable)**

| Bit   | Affected Pin#                               | Name                               | Description                                                               | Type | Power On Default |
|-------|---------------------------------------------|------------------------------------|---------------------------------------------------------------------------|------|------------------|
| Bit 7 | 5, 6, 7, 10, 11, 12, 13, 16, 17, 18, 33, 35 | PCI [0:6]<br>CPU[3:0]<br>3V66[1:0] | Spread Spectrum Enable<br>0 = Spread Off, 1 = Spread On                   | R/W  | 0                |
| Bit 6 | —                                           | —                                  | Reserved, set = 0                                                         | R    | 0                |
| Bit 5 | 35                                          | 3V66_1/VCH                         | VCH Select 66 MHz/48 MHz<br>0 = 66 MHz, 1 = 48 MHz                        | R/W  | 0                |
| Bit 4 | —                                           | —                                  | Reserved                                                                  | R    | 1                |
| Bit 3 | 10, 11, 12, 13, 16, 17, 18                  | PCI [6:0]                          | PCI_STOP#, 0 = stopped, 1 = running<br>(Does not affect PCI_F [2:0] pins) | R/W  | 1                |
| Bit 2 | 40                                          | S2                                 | S2<br>Reflects the value of the S2 pin sampled on Power-up                | R    | HW               |
| Bit 1 | 55                                          | S1                                 | S1<br>Reflects the value of the S1 pin sampled on Power-up                | R    | HW               |
| Bit 0 | —                                           | —                                  | Reserved                                                                  | R    | 1                |

**Data Byte 1:**

| Bit   | Pin#   | Name          | Description                                     | Type | Power On Default |
|-------|--------|---------------|-------------------------------------------------|------|------------------|
| Bit 7 | —      |               | CPU Mult0 Value                                 | R    | HW               |
| Bit 6 | 53, 54 | CPU3<br>CPU3# | CPU3 Output Enable<br>1 = Enabled; 0 = Disabled | R/W  | 1                |
| Bit 5 | —      | —             | Reserved, set = 0                               | R/W  | 0                |
| Bit 4 | —      | —             | Reserved, set = 0                               | R/W  | 0                |
| Bit 3 | —      | —             | Reserved, set = 0                               | R/W  | 0                |
| Bit 2 | 44, 45 | CPU2<br>CPU2# | CPU2 Output Enable<br>1 = Enabled; 0 = Disabled | R/W  | 1                |
| Bit 1 | 48, 49 | CPU1<br>CPU1# | CPU1 Output Enable<br>1 = Enabled; 0 = Disabled | R/W  | 1                |
| Bit 0 | 51, 52 | CPU0<br>CPU0# | CPU0 Output Enable<br>1 = Enabled; 0 = Disabled | R/W  | 1                |

**Data Byte 2:**

| Bit   | Pin# | Name | Pin Description                                 | Type | Power On Default |
|-------|------|------|-------------------------------------------------|------|------------------|
| Bit 7 | —    | —    | Reserved, set = 0                               | R    | 0                |
| Bit 6 | 18   | PCI6 | PCI6 Output Enable<br>1 = Enabled; 0 = Disabled | R/W  | 1                |
| Bit 5 | 17   | PCI5 | PCI5 Output Enable<br>1 = Enabled; 0 = Disabled | R/W  | 1                |
| Bit 4 | 16   | PCI4 | PCI4 Output Enable<br>1 = Enabled; 0 = Disabled | R/W  | 1                |
| Bit 3 | 13   | PCI3 | PCI3 Output Enable<br>1 = Enabled; 0 = Disabled | R/W  | 1                |
| Bit 2 | 12   | PCI2 | PCI2 Output Enable<br>1 = Enabled; 0 = Disabled | R/W  | 1                |
| Bit 1 | 11   | PCI1 | PCI1 Output Enable<br>1 = Enabled; 0 = Disabled | R/W  | 1                |
| Bit 0 | 10   | PCI0 | PCI0 Output Enable<br>1 = Enabled; 0 = Disabled | R/W  | 1                |

**Data Byte 3:**

| Bit   | Pin# | Name   | Pin Description                                                                                     | Type | Power On Default |
|-------|------|--------|-----------------------------------------------------------------------------------------------------|------|------------------|
| Bit 7 | 38   | DOT    | DOT 48 MHz Output Enable, 1 = enabled, 0 = disabled                                                 | R/W  | 1                |
| Bit 6 | 39   | USB    | USB 48 MHz Output Enable, 1 = enabled, 0 = disabled                                                 | R/W  | 1                |
| Bit 5 | 7    | PCI_F2 | Allow control of PCI_F2 with assertion of PCI_STOP#<br>0 = Free running; 1 = Stopped with PCI_STOP# | R/W  | 0                |
| Bit 4 | 6    | PCI_F1 | Allow control of PCI_F1 with assertion of PCI_STOP#<br>0 = Free running; 1 = Stopped with PCI_STOP# | R/W  | 0                |
| Bit 3 | 5    | PCI_F0 | Allow control of PCI_F0 with assertion of PCI_STOP#<br>0 = Free running; 1 = Stopped with PCI_STOP# | R/W  | 0                |
| Bit 2 | 7    | PCI_F2 | PCI_F2 Output Enable, 1 = enabled, 0 = disabled                                                     | R/W  | 1                |
| Bit 1 | 6    | PCI_F1 | PCI_F1 Output Enable, 1 = enabled, 0 = disabled                                                     | R/W  | 1                |
| Bit 0 | 5    | PCI_F0 | PCI_F0 Output Enable, 1 = enabled, 0 = disabled                                                     | R/W  | 1                |

**Data Byte 4:**

| Bit   | Pin# | Name        | Pin Description                                                                                                                                                                                    | Type | Power On Default |
|-------|------|-------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|------------------|
| Bit 7 | —    |             | Reserved, set = 0                                                                                                                                                                                  | R    | 0                |
| Bit 6 | —    |             | Reserved, set = 0                                                                                                                                                                                  | R    | 0                |
| Bit 5 | 33   | 3V66_0      | 3V66_0 Output Enable<br>1 = Enabled; 0 = Disabled                                                                                                                                                  | R/W  | 1                |
| Bit 4 | 35   | 3V66_1/VCH  | 3V66_1/VCH Output Enable<br>1 = Enabled; 0 = Disabled                                                                                                                                              | R/W  | 1                |
| Bit 3 | 24   | 66IN/3V66_5 | 3V66_5 Output Enable<br>1 = Enable; 0 = Disable<br><b>Note:</b> This bit should be used when pin 24 is configured as 3V66_5 output. do not clear this bit when pin 24 is configured as 66IN input. | R/W  | 1                |
| Bit 2 | 23   | 66BUFF2     | 66-MHz Buffered 2 Output Enable<br>1 = Enabled; 0 = Disabled                                                                                                                                       | R/W  | 1                |
| Bit 1 | 22   | 66BUFF1     | 66-MHz Buffered 1 Output Enable<br>1 = Enabled; 0 = Disabled                                                                                                                                       | R/W  | 1                |
| Bit 0 | 21   | 66BUFF0     | 66-MHz Buffered 0 Output Enable<br>1 = Enabled; 0 = Disabled                                                                                                                                       | R/W  | 1                |

**Data Byte 5:**

| Bit   | Pin#     | Name         | Pin Description                              | Type | Power On Default |
|-------|----------|--------------|----------------------------------------------|------|------------------|
| Bit 7 |          |              | Reserved, set = 0                            | R    | 0                |
| Bit 6 |          |              | Reserved, set = 0                            | R    | 0                |
| Bit 5 | 21,22,23 | 66BUFF [2:0] | Tpd 66IN to 66BUFF propagation delay control | R/W  | 0                |
| Bit 4 |          |              |                                              | R/W  | 0                |
| Bit 3 | 38       | DOT          | DOT edge rate control                        | R/W  | 0                |
| Bit 2 |          |              |                                              | R/W  | 0                |
| Bit 1 | 39       | USB          | USB edge rate control                        | R/W  | 0                |
| Bit 0 |          |              |                                              | R/W  | 0                |

**Byte 6: Vendor ID**

| Bit   | Description         | Type | Power On Default |
|-------|---------------------|------|------------------|
| Bit 7 | Revision Code Bit 3 | R    | 0                |
| Bit 6 | Revision Code Bit 2 | R    | 0                |
| Bit 5 | Revision Code Bit 1 | R    | 0                |
| Bit 4 | Revision Code Bit 0 | R    | 0                |
| Bit 3 | Vendor ID Bit 3     | R    | 1                |
| Bit 2 | Vendor ID Bit 2     | R    | 0                |
| Bit 1 | Vendor ID Bit 1     | R    | 0                |
| Bit 0 | Vendor ID Bit 0     | R    | 0                |

**Absolute Maximum Conditions**

(Above which the useful life may be impaired. For user guidelines, not tested.)

Supply Voltage.....-0.5 to +7.0V

Input Voltage..... -0.5V to  $V_{DD} + 0.5$

Storage Temperature (Non-Condensing) ....-65°C to +150°C

Max. Soldering Temperature (10 sec.) ..... +260°C

Junction Temperature..... +150°C

Package Power Dissipation..... 1W

Static Discharge Voltage .....  
(per MIL-STD-883, Method 3015) ..... > 2000V

**Operating Conditions** over which electrical parameters are guaranteed<sup>[7]</sup>

| Parameter                                                                                                    | Description                                            | Min.   | Max.     | Unit |
|--------------------------------------------------------------------------------------------------------------|--------------------------------------------------------|--------|----------|------|
| $V_{DD\_REF}$ , $V_{DD\_PCI}$ , $V_{DD\_CORE}$ ,<br>$V_{DD\_3V66}$ , $V_{DD\_48\text{ MHz}}$ , $V_{DD\_CPU}$ | 3.3V Supply Voltages                                   | 3.135  | 3.465    | V    |
| $T_A$                                                                                                        | Operating Temperature, Ambient                         | 0      | 70       | °C   |
| $C_{in}$                                                                                                     | Input Pin Capacitance                                  |        | 5        | pF   |
| $C_{XTAL}$                                                                                                   | XTAL Pin Capacitance                                   |        | 22.5     | pF   |
| $C_L$                                                                                                        | Max. Capacitive Load on<br>USBCLK, REF<br>PCICLK, 3V66 |        | 20<br>30 | pF   |
| $f_{(REF)}$                                                                                                  | Reference Frequency, Oscillator Nominal Value          | 14.318 | 14.318   | MHz  |

**DC Electrical Specifications** Over the Operating Range

| Parameter   | Description               | Test Conditions                                                      | Min.                      | Max. | Unit |
|-------------|---------------------------|----------------------------------------------------------------------|---------------------------|------|------|
| $V_{IH}$    | High-level Input Voltage  | Except Crystal Pads. Threshold voltage for crystal pads = $V_{DD}/2$ | 2.0                       |      | V    |
| $V_{IL}$    | Low-level Input Voltage   | Except Crystal Pads                                                  |                           | 0.8  | V    |
| $V_{OH}$    | High-level Output Voltage | USB, REF, 3V66                                                       | $I_{OH} = -1\text{ mA}$   | 2.4  | V    |
|             |                           | PCI                                                                  | $I_{OH} = -1\text{ mA}$   | 2.4  | V    |
| $V_{OL}$    | Low-level Output Voltage  | USB, REF, 3V66                                                       | $I_{OL} = 1\text{ mA}$    | 0.4  | V    |
|             |                           | PCI                                                                  | $I_{OL} = 1\text{ mA}$    | 0.55 | V    |
| $I_{IH}$    | Input High Current        | $0 \leq V_{IN} \leq V_{DD}$                                          | -5                        | 5    | mA   |
| $I_{IL}$    | Input Low Current         | $0 \leq V_{IN} \leq V_{DD}$                                          | -5                        | 5    | mA   |
| $I_{OH}$    | High-level Output Current | CPU<br>For $I_{OH} = 6 \cdot I_{REF}$ Configuration                  | Type X1, $V_{OH} = 0.65V$ | 12.9 | mA   |
|             |                           |                                                                      | Type X1, $V_{OH} = 0.74V$ | 14.9 |      |
|             |                           | REF, DOT, USB                                                        | Type 3, $V_{OH} = 1.00V$  | -29  |      |
|             |                           |                                                                      | Type 3, $V_{OH} = 3.135V$ | -23  |      |
|             |                           | 3V66, DOT, PCI                                                       | Type 5, $V_{OH} = 1.00V$  | -33  |      |
|             |                           |                                                                      | Type 5, $V_{OH} = 3.135V$ | -33  |      |
| $I_{OL}$    | Low-level Output Current  | REF, DOT, USB                                                        | Type 3, $V_{OL} = 1.95V$  | 29   | mA   |
|             |                           |                                                                      | Type 3, $V_{OL} = 0.4V$   | 27   |      |
|             |                           | 3V66, PCI                                                            | Type 5, $V_{OL} = 1.95V$  | 30   |      |
|             |                           |                                                                      | Type 5, $V_{OL} = 0.4V$   | 38   |      |
| $I_{OZ}$    | Output Leakage Current    | Three-state                                                          |                           | 10   | mA   |
| $I_{DD3}$   | 3.3V Power Supply Current | $V_{DD\_CORE}/V_{DD3.3} = 3.465V$ , $F_{CPU} = 133\text{ MHz}$       |                           | 360  | mA   |
| $I_{DDPD3}$ | 3.3V Shutdown Current     | $V_{DD\_CORE}/V_{DD3.3} = 3.465V$ and @ $I_{REF} = 2.32\text{ mA}$   |                           | 25   | mA   |
| $I_{DDPD3}$ | 3.3V Shutdown Current     | $V_{DD\_CORE}/V_{DD3.3} = 3.465V$ and @ $I_{REF} = 5.0\text{ mA}$    |                           | 45   | mA   |

**Note:**

7. Multiple Supplies: the voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.

**Switching Characteristics** Over the Operating Range<sup>[8]</sup>

| Parameter              | Output        | Description                                   | Test Conditions                                                                                      | Min.  | Max.  | Unit |
|------------------------|---------------|-----------------------------------------------|------------------------------------------------------------------------------------------------------|-------|-------|------|
| t <sub>1</sub>         | All           | Output Duty Cycle <sup>[9]</sup>              | Measured at 1.5V                                                                                     | 45    | 55    | %    |
| t <sub>2</sub>         | CPU           | Rise Time                                     | Measured differential waveform from –0.35V to +0.35V                                                 | 175   | 700   | ns   |
| t <sub>2</sub>         | USB, REF, DOT | Rising Edge Rate                              | Between 0.4V and 2.4V                                                                                | 0.5   | 2.0   | ns   |
| t <sub>2</sub>         | PCI, 3V66     | Rising Edge Rate                              | Between 0.4V and 2.4V                                                                                | 1.0   | 4.0   | V/ns |
| t <sub>3</sub>         | CPU           | Fall Time                                     | Measured differential waveform from –0.35V to +0.35V                                                 | 175   | 700   | ps   |
| t <sub>3</sub>         | USB, REF, DOT | Falling Edge Rate                             | Between 2.4V and 0.4V                                                                                | 0.5   | 2.0   | ns   |
| t <sub>3</sub>         | PCI, 3V66     | Falling Edge Rate                             | Between 2.4V and 0.4V                                                                                | 1.0   | 4.0   | V/ns |
| t <sub>4</sub>         | CPU           | CPU-CPU Skew                                  | Measured at Crossover                                                                                |       | 150   | ps   |
| t <sub>5</sub>         | 3V66 [0:1]    | 3V66-3V66 Skew                                | Measured at 1.5V                                                                                     |       | 500   | ps   |
| t <sub>5</sub>         | 66BUFF[0:2]   | 66BUFF-66BUFF Skew                            | Measured at 1.5V                                                                                     |       | 175   | ps   |
| t <sub>6</sub>         | PCI           | PCI-PCI Skew                                  | Measured at 1.5V                                                                                     |       | 500   | ps   |
| t <sub>7</sub>         | 3V66, PCI     | 3V66-PCI Clock Skew                           | 3V66 leads. Measured at 1.5V                                                                         | 1.5   | 3.5   | ns   |
| t <sub>8</sub>         | CPU           | Cycle-Cycle Clock Jitter                      | Measured at Crossover t <sub>8</sub> = t <sub>8A</sub> – t <sub>8B</sub><br>With all outputs running |       | 150   | ps   |
| t <sub>9</sub>         | 3V66          | Cycle-Cycle Clock Jitter                      | Measured at 1.5V t <sub>9</sub> = t <sub>9A</sub> – t <sub>9B</sub>                                  |       | 250   | ps   |
| t <sub>9</sub>         | USB, DOT      | Cycle-Cycle Clock Jitter                      | Measured at 1.5V t <sub>9</sub> = t <sub>9A</sub> – t <sub>9B</sub>                                  |       | 350   | ps   |
| t <sub>9</sub>         | PCI           | Cycle-Cycle Clock Jitter                      | Measured at 1.5V t <sub>9</sub> = t <sub>9A</sub> – t <sub>9B</sub>                                  |       | 500   | ps   |
| t <sub>9</sub>         | REF           | Cycle-Cycle Clock Jitter                      | Measured at 1.5V t <sub>9</sub> = t <sub>9A</sub> – t <sub>9B</sub>                                  |       | 1000  | ps   |
| t <sub>10</sub>        | ALL           | POR timing                                    | Measured at 1.5V <sup>[10, 11]</sup>                                                                 | 1.0   | 4.0   | ms   |
|                        | CPU           | Rise/Fall Matching                            | Measured with test loads <sup>[12, 13]</sup>                                                         |       | 235   | mV   |
| V <sub>oh</sub>        | CPU           | High-level Output Voltage including overshoot | Measured with test loads <sup>[13]</sup>                                                             | 0.92  | 1.45  | V    |
| V <sub>ol</sub>        | CPU           | Low-level Output Voltage including undershoot | Measured with test loads <sup>[13]</sup>                                                             | –0.2  | 0.35  | V    |
| V <sub>crossover</sub> | CPU           | Crossover Voltage                             | Measured with test loads <sup>[13]</sup>                                                             | 0.250 | 0.550 | V    |

**Notes:**

8. All parameters specified with loaded outputs.

9. Duty cycle is measured at 1.5V when V<sub>DD</sub> = 3.3V. When V<sub>DD</sub> = 2.5V, duty cycle is measured at 1.25V.

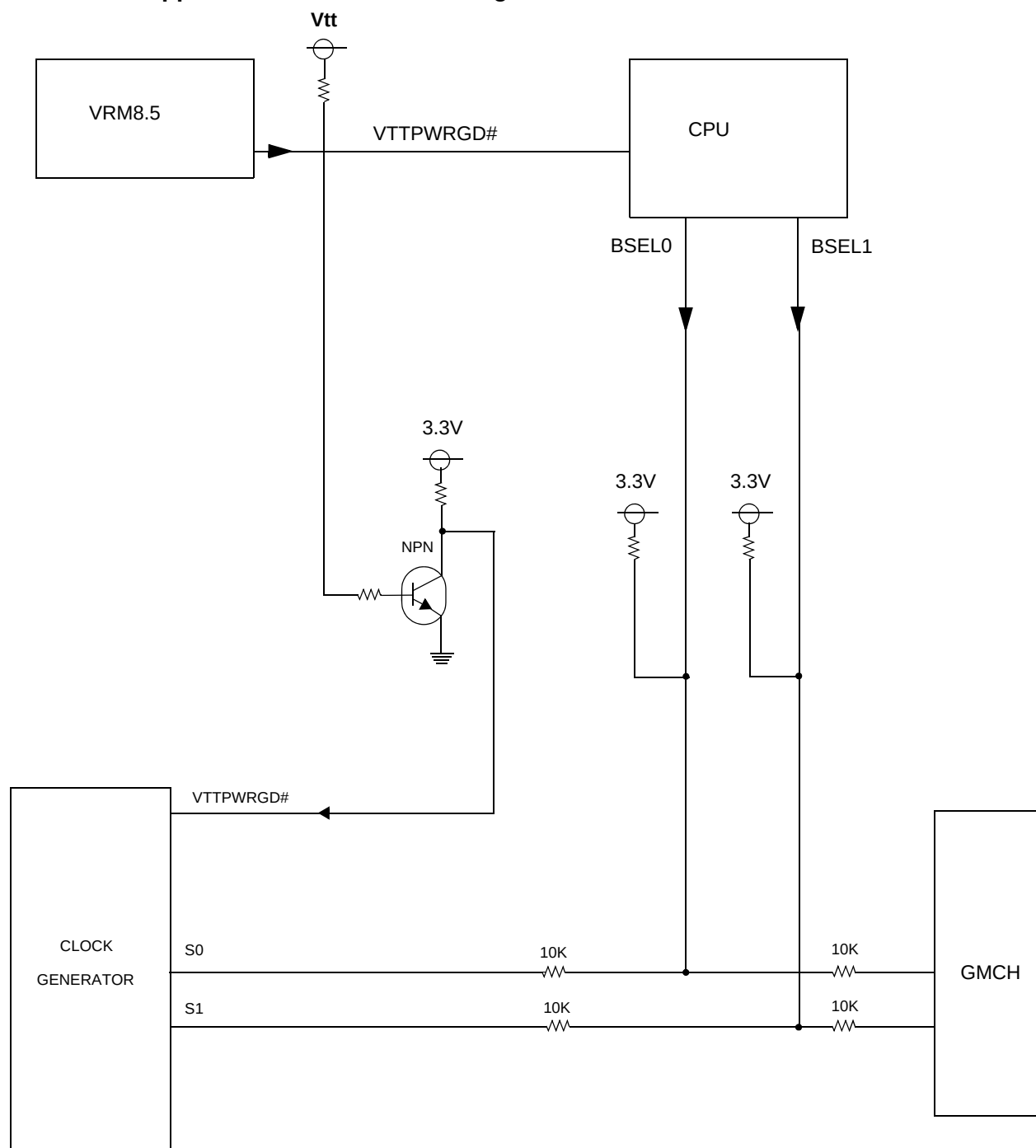
10. POR starts when V<sub>DD</sub> reaches 1.5V.

11. All PULL-UPS must ramp at the same rate as V<sub>DD</sub>.

12. Determined as a fraction of 2\*(Trp – Trn)/(Trp + Trn) Where Trp is a rising edge and Trn is an intersecting falling edge.

13. The test load is R<sub>s</sub> = 33.2Ω, R<sub>p</sub> = 49.9Ω in test circuit.

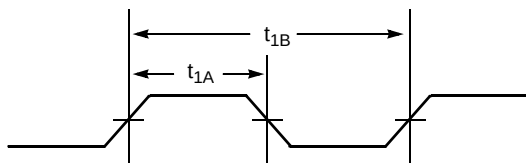
## Definition and Application of VTPWRGD# Signal



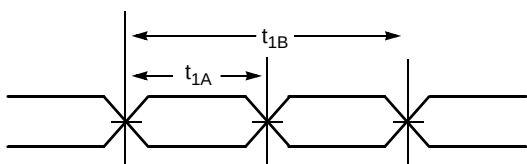


## Switching Waveforms

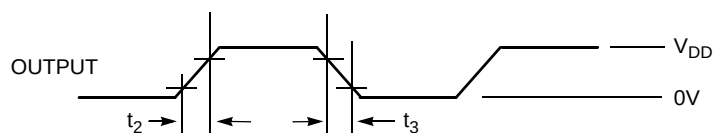
### Duty Cycle Timing (Single-Ended Output)



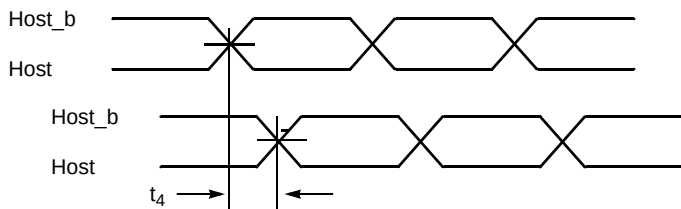
### Duty Cycle Timing (CPU Differential Output)



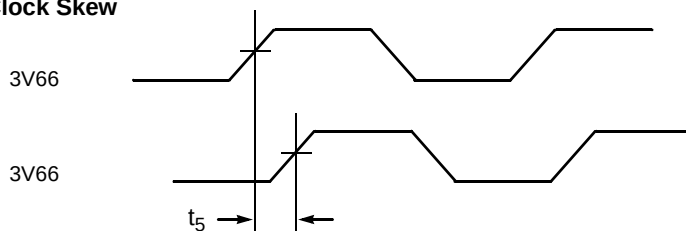
### All Outputs Rise/Fall Time



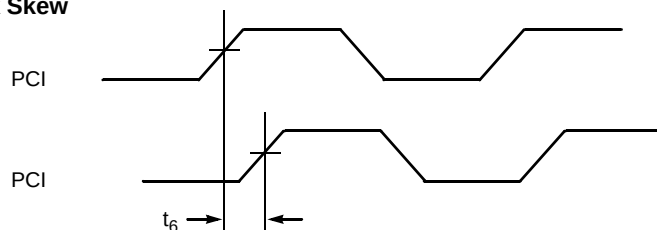
### CPU-CPU Clock Skew



### 3V66-3V66 Clock Skew

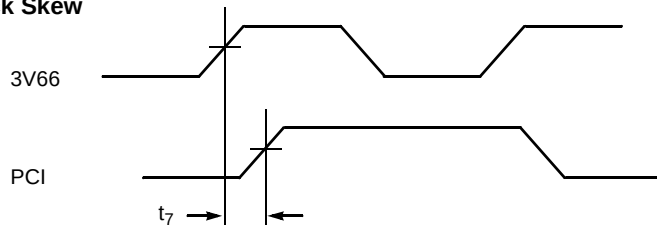


### PCI-PCI Clock Skew

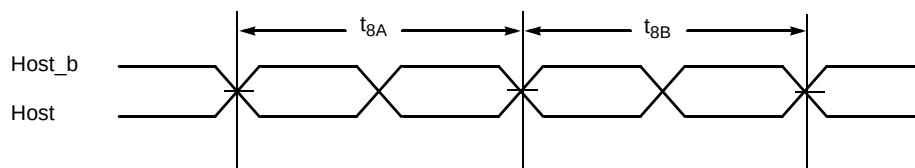


## Switching Waveforms (continued)

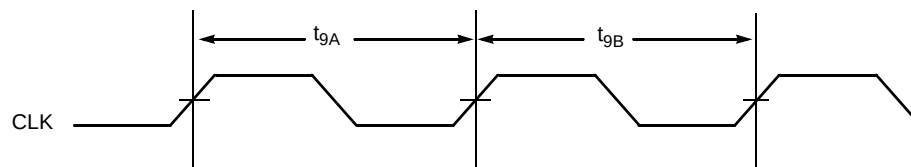
### 3V66-PCI Clock Skew



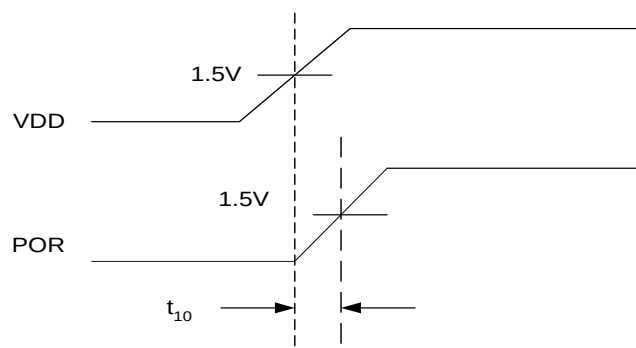
### CPU Clock Cycle-Cycle Jitter



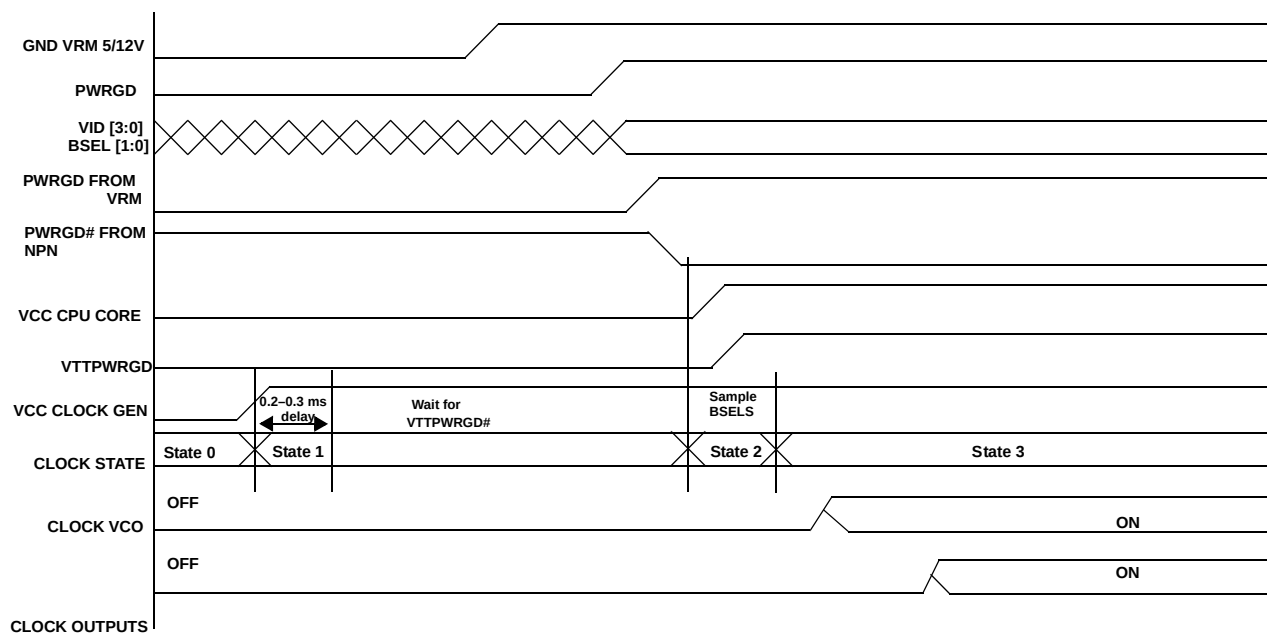
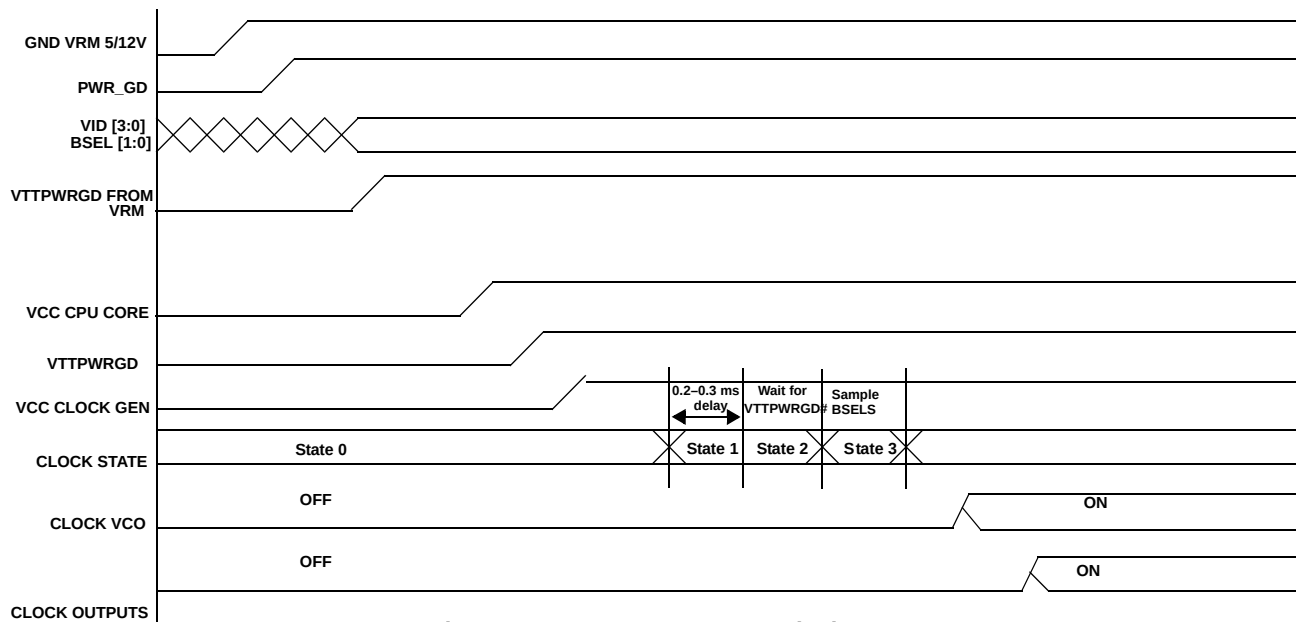
### Cycle-Cycle Clock Jitter



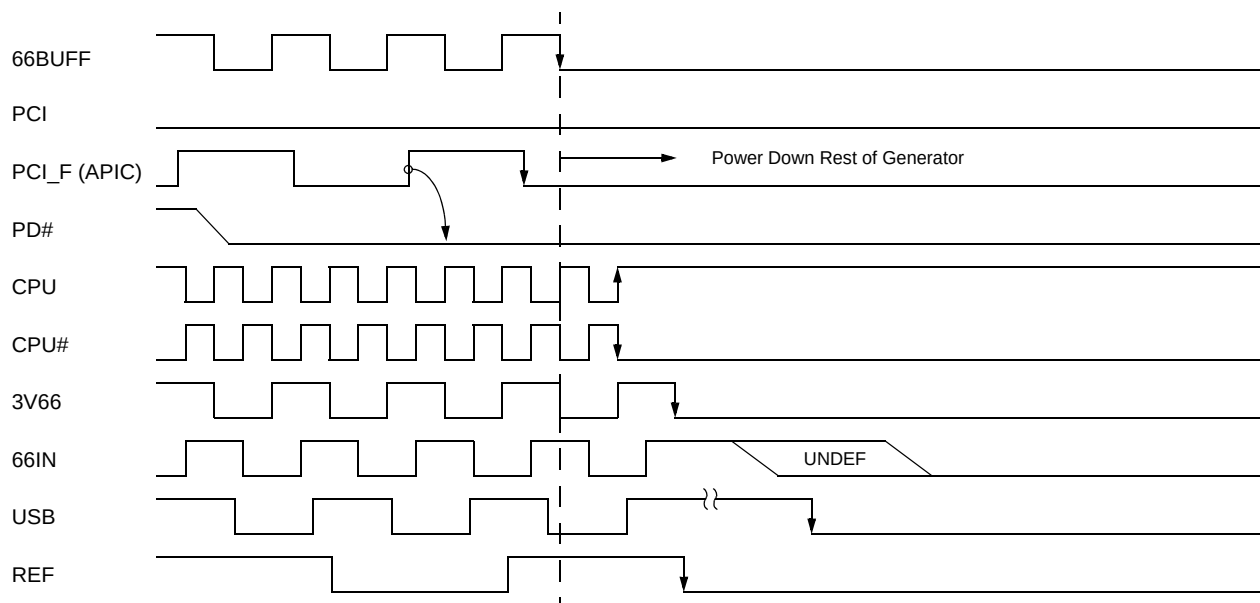
## VDD and POR Timing



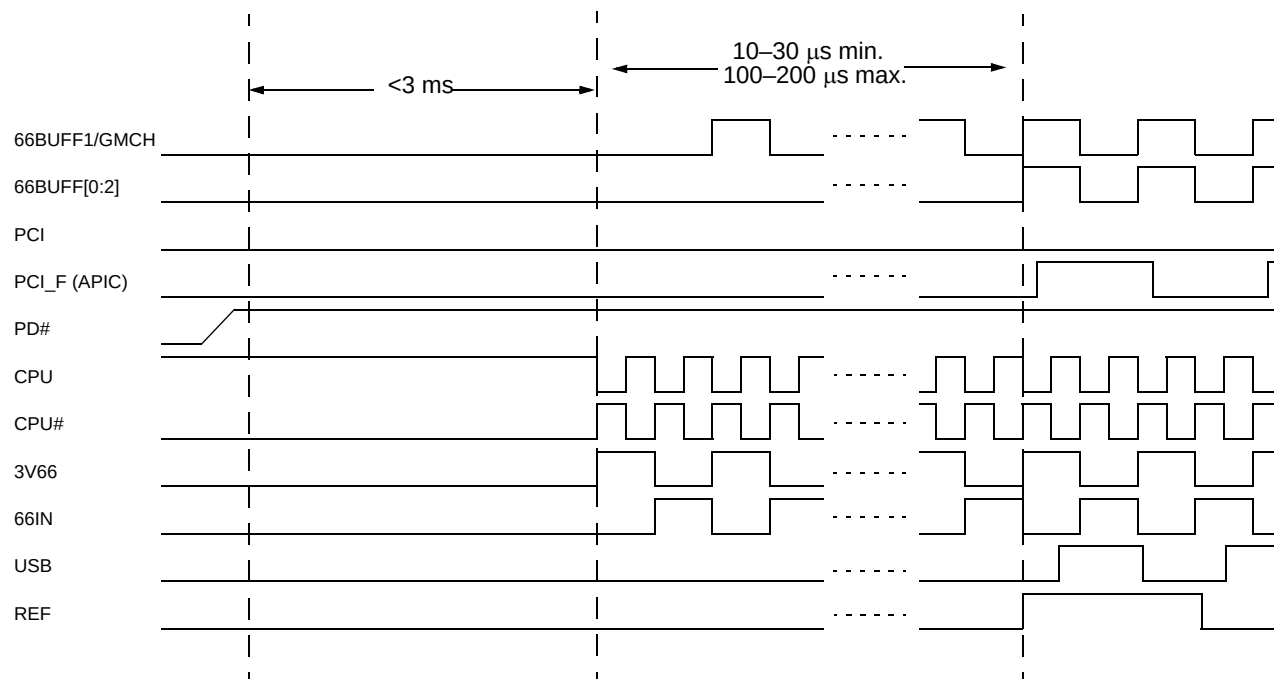
## VTPWRGD# Timing Diagrams



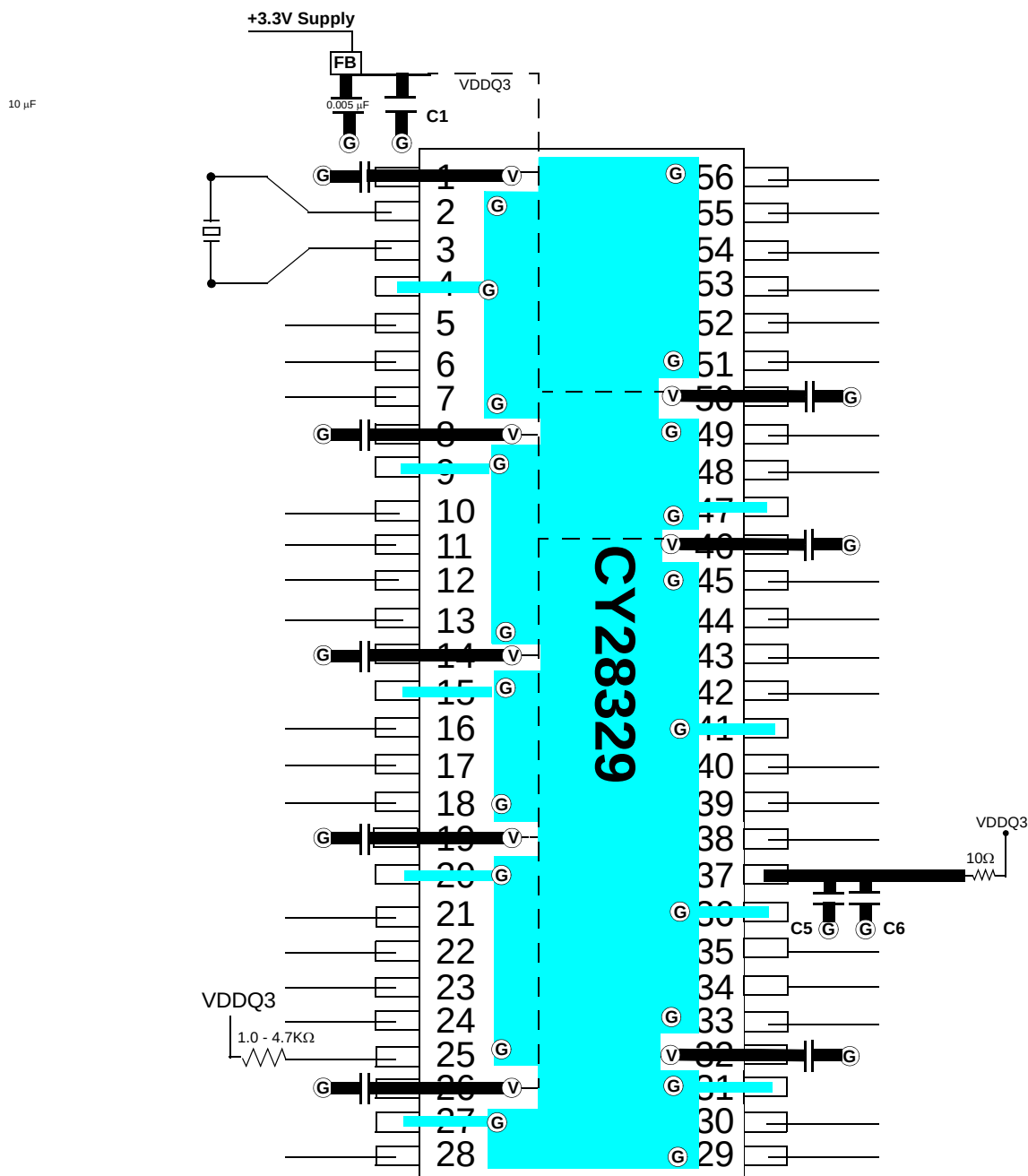
### PD# Assertion



### PD# Deassertion



## Layout Example



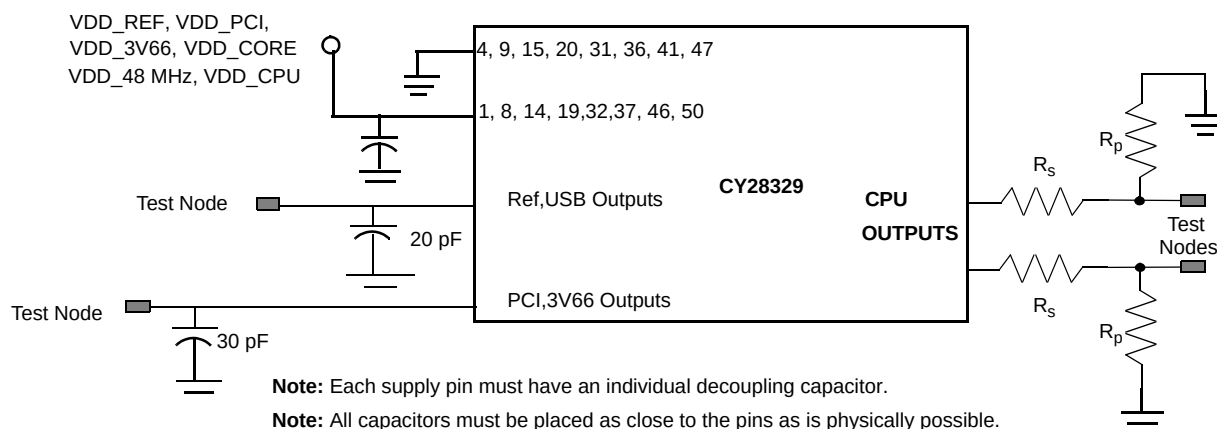
FB = Dale ILB1206 - 300 or 2TDKACB2012L-120 or 2 Murata BLM21B601S

Ceramic Caps C1 = 10-22  $\mu\text{F}$  C2 = 0.005  $\mu\text{F}$  C5 = 0.1  $\mu\text{F}$  C6 = 10  $\mu\text{F}$

ⓐ = VIA to GND plane layer ⓑ = VIA to respective supply plane layer

Note: Each supply plane or strip should have a ferrite bead and capacitors

## Test Circuit

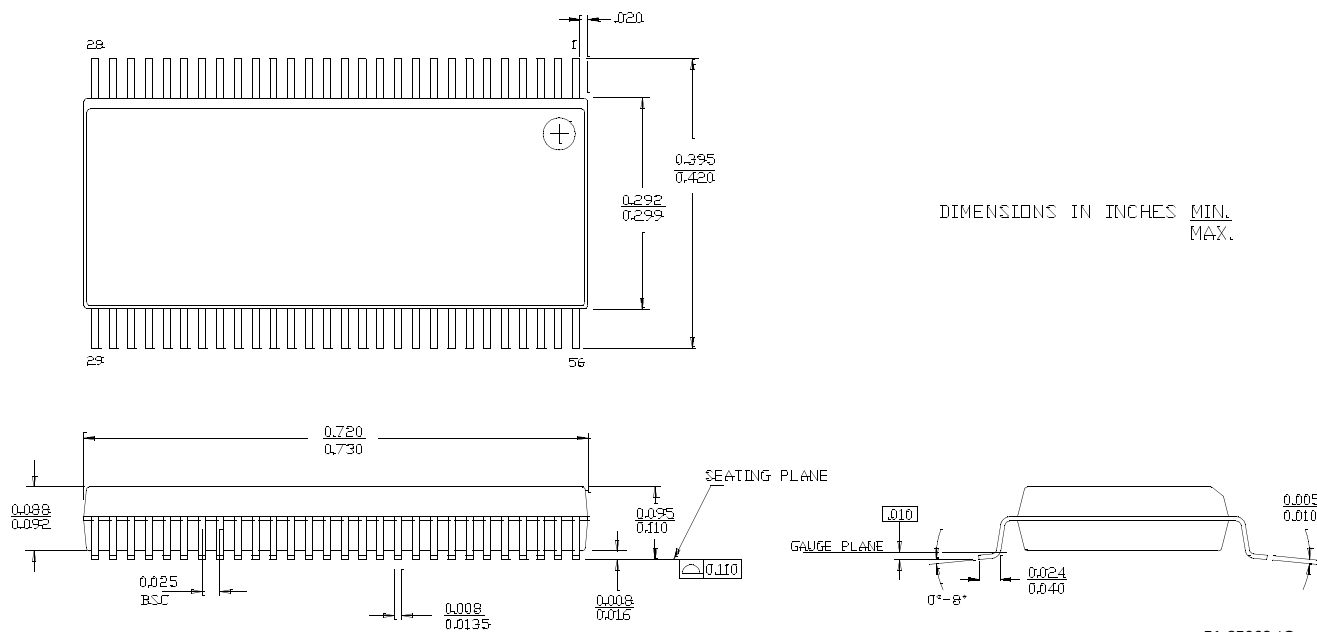


## Ordering Information

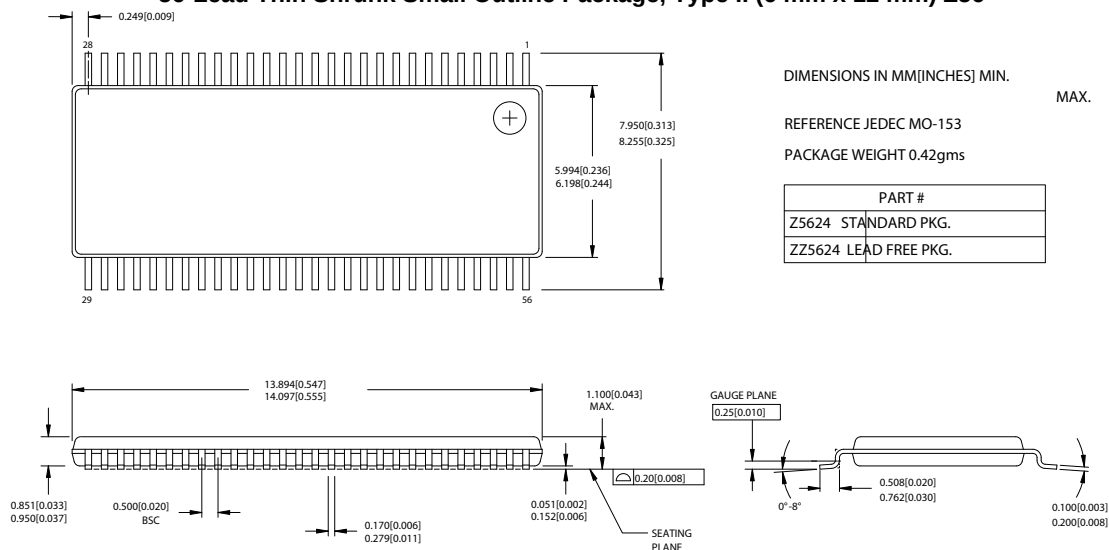
| Ordering Code    | Package Type                                                     | Operating Range |
|------------------|------------------------------------------------------------------|-----------------|
| <b>Standard</b>  |                                                                  |                 |
| CY28329PVC       | 56-Pin Small Shrunk Outline Package (SSOP)                       | Commercial      |
| CY28329PVCT      | 56-Pin Small Shrunk Outline Package (SSOP) - Tape and Reel       | Commercial      |
| CY28329ZC        | 56-Pin Thin Small Shrunk Outline Package (TSSOP)                 | Commercial      |
| CY28329ZCT       | 56-Pin Thin Small Shrunk Outline Package (TSSOP) - Tape and Reel | Commercial      |
| <b>Lead-free</b> |                                                                  |                 |
| CY28329OXC       | 56-Pin Small Shrunk Outline Package (SSOP)                       | Commercial      |
| CY28329OXCT      | 56-Pin Small Shrunk Outline Package (SSOP) - Tape and Reel       | Commercial      |
| CY28329ZXC       | 56-Pin Thin Small Shrunk Outline Package (TSSOP)                 | Commercial      |
| CY28329ZXCT      | 56-Pin Thin Small Shrunk Outline Package (TSSOP)                 | Commercial      |

## Package Drawing and Dimensions

### 56-Lead Shrink Small Outline Package O56



### 56-Lead Thin Shrink Small Outline Package, Type II (6 mm x 12 mm) Z56



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