Typical Applications Circuit

Figure 1 Typical Application Circuit

Pin Descriptions

Pin Name	Pin Number			Function
	SO-8EP	MSOP-8EP	U-DFN3030-10	
PG	1	1	5	Power Good.Output open drain to indicate the status of V_{OUT} via monitoring the FB pin. This pin is pulled low when the voltage is outside the limits, during thermal shutdown and if either V_{CNTL} or V_{IN} go below their thresholds.
EN	2	2	6	Enable Pin. Driving this pin low will disable the part. When left floating an internal current source will pull this pin high and enable it.
VIN	3	3	7,8,9	Power Input Pin for current supply. Connect a decoupling capacitor (≥10µF) as close as possible to the pin for noise filtering
VCNTL	4	4	10	BIAS supply for the controller, recommended 5V. Connect a decoupling capacitor (≥1µF) as close as possible to the pin for noise filtering.
NC	5	5		No Connection
V_{OUT}	6	6	1,2,3	Power output pin
FB	7	7	4	Feedback to set the output voltage via an external resistor divider between V_{OUT} and GND
GND	8	8	11	Ground
PAD	EP	EP	EP	Exposed pad connected to GND for good thermal conductivity

Functional Block Diagram

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Absolute Maximum Ratings (Note 4) (@T$_A$ = +25°C, unless otherwise specified.)

Symbol	Parameter	Rating	Unit
V$_{IN}$	V$_{IN}$ Supply Voltage (V$_{IN}$ to GND)	-0.3 to +4.0	V
V$_{CNTL}$	V$_{CNTL}$ Supply Voltage (V$_{CNTL}$ to GND)	-0.3 to +7.0	V
V$_{OUT}$	V$_{OUT}$ to GND Voltage	-0.3 to V$_{IN}$ +0.3	V
	PG to GND Voltage	-0.3 to +7.0	V
	EN, FB to GND Voltage	-0.3 to V$_{CNTL}$ +0.3	V
P$_D$	Power Dissipation (SO-8EP)	1.7	W
	Power Dissipation (MSOP-8EP)	1.5	
	Power Dissipation (U-DFN3030-10)	1.9	
T$_J$	Maximum Junction Temperature	150	°C
T$_{STG}$	Storage Temperature	-65 to +150	°C
T$_{SDR}$	Maximum Lead Soldering Temperature, 10 Seconds	260	°C

Note: 4. Stresses greater than the 'Absolute Maximum Ratings' specified above, may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions exceeding those indicated in this specification is not implied. Device reliability may be affected by exposure to absolute maximum rating conditions for extended periods of time.

Recommended Operating Conditions (@T$_A$ = +25°C, unless otherwise specified.)

Symbol	Parameter	Test Condition	Range	Unit
V$_{CNTL}$	V$_{CNTL}$ Supply Voltage		3.0 to 5.5	V
V$_{IN}$	V$_{IN}$ Supply Voltage		1.2 to 3.65	V
V$_{OUT}$	V$_{OUT}$ Output Voltage (when V$_{CNTL}$ - V$_{OUT}$ >1.9V)		0.8 to V$_{IN}$ – V$_{DROP}$	V
I$_{OUT}$	V$_{OUT}$ Output Current		0 to 3	A
C$_{OUT}$	V$_{OUT}$ Output Capacitance	I$_{OUT}$ = 3A at 25% nominal V$_{OUT}$	8 to 1100	µF
		I$_{OUT}$ = 2A at 25% nominal V$_{OUT}$	8 to 1700	
		I$_{OUT}$ = 1A at 25% nominal V$_{OUT}$	8 to 2400	
E$_{SRCOUT}$	ESR of V$_{OUT}$ Output Capacitor		0 to 200	mΩ
T$_A$	Ambient Temperature		-40 to +85	°C
T$_J$	Junction Temperature		-40 to +125	°C

Electrical Characteristics (Specifications apply over V$_{CNTL}$ = 5V, V$_{IN}$ = 1.8V, V$_{OUT}$ = 1.2V and T$_A$ = -40°C to +85°C, typical values @T$_A$ = +25°C, unless otherwise specified.)
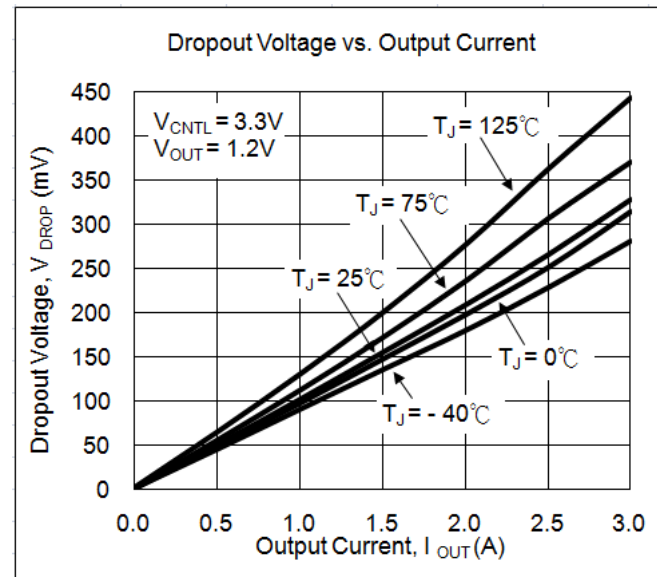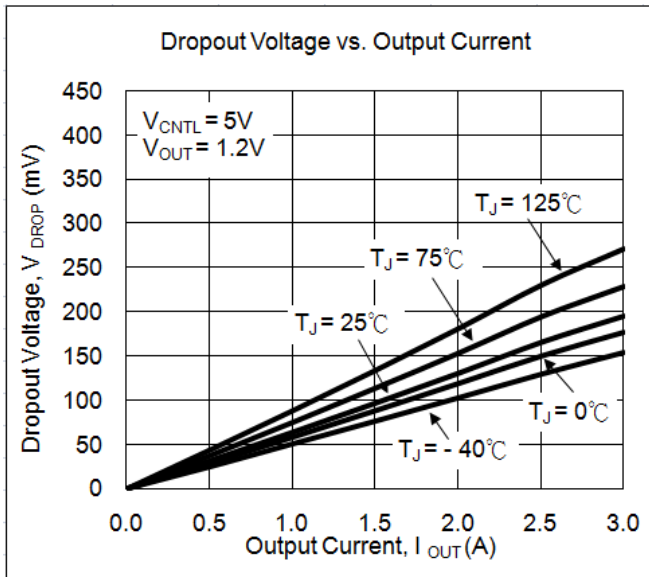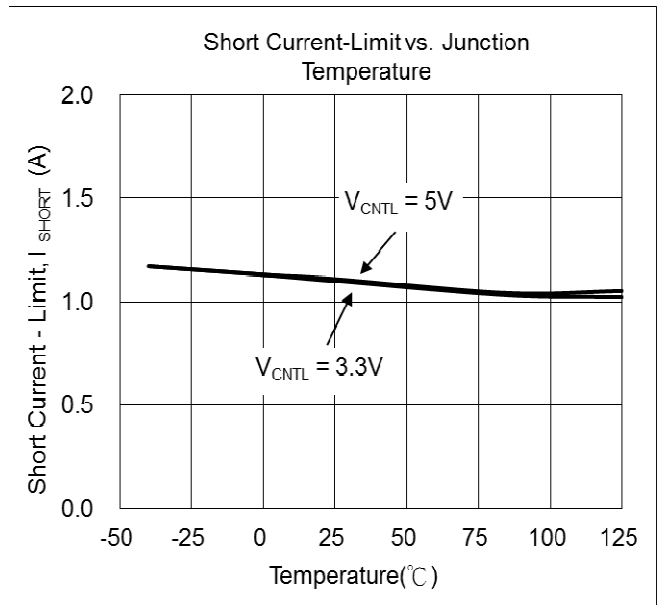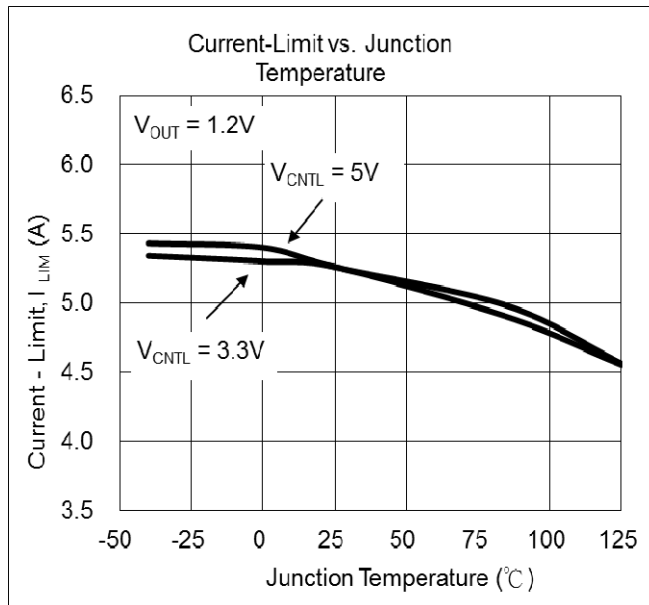
Symbol	Parameter	Conditions	AP7176B			Unit
			Min	Typ	Max	
SUPPLY CURRENT						
IV$_{CNTL}$	V$_{CNTL}$ Supply Current	EN = V$_{CNTL}$, I$_{OUT}$ = 0A	—	1.0	1.5	mA
I$_{SD}$	V$_{CNTL}$ Supply Current at Shutdown	EN = GND	—	15	30	µA
	V$_{IN}$ Supply Current at Shutdown	EN = GND, V$_{IN}$ = 3.65V	—	—	1	µA
POWER-ON-RESET (POR)						
	Rising V$_{CNTL}$ POR Threshold		2.50	2.70	2.95	V
	V$_{CNTL}$ POR Hysteresis		—	0.4	—	V
	Rising V$_{IN}$ POR Threshold		0.8	0.9	1.0	V
	V$_{IN}$ POR Hysteresis		—	0.5	—	V

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Electrical Characteristics (cont.) (Specifications apply over V_{CNTL} = 5V, V_{IN} = 1.8V, V_{OUT} = 1.2V and T_A = -40°C to +85°C, typical values @T_A = +25°C, unless otherwise specified.)

Symbol	Parameter	Conditions			AP7176B			Unit
					Min	Typ	Max	
OUTPUT VOLTAGE								
V_{REF}	Reference Voltage	FB=V_{OUT}			—	0.8	—	V
	Output Voltage Accuracy	V_{CNTL} = 3.0 ~ 5.5V, I_{OUT} = 0~3A, T_J = -40 to +125°C			-1.5	—	+1.5	%
	Load Regulation	I_{OUT} =0A to 3A			—	0.06	0.25	%
	Line Regulation	I_{OUT} =10mA, V_{CNTL} = 3.0 to 5.5V			-0.15	—	+0.15	%/V
	V_{OUT} Pull-low Resistance	V_{CNTL} = 3.3V, V_{EN} = 0V, V_{OUT} <0.8V			—	10	—	Ω
	FB Input Current	V_{FB} = 0.8V			-100	—	+100	nA
DROPOUT VOLTAGE								
V_{DROP}	V_{IN}-to-V_{OUT} Dropout Voltage (Note 5)	V_{CNTL} = 5.0V, I_{OUT} = 3A	V_{OUT} = 2.5V	T_J = 25°C	—	0.33	0.38	V
				T_J = -40°C to +125°C	—		0.53	
			V_{OUT} = 1.8V	T_J = +25°C	—	0.31	0.36	
				T_J = -40°C to +125°C	—		0.50	
			V_{OUT} = 1.2V	T_J = +25°C	—	0.30	0.35	
				T_J = -40°C to +125°C	—	—	0.48	
I_{LIM}	Current-Limit Level	T_J = +25°C, V_{OUT} = 80% $V_{NOMINAL}$			4.5	5.7	6.7	A
		T_J = -40°C to +125°C			4.2	—	—	A
PROTECTIONS								
I_{SHORT}	Short Current-Limit Level	V_{FB} < 0.2V			—	1.1	—	A
T_{SD}	Thermal Shutdown Temperature	T_J rising			—	170	—	°C
	Thermal Shutdown Hysteresis				—	50	—	°C
ENABLE AND SOFT-START								
	EN Logic High Threshold Voltage	V_{EN} rising			0.5	0.8	1.1	V
	EN Hysteresis				—	0.1	—	V
	EN Pull-High Current	EN = GND			—	5	—	µA
T_{SS}	Soft-Start Interval				0.3	0.6	1.2	ms
	Turn On Delay	From being enabled to V_{OUT} rising 10%			200	350	500	µs
POWER-GOOD AND DELAY								
V_{THPG}	Rising PG Threshold Voltage	V_{FB} rising			90	92	95	%
	PG Threshold Hysteresis				—	8	—	%
	PG Pull-low Voltage	PG sinks 5mA			—	0.25	0.4	V
	PG Debounce Interval	V_{FB} < falling PG voltage threshold			—	10	—	µs
	PG Delay Time	From V_{FB} = V_{THPG} to rising edge of the V_{PG}			1	2	4	ms
THERMAL CHARACTERISTIC								
$θ_{JA}$	Thermal Resistance Junction-to-Ambient	SO-8EP (Note 6)			—	70	—	°C/W
		MSOP-8EP (Note 7)			—	80	—	°C/W
		U-DFN3030-10 (Note 6)			—	60	—	°C/W
$θ_{JC}$	Thermal Resistance Junction-to-Ambient	SO-8EP (Note 6)			—	30	—	°C/W
		MSOP-8EP (Note 7)			—	30	—	°C/W
		U-DFN3030-10 (Note 6)			—	20	—	°C/W

Notes: 5. Dropout voltage is the voltage difference between the input and the output at which the output voltage drops 2% below its nominal value.
6. Device mounted on 2"*2" FR-4 substrate PC board, 2oz copper, with minimum recommended pad on top layer and thermal vias to bottom layer ground plane.
7. Device mounted on 2"*2" FR-4 substrate PC board, 2oz copper,with minimum recommended pad layout.
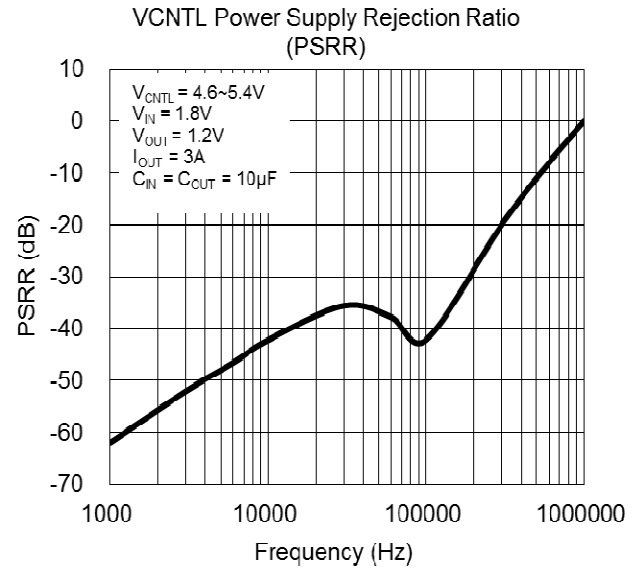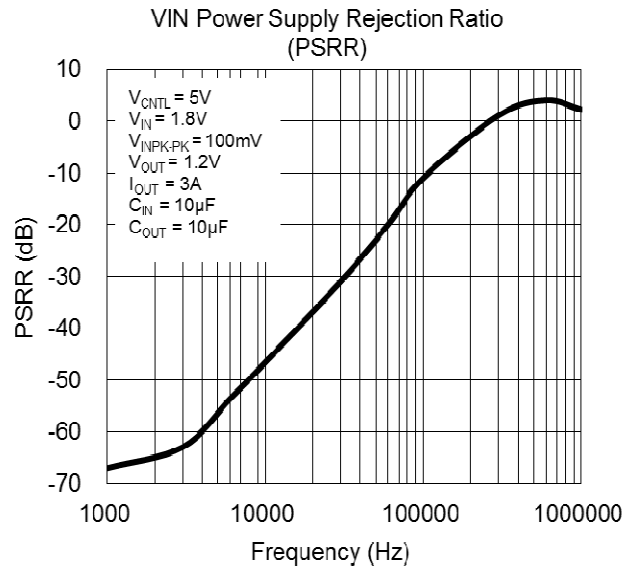
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Typical Characteristics

Current-Limit vs. Junction Temperature

Short Current-Limit vs. Junction Temperature

Dropout Voltage vs. Output Current

Dropout Voltage vs. Output Current

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Typical Characteristics (cont.)

Dropout Voltage vs. Output Current

$V_{CNTL} = 5V$
$V_{OUT} = 1.8V$

$T_J = 125℃$
$T_J = 75℃$
$T_J = 25℃$
$T_J = 0℃$
$T_J = - 40℃$

Dropout Voltage vs. Output Current

$V_{CNTL} = 5V$
$V_{OUT} = 2.5V$

$T_J = 125℃$
$T_J = 75℃$
$T_J = 25℃$
$T_J = 0℃$
$T_J = - 40℃$

Dropout Voltage vs. Output Current

$V_{CNTL} = 5V$
$V_{OUT} = 1.5V$

$T_J = 125℃$
$T_J = 75℃$
$T_J = 25℃$
$T_J = 0℃$
$T_J = - 40℃$

Reference Voltage vs. Junction Temperature

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Typical Characteristics (cont.)

VIN Power Supply Rejection Ratio
(PSRR)

V_{CNTL} = 5V
V_{IN} = 1.8V
$V_{INPK-PK}$ = 100mV
V_{OUT} = 1.2V
I_{OUT} = 3A
C_{IN} = 10µF
C_{OUT} = 10µF

PSRR (dB)

Frequency (Hz)

VCNTL Power Supply Rejection Ratio
(PSRR)

V_{CNTL} = 4.6~5.4V
V_{IN} = 1.8V
V_{OUT} = 1.2V
I_{OUT} = 3A
C_{IN} = C_{OUT} = 10µF

PSRR (dB)

Frequency (Hz)

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Operating Waveforms (Test Conditions V_{IN} = 1.8V, V_{CNTL} = 5V, V_{OUT} 1.2V, T_A = +25°C unless otherwise specified.)

Power On
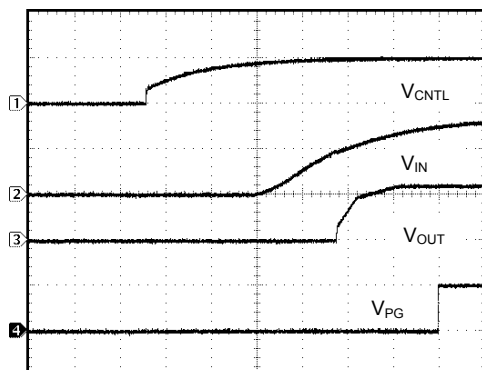
C_{OUT} =10µF, C_{IN} =10µF, R_L = 0.4Ω
CH1: V_{CNTL}, 5V/Div, DC
CH2: V_{IN}, 1V/Div, DC
CH3: V_{OUT}, 1V/Div, DC
CH4: V_{PG}, 5V/Div, DC
TIME: 2ms/Div

Power Off
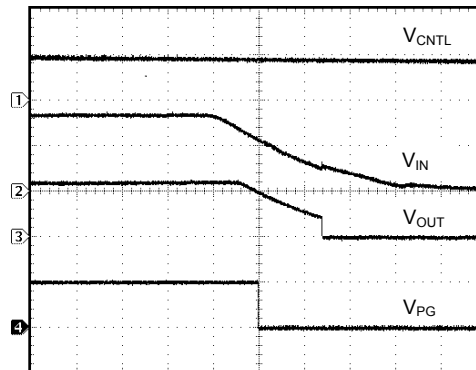
C_{OUT} = 10µF, C_{IN} =10µF, R_L = 0.4Ω
CH1: V_{CNTL}, 5V/Div, DC
CH2: V_{IN}, 1V/Div, DC
CH3: V_{OUT}, 1V/Div, DC
CH4: V_{PG}, 5V/Div, DC
TIME: 2ms/Div

Load Transient Response
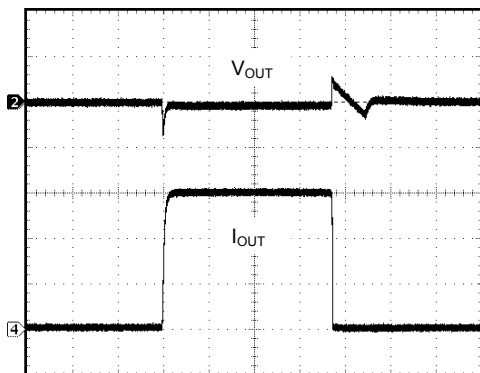
I_{OUT} = 10mA to 3A to10mA (rise / fall time = 1µs)
C_{OUT} = 10µF, C_{IN} = 10µF
CH2: V_{OUT}, 50mV/Div, AC
CH4: I_{OUT}, 1A/Div, DC
TIME: 50µs/Div

Over Current Protection
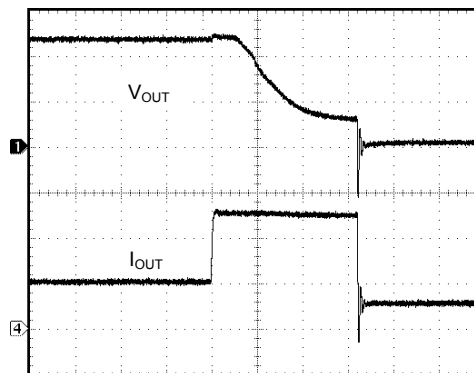
C_{OUT} = 10µF, C_{IN} = 10µF, I_{OUT} = 2A to 5.6A
CH1: V_{OUT}, 0.5V/Div, DC
CH4: I_{OUT}, 2A/Div, DC
TIME: 0.2ms/Div

Shutdown
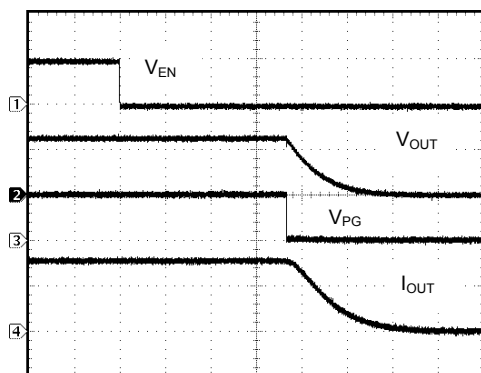
C_{OUT} = 10µF, C_{IN} = 10µF, R_L = 0.4Ω
CH1: V_{EN}, 5V/Div, DC
CH2: V_{OUT}, 1V/Div, DC
CH3: V_{PG}, 5V/Div, DC
CH4: I_{OUT}, 2A/Div, DC
TIME: 4µs/Div

Enable
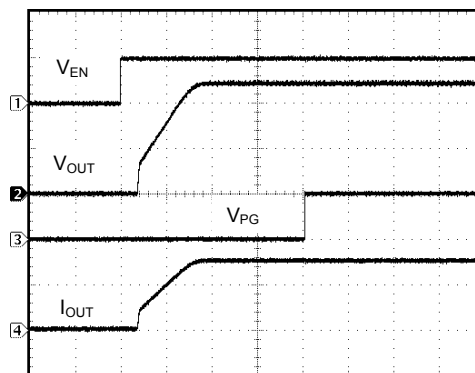
C_{OUT} = 10µF, C_{IN} = 10µF, R_L = 0.4Ω
CH1: V_{EN}, 5V/Div, DC
CH2: V_{OUT}, 1V/Div, DC
CH3: V_{PG}, 5V/Div, DC
CH4: I_{OUT}, 2A/Div, DC
TIME: 1ms/Div

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Application Information

Power Good and Delay

AP7176B monitors the feedback voltage V_{FB} on the FB pin. An internal delay timer is started after the PG voltage threshold (V_{THPG}) on the FB pin is reached. At the end of the delay time an internal NMOS of the PG is turned off to indicate that the power at the output is good (PG). This monitoring function is continued during operation and if V_{FB} falls 8% (typ) below V_{THPG}, the NMOS of the PG is turned on after a delay time of typical 10µs to avoid oscillating of the PG signal.

Power On Reset

AP7176B monitors both supply voltages, V_{CNTL} and V_{IN} to ensure operation as intended. A Soft-Start process is initiated after both voltages exceed their POR threshold during power on. During operation the POR component continues to monitor the supply voltage and pulls the PG low to indicate an out of regulation supply. This function will engage without regard to the status of the output.

Soft-Start

AP7176B incorporates an internal Soft-Start function. The output voltage rise is controlled to limit the current surge during start-up. The typical Soft-Start time is 0.6ms

Current-Limit Protection

AP7176B monitors the current flow through the NMOS and limits the maximum current to avoid damage to the load and AP7176B during overload conditions.

Short Circuit Current-Limit Protection

AP7176B incorporates a current limit function to reduce the maximum current to 1.1A (typ) when the voltage at FB falls below 0.2V (typ) during an overload or short circuit situation.

During start-up period, this function is disabled to ensure successful heavy load start-up.

Enable Control

If the enable pin (EN) is left open, an internal current source of ~5µA pulls the pin up and enables the AP7176B. This will reduce the bill of material saving an external pull up resistor. Driving the enable pin low disables the device. Driving the pin high subsequently initiates a new Soft-Start cycle.

Output Voltage Regulation

Output Voltage is set by resistor divider from V_{OUT} via FB pin to GND. Internally V_{FB} is compared to a 0.8V temperature compensated reference voltage and the NMOS pass element regulates the output voltage while delivering current from V_{IN} to V_{OUT}.

Setting the Output Voltage

A resistor divider connected to FB pin programs the output voltage.

$$V_{OUT} = V_{REF} * \left(1 + \frac{R1}{R2}\right) V$$

R1 is connected from V_{OUT} to FB with Kelvin sensing connection. R2 is connected from FB to GND. To improve load transient response and stability, a bypass capacitor can be connected in parallel with R1. (optional in typical application circuit)

Power Sequencing

AP7176B requires no specific sequencing between V_{IN} and V_{CNTL}. However, care should be taken to avoid forcing V_{OUT} for prolonged times without the presence of V_{IN}. Conduction through internal parasitic diode (from V_{OUT} to V_{IN}) could damage AP7176B.

Thermal Shutdown

The PCB layout and power requirements for AP7176B under normal operation condition should allow enough cooling to restrict the junction temperature to +125°C. The packages for AP7176B have an exposed PAD to support this. These packages provide better connection to the PCB and thermal performance. Refer to the layout considerations.

If AP7176B junction temperature reaches +170°C a thermal protection block disables the NMOS pass element and lets the part cool down. After its junction temperature drops by 50°C (typ), a new Soft-Start cycle will be initiated. A new thermal protection will start, if the load or ambient conditions continue to raise the junction temperature to +170°C. This cycle will repeat until normal operation temperature is maintained again.

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Application Information (cont.)

Output Capacitor

An output capacitor (C_{OUT}) is needed to improve transient response and maintain stability. The ESR (equivalent series resistance) and capacitance drives the selection. Care needs to be taken to cover the entire operating temperature range.

The output capacitor can be an Ultra-Low-ESR ceramic chip capacitor or a low ESR bulk capacitor like a solid tantalum, POSCap or aluminum electrolytic capacitor.

C_{OUT} is used to improve the output stability and reduces the changes of the output voltage during load transitions. The slew rate of the current sensed via the FB pin in AP7176B is reduced. If the application has large load variations, it is recommended to utilize low-ESR bulk capacitors.

It is recommended to place ceramic capacitors as close as possible to the load and the ground pin and care should be taken to reduce the impedance in the layout.

Input Capacitor

To prevent the input voltage from dropping during load steps it is recommended to utilize an input capacitor (C_{IN}). As with the output capacitor the following are acceptable, Ultra-Low-ESR ceramic chip capacitor or low ESR bulk capacitor like a solid tantalum, POSCap or aluminum electrolytic capacitor. Typically it is recommended to utilize an capacitance of at least 10µF to avoid output voltage drop due to reduced input voltage. The value can be lower if V_{IN} changes are not critical for the application.

Layout Consideration

For good ground loop and stability, the input and output capacitors should be located close to the input, output, and ground pins of the device. No other application circuit is connected within the loop. Avoid using vias within ground loop. If vias must be used, multiple vias should be used to reduce via inductance.

The regulator ground pin should be connected to the external circuit ground to reduce voltage drop caused by trace impedance. Ground plane is generally used to reduce trace impedance.

Wide trace should be used for large current paths from V_{IN} to V_{OUT}, and load circuit.

Place the R1, R2, and C1 (optional) near the LDO as close as possible to avoid noise coupling.

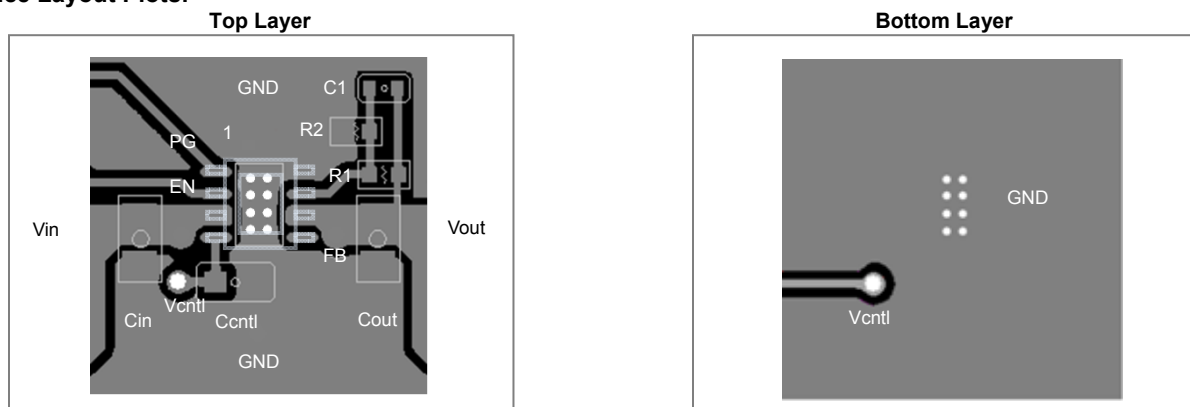R2 is placed close to device ground. Connect the ground of the R2 to the GND pin by using a dedicated trace.

Connect the pin of the R1 directly to the load for Kelvin sensing.

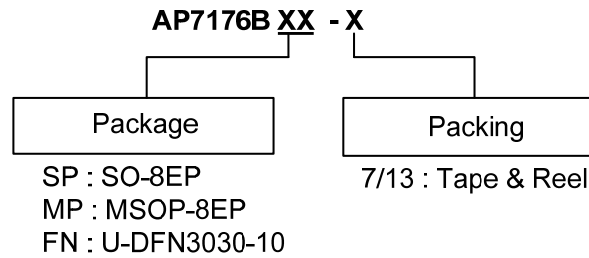No high current should flow through the ground trace of feedback loop and affect reference voltage stability.

For the packages with exposed pads, heat sinking is accomplished using the heat spreading capability of the PCB and its copper traces. Suitable PCB area on the top layer and thermal vias (0.3mm drill size with 1mm spacing, 4 to 8 vias at least) to the V_{IN} power plane can help to reduce device temperature greatly.
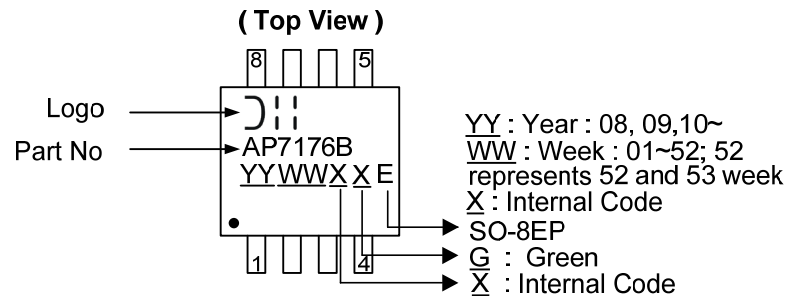
Reference Layout Plots:

Top Layer

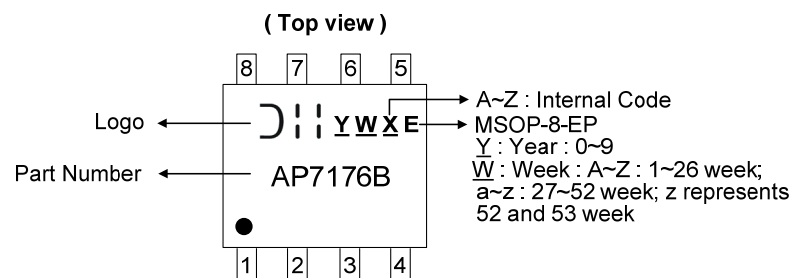

Bottom Layer

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Ordering Information

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Package	Packing
SP : SO-8EP MP : MSOP-8EP FN : U-DFN3030-10	7/13 : Tape & Reel

Part Number	Package Code	Packaging	13" Tape and Reel	
			Quantity	Part Number Suffix
AP7176BSP-13	SP	SO-8EP	2500/Tape & Reel	-13
AP7176BMP-13	MP	MSOP-8EP	2500/Tape & Reel	-13
AP7176BFN-7	FN	U-DFN3030-10	3000/Tape & Reel	-7

Marking Information

(1) SO-8EP

(Top View)

Logo

Part No

AP7176B
YYWWX X E

YY : Year : 08, 09,10~
WW : Week : 01~52; 52
represents 52 and 53 week
X : Internal Code
SO-8EP
G : Green
X : Internal Code

(2) MSOP-8EP

(Top view)

Logo

Part Number

AP7176B

Y W X E

A~Z : Internal Code
MSOP-8-EP
Y : Year : 0~9
W : Week : A~Z : 1~26 week;
a~z : 27~52 week; z represents
52 and 53 week

(3) U-DFN3030-10

(Top View)

XX

Y W X

XX : Identification Code
Y : Year : 0~9
W : Week : A~Z : 1~26 week;
a~z : 27~52 week; z represents
52 and 53 week
X : A~Z : Green
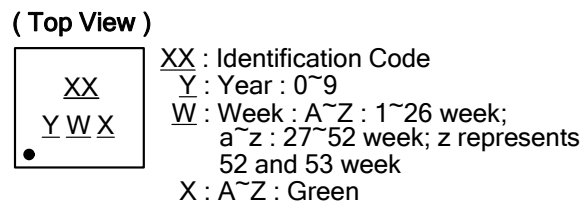
Part No.	Package	Identification Code
AP7176B	U-DFN3030-10	A7

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Package Outline Dimensions (All dimensions in mm.)

Please see AP02002 at http://www.diodes.com/datasheets/ap02002.pdf for latest version.

(1) SO-8EP

Exposed Pad

Bottom View

Gauge Plane
Seating Plane
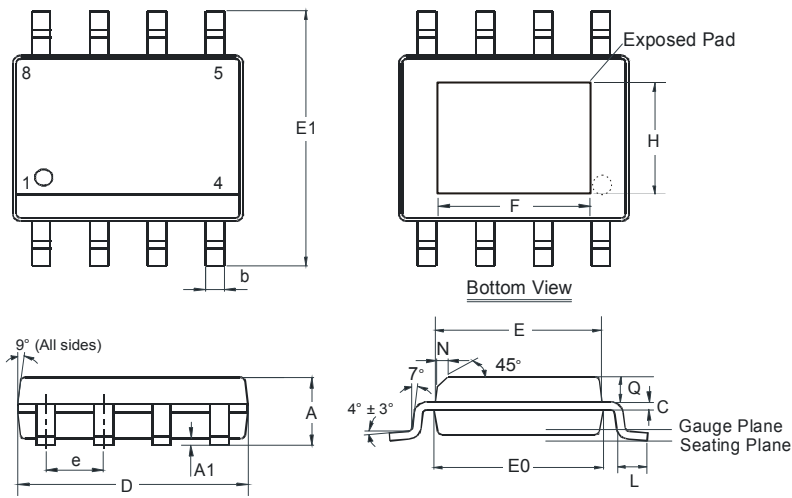
SO-8EP (SOP-8L-EP)			
Dim	Min	Max	Typ
A	1.40	1.50	1.45
A1	0.00	0.13	-
b	0.30	0.50	0.40
C	0.15	0.25	0.20
D	4.85	4.95	4.90
E	3.80	3.90	3.85
E0	3.85	3.95	3.90
E1	5.90	6.10	6.00
e	-	-	1.27
F	2.75	3.35	3.05
H	2.11	2.71	2.41
L	0.62	0.82	0.72
N	-	-	0.35
Q	0.60	0.70	0.65
All Dimensions in mm			

(2) MSOP-8EP

Gauge Plane
Seating Plane

Detail C

See Detail C
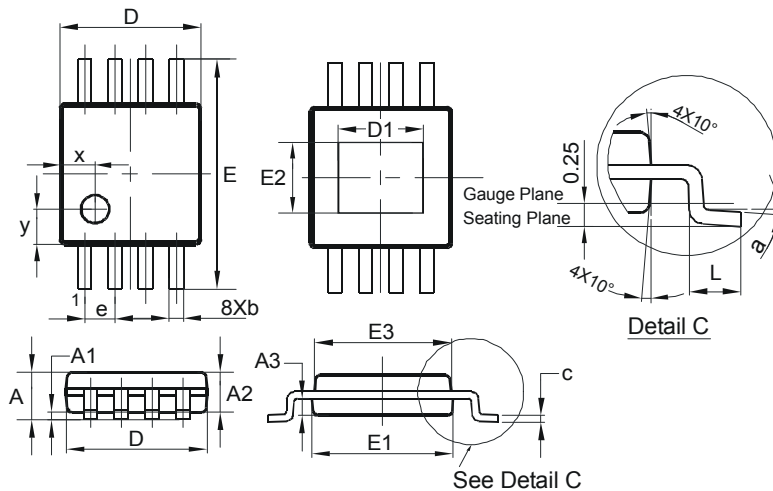
MSOP-8EP			
Dim	Min	Max	Typ
A	-	1.10	-
A1	0.05	0.15	0.10
A2	0.75	0.95	0.86
A3	0.29	0.49	0.39
b	0.22	0.38	0.30
c	0.08	0.23	0.15
D	2.90	3.10	3.00
D1	1.60	2.00	1.80
E	4.70	5.10	4.90
E1	2.90	3.10	3.00
E2	1.30	1.70	1.50
E3	2.85	3.05	2.95
e	-	-	0.65
L	0.40	0.80	0.60
a	0°	8°	4°
x	-	-	0.750
y	-	-	0.750
All Dimensions in mm			

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Package Outline Dimensions (cont.) (All dimensions in mm.)

Please see AP02002 at http://www.diodes.com/datasheets/ap02002.pdf for latest version.

(3) U-DFN3030-10

SEATING PLANE

Pin#1 ID
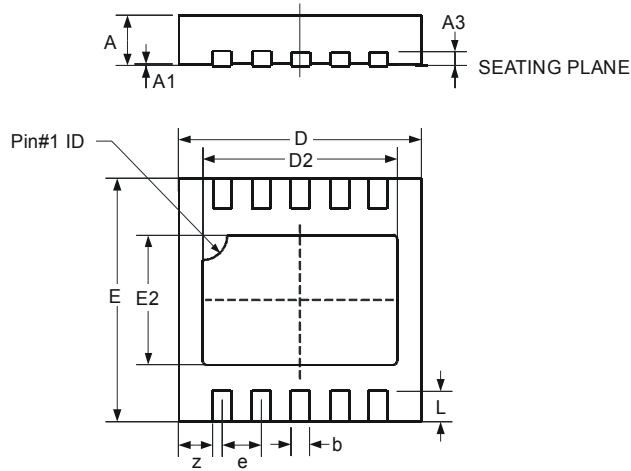
U-DFN3030-10			
Dim	**Min**	**Max**	**Typ**
A	0.57	0.63	0.60
A1	0	0.05	0.02
A3	—	—	0.15
b	0.20	0.30	0.25
D	2.90	3.10	3.00
D2	2.30	2.50	2.40
e	—	—	0.50
E	2.90	3.10	3.00
E2	1.50	1.70	1.60
L	0.25	0.55	0.40
z	—	—	0.375
All Dimensions in mm			

Suggested Pad Layout

Please see AP02001 at http://www.diodes.com/datasheets/ap02001.pdf for the latest version.

(1) SO8-EP
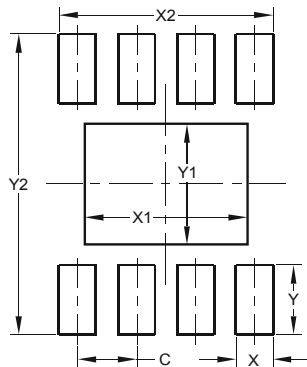
Dimensions	Value (in mm)
C	1.270
X	0.802
X1	3.502
X2	4.612
Y	1.505
Y1	2.613
Y2	6.500

(2) MSOP-8EP
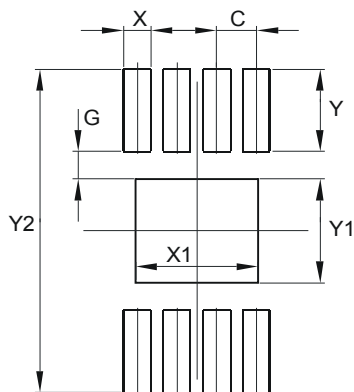
Dimensions	Value (in mm)
C	0.650
G	0.450
X	0.450
X1	2.000
Y	1.350
Y1	1.700
Y2	5.300

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(3) U-DFN3030-10
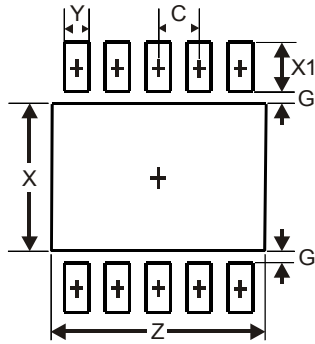
Dimensions	Value (in mm)
Z	2.60
G	0.15
X	1.80
X1	0.60
Y	0.30
C	0.50

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