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**2/2015—Rev. H to Rev. I**

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**9/2014—Rev. G to Rev. H**

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**2/2013—Rev. F to Rev. G**

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**10/2006—Revision 0: Initial Version**



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## APPLICATIONS

**Mobile handsets**
**Digital still cameras**
**Portable media and DVD players**
**Portable game consoles**
**Digital camcorders**
**Set-top box (STB)**
**Automotive infotainment (ADV7392 and ADV7393 only)**

## GENERAL DESCRIPTION

The ADV7390/ADV7391/ADV7392/ADV7393 are a family of high speed, digital-to-analog video encoders on single monolithic chips. Three 2.7 V/3.3 V, 10-bit video DACs (a single DAC for the WLCSP package) provide support for composite (CVBS), S-Video (Y-C), or component (YPrPb/RGB) analog outputs in either standard definition (SD) or high definition (HD) video formats. The single DAC WLCSP package supports CVBS (NTSC and PAL) output only in SD resolution (see Table 2).

Optimized for low power operation, occupying a minimal footprint, and requiring few external components, these encoders are ideally suited to portable and power-sensitive applications requiring TV-out functionality. Cable detection and DAC auto power-down features ensure that power consumption is kept to a minimum.

The ADV7390/ADV7391 have an 8-bit video input port that supports SD video formats over an SDR interface and HD video formats over a DDR interface. The ADV7392/ADV7393 have a 16-bit video input port that can be configured in a variety of ways. SD RGB input is supported.

All members of the family support embedded EAV/SAV timing codes, external video synchronization signals, and the I²C® and communication protocol. Table 1 and Table 2 list the video standards directly supported by the ADV7390/ADV7391/ADV7392/ADV7393 family.

**Table 1. Standards Directly Supported by the LFCSP Packages**

| Active Resolution | I/P[1] | Frame Rate (Hz) | Clock Input (MHz) | Standard |
|---|---|---|---|---|
| 720 × 240 | P | 59.94 | 27 | |
| 720 × 288 | P | 50 | 27 | |
| 720 × 480 | I | 29.97 | 27 | ITU-R BT.601/656 |
| 720 × 576 | I | 25 | 27 | ITU-R BT.601/656 |
| 640 × 480 | I | 29.97 | 24.54 | NTSC square pixel |
| 768 × 576 | I | 25 | 29.5 | PAL square pixel |
| 720 × 483 | P | 59.94 | 27 | SMPTE 293M |
| 720 × 483 | P | 59.94 | 27 | BTA T-1004 |
| 720 × 483 | P | 59.94 | 27 | ITU-R BT.1358 |
| 720 × 576 | P | 50 | 27 | ITU-R BT.1358 |
| 720 × 483 | P | 59.94 | 27 | ITU-R BT.1362 |
| 720 × 576 | P | 50 | 27 | ITU-R BT.1362 |
| 1920 × 1035 | I | 30 | 74.25 | SMPTE 240M |
| 1920 × 1035 | I | 29.97 | 74.1758 | SMPTE 240M |
| 1280 × 720 | P | 60, 50, 30, 25, 24 | 74.25 | SMPTE 296M |
| 1280 × 720 | P | 23.97, 59.94, 29.97 | 74.1758 | SMPTE 296M |
| 1920 × 1080 | I | 30, 25 | 74.25 | SMPTE 274M |
| 1920 × 1080 | I | 29.97 | 74.1758 | SMPTE 274M |
| 1920 × 1080 | P | 30, 25, 24 | 74.25 | SMPTE 274M |
| 1920 × 1080 | P | 23.98, 29.97 | 74.1758 | SMPTE 274M |
| 1920 × 1080 | P | 24 | 74.25 | ITU-R BT.709-5 |

[1] I = interlaced, P = progressive.

**Table 2. Standards Directly Supported by the WLCSP Package**

| Active Resolution | I/P[1] | Frame Rate (Hz) | Clock Input (MHz) | Standard |
|---|---|---|---|---|
| 720 × 480 | I | 29.97 | 27 | ITU-R BT.601/656 |
| 720 × 576 | I | 25 | 27 | ITU-R BT.601/656 |
| 640 × 480 | I | 29.97 | 24.54 | NTSC Square Pixel |
| 768 × 576 | I | 25 | 29.5 | PAL Square Pixel |

[1] I = interlaced, P = progressive.



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## FUNCTIONAL BLOCK DIAGRAMS

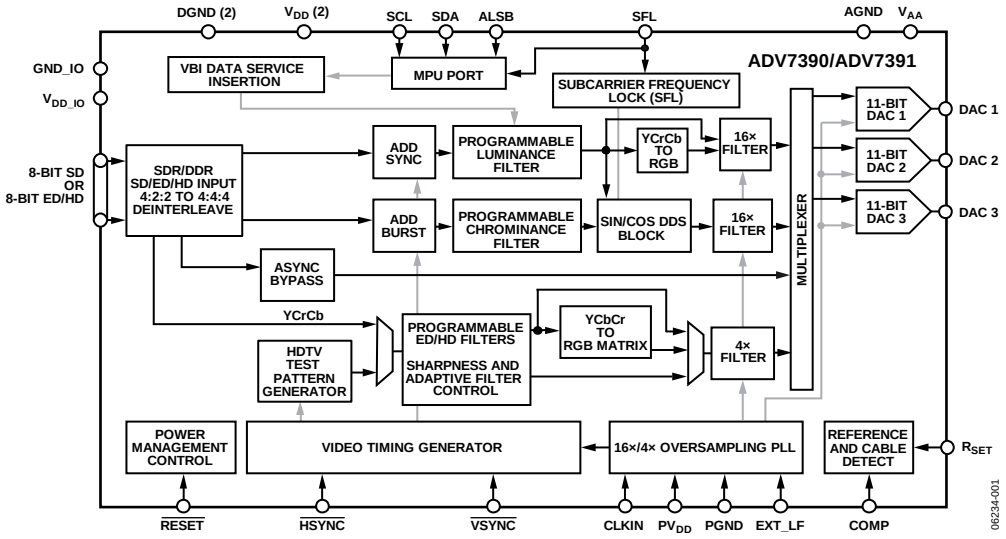


*Figure 1. ADV7390/ADV7391 (32-Lead LFCSP)*

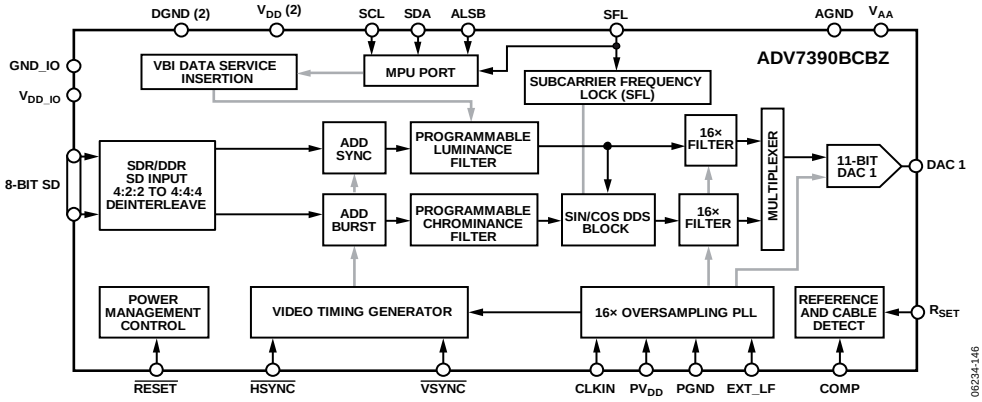


*Figure 2. ADV7390BCBZ-A (30-Ball WLCSP)*

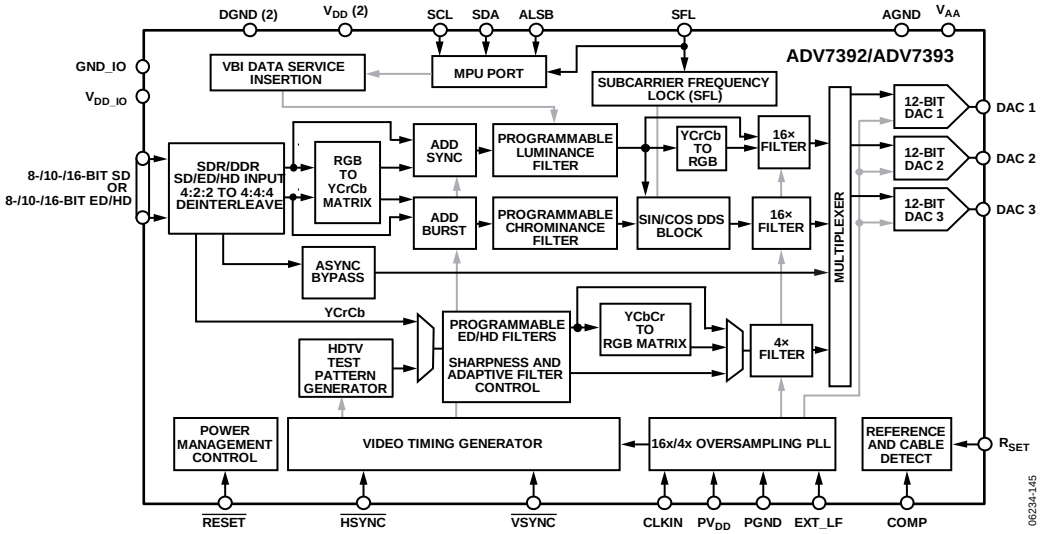


*Figure 3. ADV7392/ADV7393 (40-Lead LFCSP)*



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# SPECIFICATIONS

## POWER SUPPLY SPECIFICATIONS

All specifications $T_{MIN}$ to $T_{MAX}$ (−40°C to +85°C), unless otherwise noted.

**Table 3.**

| Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|
| SUPPLY VOLTAGES | | | | |
| $V_{DD}$ | 1.71 | 1.8 | 1.89 | V |
| $V_{DD_IO}$ | 1.71 | 3.3 | 3.63 | V |
| $PV_{DD}$ | 1.71 | 1.8 | 1.89 | V |
| $V_{AA}$ | 2.6 | 3.3 | 3.465 | V |
| POWER SUPPLY REJECTION RATIO | | 0.002 | | %/% |

## INPUT CLOCK SPECIFICATIONS

$V_{DD}$ = 1.71 V to 1.89 V, $PV_{DD}$ = 1.71 V to 1.89 V, $V_{AA}$ = 2.6 V to 3.465 V, $V_{DD_IO}$ = 1.71 V to 3.63 V. All specifications $T_{MIN}$ to $T_{MAX}$ (−40°C to +85°C), unless otherwise noted.

**Table 4.**

| Parameter | Conditions[1] | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $f_{CLKIN}$ | SD/ED | | 27 | | MHz |
| | ED (at 54 MHz) | | 54 | | MHz |
| | HD | | 74.25 | | MHz |
| CLKIN High Time, $t_9$ | | 40 | | | % of one clock cycle |
| CLKIN Low Time, $t_{10}$ | | 40 | | | % of one clock cycle |
| CLKIN Peak-to-Peak Jitter Tolerance | | | 2 | | ±ns |

[1] SD = standard definition, ED = enhanced definition (525p/625p), HD = high definition.

## ANALOG OUTPUT SPECIFICATIONS

$V_{DD}$ = 1.71 V to 1.89 V, $PV_{DD}$ = 1.71 V to 1.89 V, $V_{AA}$ = 2.6 V to 3.465 V, $V_{DD_IO}$ = 1.71 V to 3.63 V. All specifications $T_{MIN}$ to $T_{MAX}$ (−40°C to +85°C), unless otherwise noted.

**Table 5.**

| Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Full-Drive Output Current | $R_{SET}$ = 510 Ω, $R_L$ = 37.5 Ω<br>All DACs enabled | 33 | 34.6 | 37 | mA |
| | $R_{SET}$ = 510 Ω, $R_L$ = 37.5 Ω<br>DAC 1 enabled only[1] | 31.5 | 33.5 | 37 | mA |
| Low-Drive Output Current | $R_{SET}$ = 4.12 kΩ, $R_L$ = 300 Ω | | 4.3 | | mA |
| DAC-to-DAC Matching | DAC 1, DAC 2, DAC 3 | | 2.0 | | % |
| Output Compliance, $V_{OC}$ | | 0 | | 1.4 | V |
| Output Capacitance, $C_{OUT}$ | | | 10 | | pF |
| Analog Output Delay[2] | | | 6 | | ns |
| DAC Analog Output Skew | DAC 1, DAC 2, DAC 3 | | 1 | | ns |

[1] The recommended method of bringing this value back to the ideal value is by adjusting Register 0x0B to the recommended value of 0x12.
[2] Output delay measured from the 50% point of the rising edge of the input clock to the 50% point of the DAC output full-scale transition.



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## DIGITAL INPUT/OUTPUT SPECIFICATIONS—3.3 V

$V_{DD}$ = 1.71 V to 1.89 V, $PV_{DD}$ = 1.71 V to 1.89 V, $V_{AA}$ = 2.6 V to 3.465 V, $V_{DD_IO}$ = 2.97 V to 3.63 V. All specifications $T_{MIN}$ to $T_{MAX}$ (−40°C to +85°C), unless otherwise noted.

**Table 6.**

| Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Input High Voltage, $V_{IH}$ | | 2.0 | | | V |
| Input Low Voltage, $V_{IL}$ | | | | 0.8 | V |
| Input Leakage Current, $I_{IN}$ | $V_{IN} = V_{DD_IO}$ | | | ±10 | µA |
| Input Capacitance, $C_{IN}$ | | | 4 | | pF |
| Output High Voltage, $V_{OH}$ | $I_{SOURCE}$ = 400 µA | 2.4 | | | V |
| Output Low Voltage, $V_{OL}$ | $I_{SINK}$ = 3.2 mA | | | 0.4 | V |
| Three-State Leakage Current | $V_{IN}$ = 0.4 V, 2.4 V | | | ±1 | µA |
| Three-State Output Capacitance | | | 4 | | pF |

## DIGITAL INPUT/OUTPUT SPECIFICATIONS—1.8 V

When $V_{DD_IO}$ is set to 1.8 V, all the digital video inputs and control inputs, such as $I^2C$, HS, and VS, should use 1.8 V levels. $V_{DD}$ = 1.71 V to 1.89 V, $PV_{DD}$ = 1.71 V to 1.89 V, $V_{AA}$ = 2.6 V to 3.465 V, $V_{DD_IO}$ = 1.71 V to 1.89 V. All specifications $T_{MIN}$ to $T_{MAX}$ (−40°C to +85°C), unless otherwise noted.

**Table 7.**

| Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Input High Voltage, $V_{IH}$ | | 0.7 $V_{DD_IO}$ | | | V |
| Input Low Voltage, $V_{IL}$ | | | | 0.3 $V_{DD_IO}$ | V |
| Input Capacitance, $C_{IN}$ | | | 4 | | pF |
| Output High Voltage, $V_{OH}$ | $I_{SOURCE}$ = 400 µA | $V_{DD_IO}$ − 0.4 | | | V |
| Output Low Voltage, $V_{OL}$ | $I_{SINK}$ = 3.2 mA | | | 0.4 | V |
| Three-State Output Capacitance | | | 4 | | pF |

## MPU PORT TIMING SPECIFICATIONS

$V_{DD}$ = 1.71 V to 1.89 V, $PV_{DD}$ = 1.71 V to 1.89 V, $V_{AA}$ = 2.6 V to 3.465 V, $V_{DD_IO}$ = 1.71 V to 3.63 V. All specifications $T_{MIN}$ to $T_{MAX}$ (−40°C to +85°C), unless otherwise noted.

**Table 8.**

| Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| MPU PORT, $I^2C$ MODE[1] | See Figure 17 | | | | |
| SCL Frequency | | 0 | | 400 | kHz |
| SCL High Pulse Width, $t_1$ | | 0.6 | | | µs |
| SCL Low Pulse Width, $t_2$ | | 1.3 | | | µs |
| Hold Time (Start Condition), $t_3$ | | 0.6 | | | µs |
| Setup Time (Start Condition), $t_4$ | | 0.6 | | | µs |
| Data Setup Time, $t_5$ | | 100 | | | ns |
| SDA, SCL Rise Time, $t_6$ | | | | 300 | ns |
| SDA, SCL Fall Time, $t_7$ | | | | 300 | ns |
| Setup Time (Stop Condition), $t_8$ | | 0.6 | | | µs |

[1] Guaranteed by characterization.



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## DIGITAL TIMING SPECIFICATIONS—3.3 V

$V_{DD}$ = 1.71 V to 1.89 V, $PV_{DD}$ = 1.71 V to 1.89 V, $V_{AA}$ = 2.6 V to 3.465 V, $V_{DD_IO}$ = 2.97 V to 3.63 V. All specifications $T_{MIN}$ to $T_{MAX}$ (−40°C to +85°C), unless otherwise noted.

**Table 9.**

| Parameter | Conditions[1] | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| VIDEO DATA AND VIDEO CONTROL PORT[2, 3] | | | | | |
| Data Input Setup Time, $t_{11}$[4] | SD | 2.1 | | | ns |
| | ED/HD-SDR | 2.3 | | | ns |
| | ED/HD-DDR | 2.3 | | | ns |
| | ED (at 54 MHz) | 1.7 | | | ns |
| Data Input Hold Time, $t_{12}$[4] | SD | 1.0 | | | ns |
| | ED/HD-SDR | 1.1 | | | ns |
| | ED/HD-DDR | 1.1 | | | ns |
| | ED (at 54 MHz) | 1.0 | | | ns |
| Control Input Setup Time, $t_{11}$[4] | SD | 2.1 | | | ns |
| | ED/HD-SDR or ED/HD-DDR | 2.3 | | | ns |
| | ED (at 54 MHz) | 1.7 | | | ns |
| Control Input Hold Time, $t_{12}$[4] | SD | 1.0 | | | ns |
| | ED/HD-SDR or ED/HD-DDR | 1.1 | | | ns |
| | ED (at 54 MHz) | 1.0 | | | ns |
| Control Output Access Time, $t_{13}$[4] | SD | | | 12 | ns |
| | ED/HD-SDR, ED/HD-DDR, or ED (at 54 MHz) | | | 10 | ns |
| Control Output Hold Time, $t_{14}$[4] | SD | 4.0 | | | ns |
| | ED/HD-SDR, ED/HD-DDR, or ED (at 54 MHz) | 3.5 | | | ns |
| PIPELINE DELAY[5] | | | | | |
| SD[1] | | | | | |
| CVBS/Y-C Outputs (2×) | SD oversampling disabled | | 68 | | Clock cycles |
| CVBS/Y-C Outputs (8×) | SD oversampling enabled | | 79 | | Clock cycles |
| CVBS/Y-C Outputs (16×) | SD oversampling enabled | | 67 | | Clock cycles |
| Component Outputs (2×) | SD oversampling disabled | | 78 | | Clock cycles |
| Component Outputs (8×) | SD oversampling enabled | | 69 | | Clock cycles |
| Component Outputs (16×) | SD oversampling enabled | | 84 | | Clock cycles |
| ED[1] | | | | | |
| Component Outputs (1×) | ED oversampling disabled | | 41 | | Clock cycles |
| Component Outputs (4×) | ED oversampling enabled | | 49 | | Clock cycles |
| Component Outputs (8×) | ED oversampling enabled | | 46 | | Clock cycles |
| HD[1] | | | | | |
| Component Outputs (1×) | HD oversampling disabled | | 40 | | Clock cycles |
| Component Outputs (2×) | HD oversampling enabled | | 42 | | Clock cycles |
| Component Outputs (4×) | HD oversampling enabled | | 44 | | Clock cycles |
| $\overline{\text{RESET}}$ CONTROL | | | | | |
| $\overline{\text{RESET}}$ Low Time | | 100 | | | ns |

[1] SD = standard definition, ED = enhanced definition (525p/625p), HD = high definition, SDR = single data rate, DDR = dual data rate.
[2] Video data: P[15:0] for ADV7392/ADV7393 or P[7:0] for ADV7390/ADV7391.
[3] Video control: $\overline{\text{HSYNC}}$ and $\overline{\text{VSYNC}}$.
[4] Guaranteed by characterization.
[5] Guaranteed by design.



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## DIGITAL TIMING SPECIFICATIONS—1.8 V

$V_{DD}$ = 1.71 V to 1.89 V, $PV_{DD}$ = 1.71 V to 1.89 V, $V_{AA}$ = 2.6 V to 3.465 V, $V_{DD_IO}$ = 1.71 V to 1.89 V. All specifications $T_{MIN}$ to $T_{MAX}$ (−40°C to +85°C), unless otherwise noted.

**Table 10.**

| Parameter | Conditions[1] | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| VIDEO DATA AND VIDEO CONTROL PORT[2, 3] | | | | | |
| Data Input Setup Time, $t_{11}$[4] | SD | 1.4 | | | ns |
| | ED/HD-SDR | 1.9 | | | ns |
| | ED/HD-DDR | 1.9 | | | ns |
| | ED (at 54 MHz) | 1.6 | | | ns |
| Data Input Hold Time, $t_{12}$[4] | SD | 1.4 | | | ns |
| | ED/HD-SDR | 1.5 | | | ns |
| | ED/HD-DDR | 1.5 | | | ns |
| | ED (at 54 MHz) | 1.3 | | | ns |
| Control Input Setup Time, $t_{11}$[4] | SD | 1.4 | | | ns |
| | ED/HD-SDR or ED/HD-DDR | 1.2 | | | ns |
| | ED (at 54 MHz) | 1.0 | | | ns |
| Control Input Hold Time, $t_{12}$[4] | SD | 1.4 | | | ns |
| | ED/HD-SDR or ED/HD-DDR | 1.0 | | | ns |
| | ED (at 54 MHz) | 1.0 | | | ns |
| Control Output Access Time, $t_{13}$[4] | SD | | | 13 | ns |
| | ED/HD-SDR, ED/HD-DDR, or ED (at 54 MHz) | | | 12 | ns |
| Control Output Hold Time, $t_{14}$[4] | SD | 4.0 | | | ns |
| | ED/HD-SDR, ED/HD-DDR, or ED (at 54 MHz) | 5.0 | | | ns |
| PIPELINE DELAY[5] | | | | | |
| SD[1] | | | | | |
| CVBS/Y-C Outputs (2×) | SD oversampling disabled | | 68 | | Clock cycles |
| CVBS/Y-C Outputs (8×) | SD oversampling enabled | | 79 | | Clock cycles |
| CVBS/Y-C Outputs (16×) | SD oversampling enabled | | 67 | | Clock cycles |
| Component Outputs (2×) | SD oversampling disabled | | 78 | | Clock cycles |
| Component Outputs (8×) | SD oversampling enabled | | 69 | | Clock cycles |
| Component Outputs (16×) | SD oversampling enabled | | 84 | | Clock cycles |
| ED[1] | | | | | |
| Component Outputs (1×) | ED oversampling disabled | | 41 | | Clock cycles |
| Component Outputs (4×) | ED oversampling enabled | | 49 | | Clock cycles |
| Component Outputs (8×) | ED oversampling enabled | | 46 | | Clock cycles |
| HD[1] | | | | | |
| Component Outputs (1×) | HD oversampling disabled | | 40 | | Clock cycles |
| Component Outputs (2×) | HD oversampling enabled | | 42 | | Clock cycles |
| Component Outputs (4×) | HD oversampling enabled | | 44 | | Clock cycles |
| $\overline{\text{RESET}}$ CONTROL | | | | | |
| $\overline{\text{RESET}}$ Low Time | | 100 | | | ns |

[1] SD = standard definition, ED = enhanced definition (525p/625p), HD = high definition, SDR = single data rate, DDR = dual data rate.
[2] Video data: P[15:0] for ADV7392/ADV7393 or P[7:0] for ADV7390/ADV7391.
[3] Video control: $\overline{\text{HSYNC}}$ and $\overline{\text{VSYNC}}$.
[4] Guaranteed by characterization.
[5] Guaranteed by design.



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## VIDEO PERFORMANCE SPECIFICATIONS

$V_{DD}$ = 1.8 V, $PV_{DD}$ = 1.8 V, $V_{AA}$ = 3.3 V, $V_{DD_IO}$ = 3.3 V, $T_A$ = +25°C.

**Table 11.**

| Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| STATIC PERFORMANCE | | | | | |
| Resolution | | | 10 | | Bits |
| Integral Nonlinearity (INL)[1] | $R_{SET}$ = 510 Ω, $R_L$ = 37.5 Ω | | 0.5 | | LSBs |
| Differential Nonlinearity (DNL)[1, 2] | $R_{SET}$ = 510 Ω, $R_L$ = 37.5 Ω | | 0.5 | | LSBs |
| STANDARD DEFINTION (SD) MODE | | | | | |
| Luminance Nonlinearity | | | 0.5 | | ±% |
| Differential Gain | NTSC | | 0.5 | | % |
| Differential Phase | NTSC | | 0.6 | | Degrees |
| Signal-to-Noise Ratio (SNR)[3] | Luma ramp | | 58 | | dB |
| | Flat field full bandwidth | | 75 | | dB |
| ENHANCED DEFINITION (ED) MODE | | | | | |
| Luma Bandwidth | | | 12.5 | | MHz |
| Chroma Bandwidth | | | 5.8 | | MHz |
| HIGH DEFINITION (HD) MODE | | | | | |
| Luma Bandwidth | | | 30.0 | | MHz |
| Chroma Bandwidth | | | 13.75 | | MHz |

[1] Measured on DAC 1, DAC 2, and DAC 3.
[2] Differential nonlinearity (DNL) measures the deviation of the actual DAC output voltage step from the ideal. For +ve DNL, the actual step value lies above the ideal step value. For −ve DNL, the actual step value lies below the ideal step value.
[3] Measured on the ADV7392/ADV7393 operating in 10-bit input mode.

## POWER SPECIFICATIONS

$V_{DD}$ = 1.8 V, $PV_{DD}$ = 1.8 V, $V_{AA}$ = 3.3 V, $V_{DD_IO}$ = 3.3 V, $T_A$ = +25°C.

**Table 12.**

| Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| NORMAL POWER MODE[1, 2] | | | | | |
| $I_{DD}$[3] | SD (16× oversampling enabled), CVBS (only one DAC turned on) | | 33 | | mA |
| | SD (16× oversampling enabled), YPrPb (three DACs turned on) | | 68 | | mA |
| | ED (8× oversampling enabled)[4] | | 59 | | mA |
| | HD (4× oversampling enabled)[4] | | 81 | 101 | mA |
| $I_{DD_IO}$ | | | 1 | 10 | mA |
| $I_{AA}$[5] | One DAC enabled | | 50 | | mA |
| | All DACs enabled | | 122 | 151 | mA |
| $I_{PLL}$ | | | 4 | 10 | mA |
| SLEEP MODE | | | | | |
| $I_{DD}$ | | | 5 | | µA |
| $I_{AA}$ | | | 0.3 | | µA |
| $I_{DD_IO}$ | | | 0.2 | | µA |
| $I_{PLL}$ | | | 0.1 | | µA |

[1] $R_{SET}$ = 510 Ω (all DACs operating in full-drive mode).
[2] 75% color bar test pattern applied to pixel data pins.
[3] $I_{DD}$ is the continuous current required to drive the digital core.
[4] Applicable to both single data rate (SDR) and dual data rate (DDR) input modes.
[5] $I_{AA}$ is the total current required to supply all DACs.



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## TIMING DIAGRAMS

The following abbreviations are used in Figure 4 to Figure 11:

- $t_9$ = clock high time
- $t_{10}$ = clock low time
- $t_{11}$ = data setup time
- $t_{12}$ = data hold time
- $t_{13}$ = control output access time
- $t_{14}$ = control output hold time

In addition, see Table 35 for the ADV7390/ADV7391 pixel port input configuration and Table 36 for the ADV7392/ADV7393 pixel port input configuration.

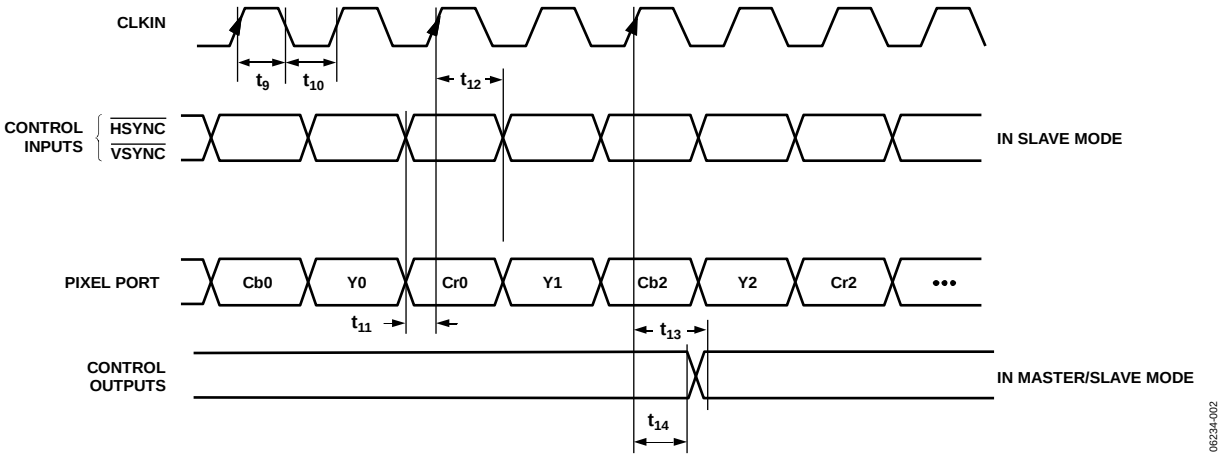


*Figure 4. SD Input, 8-/10-Bit 4:2:2 YCrCb, Input Mode 000*

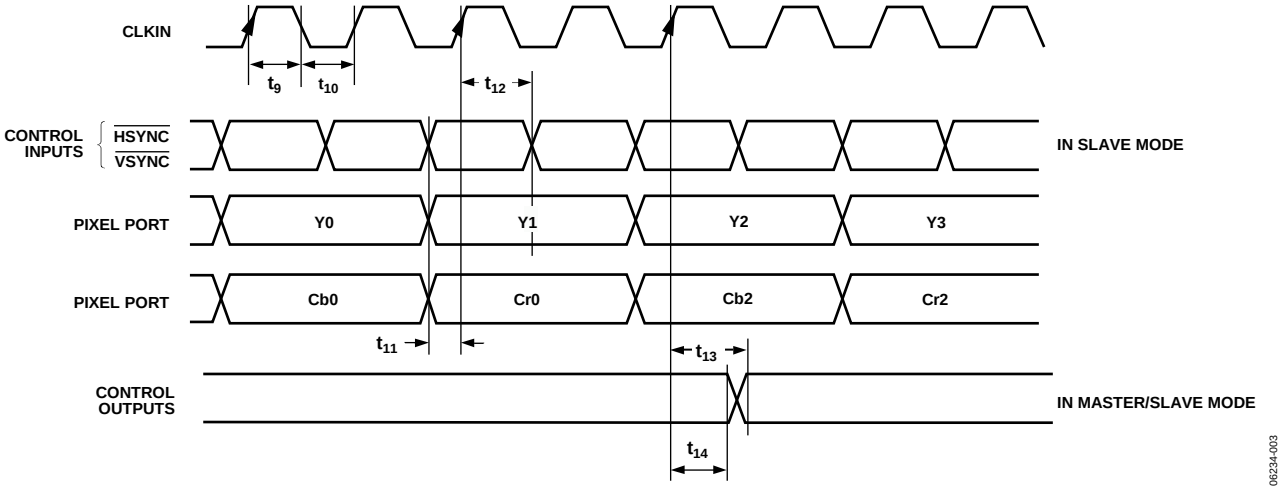


*Figure 5. SD Input, 16-Bit 4:2:2 YCrCb, Input Mode 000*



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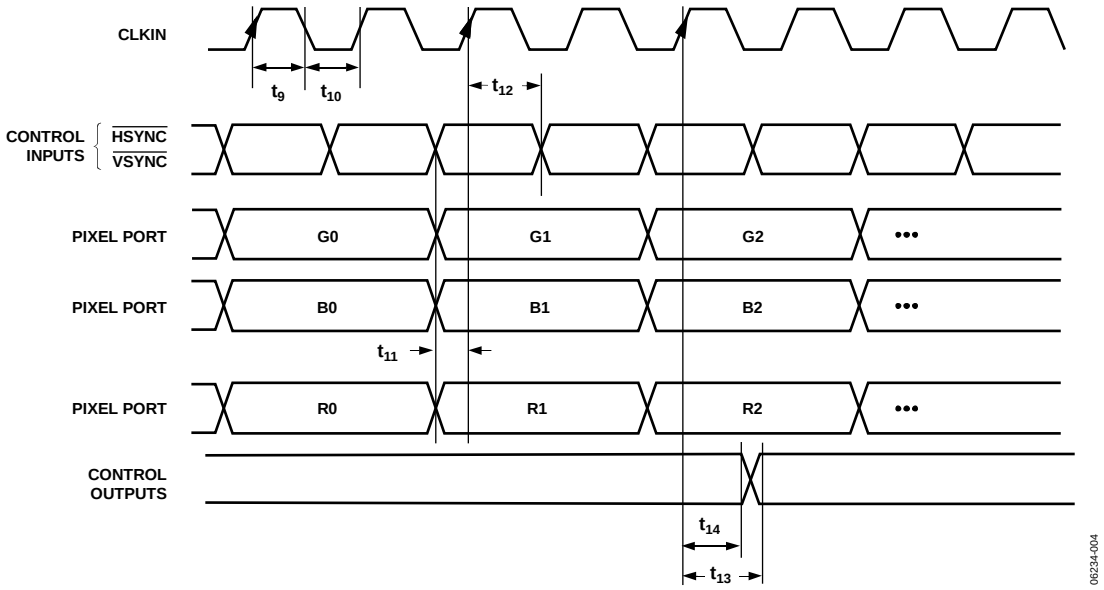


*Figure 6. SD Input, 16-Bit 4:4:4 RGB, Input Mode 000*

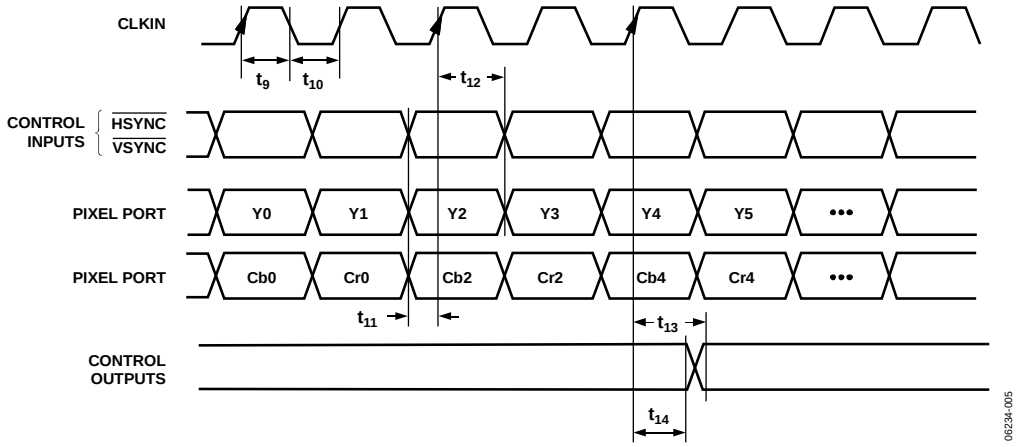


*Figure 7. ED/HD-SDR Input, 16-Bit 4:2:2 YCrCb, Input Mode 001*

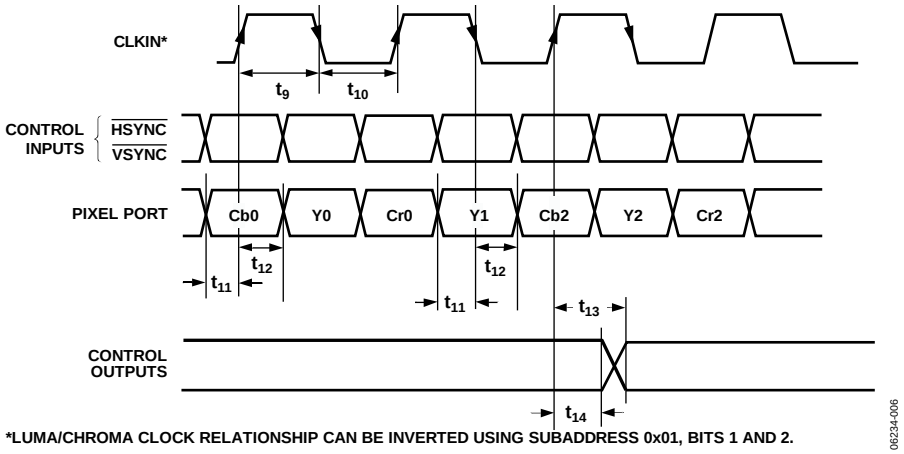


*Figure 8. ED/HD-DDR Input, 8-/10-Bit 4:2:2 YCrCb (HSYNC/VSYNC), Input Mode 010*



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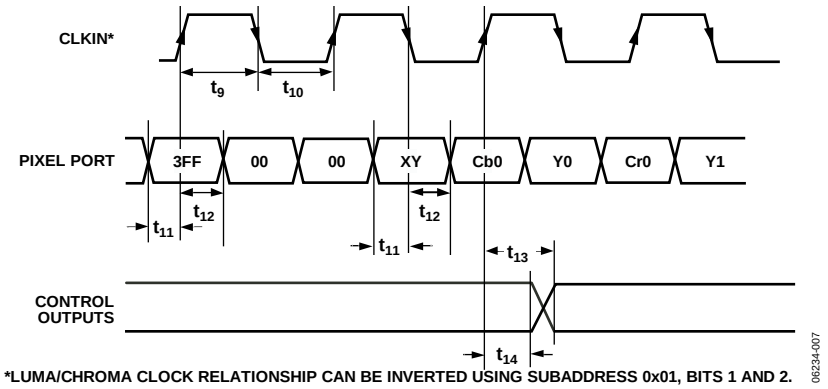


*Figure 9. ED/HD-DDR Input, 8-/10-Bit 4:2:2 YCrCb (EAV/SAV), Input Mode 010*

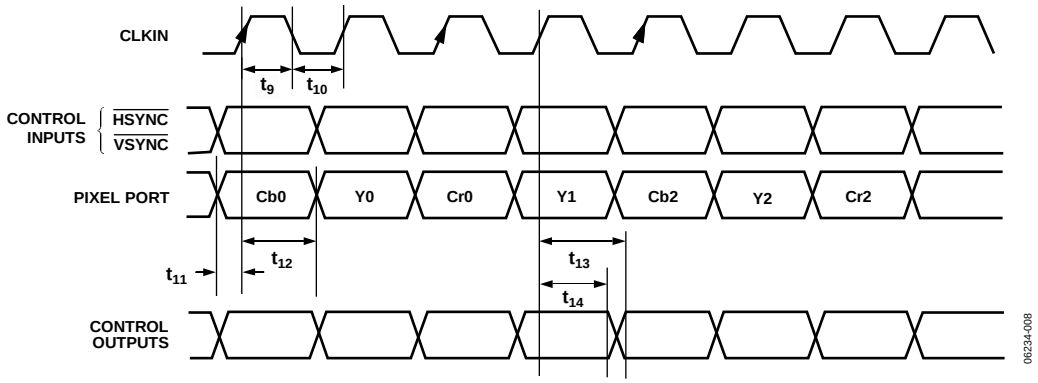


*Figure 10. ED (at 54 MHz) Input, 8-/10-Bit 4:2:2 YCrCb (HSYNC/VSYNC), Input Mode 111*

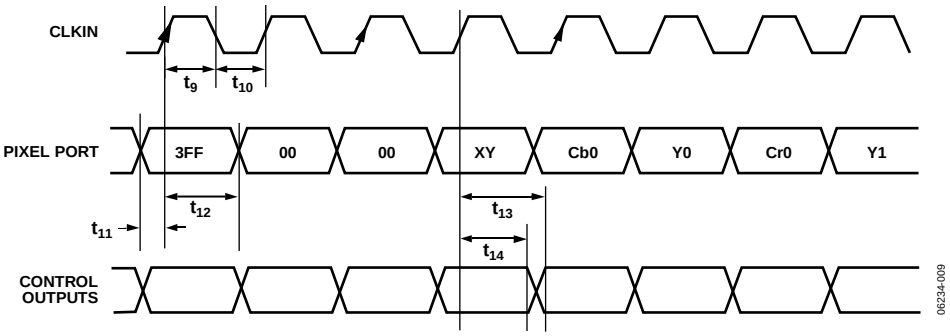


*Figure 11. ED (at 54 MHz) Input, 8-/10-Bit 4:2:2 YCrCb (EAV/SAV), Input Mode 111*



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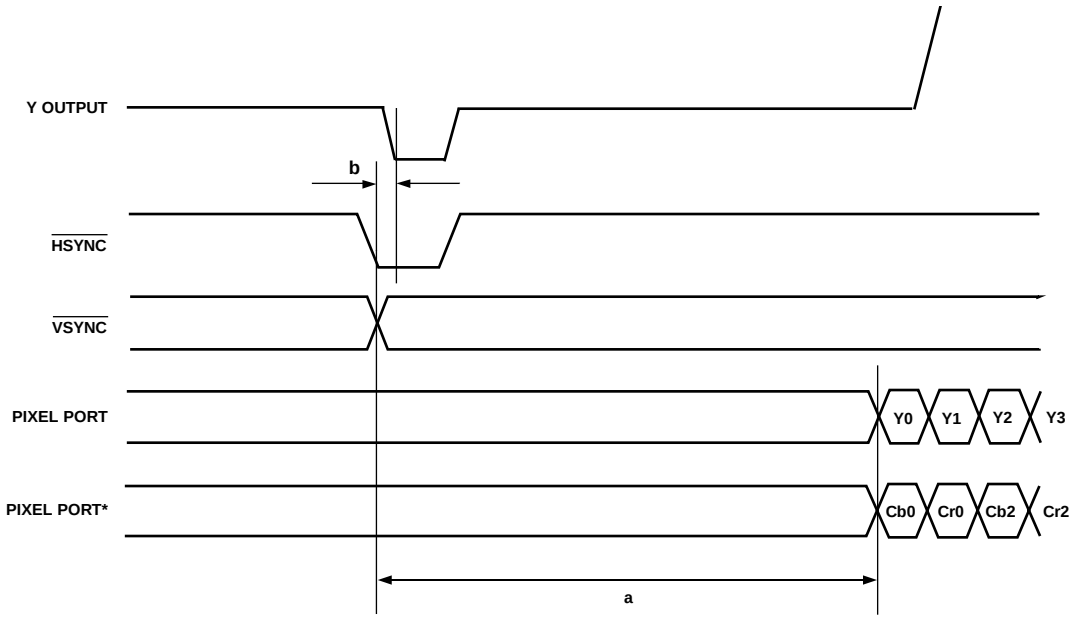


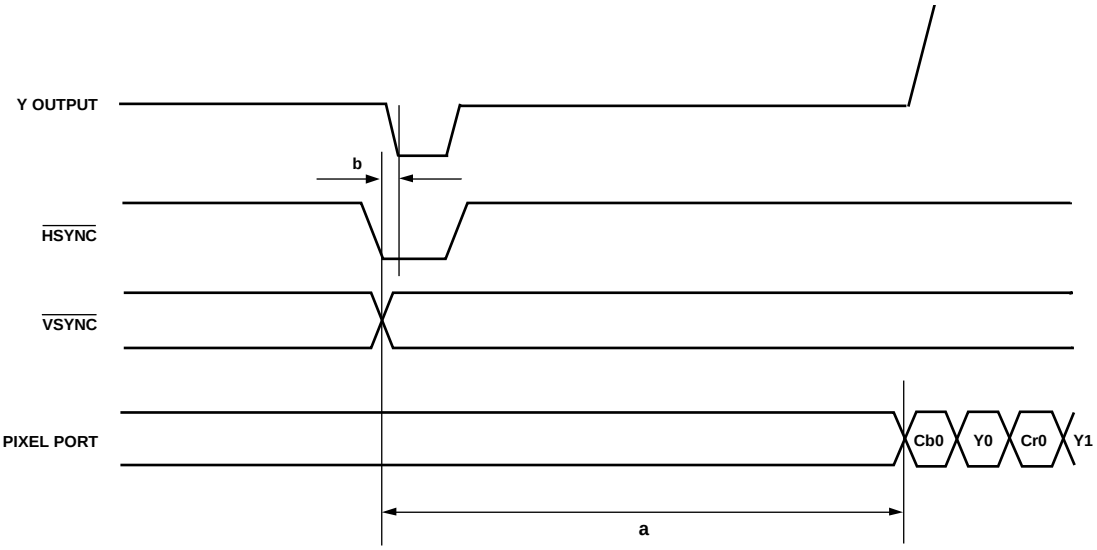

a = AS PER RELEVANT STANDARD.

b = PIPELINE DELAY. PLEASE REFER TO RELEVANT PIPELINE DELAY. THIS CAN BE FOUND IN THE DIGITAL TIMING SPECIFICATION SECTION OF THE DATA SHEET.

A FALLING EDGE OF $\overline{\text{HSYNC}}$ INTO THE ENCODER GENERATES A SYNC FALLING EDGE ON THE OUTPUT AFTER A TIME EQUAL TO THE PIPELINE DELAY.

06234-010

*Figure 12. ED-SDR, 16-Bit 4:2:2 YCrCb ($\overline{\text{HSYNC}}$/$\overline{\text{VSYNC}}$) Input Timing Diagram*




a(MIN) = 244 CLOCK CYCLES FOR 525p.
a(MIN) = 264 CLOCK CYCLES FOR 625p.

b = PIPELINE DELAY. PLEASE REFER TO RELEVANT PIPELINE DELAY. THIS CAN BE FOUND IN THE DIGITAL TIMING SPECIFICATION SECTION OF THE DATA SHEET.

A FALLING EDGE OF $\overline{\text{HSYNC}}$ INTO THE ENCODER GENERATES A SYNC FALLING EDGE ON THE OUTPUT AFTER A TIME EQUAL TO THE PIPELINE DELAY.

06234-011

*Figure 13. ED-DDR, 8-/10-Bit 4:2:2 YCrCb ($\overline{\text{HSYNC}}$/$\overline{\text{VSYNC}}$) Input Timing Diagram*



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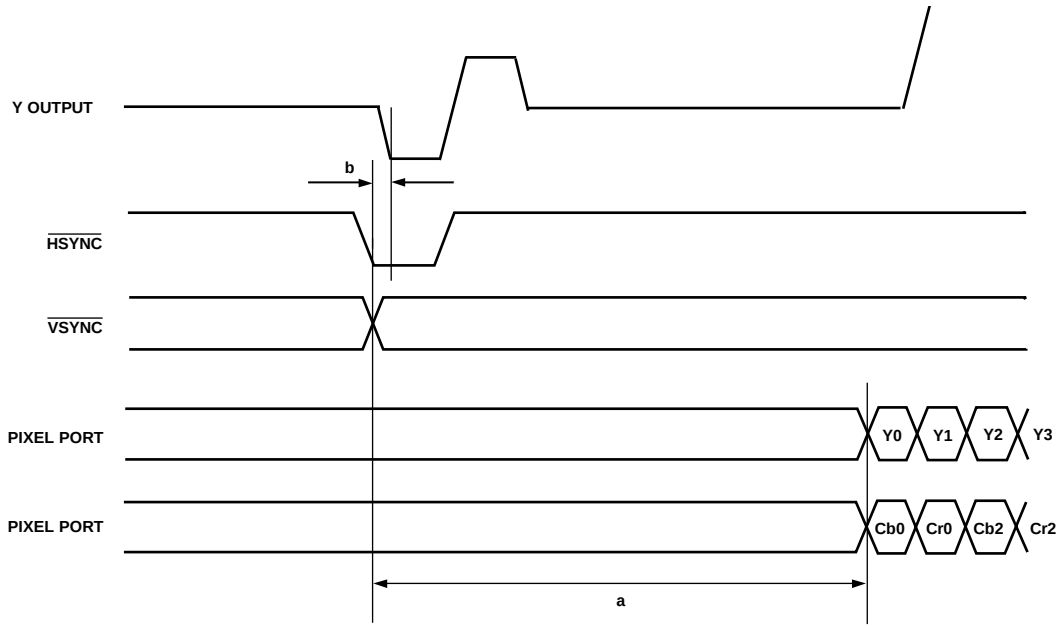


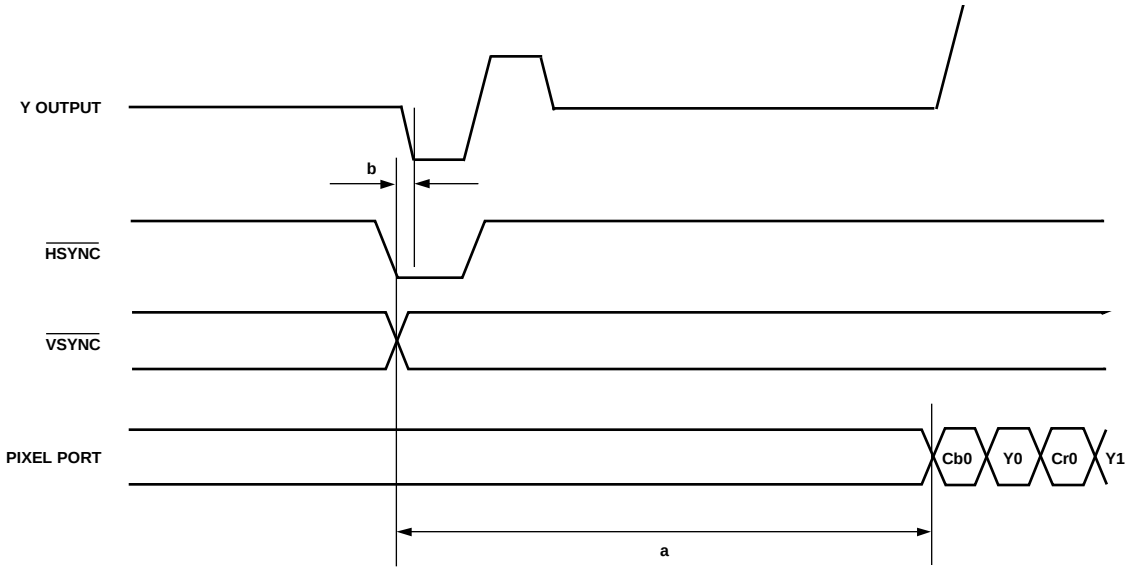

a = AS PER RELEVANT STANDARD.

b = PIPELINE DELAY. PLEASE REFER TO RELEVANT PIPELINE DELAY. THIS CAN BE FOUND IN THE DIGITAL TIMING SPECIFICATION SECTION OF THE DATA SHEET.

A FALLING EDGE OF $\overline{\text{HSYNC}}$ INTO THE ENCODER GENERATES A FALLING EDGE OF TRI-LEVEL SYNC ON THE OUTPUT AFTER A TIME EQUAL TO THE PIPELINE DELAY.

06234-012

*Figure 14. HD-SDR, 16-Bit 4:2:2 YCrCb ($\overline{\text{HSYNC}}$/$\overline{\text{VSYNC}}$) Input Timing Diagram*




a = AS PER RELEVANT STANDARD.

b = PIPELINE DELAY. PLEASE REFER TO RELEVANT PIPELINE DELAY. THIS CAN BE FOUND IN THE DIGITAL TIMING SPECIFICATION SECTION OF THE DATA SHEET.

A FALLING EDGE OF $\overline{\text{HSYNC}}$ INTO THE ENCODER GENERATES A FALLING EDGE OF TRI-LEVEL SYNC ON THE OUTPUT AFTER A TIME EQUAL TO THE PIPELINE DELAY.

06234-013

*Figure 15. HD-DDR, 8-/10-Bit 4:2:2 YCrCb ($\overline{\text{HSYNC}}$/$\overline{\text{VSYNC}}$) Input Timing Diagram*



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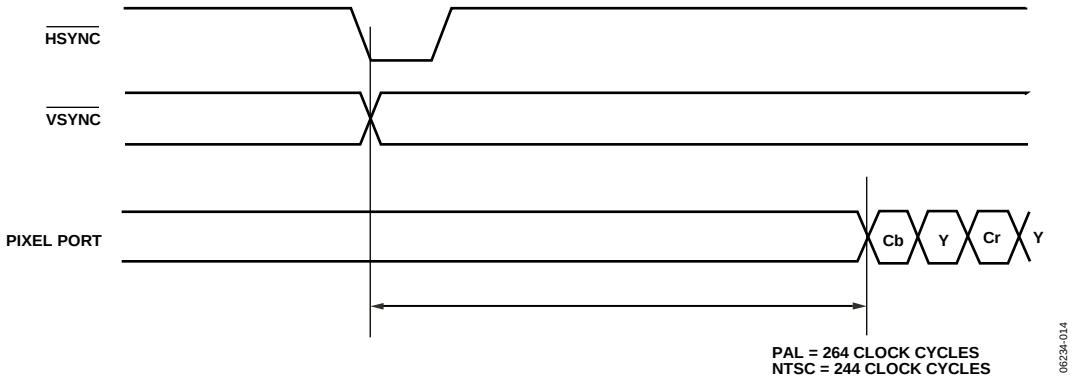


*Figure 16. SD Input Timing Diagram (Timing Mode 1)*

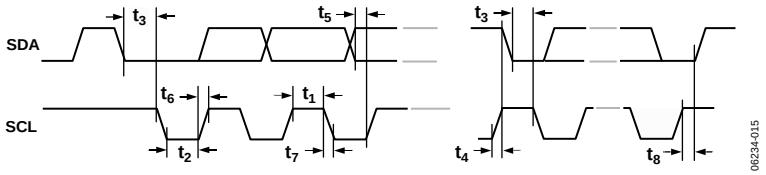


*Figure 17. MPU Port Timing Diagram ($I^2C$ Mode)*



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# ABSOLUTE MAXIMUM RATINGS

**Table 13.**

| Parameter[1] | Rating |
|---|---|
| $V_{AA}$ to AGND | −0.3 V to +3.9 V |
| $V_{DD}$ to DGND | −0.3 V to +2.3 V |
| $PV_{DD}$ to PGND | −0.3 V to +2.3 V |
| $V_{DD_IO}$ to GND_IO | −0.3 V to +3.9 V |
| AGND to DGND | −0.3 V to +0.3 V |
| AGND to PGND | −0.3 V to +0.3 V |
| AGND to GND_IO | −0.3 V to +0.3 V |
| DGND to PGND | −0.3 V to +0.3 V |
| DGND to GND_IO | −0.3 V to +0.3 V |
| PGND to GND_IO | −0.3 V to +0.3 V |
| Digital Input Voltage to GND_IO | −0.3 V to $V_{DD_IO}$ + 0.3 V |
| Analog Outputs to AGND | −0.3 V to $V_{AA}$ |
| Max CLKIN Input Frequency | 80 MHz |
| Storage Temperature Range ($t_S$) | −60°C to +150°C |
| Junction Temperature ($t_J$) | 150°C |
| Lead Temperature (Soldering, 10 sec) | 260°C |

[1] Analog output short circuit to any power supply or common can be of an indefinite duration.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

## THERMAL RESISTANCE

$\theta_{JA}$ is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

**Table 14. Thermal Resistance[1]**

| Package Type | $\theta_{JA}$[2] | $\theta_{JC\text{-}TOP}$[3] | $\theta_{JC\text{-}BOTTOM}$[4] | Unit |
|---|---|---|---|---|
| 30-Ball WLCSP | 35 | 1 | N/A | °C/W |
| 32-Lead LFCSP | 27 | 32 | 1.2 | °C/W |
| 40-Lead LFCSP | 26 | 32 | 1 | °C/W |

[1] Values are based on a JEDEC 4-layer test board.
[2] With the exposed metal paddle on the underside of the LFCSP soldered to the PCB ground.
[3] This is the thermal resistance of the junction to the top of the package.
[4] This is the thermal resistance of the junction to the bottom of the package.

The ADV7390/ADV7391/ADV7392/ADV7393 are RoHS-compliant, Pb-free products. The lead finish is 100% pure Sn electroplate. The device is suitable for Pb-free applications up to 255°C (±5°C) IR reflow (JEDEC STD-20).

The ADV7390/ADV7391/ADV7392/ADV7393 are backward compatible with conventional SnPb soldering processes. The electroplated Sn coating can be soldered with SnPb solder pastes at conventional reflow temperatures of 220°C to 235°C.

## ESD CAUTION

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.



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# PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

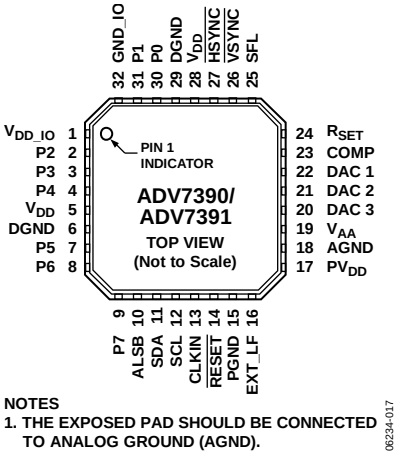


Figure 18. ADV7390/ADV7391 Pin Configuration

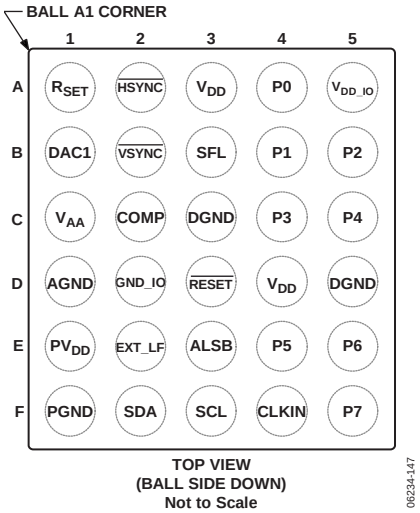


Figure 20. ADV7390BCBZ-A Pin Configuration

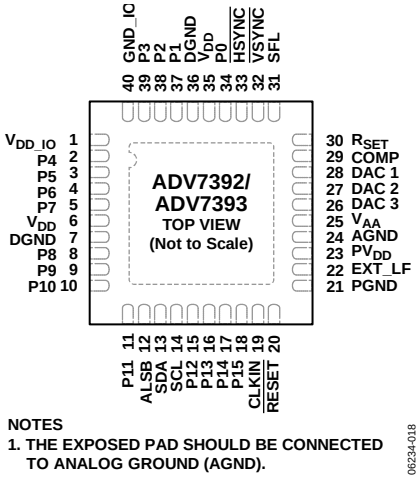


Figure 19. ADV7392/ADV7393 Pin Configuration

**Table 15. Pin Function Descriptions**

| Pin No.[1] | | | | | |
|---|---|---|---|---|---|
| ADV7390/ ADV7391 | ADV7392/ ADV7393 | ADV7390 WLCSP | Mnemonic | Input/ Output | Description |
| 9 to 7, 4 to 2, 31, 30 | N/A | F5, E5, E4, C5, C4, B5, B4, A4 | P7 to P0 | I | 8-Bit Pixel Port (P7 to P0). P0 is the LSB. See Table 35 for input modes (ADV7390/ADV7391). |
| N/A | 18 to 15, 11 to 8, 5 to 2, 39 to 37, 34 | N/A | P15 to P0 | I | 16-Bit Pixel Port (P15 to P0). P0 is the LSB. See Table 36 for input modes (ADV7392/ADV7393). |
| 13 | 19 | F4 | CLKIN | I | Pixel Clock Input for HD (74.25 MHz), ED[2] (27 MHz or 54 MHz), or SD (27 MHz). |
| 27 | 33 | A2 | $\overline{\text{HSYNC}}$ | I/O | Horizontal Synchronization Signal. This pin can also be configured to output an SD, ED, or HD horizontal synchronization signal. See the External Horizontal and Vertical Synchronization Control section. |
| 26 | 32 | B2 | $\overline{\text{VSYNC}}$ | I/O | Vertical Synchronization Signal. This pin can also be configured to output an SD, ED, or HD vertical synchronization signal. See the External Horizontal and Vertical Synchronization Control section. |
| 25 | 31 | B3 | SFL | I/O | Subcarrier Frequency Lock (SFL) Input. |



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| Pin No.[1] | | | Mnemonic | Input/ Output | Description |
|---|---|---|---|---|---|
| ADV7390/ ADV7391 | ADV7392/ ADV7393 | ADV7390 WLCSP | | | |
| 24 | 30 | A1 | $R_{SET}$ | I | Controls the amplitudes of the DAC 1, DAC 2, and DAC 3 outputs. For full-drive operation (for example, into a 37.5 Ω load), a 510 Ω resistor must be connected from $R_{SET}$ to AGND. For low-drive operation (for example, into a 300 Ω load), a 4.12 kΩ resistor must be connected from $R_{SET}$ to AGND. |
| 23 | 29 | C2 | COMP | O | Compensation Pin. Connect a 2.2 nF capacitor from COMP to $V_{AA}$. |
| N/A | N/A | B1 | DAC 1 | O | DAC Output. Full-drive and low-drive capable DAC |
| 22, 21, 20 | 28, 27, 26 | N/A | DAC 1, DAC 2, DAC 3 | O | DAC Outputs. Full-drive and low-drive capable DACs. |
| 12 | 14 | F3 | SCL | I | $I^2C$ Clock Input. |
| 11 | 13 | F2 | SDA | I/O | $I^2C$ Data Input/Output. |
| 10 | 12 | E3 | ALSB | I | ALSB sets up the LSB[3] of the MPU $I^2C$ address. |
| 14 | 20 | D3 | $\overline{\text{RESET}}$ | I | Resets the on-chip timing generator and sets the ADV7390/ADV7391/ADV7392/ADV7393 into its default mode. |
| 19 | 25 | C1 | $V_{AA}$ | P | Analog Power Supply (2.7 V or 3.3 V). |
| 5, 28 | 6, 35 | A3, D4 | $V_{DD}$ | P | Digital Power Supply (1.8 V). For dual-supply configurations, $V_{DD}$ can be connected to other 1.8 V supplies through a ferrite bead or suitable filtering. |
| 1 | 1 | A5 | $V_{DD_IO}$ | P | Input/Output Digital Power Supply (1.8 V or 3.3 V). |
| 17 | 23 | E1 | $PV_{DD}$ | P | PLL Power Supply (1.8 V). For dual-supply configurations, $PV_{DD}$ can be connected to other 1.8 V supplies through a ferrite bead or suitable filtering. |
| 16 | 22 | E2 | EXT_LF | I | External Loop Filter for the Internal PLL. |
| 15 | 21 | F1 | PGND | G | PLL Ground Pin. |
| 18 | 24 | D1 | AGND | G | Analog Ground Pin. |
| 6, 29 | 7, 36 | C3, D5 | DGND | G | Digital Ground Pin. |
| 32 | 40 | D2 | GND_IO | G | Input/Output Supply Ground Pin. |
| | | | EPAD | G | Exposed Pad. Connect to analog ground (AGND). |

[1] N/A means not applicable.
[2] ED = enhanced definition = 525p and 625p.
[3] LSB = least significant bit. In the ADV7390/ADV7392, setting the LSB to 0 sets the $I^2C$ address to 0xD4. Setting it to 1 sets the $I^2C$ address to 0xD6. In the ADV7391/ADV7393, setting the LSB to 0 sets the $I^2C$ address to 0x54. Setting it to 1 sets the $I^2C$ address to 0x56.



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# TYPICAL PERFORMANCE CHARACTERISTICS

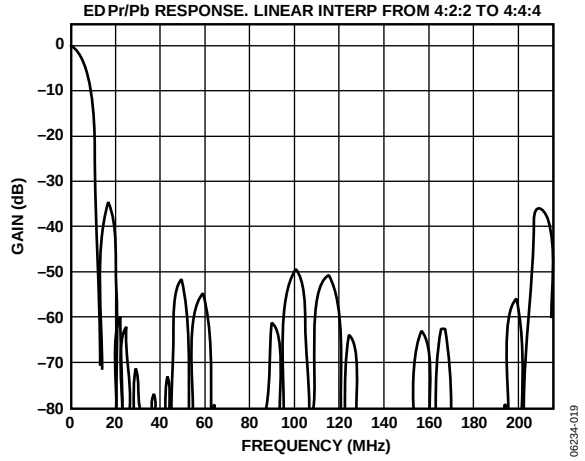


Figure 21. ED 8× Oversampling, PrPb Filter (Linear) Response

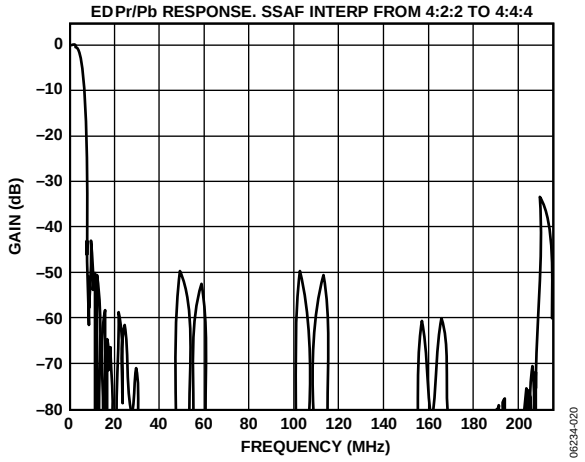


Figure 22. ED 8× Oversampling, PrPb Filter (SSAF™) Response

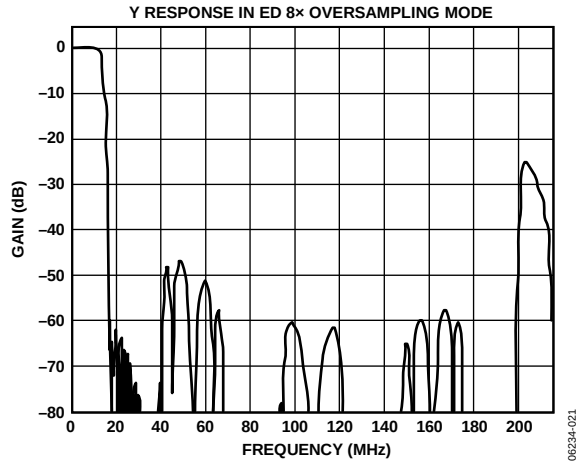


Figure 23. ED 8× Oversampling, Y Filter Response

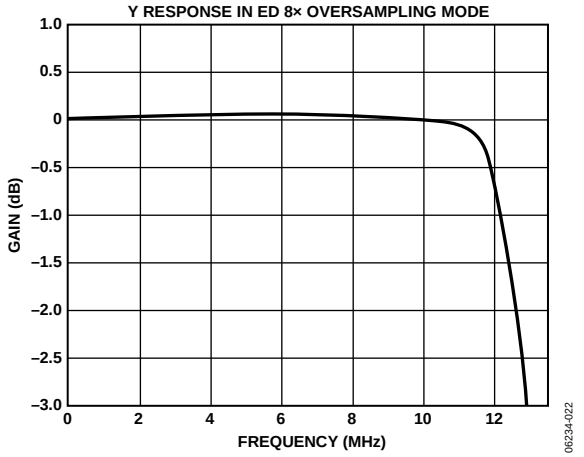


Figure 24. ED 8× Oversampling, Y Filter Response (Focus on Pass Band)

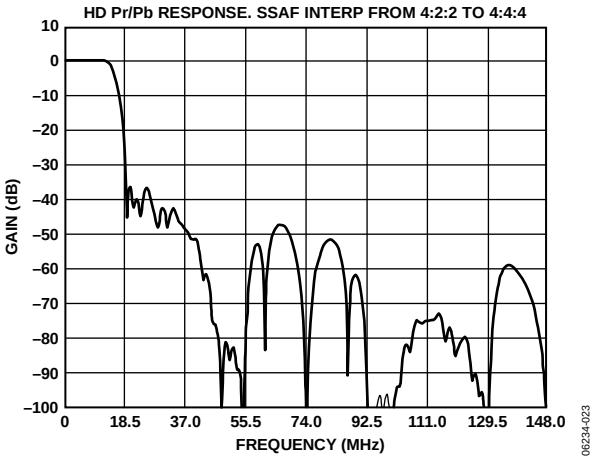


Figure 25. HD 4× Oversampling, PrPb (SSAF) Filter Response (4:2:2 Input)

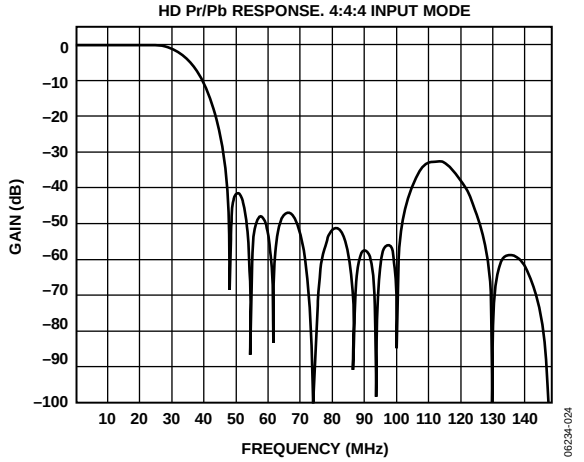


Figure 26. HD 4× Oversampling, PrPb (SSAF) Filter Response (4:4:4 Input)



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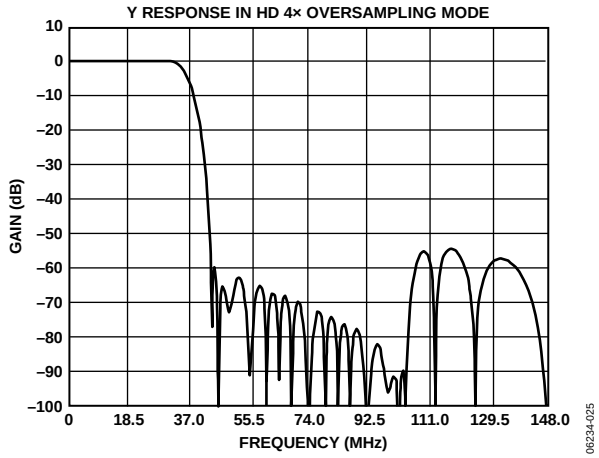


Figure 27. HD 4× Oversampling, Y Filter Response

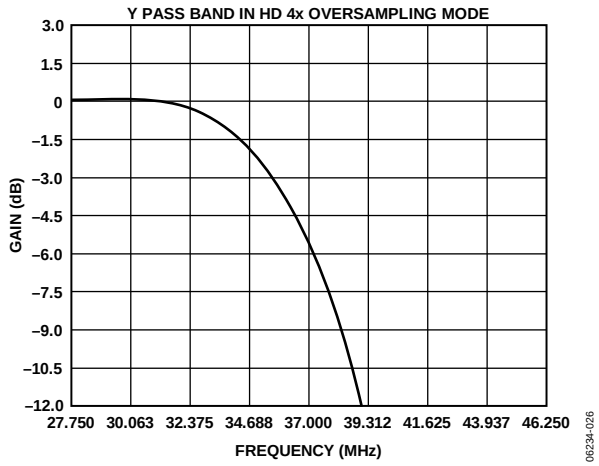


Figure 28. HD 4× Oversampling, Y Filter Response (Focus on Pass Band)

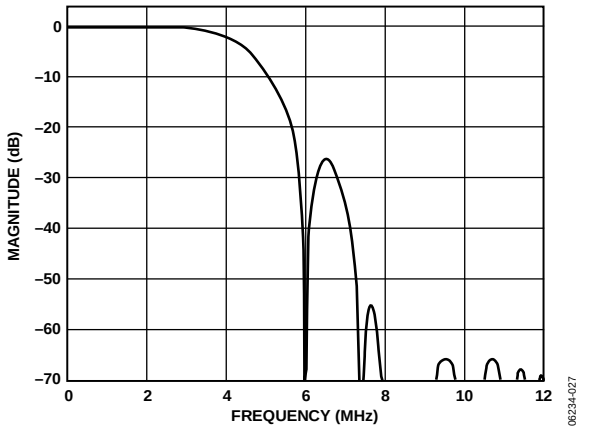


Figure 29. SD NTSC, Luma Low-Pass Filter Response

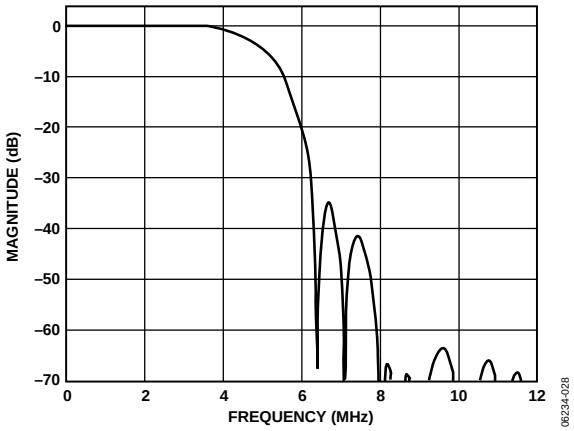


Figure 30. SD PAL, Luma Low-Pass Filter Response

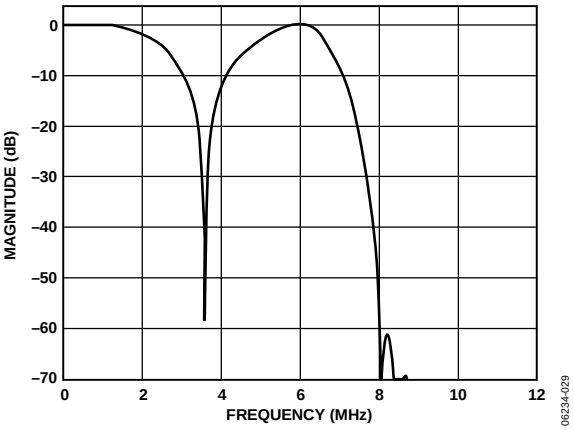


Figure 31. SD NTSC, Luma Notch Filter Response

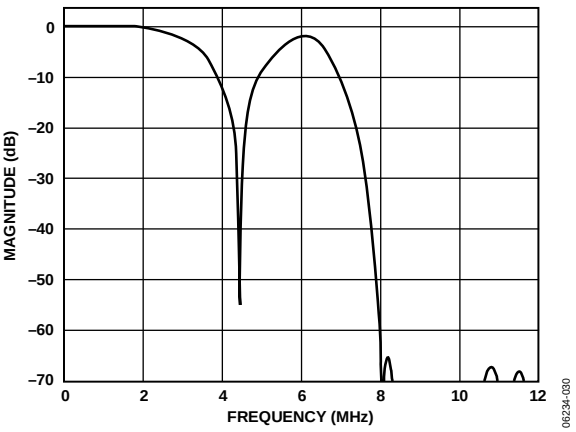


Figure 32. SD PAL, Luma Notch Filter Response



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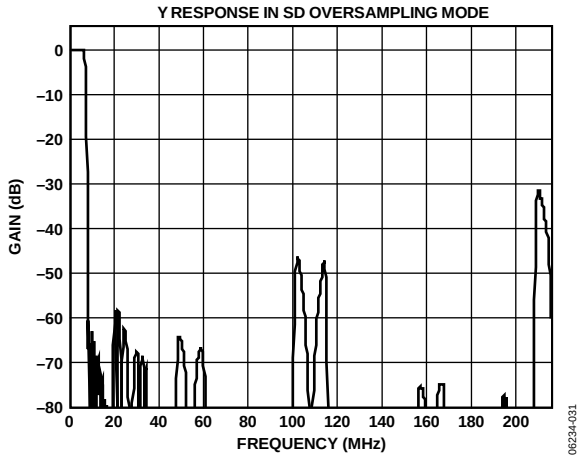


Figure 33. SD 16× Oversampling, Y Filter Response

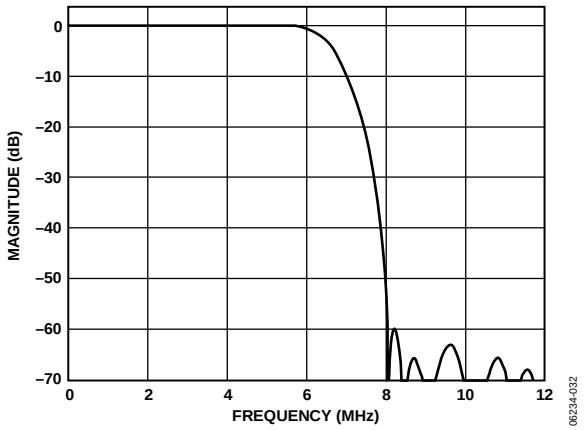


Figure 34. SD Luma SSAF Filter Response up to 12 MHz

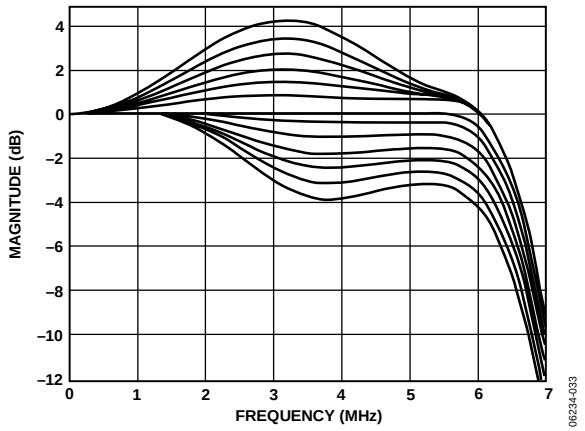


Figure 35. SD Luma SSAF Filter, Programmable Responses

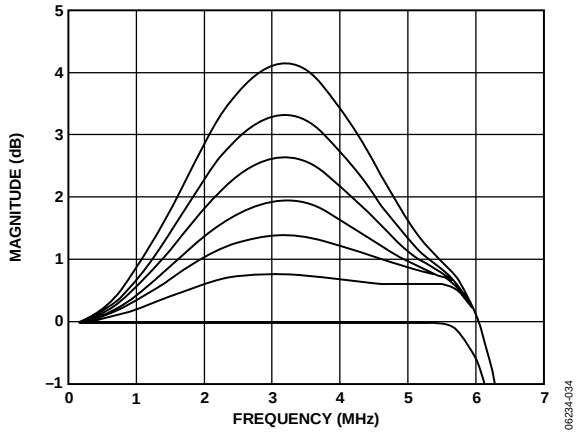


Figure 36. SD Luma SSAF Filter, Programmable Gain

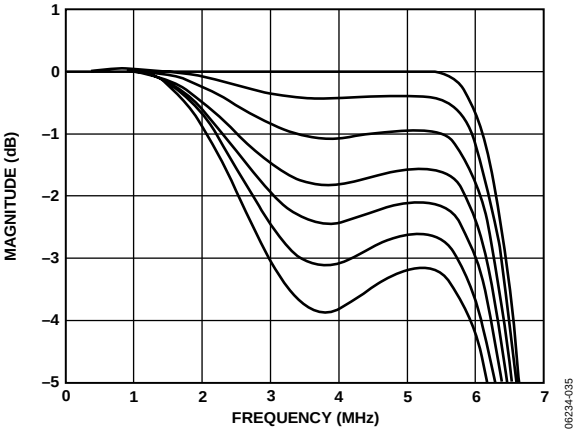


Figure 37. SD Luma SSAF Filter, Programmable Attenuation

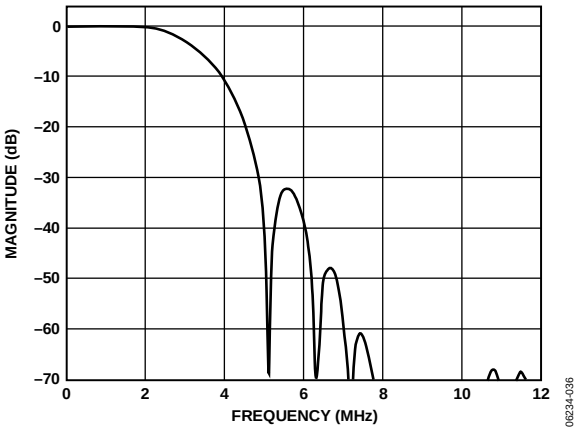


Figure 38. SD Luma CIF Low-Pass Filter Response



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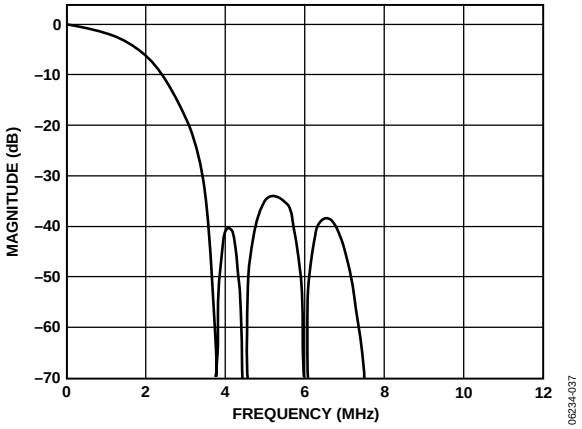


Figure 39. SD Luma QCIF Low-Pass Filter Response

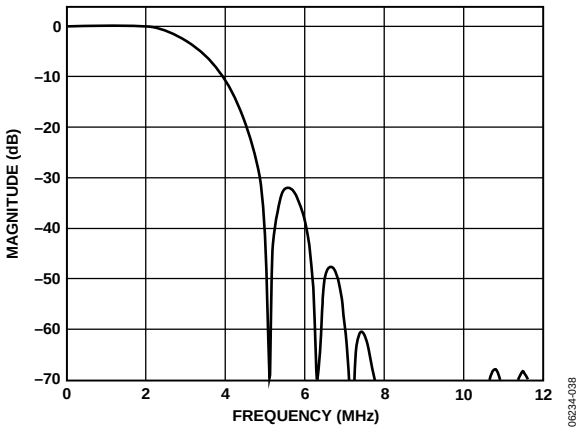


Figure 40. SD Chroma 3.0 MHz Low-Pass Filter Response

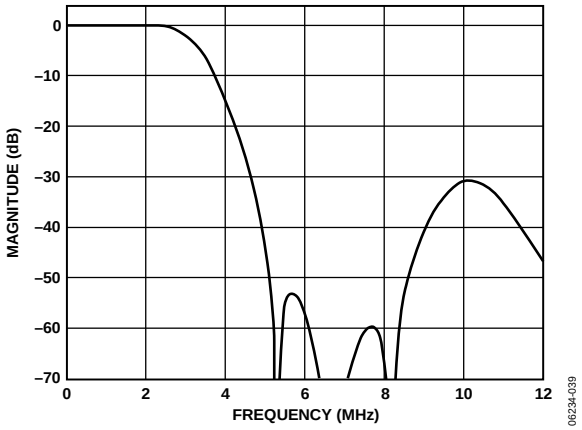


Figure 41. SD Chroma 2.0 MHz Low-Pass Filter Response

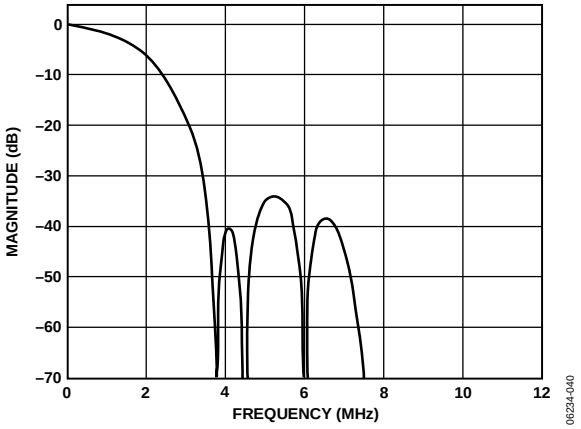


Figure 42. SD Chroma 1.3 MHz Low-Pass Filter Response

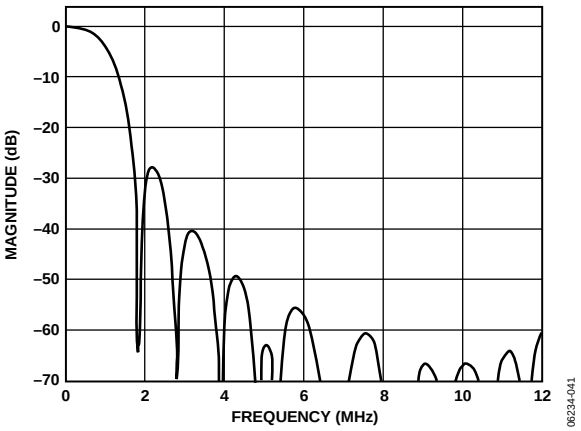


Figure 43. SD Chroma 1.0 MHz Low-Pass Filter Response

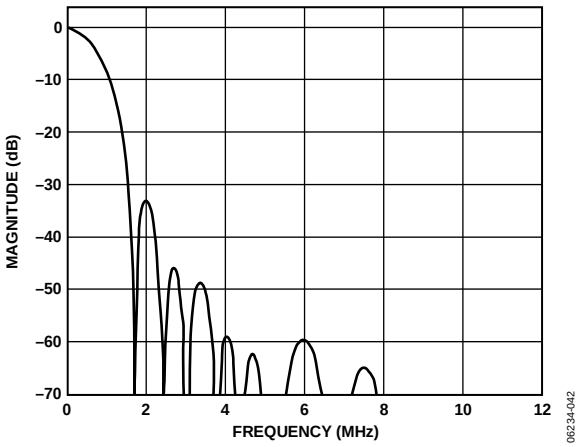


Figure 44. SD Chroma 0.65 MHz Low-Pass Filter Response



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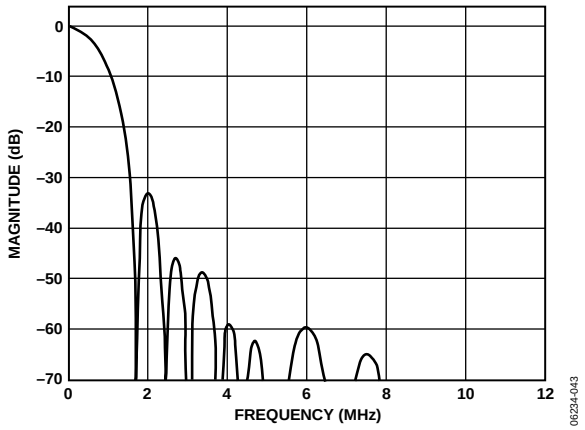


Figure 45. SD Chroma CIF Low-Pass Filter Response

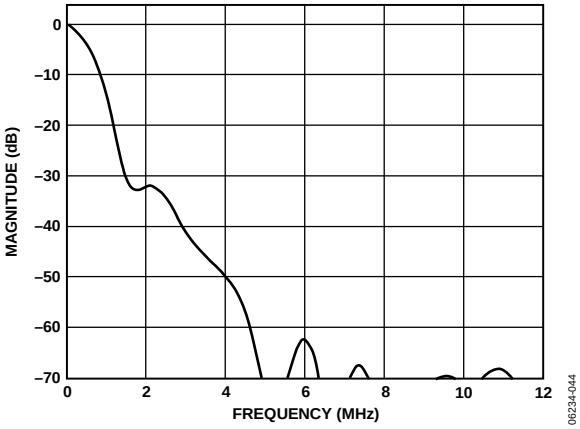


Figure 46. SD Chroma QCIF Low-Pass Filter Response



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# MPU PORT DESCRIPTION

Devices such as a microprocessor can communicate with the ADV7390/ADV7391/ADV7392/ADV7393 through a 2-wire serial (I²C-compatible) bus. After power-up or reset, the MPU port is configured for I²C operation.

## I²C OPERATION

The ADV7390/ADV7391/ADV7392/ADV7393 support a 2-wire serial (I²C-compatible) microprocessor bus driving multiple peripherals. This port operates in an open-drain configuration. Two wires, serial data (SDA) and serial clock (SCL), carry information between any device connected to the bus and the ADV7390/ADV7391/ADV7392/ADV7393. The slave address depends on the device (ADV7390, ADV7391, ADV7392, or ADV7393), the operation (read or write), and the state of the ALSB pin (0 or 1). See Table 16, Figure 47, and Figure 48. The LSB sets either a read or a write operation. Logic 1 corresponds to a read operation, and Logic 0 corresponds to a write operation. A1 is controlled by setting the ALSB pin of the ADV7390/ADV7391/ADV7392/ADV7393 to Logic 0 or Logic 1.

**Table 16. ADV7390/ADV7391/ADV7392/ADV7393 I²C Slave Addresses**

| Device | ALSB | Operation | Slave Address |
|---|---|---|---|
| ADV7390 and ADV7392 | 0 | Write | 0xD4 |
| | 0 | Read | 0xD5 |
| | 1 | Write | 0xD6 |
| | 1 | Read | 0xD7 |
| ADV7391 and ADV7393 | 0 | Write | 0x54 |
| | 0 | Read | 0x55 |
| | 1 | Write | 0x56 |
| | 1 | Read | 0x57 |

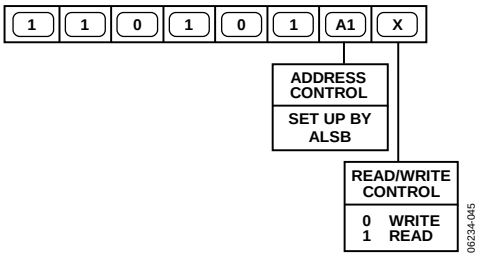


*Figure 47. ADV7390/ADV7392 I²C Slave Address*

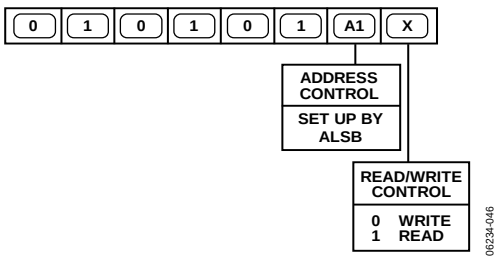


*Figure 48. ADV7391/ADV7393 I²C Slave Address*

The various devices on the bus use the following protocol. The master initiates a data transfer by establishing a start condition, defined by a high-to-low transition on SDA while SCL remains high. This indicates that an address/data stream follows. All peripherals respond to the start condition and shift the next eight bits (7-bit address plus the R/$\overline{W}$ bit).

The bits are transferred from MSB down to LSB. The peripheral that recognizes the transmitted address responds by pulling the data line low during the ninth clock pulse. This is known as an acknowledge bit. All other devices withdraw from the bus at this point and maintain an idle condition. The idle condition occurs when the device monitors the SDA and SCL lines waiting for the start condition and the correct transmitted address. The R/$\overline{W}$ bit determines the direction of the data.

Logic 0 on the LSB of the first byte means that the master writes information to the peripheral. Logic 1 on the LSB of the first byte means that the master reads information from the peripheral.

The ADV7390/ADV7391/ADV7392/ADV7393 act as a standard slave device on the bus. The data on the SDA pin is eight bits long, supporting the 7-bit addresses plus the R/$\overline{W}$ bit. It interprets the first byte as the device address and the second byte as the starting subaddress. There is a subaddress auto-increment facility. This allows data to be written to or read from registers in ascending subaddress sequence starting at any valid subaddress. A data transfer is always terminated by a stop condition. The user can also access any unique subaddress register on a one-by-one basis without updating all the registers.

Stop and start conditions can be detected at any stage during the data transfer. If these conditions are asserted out of sequence with normal read and write operations, they cause an immediate jump to the idle condition. During a given SCL high period, the user should issue only a start condition, a stop condition, or a stop condition followed by a start condition. If an invalid subaddress is issued by the user, the ADV7390/ADV7391/ADV7392/ADV7393 do not issue an acknowledge but returns to the idle condition. If the user uses the auto-increment method of addressing the encoder and exceeds the highest subaddress, the following actions are taken:

- In read mode, the highest subaddress register contents are output until the master device issues a no acknowledge. This indicates the end of a read. A no acknowledge condition occurs when the SDA line is not pulled low on the ninth pulse.
- In write mode, the data for the invalid byte is not loaded into any subaddress register, a no acknowledge is issued by the ADV7390/ADV7391/ADV7392/ADV7393, and the part returns to the idle condition.

Figure 49 shows an example of data transfer for a write sequence and the start and stop conditions. Figure 50 shows bus write and read sequences.



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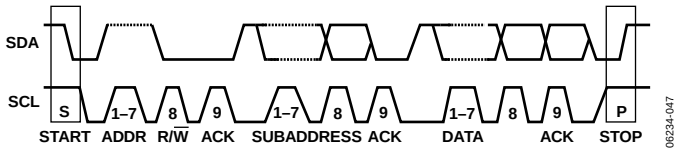


*Figure 49. I²C Data Transfer*

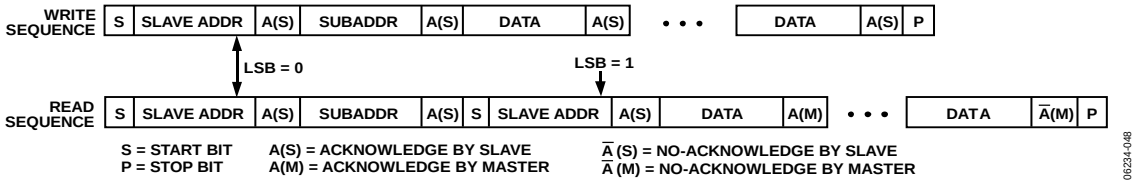


*Figure 50. I²C Read and Write Sequence*



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# REGISTER MAP ACCESS

A microprocessor can read from or write to all registers of the ADV7390/ADV7391/ADV7392/ADV7393 via the MPU port, except for registers that are specified as read-only or write-only registers.

The subaddress register determines the register accessed by the next read or write operation. All communication through the MPU port starts with an access to the subaddress register. A read/write operation is then performed from/to the target address, incrementing to the next address until the transaction is complete.

## REGISTER PROGRAMMING

Table 17 to Table 34 describe the functionality of each register. All registers can be read from as well as written to, unless otherwise stated.

## SUBADDRESS REGISTER (SR7 TO SR0)

The subaddress register is an 8-bit write-only register. After the MPU port is accessed and a read/write operation is selected, the subaddress is set up. The subaddress register determines which register performs the next operation.

**Table 17. Register 0x00**

| SR7 to SR0 | Register | Bit Description | Bit Number 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Register Setting | Reset Value |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0x00 | Power mode | Sleep mode. With this control enabled, the current consumption is reduced to µA level. All DACs and the internal PLL circuit are disabled. Registers can be read from and written to in sleep mode. | | | | | | | | 0<br>1 | Sleep mode off<br>Sleep mode on | 0x12 |
| | | PLL and oversampling control. This control allows the internal PLL circuit to be powered down and the oversampling to be switched off. | | | | | | | 0<br>1 | | PLL on<br>PLL off | |
| | | DAC 3: power on/off. | | | | | | 0<br>1 | | | DAC 3 off<br>DAC 3 on | |
| | | DAC 2: power on/off. | | | | | 0<br>1 | | | | DAC 2 off<br>DAC 2 on | |
| | | DAC 1: power on/off. | | | | 0<br>1 | | | | | DAC 1 off<br>DAC 1 on | |
| | | Reserved. | 0 | 0 | 0 | | | | | | | |

**Table 18. Register 0x01 to Register 0x09**

| SR7 to SR0 | Register | Bit Description | Bit Number[1] 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Register Setting | Reset Value |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0x01 | Mode select | Reserved. | | | | | | | | 0 | | 0x00 |
| | | DDR clock edge alignment (used only for ED[2] and HD DDR modes) | | | | | | 0<br>0<br>1<br>1 | 0<br>1<br>0<br>1 | | Chroma clocked in on rising clock edge and luma clocked in on falling clock edge.<br>Reserved.<br>Reserved.<br>Luma clocked in on rising clock edge and chroma clocked in on falling clock edge. | |
| | | Reserved | | | | | 0 | | | | | |
| | | Input mode (see Subaddress 0x30, Bits[7:3] for ED/HD standard selection) | | 0<br>0<br>0<br>0<br>1<br>1<br>1<br>1 | 0<br>0<br>1<br>1<br>0<br>0<br>1<br>1 | 0<br>1<br>0<br>1<br>0<br>1<br>0<br>1 | | | | | SD input.<br>ED/HD-SDR input.[3]<br>ED/HD-DDR input.<br>Reserved.<br>Reserved.<br>Reserved.<br>Reserved.<br>ED (at 54 MHz) input. | |
| | | Reserved | 0 | | | | | | | | | |



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| SR7 to SR0 | Register | Bit Description | Bit Number[1] 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Register Setting | Reset Value |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0x02 | Mode Register 0 | Reserved | | | | | | | | 0 | Zero must be written to this bit. | 0x20 |
| | | HD interlace external $\overline{VSYNC}$ and $\overline{HSYNC}$ | | | | | | | 0<br>1 | | Default.<br>If using HD $\overline{HSYNC}$/$\overline{VSYNC}$interlace mode, setting this bit to 1 is recommended (see the HD Interlace External $\overline{HSYNC}$ and $\overline{VSYNC}$ Considerations section for more information). | |
| | | Test pattern black bar[4] | | | | | | 0<br>1 | | | Disabled.<br>Enabled. | |
| | | Manual CSC matrix adjust | | | | | 0<br>1 | | | | Disable manual CSC matrix adjust.<br>Enable manual CSC matrix adjust. | |
| | | Sync on RGB | | | | 0<br>1 | | | | | No sync.<br>Sync on all RGB outputs. | |
| | | RGB/YPrPb output select | | | 0<br>1 | | | | | | RGB component outputs.<br>YPrPb component outputs. | |
| | | SD sync output enable | | 0<br>1 | | | | | | | No sync output.<br>Output SD syncs on $\overline{HSYNC}$ and $\overline{VSYNC}$ pins. | |
| | | ED/HD sync output enable | 0<br>1 | | | | | | | | No sync output.<br>Output ED/HD syncs on $\overline{HSYNC}$ and $\overline{VSYNC}$ pins. | |
| 0x03 | ED/HD CSC Matrix 0 | | | | | | | | x | x | LSBs for GY. | 0x03 |
| 0x04 | ED/HD CSC Matrix 1 | | x | x | x | x | x | x | x | x | LSBs for RV.<br>LSBs for BU.<br>LSBs for GV.<br>LSBs for GU. | 0xF0 |
| 0x05 | ED/HD CSC Matrix 2 | | x | x | x | x | x | x | x | x | Bits[9:2] for GY. | 0x4E |
| 0x06 | ED/HD CSC Matrix 3 | | x | x | x | x | x | x | x | x | Bits[9:2] for GU. | 0x0E |
| 0x07 | ED/HD CSC Matrix 4 | | x | x | x | x | x | x | x | x | Bits[9:2] for GV. | 0x24 |
| 0x08 | ED/HD CSC Matrix 5 | | x | x | x | x | x | x | x | x | Bits[9:2] for BU. | 0x92 |
| 0x09 | ED/HD CSC Matrix 6 | | x | x | x | x | x | x | x | x | Bits[9:2] for RV. | 0x7C |

[1] x = Logic 0 or Logic 1.
[2] ED = enhanced definition = 525p and 625p.
[3] Available on the ADV7392/ADV7393 (40-pin devices) only.
[4] Subaddress 0x31, Bit 2 must also be enabled (ED/HD). Subaddress 0x84, Bit 6 must also be enabled (SD).



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**Table 19. Register 0x0B to Register 0x17**

| SR7 to SR0 | Register | Bit Description | Bit Number[1] 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Register Setting | Reset Value |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0x0B | DAC 1, DAC 2, DAC 3 output levels | Positive gain to DAC output voltage | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0%. | 0x00 |
| | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | +0.018%. | |
| | | | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | +0.036%. | |
| | | | … | … | … | … | … | … | … | … | … | |
| | | | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | +7.382%. | |
| | | | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | +7.5%. | |
| | | Negative gain to DAC output voltage | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | −7.5%. | |
| | | | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | −7.382%. | |
| | | | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | −7.364%. | |
| | | | … | … | … | … | … | … | … | … | … | |
| | | | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | −0.018%. | |
| 0x0D | DAC power mode | DAC 1 low power mode | | | | | | | | 0 | DAC 1 low power disabled. | 0x00 |
| | | | | | | | | | | 1 | DAC 1 low power enabled. | |
| | | DAC 2 low power mode | | | | | | | 0 | | DAC 2 low power disabled. | |
| | | | | | | | | | 1 | | DAC 2 low power enabled. | |
| | | DAC 3 low power mode | | | | | | 0 | | | DAC 3 low power disabled. | |
| | | | | | | | | 1 | | | DAC 3 low power enabled. | |
| | | SD/ED oversample rate select | | | | | 0 | | | | SD = 16×, ED = 8×. | |
| | | | | | | | 1 | | | | SD = 8×, ED = 4×. | |
| | | Reserved | 0 | 0 | 0 | 0 | | | | | | |
| 0x10 | Cable detection | DAC 1 cable detect | | | | | | | | 0 | Cable detected on DAC 1. | 0x00 |
| | | Read only | | | | | | | | 1 | DAC 1 unconnected. | |
| | | DAC 2 cable detect | | | | | | | 0 | | Cable detected on DAC 2. | |
| | | Read only | | | | | | | 1 | | DAC 2 unconnected. | |
| | | Reserved | | | | | 0 | 0 | | | | |
| | | Unconnected DAC autopower-down | | | | 0 | | | | | DAC autopower-down disable. | |
| | | | | | | 1 | | | | | DAC autopower-down enable. | |
| | | Reserved | 0 | 0 | 0 | | | | | | | |
| 0x13 | Pixel Port Readback A[2] | P[7:0] readback (ADV7390/ADV7391) P[15:8] readback (ADV7392/ADV7393) | x | x | x | x | x | x | x | x | Read only. | 0xXX |
| 0x14 | Pixel Port Readback B[2] | P[7:0] readback (ADV7392/ADV7393) | x | x | x | x | x | x | x | x | Read only. | 0xXX |
| 0x16 | Control port readback[2] | Reserved | | | | | | x | x | x | Read only. | 0xXX |
| | | $\overline{\text{VSYNC}}$ readback | | | | | x | | | | | |
| | | $\overline{\text{HSYNC}}$ readback | | | | x | | | | | | |
| | | SFL readback | | | x | | | | | | | |
| | | Reserved | x | x | | | | | | | | |
| 0x17 | Software reset | Reserved | | | | | | | | 0 | | 0x00 |
| | | Software reset | | | | | | | 0 | | | |
| | | | | | | | | | 1 | | Writing a 1 resets the device; this is a self-clearing bit. | |
| | | Reserved. | 0 | 0 | 0 | 0 | 0 | 0 | | | | |

[1] x = Logic 0 or Logic 1.
[2] For correct operation, Subaddress 0x01[6:4] must equal the default value of 000.



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**Table 20. Register 0x30**

| SR7 to SR0 | Register | Bit Description | Bit Number 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Register Setting | Note | Reset Value |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0x30 | ED/HD Mode Register 1 | ED/HD output standard | | | | | | | 0 | 0 | EIA-770.2 output<br>EIA-770.3 output | ED<br>HD | 0x00 |
| | | | | | | | | | 0 | 1 | EIA-770.1 output | | |
| | | | | | | | | | 1 | 0 | Output levels for full input range | | |
| | | | | | | | | | 1 | 1 | Reserved | | |
| | | ED/HD input synchronization format | | | | | | 0 | | | External $\overline{\text{HSYNC}}$, $\overline{\text{VSYNC}}$ and field inputs[1] | | |
| | | | | | | | | 1 | | | Embedded EAV/SAV codes | | |
| | | ED/HD standard[2] | 0 | 0 | 0 | 0 | 0 | | | | SMPTE 293M, ITU-BT.1358 | 525p at 59.94 Hz | |
| | | | 0 | 0 | 0 | 1 | 0 | | | | BTA-1004, ITU-BT.1362 | 525p at 59.94 Hz | |
| | | | 0 | 0 | 0 | 1 | 1 | | | | ITU-BT.1358 | 625p at 50 Hz | |
| | | | 0 | 0 | 1 | 0 | 0 | | | | ITU-BT.1362 | 625p at 50 Hz | |
| | | | 0 | 0 | 1 | 0 | 1 | | | | SMPTE 296M-1, SMPTE 274M-2 | 720p at 60 Hz/59.94 Hz | |
| | | | 0 | 0 | 1 | 1 | 0 | | | | SMPTE 296M-3 | 720p at 50 Hz | |
| | | | 0 | 0 | 1 | 1 | 1 | | | | SMPTE 296M-4, SMPTE 274M-5 | 720p at 30 Hz/29.97 Hz | |
| | | | 0 | 1 | 0 | 0 | 0 | | | | SMPTE 296M-6 | 720p at 25 Hz | |
| | | | 0 | 1 | 0 | 0 | 1 | | | | SMPTE 296M-7, SMPTE 296M-8 | 720p at 24 Hz/23.98 Hz | |
| | | | 0 | 1 | 0 | 1 | 0 | | | | SMPTE 240M | 1035i at 60 Hz/59.94 Hz | |
| | | | 0 | 1 | 0 | 1 | 1 | | | | Reserved | | |
| | | | 0 | 1 | 1 | 0 | 0 | | | | Reserved | | |
| | | | 0 | 1 | 1 | 0 | 1 | | | | SMPTE 274M-4, SMPTE 274M-5 | 1080i at 30 Hz/29.97 Hz | |
| | | | 0 | 1 | 1 | 1 | 0 | | | | SMPTE 274M-6 | 1080i at 25 Hz | |
| | | | 0 | 1 | 1 | 1 | 1 | | | | SMPTE 274M-7, SMPTE 274M-8 | 1080p at 30 Hz/29.97 Hz | |
| | | | 1 | 0 | 0 | 0 | 0 | | | | SMPTE 274M-9 | 1080p at 25 Hz | |
| | | | 1 | 0 | 0 | 0 | 1 | | | | SMPTE 274M-10, SMPTE 274M-11 | 1080p at 24 Hz/23.98 Hz | |
| | | | 1 | 0 | 0 | 1 | 0 | | | | ITU-R BT.709-5 | 1080Psf at 24 Hz | |
| | | | 10011 to 11111 | | | | | | | | Reserved | | |

[1] Synchronization can be controlled with a combination of either $\overline{\text{HSYNC}}$ and $\overline{\text{VSYNC}}$ inputs or $\overline{\text{HSYNC}}$ and field inputs, depending on Subaddress 0x34, Bit 6.

[2] See the HD Interlace External $\overline{\text{HSYNC}}$ and $\overline{\text{VSYNC}}$ Considerations section for more information.



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**Table 21. Register 0x31 to Register 0x33**

| SR7 to SR0 | Register | Bit Description | Bit Number 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Register Setting | Reset Value |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0x31 | ED/HD Mode Register 2 | ED/HD pixel data valid | | | | | | | | 0 | Pixel data valid off. | 0x00 |
| | | | | | | | | | | 1 | Pixel data valid on. | |
| | | HD oversample rate select | | | | | | | 0 | | 4×. | |
| | | | | | | | | | 1 | | 2×. | |
| | | ED/HD test pattern enable | | | | | | 0 | | | HD test pattern off. | |
| | | | | | | | | 1 | | | HD test pattern on. | |
| | | ED/HD test pattern hatch/field | | | | | 0 | | | | Hatch. | |
| | | | | | | | 1 | | | | Field/frame. | |
| | | ED/HD vertical blanking interval (VBI) open | | | | 0 | | | | | Disabled. | |
| | | | | | | 1 | | | | | Enabled. | |
| | | ED/HD undershoot limiter | | 0 | 0 | | | | | | Disabled. | |
| | | | | 0 | 1 | | | | | | −11 IRE. | |
| | | | | 1 | 0 | | | | | | −6 IRE. | |
| | | | | 1 | 1 | | | | | | −1.5 IRE. | |
| | | ED/HD sharpness filter | 0 | | | | | | | | Disabled. | |
| | | | 1 | | | | | | | | Enabled. | |
| 0x32 | ED/HD Mode Register 3 | ED/HD Y delay with respect to the falling edge of HSYNC | | | | | | 0 | 0 | 0 | 0 clock cycles. | 0x00 |
| | | | | | | | | 0 | 0 | 1 | One clock cycle. | |
| | | | | | | | | 0 | 1 | 0 | Two clock cycles. | |
| | | | | | | | | 0 | 1 | 1 | Three clock cycles. | |
| | | | | | | | | 1 | 0 | 0 | Four clock cycles. | |
| | | ED/HD color delay with respect to the falling edge of HSYNC | | | 0 | 0 | 0 | | | | 0 clock cycles. | |
| | | | | | 0 | 0 | 1 | | | | One clock cycle. | |
| | | | | | 0 | 1 | 0 | | | | Two clock cycles. | |
| | | | | | 0 | 1 | 1 | | | | Three clock cycles. | |
| | | | | | 1 | 0 | 0 | | | | Four clock cycles. | |
| | | ED/HD CGMS enable | | 0 | | | | | | | Disabled. | |
| | | | | 1 | | | | | | | Enabled. | |
| | | ED/HD CGMS CRC enable | 0 | | | | | | | | Disabled. | |
| | | | 1 | | | | | | | | Enabled. | |
| 0x33 | ED/HD Mode Register 4 | ED/HD Cr/Cb sequence | | | | | | | | 0 | Cb after falling edge of HSYNC. | 0x68 |
| | | | | | | | | | | 1 | Cr after falling edge of HSYNC. | |
| | | Reserved | | | | | | | 0 | | 0 must be written to this bit. | |
| | | ED/HD input format | | | | | | 0 | | | 8-bit input. | |
| | | | | | | | | 1 | | | 10-bit input[1]. | |
| | | Sinc compensation filter on DAC 1, DAC 2, DAC 3 | | | | | 0 | | | | Disabled. | |
| | | | | | | | 1 | | | | Enabled. | |
| | | Reserved | | | | 0 | | | | | 0 must be written to this bit. | |
| | | ED/HD chroma SSAF filter | | | 0 | | | | | | Disabled. | |
| | | | | | 1 | | | | | | Enabled. | |
| | | Reserved | | 1 | | | | | | | 1 must be written to this bit. | |
| | | ED/HD double buffering | 0 | | | | | | | | Disabled. | |
| | | | 1 | | | | | | | | Enabled. | |

[1] Available on the ADV7392/ADV7393 (40-pin devices) only.



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**Table 22. Register 0x34 to Register 0x38**

| SR7 to SR0 | Register | Bit Description | Bit Number[1] 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Register Setting | Reset Value |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0x34 | ED/HD Mode Register 5 | ED/HD timing reset | | | | | | | | 0<br>1 | Internal ED/HD timing counters enabled.<br>Resets the internal ED/HD timing counters. | 0x48 |
| | | ED/HD $\overline{\text{HSYNC}}$ control[2] | | | | | | | 0<br>1 | | $\overline{\text{HSYNC}}$ output control (see Table 55). | |
| | | ED/HD $\overline{\text{VSYNC}}$ control[2] | | | | | | 0<br>1 | | | $\overline{\text{VSYNC}}$ output control (see Table 56). | |
| | | Reserved | | | | | 1 | | | | | |
| | | ED Macrovision® enable[3] | | | | 0<br>1 | | | | | ED Macrovision disabled.<br>ED Macrovision enabled. | |
| | | Reserved | | | 0 | | | | | | 0 must be written to this bit. | |
| | | ED/HD $\overline{\text{VSYNC}}$ input/field input | | 0<br>1 | | | | | | | 0 = Field input.<br>1 = $\overline{\text{VSYNC}}$ input. | |
| | | ED/HD horizontal/vertical counter mode[4] | 0<br>1 | | | | | | | | Update field/line counter.<br>Field/line counter free running. | |
| 0x35 | ED/HD Mode Register 6 | Reserved | | | | | | | | 0 | | 0x00 |
| | | Reserved | | | | | | | 0 | | | |
| | | ED/HD sync on PrPb | | | | | | 0<br>1 | | | Disabled.<br>Enabled. | |
| | | ED/HD color DAC swap | | | | | 0<br>1 | | | | DAC 2 = Pb, DAC 3 = Pr.<br>DAC 2 = Pr, DAC 3 = Pb. | |
| | | ED/HD gamma correction curve select | | | | 0<br>1 | | | | | Gamma Correction Curve A.<br>Gamma Correction Curve B. | |
| | | ED/HD gamma correction enable | | | 0<br>1 | | | | | | Disabled.<br>Enabled. | |
| | | ED/HD adaptive filter mode | | 0<br>1 | | | | | | | Mode A.<br>Mode B. | |
| | | ED/HD adaptive filter enable | 0<br>1 | | | | | | | | Disabled.<br>Enabled. | |
| 0x36 | ED/HD Y level[5] | ED/HD Test Pattern Y level | x | x | x | x | x | x | x | x | Y level value. | 0xA0 |
| 0x37 | ED/HD Cr level[5] | ED/HD Test Pattern Cr level | x | x | x | x | x | x | x | x | Cr level value. | 0x80 |
| 0x38 | ED/HD Cb level[5] | ED/HD Test Pattern Cb level | x | x | x | x | x | x | x | x | Cb level value. | 0x80 |

[1] x = Logic 0 or Logic 1.
[2] Used in conjunction with ED/HD sync output enable in Subaddress 0x02, Bit 7 = 1.
[3] Applies to the ADV7390 and ADV7392 only.
[4] When set to 0, the horizontal/vertical counters automatically wrap around at the end of the line/field/frame of the selected standard. When set to 1, the horizontal/vertical counters are free running and wrap around when external sync signals indicate to do so.
[5] For use with ED/HD internal test patterns only (Subaddress 0x31, Bit 2 = 1).



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**Table 23. Register 0x39 to Register 0x43**

| SR7 to SR0 | Register | Bit Description | Bit Number | | | | | | | | Register Setting | Reset Value |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | |
| 0x39 | ED/HD Mode Register 7 | Reserved | | | | 0 | 0 | 0 | 0 | 0 | | 0x00 |
| | | ED/HD EIA/CEA-861B synchronization compliance | | | 0<br>1 | | | | | | Disabled<br>Enabled | |
| | | Reserved | 0 | 0 | | | | | | | | |
| 0X3A | ED/HD Mode Register 8 | INV_PHSYNC_POL | | | | | | | | 0<br>1 | Disabled<br>Enabled | 0x00 |
| | | INV_PVSYNC_POL | | | | | | | 0<br>1 | | Disabled<br>Enabled | |
| | | INV_PBLANK_POL | | | | | | 0<br>1 | | | Disabled<br>Enabled | |
| | | Reserved | 0 | 0 | 0 | 0 | 0 | | | | | |
| 0x40 | ED/HD sharpness filter gain | ED/HD sharpness filter gain Value A | | | | | 0<br>0<br>…<br>0<br>1<br>…<br>1 | 0<br>0<br>…<br>1<br>0<br>…<br>1 | 0<br>0<br>…<br>1<br>0<br>… | 0<br>1<br>…<br>1<br>0<br>…<br>1 | Gain A = 0<br>Gain A = +1<br>…<br>Gain A = +7<br>Gain A = −8<br>…<br>Gain A = −1 | 0x00 |
| | | ED/HD sharpness filter gain Value B | 0<br>0<br>…<br>0<br>1<br>…<br>1 | 0<br>0<br>…<br>1<br>0<br>…<br>1 | 0<br>0<br>…<br>1<br>0<br>…<br>1 | 0<br>1<br>…<br>1<br>0<br>…<br>1 | | | | | Gain B = 0<br>Gain B = +1<br>…<br>Gain B = +7<br>Gain B = −8<br>…<br>Gain B = −1 | |
| 0x41 | ED/HD CGMS Data 0 | ED/HD CGMS data bits | 0 | 0 | 0 | 0 | C19 | C18 | C17 | C16 | CGMS C19 to C16 | 0x00 |
| 0x42 | ED/HD CGMS Data 1 | ED/HD CGMS data bits | C15 | C14 | C13 | C12 | C11 | C10 | C9 | C8 | CGMS C15 to C8 | 0x00 |
| 0x43 | ED/HD CGMS Data 2 | ED/HD CGMS data bits | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 | CGMS C7 to C0 | 0x00 |



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**Table 24. Register 0x44 to Register 0x57**

| SR7 to SR0 | Register | Bit Description | Bit Number[1] | | | | | | | | Register Setting | Reset Value |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | |
| 0x44 | ED/HD Gamma A0 | ED/HD Gamma Curve A (Point 24) | x | x | x | x | x | x | x | x | A0 | 0x00 |
| 0x45 | ED/HD Gamma A1 | ED/HD Gamma Curve A (Point 32) | x | x | x | x | x | x | x | x | A1 | 0x00 |
| 0x46 | ED/HD Gamma A2 | ED/HD Gamma Curve A (Point 48) | x | x | x | x | x | x | x | x | A2 | 0x00 |
| 0x47 | ED/HD Gamma A3 | ED/HD Gamma Curve A (Point 64) | x | x | x | x | x | x | x | x | A3 | 0x00 |
| 0x48 | ED/HD Gamma A4 | ED/HD Gamma Curve A (Point 80) | x | x | x | x | x | x | x | x | A4 | 0x00 |
| 0x49 | ED/HD Gamma A5 | ED/HD Gamma Curve A (Point 96) | x | x | x | x | x | x | x | x | A5 | 0x00 |
| 0x4A | ED/HD Gamma A6 | ED/HD Gamma Curve A (Point 128) | x | x | x | x | x | x | x | x | A6 | 0x00 |
| 0x4B | ED/HD Gamma A7 | ED/HD Gamma Curve A (Point 160) | x | x | x | x | x | x | x | x | A7 | 0x00 |
| 0x4C | ED/HD Gamma A8 | ED/HD Gamma Curve A (Point 192) | x | x | x | x | x | x | x | x | A8 | 0x00 |
| 0x4D | ED/HD Gamma A9 | ED/HD Gamma Curve A (Point 224) | x | x | x | x | x | x | x | x | A9 | 0x00 |
| 0x4E | ED/HD Gamma B0 | ED/HD Gamma Curve B (Point 24) | x | x | x | x | x | x | x | x | B0 | 0x00 |
| 0x4F | ED/HD Gamma B1 | ED/HD Gamma Curve B (Point 32) | x | x | x | x | x | x | x | x | B1 | 0x00 |
| 0x50 | ED/HD Gamma B2 | ED/HD Gamma Curve B (Point 48) | x | x | x | x | x | x | x | x | B2 | 0x00 |
| 0x51 | ED/HD Gamma B3 | ED/HD Gamma Curve B (Point 64) | x | x | x | x | x | x | x | x | B3 | 0x00 |
| 0x52 | ED/HD Gamma B4 | ED/HD Gamma Curve B (Point 80) | x | x | x | x | x | x | x | x | B4 | 0x00 |
| 0x53 | ED/HD Gamma B5 | ED/HD Gamma Curve B (Point 96) | x | x | x | x | x | x | x | x | B5 | 0x00 |
| 0x54 | ED/HD Gamma B6 | ED/HD Gamma Curve B (Point 128) | x | x | x | x | x | x | x | x | B6 | 0x00 |
| 0x55 | ED/HD Gamma B7 | ED/HD Gamma Curve B (Point 160) | x | x | x | x | x | x | x | x | B7 | 0x00 |
| 0x56 | ED/HD Gamma B8 | ED/HD Gamma Curve B (Point 192) | x | x | x | x | x | x | x | x | B8 | 0x00 |
| 0x57 | ED/HD Gamma B9 | ED/HD Gamma Curve B (Point 224) | x | x | x | x | x | x | x | x | B9 | 0x00 |

[1] x = Logic 0 or Logic 1.



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**Table 25. Register 0x58 to Register 0x5D**

| SR7 to SR0 | Register | Bit Description | Bit Number[1] 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Register Setting | Reset Value |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0x58 | ED/HD Adaptive Filter Gain 1 | ED/HD Adaptive Filter Gain 1, Value A | | | | | 0 | 0 | 0 | 0 | Gain A = 0 | 0x00 |
| | | | | | | | 0 | 0 | 0 | 1 | Gain A = +1 | |
| | | | | | | | … | … | … | … | … | |
| | | | | | | | 0 | 1 | 1 | 1 | Gain A = +7 | |
| | | | | | | | 1 | 0 | 0 | 0 | Gain A = −8 | |
| | | | | | | | … | … | … | … | … | |
| | | | | | | | 1 | 1 | 1 | 1 | Gain A = −1 | |
| | | ED/HD Adaptive Filter Gain 1, Value B | 0 | 0 | 0 | 0 | | | | | Gain B = 0 | |
| | | | 0 | 0 | 0 | 1 | | | | | Gain B = +1 | |
| | | | … | … | … | … | | | | | … | |
| | | | 0 | 1 | 1 | 1 | | | | | Gain B = +7 | |
| | | | 1 | 0 | 0 | 0 | | | | | Gain B = −8 | |
| | | | … | … | … | … | | | | | … | |
| | | | 1 | 1 | 1 | 1 | | | | | Gain B = −1 | |
| 0x59 | ED/HD Adaptive Filter Gain 2 | ED/HD Adaptive Filter Gain 2, Value A | | | | | 0 | 0 | 0 | 0 | Gain A = 0 | 0x00 |
| | | | | | | | 0 | 0 | 0 | 1 | Gain A = +1 | |
| | | | | | | | … | … | … | … | … | |
| | | | | | | | 0 | 1 | 1 | 1 | Gain A = +7 | |
| | | | | | | | 1 | 0 | 0 | 0 | Gain A = −8 | |
| | | | | | | | … | … | … | … | … | |
| | | | | | | | 1 | 1 | 1 | 1 | Gain A = −1 | |
| | | ED/HD Adaptive Filter Gain 2, Value B | 0 | 0 | 0 | 0 | | | | | Gain B = 0 | |
| | | | 0 | 0 | 0 | 1 | | | | | Gain B = +1 | |
| | | | … | … | … | … | | | | | … | |
| | | | 0 | 1 | 1 | 1 | | | | | Gain B = +7 | |
| | | | 1 | 0 | 0 | 0 | | | | | Gain B = −8 | |
| | | | … | … | … | … | | | | | … | |
| | | | 1 | 1 | 1 | 1 | | | | | Gain B = −1 | |
| 0x5A | ED/HD Adaptive Filter Gain 3 | ED/HD Adaptive Filter Gain 3, Value A | | | | | 0 | 0 | 0 | 0 | Gain A = 0 | 0x00 |
| | | | | | | | 0 | 0 | 0 | 1 | Gain A = +1 | |
| | | | | | | | … | … | … | … | … | |
| | | | | | | | 0 | 1 | 1 | 1 | Gain A = +7 | |
| | | | | | | | 1 | 0 | 0 | 0 | Gain A = −8 | |
| | | | | | | | … | … | … | … | … | |
| | | | | | | | 1 | 1 | 1 | 1 | Gain A = −1 | |
| | | ED/HD Adaptive Filter Gain 3, Value B | 0 | 0 | 0 | 0 | | | | | Gain B = 0 | |
| | | | 0 | 0 | 0 | 1 | | | | | Gain B = +1 | |
| | | | … | … | … | … | | | | | … | |
| | | | 0 | 1 | 1 | 1 | | | | | Gain B = +7 | |
| | | | 1 | 0 | 0 | 0 | | | | | Gain B = −8 | |
| | | | … | … | … | … | | | | | … | |
| | | | 1 | 1 | 1 | 1 | | | | | Gain B = −1 | |
| 0x5B | ED/HD Adaptive Filter Threshold A | ED/HD Adaptive Filter Threshold A | x | x | x | x | x | x | x | x | Threshold A | 0x00 |
| 0x5C | ED/HD Adaptive Filter Threshold B | ED/HD Adaptive Filter Threshold B | x | x | x | x | x | x | x | x | Threshold B | 0x00 |
| 0x5D | ED/HD Adaptive Filter Threshold C | ED/HD Adaptive Filter Threshold C | x | x | x | x | x | x | x | x | Threshold C | 0x00 |

[1] x = Logic 0 or Logic 1.



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**Table 26. Register 0x5E to Register 0x6E**

| SR7 to SR0 | Register | Bit Description | Bit Number | | | | | | | | Register Setting | Reset Value |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | |
| 0x5E | ED/HD CGMS Type B Register 0 | ED/HD CGMS Type B enable | | | | | | | | 0<br>1 | Disabled<br>Enabled | 0x00 |
| | | ED/HD CGMS Type B CRC enable | | | | | | | 0<br>1 | | Disabled<br>Enabled | |
| | | ED/HD CGMS Type B header bits | H5 | H4 | H3 | H2 | H1 | H0 | | | H5 to H0 | |
| 0x5F | ED/HD CGMS Type B Register 1 | ED/HD CGMS Type B data bits | P7 | P6 | P5 | P4 | P3 | P2 | P1 | P0 | P7 to P0 | 0x00 |
| 0x60 | ED/HD CGMS Type B Register 2 | ED/HD CGMS Type B data bits | P15 | P14 | P13 | P12 | P11 | P10 | P9 | P8 | P15 to P8 | 0x00 |
| 0x61 | ED/HD CGMS Type B Register 3 | ED/HD CGMS Type B data bits | P23 | P22 | P21 | P20 | P19 | P18 | P17 | P16 | P23 to P16 | 0x00 |
| 0x62 | ED/HD CGMS Type B Register 4 | ED/HD CGMS Type B data bits | P31 | P30 | P29 | P28 | P27 | P26 | P25 | P24 | P31 to P24 | 0x00 |
| 0x63 | ED/HD CGMS Type B Register 5 | ED/HD CGMS Type B data bits | P39 | P38 | P37 | P36 | P35 | P34 | P33 | P32 | P39 to P32 | 0x00 |
| 0x64 | ED/HD CGMS Type B Register 6 | ED/HD CGMS Type B data bits | P47 | P46 | P45 | P44 | P43 | P42 | P41 | P40 | P47 to P40 | 0x00 |
| 0x65 | ED/HD CGMS Type B Register 7 | ED/HD CGMS Type B data bits | P55 | P54 | P53 | P52 | P51 | P50 | P49 | P48 | P55 to P48 | 0x00 |
| 0x66 | ED/HD CGMS Type B Register 8 | ED/HD CGMS Type B data bits | P63 | P62 | P61 | P60 | P59 | P58 | P57 | P56 | P63 to P56 | 0x00 |
| 0x67 | ED/HD CGMS Type B Register 9 | ED/HD CGMS Type B data bits | P71 | P70 | P69 | P68 | P67 | P66 | P65 | P64 | P71 to P64 | 0x00 |
| 0x68 | ED/HD CGMS Type B Register 10 | ED/HD CGMS Type B data bits | P79 | P78 | P77 | P76 | P75 | P74 | P73 | P72 | P79 to P72 | 0x00 |
| 0x69 | ED/HD CGMS Type B Register 11 | ED/HD CGMS Type B data bits | P87 | P86 | P85 | P84 | P83 | P82 | P81 | P80 | P87 to P80 | 0x00 |
| 0x6A | ED/HD CGMS Type B Register 12 | ED/HD CGMS Type B data bits | P95 | P94 | P93 | P92 | P91 | P90 | P89 | P88 | P95 to P88 | 0x00 |
| 0x6B | ED/HD CGMS Type B Register 13 | ED/HD CGMS Type B data bits | P103 | P102 | P101 | P100 | P99 | P98 | P97 | P96 | P103 to P96 | 0x00 |
| 0x6C | ED/HD CGMS Type B Register 14 | ED/HD CGMS Type B data bits | P111 | P110 | P109 | P108 | P107 | P106 | P105 | P104 | P111 to P104 | 0x00 |
| 0x6D | ED/HD CGMS Type B Register 15 | ED/HD CGMS Type B data bits | P119 | P118 | P117 | P116 | P115 | P114 | P113 | P112 | P119 to P112 | 0x00 |
| 0x6E | ED/HD CGMS Type B Register 16 | ED/HD CGMS Type B data bits | P127 | P126 | P125 | P124 | P123 | P122 | P121 | P120 | P127 to P120 | 0x00 |



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**Table 27. Register 0x80 to Register 0x83**

| SR7 to SR0 | Register | Bit Description | Bit Number 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Register Setting | Reset Value |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0x80 | SD Mode Register 1 | SD standard | | | | | | | 0 | 0 | NTSC | 0x10 |
| | | | | | | | | | 0 | 1 | PAL B, PAL D, PAL G, PAL H, PAL I | |
| | | | | | | | | | 1 | 0 | PAL M | |
| | | | | | | | | | 1 | 1 | PAL N | |
| | | SD luma filter | | | | 0 | 0 | 0 | | | LPF NTSC | |
| | | | | | | 0 | 0 | 1 | | | LPF PAL | |
| | | | | | | 0 | 1 | 0 | | | Notch NTSC | |
| | | | | | | 0 | 1 | 1 | | | Notch PAL | |
| | | | | | | 1 | 0 | 0 | | | Luma SSAF | |
| | | | | | | 1 | 0 | 1 | | | Luma CIF | |
| | | | | | | 1 | 1 | 0 | | | Luma QCIF | |
| | | | | | | 1 | 1 | 1 | | | Reserved | |
| | | SD chroma filter | 0 | 0 | 0 | | | | | | 1.3 MHz | |
| | | | 0 | 0 | 1 | | | | | | 0.65 MHz | |
| | | | 0 | 1 | 0 | | | | | | 1.0 MHz | |
| | | | 0 | 1 | 1 | | | | | | 2.0 MHz | |
| | | | 1 | 0 | 0 | | | | | | Reserved | |
| | | | 1 | 0 | 1 | | | | | | Chroma CIF | |
| | | | 1 | 1 | 0 | | | | | | Chroma QCIF | |
| | | | 1 | 1 | 1 | | | | | | 3.0 MHz | |
| 0x82 | SD Mode Register 2 | SD PrPb SSAF filter | | | | | | | | 0 | Disabled | 0x0B |
| | | | | | | | | | | 1 | Enabled | |
| | | SD DAC Output 1 | | | | | | | 0 | | See Table 37 | |
| | | | | | | | | | 1 | | | |
| | | Reserved | | | | | | 0 | | | | |
| | | SD pedestal | | | | | 0 | | | | Disabled | |
| | | | | | | | 1 | | | | Enabled | |
| | | SD square pixel mode | | | | 0 | | | | | Disabled | |
| | | | | | | 1 | | | | | Enabled | |
| | | SD VCR FF/RW sync | | | 0 | | | | | | Disabled | |
| | | | | | 1 | | | | | | Enabled | |
| | | SD pixel data valid | | 0 | | | | | | | Disabled | |
| | | | | 1 | | | | | | | Enabled | |
| | | SD active video edge control | 0 | | | | | | | | Disabled | |
| | | | 1 | | | | | | | | Enabled | |
| 0x83 | SD Mode Register 3 | SD pedestal YPrPb output | | | | | | | | 0 | No pedestal on YPrPb | 0x04 |
| | | | | | | | | | | 1 | 7.5 IRE pedestal on YPrPb | |
| | | SD Output Levels Y | | | | | | | 0 | | Y = 700 mV/300 mV | |
| | | | | | | | | | 1 | | Y = 714 mV/286 mV | |
| | | SD Output Levels PrPb | | | | | 0 | 0 | | | 700 mV p-p (PAL), 1000 mV p-p (NTSC) | |
| | | | | | | | 0 | 1 | | | 700 mV p-p | |
| | | | | | | | 1 | 0 | | | 1000 mV p-p | |
| | | | | | | | 1 | 1 | | | 648 mV p-p | |
| | | SD vertical blanking interval (VBI) open | | | | 0 | | | | | Disabled | |
| | | | | | | 1 | | | | | Enabled | |
| | | SD closed captioning field control | | 0 | 0 | | | | | | Closed captioning disabled | |
| | | | | 0 | 1 | | | | | | Closed captioning on odd field only | |
| | | | | 1 | 0 | | | | | | Closed captioning on even field only | |
| | | | | 1 | 1 | | | | | | Closed captioning on both fields | |
| | | Reserved | 0 | | | | | | | | Reserved | |



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**Table 28. Register 0x84 to Register 0x87**

| SR7 to SR0 | Register | Bit Description | Bit Number 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Register Setting | Reset Value |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0x84 | SD Mode Register 4 | Reserved | | | | | | | | 0 | | 0x00 |
| | | SD SFL/SCR/TR mode select | | | | | | 0 | 0 | | Disabled. | |
| | | | | | | | | 1 | 1 | | SFL mode enabled. | |
| | | SD active video length | | | | | 0 | | | | 720 pixels. | |
| | | | | | | | 1 | | | | 710 (NTSC), 702 (PAL). | |
| | | SD chroma | | | | 0 | | | | | Chroma enabled. | |
| | | | | | | 1 | | | | | Chroma disabled. | |
| | | SD burst | | | 0 | | | | | | Enabled. | |
| | | | | | 1 | | | | | | Disabled. | |
| | | SD color bars | | 0 | | | | | | | Disabled. | |
| | | | | 1 | | | | | | | Enabled. | |
| | | SD luma/chroma swap | 0 | | | | | | | | DAC 2 = luma, DAC 3 = chroma. | |
| | | | 1 | | | | | | | | DAC 2 = chroma, DAC 3 = luma. | |
| 0x86 | SD Mode Register 5 | NTSC color subcarrier adjust (delay from the falling edge of output HSYNC pulse to the start of color burst) | | | | | | | 0 | 0 | 5.17 µs. | 0x02 |
| | | | | | | | | | 0 | 1 | 5.31 µs. | |
| | | | | | | | | | 1 | 0 | 5.59 µs (must be set for Macrovision compliance). | |
| | | | | | | | | | 1 | 1 | Reserved. | |
| | | Reserved | | | | | | 0 | | | | |
| | | SD EIA/CEA-861B synchronization compliance | | | | | 0 | | | | Disabled. | |
| | | | | | | | 1 | | | | Enabled. | |
| | | Reserved | | | 0 | 0 | | | | | | |
| | | SD horizontal/vertical counter mode[1] | | 0 | | | | | | | Update field/line counter. | |
| | | | | 1 | | | | | | | Field/line counter free running. | |
| | | SD RGB color swap[2] | 0 | | | | | | | | Normal. | |
| | | | 1 | | | | | | | | Color reversal enabled. | |
| 0x87 | SD Mode Register 6 | SD luma and color scale control | | | | | | | | 0 | Disabled. | 0x00 |
| | | | | | | | | | | 1 | Enabled. | |
| | | SD luma scale saturation | | | | | | | 0 | | Disabled. | |
| | | | | | | | | | 1 | | Enabled. | |
| | | SD hue adjust | | | | | | 0 | | | Disabled. | |
| | | | | | | | | 1 | | | Enabled. | |
| | | SD brightness | | | | | 0 | | | | Disabled. | |
| | | | | | | | 1 | | | | Enabled. | |
| | | SD luma SSAF gain | | | | 0 | | | | | Disabled. | |
| | | | | | | 1 | | | | | Enabled. | |
| | | SD input standard autodetection | | | 0 | | | | | | Disabled. | |
| | | | | | 1 | | | | | | Enabled. | |
| | | Reserved | | 0 | | | | | | | 0 must be written to this bit. | |
| | | SD RGB input enable[2] | 0 | | | | | | | | SD YCrCb input. | |
| | | | 1 | | | | | | | | SD RGB input. | |

[1] When set to 0, the horizontal/vertical counters automatically wrap around at the end of the line/field/frame of the selected standard. When set to 1, the horizontal/vertical counters are free running and wrap around when external sync signals indicate to do so.
[2] Available on the ADV7392/ADV7393 (40-pin devices) only.



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**Table 29. Register 0x88 to Register 0x89**

| SR7 to SR0 | Register | Bit Description | Bit Number 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Register Setting | Reset Value |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0x88 | SD Mode Register 7 | Reserved | | | | | | | | 0 | | 0x00 |
| | | SD noninterlaced mode | | | | | | | 0 | | Disabled. | |
| | | | | | | | | | 1 | | Enabled. | |
| | | SD double buffering | | | | | | 0 | | | Disabled. | |
| | | | | | | | | 1 | | | Enabled. | |
| | | SD input format | | | | 0 | 0 | | | | 8-bit YCbCr input. | |
| | | | | | | 0 | 1 | | | | 16-bit YCbCr input.[1] | |
| | | | | | | 1 | 0 | | | | 10-bit YCbCr/16-bit SD RGB input.[1] | |
| | | | | | | 1 | 1 | | | | Reserved. | |
| | | SD digital noise reduction | | | 0 | | | | | | Disabled. | |
| | | | | | 1 | | | | | | Enabled. | |
| | | SD gamma correction enable | | 0 | | | | | | | Disabled. | |
| | | | | 1 | | | | | | | Enabled. | |
| | | SD gamma correction curve select | 0 | | | | | | | | Gamma Correction Curve A. | |
| | | | 1 | | | | | | | | Gamma Correction Curve B. | |
| 0x89 | SD Mode Register 8 | SD undershoot limiter | | | | | | | 0 | 0 | Disabled. | 0x00 |
| | | | | | | | | | 0 | 1 | −11 IRE. | |
| | | | | | | | | | 1 | 0 | −6 IRE. | |
| | | | | | | | | | 1 | 1 | −1.5 IRE. | |
| | | Reserved | | | | | | 0 | | | 0 must be written to this bit. | |
| | | Reserved | | | | | 0 | | | | Reserved. | |
| | | SD chroma delay | | | 0 | 0 | | | | | Disabled. | |
| | | | | | 0 | 1 | | | | | 4 clock cycles. | |
| | | | | | 1 | 0 | | | | | 8 clock cycles. | |
| | | | | | 1 | 1 | | | | | Reserved. | |
| | | Reserved | 0 | 0 | | | | | | | 0 must be written to these bits. | |

[1] Available on the ADV7392/ADV7393 (40-pin devices) only.

**Table 30. Register 0x8A to Register 0x98**

| SR7 to SR0 | Register | Bit Description | Bit Number[1] 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Register Setting | Reset Value |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0x8A | SD Timing Register 0 | SD slave/master mode | | | | | | | | 0 | Slave mode. | 0x08 |
| | | | | | | | | | | 1 | Master mode. | |
| | | SD timing mode | | | | | | 0 | 0 | | Mode 0. | |
| | | | | | | | | 0 | 1 | | Mode 1. | |
| | | | | | | | | 1 | 0 | | Mode 2. | |
| | | | | | | | | 1 | 1 | | Mode 3. | |
| | | Reserved | | | | | 1 | | | | | |
| | | SD luma delay | | | 0 | 0 | | | | | No delay. | |
| | | | | | 0 | 1 | | | | | Two clock cycles. | |
| | | | | | 1 | 0 | | | | | Four clock cycles. | |
| | | | | | 1 | 1 | | | | | Six clock cycles. | |
| | | SD minimum luma value | | 0 | | | | | | | −40 IRE. | |
| | | | | 1 | | | | | | | −7.5 IRE. | |
| | | SD timing reset | x | | | | | | | | A low-high-low transition resets the internal SD timing counters. | |



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| SR7 to SR0 | Register | Bit Description | Bit Number[1] 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Register Setting | Reset Value |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0x8B | SD Timing Register 1 Note: Applicable in master modes only, that is, Subaddress 0x8A, Bit 0 = 1. | SD $\overline{HSYNC}$ width | | | | | | | 0 | 0 | $t_a$ = one clock cycle. | 0x00 |
| | | | | | | | | | 0 | 1 | $t_a$ = four clock cycles. | |
| | | | | | | | | | 1 | 0 | $t_a$ = 16 clock cycles. | |
| | | | | | | | | | 1 | 1 | $t_a$ = 128 clock cycles. | |
| | | SD $\overline{HSYNC}$ to $\overline{VSYNC}$ delay | | | | | 0 | 0 | | | $t_b$ = 0 clock cycles. | |
| | | | | | | | 0 | 1 | | | $t_b$ = four clock cycles. | |
| | | | | | | | 1 | 0 | | | $t_b$ = eight clock cycles. | |
| | | | | | | | 1 | 1 | | | $t_b$ = 18 clock cycles. | |
| | | SD $\overline{HSYNC}$ to $\overline{VSYNC}$ rising edge delay (Mode 1 only) | | | X[2] | 0 | | | | | $t_c = t_b$. | |
| | | | | | X[2] | 1 | | | | | $t_c = t_b$ + 32 µs. | |
| | | SD $\overline{VSYNC}$ width (Mode 2 only) | | | 0 | 0 | | | | | One clock cycle. | |
| | | | | | 0 | 1 | | | | | Four clock cycles. | |
| | | | | | 1 | 0 | | | | | 16 clock cycles. | |
| | | | | | 1 | 1 | | | | | 128 clock cycles. | |
| | | SD $\overline{HSYNC}$ to pixel data adjust | 0 | 0 | | | | | | | 0 clock cycles. | |
| | | | 0 | 1 | | | | | | | One clock cycle. | |
| | | | 1 | 0 | | | | | | | Two clock cycles. | |
| | | | 1 | 1 | | | | | | | Three clock cycles. | |
| 0x8C | SD $F_{SC}$ Register 0[3] | Subcarrier Frequency Bits[7:0] | x | x | x | x | x | x | x | x | Subcarrier Frequency Bits[7:0]. | 0x1F |
| 0x8D | SD $F_{SC}$ Register 1[3] | Subcarrier Frequency Bits[15:8] | x | x | x | x | x | x | x | x | Subcarrier Frequency Bits[15:8]. | 0x7C |
| 0x8E | SD $F_{SC}$ Register 2[3] | Subcarrier Frequency Bits[23:16] | x | x | x | x | x | x | x | x | Subcarrier Frequency Bits[23:16]. | 0xF0 |
| 0x8F | SD $F_{SC}$ Register 3[3] | Subcarrier Frequency Bits[31:24] | x | x | x | x | x | x | x | x | Subcarrier Frequency Bits[31:24]. | 0x21 |
| 0x90 | SD $F_{SC}$ Phase | Subcarrier Phase Bits[9:2] | x | x | x | x | x | x | x | x | Subcarrier Phase Bits[9:2]. | 0x00 |
| 0x91 | SD Closed Captioning | Extended data on even fields | x | x | x | x | x | x | x | x | Extended Data Bits[7:0]. | 0x00 |
| 0x92 | SD Closed Captioning | Extended data on even fields | x | x | x | x | x | x | x | x | Extended Data Bits[15:8]. | 0x00 |
| 0x93 | SD Closed Captioning | Data on odd fields | x | x | x | x | x | x | x | x | Data Bits[7:0]. | 0x00 |
| 0x94 | SD Closed Captioning | Data on odd fields | x | x | x | x | x | x | x | x | Data Bits[15:8]. | 0x00 |
| 0x95 | SD Pedestal Register 0 | Pedestal on odd fields | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | Setting any of these bits to 1 disables the pedestal on the line number indicated by the bit settings. | 0x00 |
| 0x96 | SD Pedestal Register 1 | Pedestal on odd fields | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | | 0x00 |
| 0x97 | SD Pedestal Register 2 | Pedestal on even fields | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | | 0x00 |
| 0x98 | SD Pedestal Register 3 | Pedestal on even fields | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | | 0x00 |

[1] x = Logic 0 or Logic 1.
[2] X = don't care.
[3] SD subcarrier frequency registers default to NTSC subcarrier frequency values.

**Table 31. Register 0x99 to Register 0xA5**

| SR7 to SR0 | Register | Bit Description | Bit Number[1] 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Register Setting | Reset Value |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0x99 | SD CGMS/WSS 0 | SD CGMS data | | | | | x | x | x | x | CGMS Data Bits[C19:C16] | 0x00 |
| | | SD CGMS CRC | | | | 0 | | | | | Disabled | |
| | | | | | | 1 | | | | | Enabled | |
| | | SD CGMS on odd fields | | | 0 | | | | | | Disabled | |
| | | | | | 1 | | | | | | Enabled | |
| | | SD CGMS on even fields | | 0 | | | | | | | Disabled | |
| | | | | 1 | | | | | | | Enabled | |
| | | SD WSS | 0 | | | | | | | | Disabled | |
| | | | 1 | | | | | | | | Enabled | |
| 0x9A | SD CGMS/WSS 1 | SD CGMS/WSS data | | | x | x | x | x | x | x | CGMS Data Bits[C13:C8] or WSS Data Bits[W13:W8] | 0x00 |



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| SR7 to SR0 | Register | Bit Description | Bit Number[1] 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Register Setting | Reset Value |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | SD CGMS data | x | x | | | | | | | CGMS Data Bits[C15:C14] | |
| 0x9B | SD CGMS/WSS 2 | SD CGMS/WSS data | x | x | x | x | x | x | x | x | CGMS Data Bits[C7:C0] or WSS Data Bits[W7:W0] | 0x00 |
| 0x9C | SD scale LSB | LSBs for SD Y scale value | | | | | | | x | x | SD Y Scale Bits[1:0] | 0x00 |
| | | LSBs for SD Cb scale value | | | | | x | x | | | SD Cb Scale Bits[1:0] | |
| | | LSBs for SD Cr scale value | | | x | x | | | | | SD Cr Scale Bits[1:0] | |
| | | LSBs for SD $F_{SC}$ phase | x | x | | | | | | | Subcarrier Phase Bits[1:0] | |
| 0x9D | SD Y scale | SD Y scale value | x | x | x | x | x | x | x | x | SD Y Scale Bits[9:2] | 0x00 |
| 0x9E | SD Cb scale | SD Cb scale value | x | x | x | x | x | x | x | x | SD Cb Scale Bits[9:2] | 0x00 |
| 0x9F | SD Cr scale | SD Cr scale value | x | x | x | x | x | x | x | x | SD Cr Scale Bits[9:2] | 0x00 |
| 0xA0 | SD hue adjust | SD hue adjust value | x | x | x | x | x | x | x | x | SD Hue Adjust Bits[7:0] | 0x00 |
| 0xA1 | SD brightness/WSS | SD brightness value | | x | x | x | x | x | x | x | SD Brightness Bits[6:0] | 0x00 |
| | | SD blank WSS data | 0 | | | | | | | | Disabled | |
| | | | 1 | | | | | | | | Enabled | |
| 0xA2 | SD luma SSAF | SD luma SSAF gain/attenuation (only applicable if Subaddress 0x87, Bit 4 = 1) | | | | | 0 | 0 | 0 | 0 | −4 dB | 0x00 |
| | | | | | | | … | … | … | … | … | |
| | | | | | | | 0 | 1 | 1 | 0 | 0 dB | |
| | | | | | | | … | … | … | … | … | |
| | | | | | | | 1 | 1 | 0 | 0 | +4 dB | |
| | | Reserved | 0 | 0 | 0 | 0 | | | | | | |
| 0xA3 | SD DNR 0 | Coring gain border (in DNR mode, the values in brackets apply) | | | | | 0 | 0 | 0 | 0 | No gain | 0x00 |
| | | | | | | | 0 | 0 | 0 | 1 | +1/16 [−1/8] | |
| | | | | | | | 0 | 0 | 1 | 0 | +2/16 [−2/8] | |
| | | | | | | | 0 | 0 | 1 | 1 | +3/16 [−3/8] | |
| | | | | | | | 0 | 1 | 0 | 0 | +4/16 [−4/8] | |
| | | | | | | | 0 | 1 | 0 | 1 | +5/16 [−5/8] | |
| | | | | | | | 0 | 1 | 1 | 0 | +6/16 [−6/8] | |
| | | | | | | | 0 | 1 | 1 | 1 | +7/16 [−7/8] | |
| | | | | | | | 1 | 0 | 0 | 0 | +8/16 [−1] | |
| | | Coring gain data (in DNR mode, the values in brackets apply) | 0 | 0 | 0 | 0 | | | | | No gain | |
| | | | 0 | 0 | 0 | 1 | | | | | +1/16 [−1/8] | |
| | | | 0 | 0 | 1 | 0 | | | | | +2/16 [−2/8] | |
| | | | 0 | 0 | 1 | 1 | | | | | +3/16 [−3/8] | |
| | | | 0 | 1 | 0 | 0 | | | | | +4/16 [−4/8] | |
| | | | 0 | 1 | 0 | 1 | | | | | +5/16 [−5/8] | |
| | | | 0 | 1 | 1 | 0 | | | | | +6/16 [−6/8] | |
| | | | 0 | 1 | 1 | 1 | | | | | +7/16 [−7/8] | |
| | | | 1 | 0 | 0 | 0 | | | | | +8/16 [−1] | |



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| SR7 to SR0 | Register | Bit Description | Bit Number[1] 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Register Setting | Reset Value |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0xA4 | SD DNR 1 | DNR threshold | | | 0<br>0<br>…<br>1<br>1 | 0<br>0<br>…<br>1<br>1 | 0<br>0<br>…<br>1<br>1 | 0<br>0<br>…<br>1<br>1 | 0<br>0<br>…<br>1<br>1 | 0<br>1<br>…<br>0<br>1 | 0<br>1<br>…<br>62<br>63 | 0x00 |
| | | Border area | | 0<br>1 | | | | | | | Two pixels<br>Four pixels | |
| | | Block size | 0<br>1 | | | | | | | | Eight pixels<br>16 pixels | |
| 0xA5 | SD DNR 2 | DNR input select | | | | | | 0<br>0<br>0<br>1 | 0<br>1<br>1<br>0 | 1<br>0<br>1<br>0 | Filter A<br>Filter B<br>Filter C<br>Filter D | 0x00 |
| | | DNR mode | | | | | 0<br>1 | | | | DNR mode<br>DNR sharpness mode | |
| | | DNR block offset | 0<br>0<br>…<br>1<br>1 | 0<br>0<br>…<br>1<br>1 | 0<br>0<br>…<br>1<br>1 | 0<br>1<br>…<br>0<br>1 | | | | | 0 pixel offset<br>One pixel offset<br>…<br>14 pixel offset<br>15 pixel offset | |

[1] x = Logic 0 or Logic 1.

**Table 32. Register 0xA6 to Register 0xBB**

| SR7 to SR0 | Register | Bit Description | Bit Number[1] 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Register Setting | Reset Value |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0xA6 | SD Gamma A0 | SD Gamma Curve A (Point 24) | x | x | x | x | x | x | x | x | A0 | 0x00 |
| 0xA7 | SD Gamma A1 | SD Gamma Curve A (Point 32) | x | x | x | x | x | x | x | x | A1 | 0x00 |
| 0xA8 | SD Gamma A2 | SD Gamma Curve A (Point 48) | x | x | x | x | x | x | x | x | A2 | 0x00 |
| 0xA9 | SD Gamma A3 | SD Gamma Curve A (Point 64) | x | x | x | x | x | x | x | x | A3 | 0x00 |
| 0xAA | SD Gamma A4 | SD Gamma Curve A (Point 80) | x | x | x | x | x | x | x | x | A4 | 0x00 |
| 0xAB | SD Gamma A5 | SD Gamma Curve A (Point 96) | x | x | x | x | x | x | x | x | A5 | 0x00 |
| 0xAC | SD Gamma A6 | SD Gamma Curve A (Point 128) | x | x | x | x | x | x | x | x | A6 | 0x00 |
| 0xAD | SD Gamma A7 | SD Gamma Curve A (Point 160) | x | x | x | x | x | x | x | x | A7 | 0x00 |
| 0xAE | SD Gamma A8 | SD Gamma Curve A (Point 192) | x | x | x | x | x | x | x | x | A8 | 0x00 |
| 0xAF | SD Gamma A9 | SD Gamma Curve A (Point 224) | x | x | x | x | x | x | x | x | A9 | 0x00 |
| 0xB0 | SD Gamma B0 | SD Gamma Curve B (Point 24) | x | x | x | x | x | x | x | x | B0 | 0x00 |
| 0xB1 | SD Gamma B1 | SD Gamma Curve B (Point 32) | x | x | x | x | x | x | x | x | B1 | 0x00 |
| 0xB2 | SD Gamma B2 | SD Gamma Curve B (Point 48) | x | x | x | x | x | x | x | x | B2 | 0x00 |
| 0xB3 | SD Gamma B3 | SD Gamma Curve B (Point 64) | x | x | x | x | x | x | x | x | B3 | 0x00 |
| 0xB4 | SD Gamma B4 | SD Gamma Curve B (Point 80) | x | x | x | x | x | x | x | x | B4 | 0x00 |
| 0xB5 | SD Gamma B5 | SD Gamma Curve B (Point 96) | x | x | x | x | x | x | x | x | B5 | 0x00 |
| 0xB6 | SD Gamma B6 | SD Gamma Curve B (Point 128) | x | x | x | x | x | x | x | x | B6 | 0x00 |
| 0xB7 | SD Gamma B7 | SD Gamma Curve B (Point 160) | x | x | x | x | x | x | x | x | B7 | 0x00 |
| 0xB8 | SD Gamma B8 | SD Gamma Curve B (Point 192) | x | x | x | x | x | x | x | x | B8 | 0x00 |
| 0xB9 | SD Gamma B9 | SD Gamma Curve B (Point 224) | x | x | x | x | x | x | x | x | B9 | 0x00 |
| 0xBA | SD brightness detect | SD brightness value | x | x | x | x | x | x | x | x | Read only | 0xXX |



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| SR7 to SR0 | Register | Bit Description | Bit Number[1] 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Register Setting | Reset Value |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0xBB | Field count | Field count | | | | | | x | x | x | Read only | 0x0X |
| | | Reserved | | | 0 | 0 | 0 | | | | Reserved | |
| | | Encoder version code | 0 | 0 | | | | | | | Read only; first encoder version[2] | |
| | | | 0 | 1 | | | | | | | Read only; second encoder version | |

[1] x = Logic 0 or Logic 1.
[2] See the HD Interlace External $\overline{\text{HSYNC}}$ and $\overline{\text{VSYNC}}$ Considerations section for information about the first encoder version.

**Table 33. Register 0xC9 to Register 0xCE**

| SR7 to SR0 | Register | Bit Description | Bit Number 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Register Setting | Reset Value |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0xC9 | Teletext control | Teletext enable | | | | | | | | 0 | Disabled. | 0x00 |
| | | | | | | | | | | 1 | Enabled. | |
| | | Teletext request mode | | | | | | | 0 | | Line request signal. | |
| | | | | | | | | | 1 | | Bit request signal. | |
| | | Teletext input pin select[1] | | | | | | 0 | | | $\overline{\text{VSYNC}}$. | |
| | | | | | | | | 1 | | | P0. | |
| | | Reserved | 0 | 0 | 0 | 0 | 0 | | | | Reserved. | |
| 0xCA | Teletext request control | Teletext request falling edge position control | | | | | 0 | 0 | 0 | 0 | 0 clock cycles. | 0x00 |
| | | | | | | | 0 | 0 | 0 | 1 | One clock cycle. | |
| | | | | | | | … | … | … | … | … | |
| | | | | | | | 1 | 1 | 1 | 0 | 14 clock cycles. | |
| | | | | | | | 1 | 1 | 1 | 1 | 15 clock cycles. | |
| | | Teletext request rising edge position control | 0 | 0 | 0 | 0 | | | | | 0 clock cycles. | |
| | | | 0 | 0 | 0 | 1 | | | | | One clock cycle. | |
| | | | … | … | … | … | | | | | … | |
| | | | 1 | 1 | 1 | 0 | | | | | 14 clock cycles. | |
| | | | 1 | 1 | 1 | 1 | | | | | 15 clock cycles. | |
| 0xCB | TTX Line Enable 0 | Teletext on odd fields | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | Setting any of these bits to 1 enables teletext on the line number indicated by the bit settings. | 0x00 |
| 0xCC | TTX Line Enable 1 | Teletext on odd fields | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | | 0x00 |
| 0xCD | TTX Line Enable 2 | Teletext on even fields | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | | 0x00 |
| 0xCE | TTX Line Enable 3 | Teletext on even fields | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | | 0x00 |

[1] The use of P0 as the teletext input pin is available on the ADV7392/ADV7393 (40-pin devices) only.



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**Table 34. Register 0xE0 to Register 0xF1**

| SR7 to SR0 | Register[2] | Bit Description | Bit Number[1] | | | | | | | | Register Setting | Reset Value |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | |
| 0xE0 | Macrovision | MV control bits | x | x | x | x | x | x | x | x | | 0x00 |
| 0xE1 | Macrovision | MV control bits | x | x | x | x | x | x | x | x | | 0x00 |
| 0xE2 | Macrovision | MV control bits | x | x | x | x | x | x | x | x | | 0x00 |
| 0xE3 | Macrovision | MV control bits | x | x | x | x | x | x | x | x | | 0x00 |
| 0xE4 | Macrovision | MV control bits | x | x | x | x | x | x | x | x | | 0x00 |
| 0xE5 | Macrovision | MV control bits | x | x | x | x | x | x | x | x | | 0x00 |
| 0xE6 | Macrovision | MV control bits | x | x | x | x | x | x | x | x | | 0x00 |
| 0xE7 | Macrovision | MV control bits | x | x | x | x | x | x | x | x | | 0x00 |
| 0xE8 | Macrovision | MV control bits | x | x | x | x | x | x | x | x | | 0x00 |
| 0xE9 | Macrovision | MV control bits | x | x | x | x | x | x | x | x | | 0x00 |
| 0xEA | Macrovision | MV control bits | x | x | x | x | x | x | x | x | | 0x00 |
| 0xEB | Macrovision | MV control bits | x | x | x | x | x | x | x | x | | 0x00 |
| 0xEC | Macrovision | MV control bits | x | x | x | x | x | x | x | x | | 0x00 |
| 0xED | Macrovision | MV control bits | x | x | x | x | x | x | x | x | | 0x00 |
| 0xEE | Macrovision | MV control bits | x | x | x | x | x | x | x | x | | 0x00 |
| 0xEF | Macrovision | MV control bits | x | x | x | x | x | x | x | x | | 0x00 |
| 0xF0 | Macrovision | MV control bits | x | x | x | x | x | x | x | x | | 0x00 |
| 0xF1 | Macrovision | MV control bits | 0 | 0 | 0 | 0 | 0 | 0 | 0 | x | Bits[7:1] must be 0. | 0x00 |

[1] x = Logic 0 or Logic 1.
[2] Macrovision registers are available on the ADV7390 and the ADV7392 only.



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# ADV7390/ADV7391 INPUT CONFIGURATION

The ADV7390/ADV7391 support a number of different input modes. The desired input mode is selected using Subaddress 0x01, Bits[6:4]. The ADV7390/ADV7391 default to standard definition (SD) mode on power-up. Table 35 provides an overview of all possible input configurations. Each input mode is described in detail in this section. Note that the WLCSP option is only configured to support SD as shown in Figure 51.

**Table 35. ADV7390/ADV7391 Input Configuration**

| Input Mode | | P7 | P6 | P5 | P4 | P3 | P2 | P1 | P0 |
|---|---|---|---|---|---|---|---|---|---|
| 000 | SD | YCrCb | | | | | | | |
| 010 | ED/HD-DDR | YCrCb | | | | | | | |
| 111 | ED (at 54 MHz) | YCrCb | | | | | | | |

## STANDARD DEFINITION

### *Subaddress 0x01, Bits[6:4] = 000*

SD YCrCb data can be input in an interleaved 4:2:2 format over an 8-bit bus rate of 27 MHz. A 27 MHz clock signal must be provided on the CLKIN pin. If required, external synchronization signals can be provided on the $\overline{\text{HSYNC}}$ and $\overline{\text{VSYNC}}$ pins.

Embedded EAV/SAV timing codes are also supported. The ITU-R BT.601/656 input standard is supported. The interleaved pixel data is input on Pin P7 to Pin P0, with Pin P0 being the LSB.

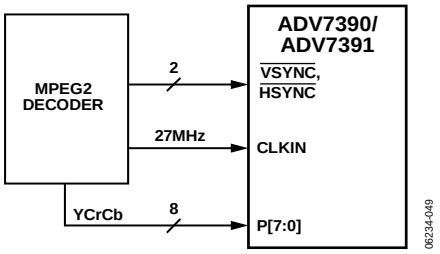


*Figure 51. SD Example Application*

## ENHANCED DEFINITION/HIGH DEFINITION

### *Subaddress 0x01, Bits[6:4] = 010*

Enhanced definition (ED) or high definition (HD) YCrCb data can be input in an interleaved 4:2:2 format over an 8-bit DDR bus. The clock signal must be provided on the CLKIN pin. If required, external synchronization signals can be provided on the $\overline{\text{HSYNC}}$ and $\overline{\text{VSYNC}}$ pins. Embedded EAV/SAV timing codes are also supported.

### *8-Bit 4:2:2 ED/HD YCrCb Mode (DDR)*

In 8-bit DDR 4:2:2 YCrCb input mode, the Y pixel data is input on Pin P7 to Pin P0 on either the rising or falling edge of CLKIN. Pin P0 is the LSB.

The CrCb pixel data is also input on Pin P7 to Pin P0 on the opposite edge of CLKIN. Pin P0 is the LSB.

Whether the Y data is clocked in on the rising or falling edge of CLKIN is determined by Subaddress 0x01, Bits[2:1] (see Figure 52 and Figure 53).

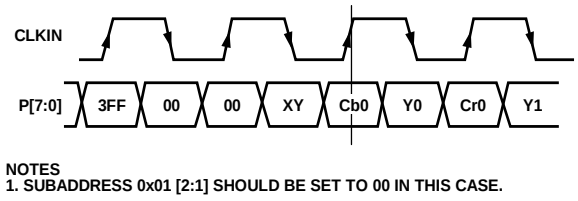


*Figure 52. ED/HD-DDR Input Sequence (EAV/SAV)—Option A*

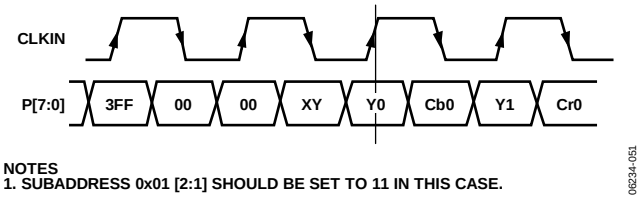


*Figure 53. ED/HD-DDR Input Sequence (EAV/SAV)—Option B*

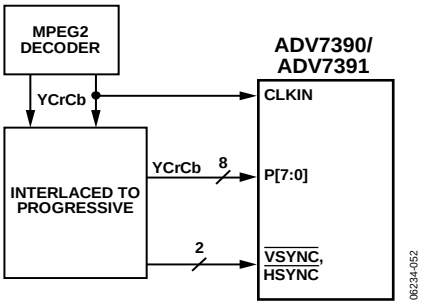


*Figure 54. ED/HD-DDR Example Application*

## ENHANCED DEFINITION (AT 54 MHz)

### *Subaddress 0x01, Bits[6:4] = 111*

ED YCrCb data can be input in an interleaved 4:2:2 format over an 8-bit bus rate of 54 MHz.

A 54 MHz clock signal must be provided on the CLKIN pin. Embedded EAV/SAV timing codes are supported. External synchronization signals are not supported in this mode.

The interleaved pixel data is input on Pin P7 to Pin P0, with Pin P0 being the LSB.

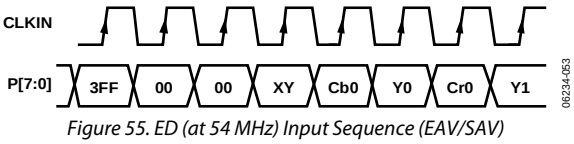


*Figure 55. ED (at 54 MHz) Input Sequence (EAV/SAV)*



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# ADV7392/ADV7393 INPUT CONFIGURATION

The ADV7392/ADV7393 support a number of different input modes. The desired input mode is selected using Subaddress 0x01, Bits[6:4]. The ADV7392/ADV7393 default to standard definition (SD) mode on power-up. Table 36 provides an overview of all possible input configurations. Each input mode is described in detail in this section.

## STANDARD DEFINITION

### *Subaddress 0x01, Bits[6:4] = 000*

Standard definition YCrCb data can be input in 4:2:2 format over an 8-, 10-, or 16-bit bus. SD RGB data can be input in 4:4:4 format over a 16-bit bus.

A 27 MHz clock signal must be provided on the CLKIN pin. If required, external synchronization signals can be provided on the $\overline{\text{HSYNC}}$ and $\overline{\text{VSYNC}}$ pins. Embedded EAV/SAV timing codes are also supported in 8-bit and 10-bit modes.

### *8-Bit 4:2:2 YCrCb Mode*

**Subaddress 0x87, Bit 7 = 0;**
**Subaddress 0x88, Bits[4:3] = 00**

In 8-bit 4:2:2 YCrCb input mode, the interleaved pixel data is input on Pin P15 to Pin P8, with Pin P8 being the LSB. The ITU-R BT.601/656 input standard is supported.

### *10-Bit 4:2:2 YCrCb Mode*

**Subaddress 0x87, Bit 7 = 0;**
**Subaddress 0x88, Bits[4:3] = 10**

In 10-bit 4:2:2 YCrCb input mode, the interleaved pixel data is input on Pin P15 to Pin P6, with Pin P6 being the LSB. The ITU-R BT.601/656 input standard is supported.

### *16-Bit 4:2:2 YCrCb Mode*

**Subaddress 0x87, Bit 7 = 0;**
**Subaddress 0x88, Bits[4:3] = 01**

In 16-bit 4:2:2 YCrCb input mode, the Y pixel data is input on Pin P15 to Pin P8, with Pin P8 being the LSB.

The CrCb pixel data is input on Pin P7 to Pin P0, with Pin P0 being the LSB.

The pixel data is updated at half the rate of the clock, that is, at a rate of 13.5 MHz (see Figure 5).

### *16-Bit 4:4:4 RGB Mode*

Embedded EAV/SAV timing codes are not supported with SD RGB mode. Also, master timing mode is not supported for SD RGB input mode, therefore, external synchronization must be used.

**Subaddress 0x87, Bit 7 = 1**

In 16-bit 4:4:4 RGB input mode, the red pixel data is input on Pin P4 to Pin P0, the green pixel data is input on Pin P10 to Pin P5, and the blue pixel data is input on Pin P15 to Pin P11. The P0, P5, and P11 pins are the respective bus LSBs.

The pixel data is updated at half the rate of the clock, that is, at a rate of 13.5 MHz (see Figure 6).

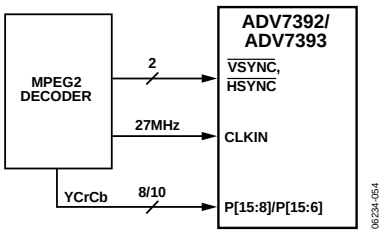


*Figure 56. SD Example Application*

**Table 36. ADV7392/ADV7393 Input Configuration**

| Input Mode[1] | | P15 | P14 | P13 | P12 | P11 | P10 | P9 | P8 | P7 | P6 | P5 | P4 | P3 | P2 | P1 | P0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 000 | SD[2] | **SD RGB input enable (0x87[7]) = 0** | | | | | | | | | | | | | | | |
| | 8-bit | YCrCb | | | | | | | | | | | | | | | |
| | 10-bit | YCrCb | | | | | | | | | | | | | | | |
| | 16-bit[3] | Y | | | | | | | | CrCb | | | | | | | |
| | | **SD RGB input enable (0x87[7]) = 1** | | | | | | | | | | | | | | | |
| | 16-bit[3] | B | | | | | | G | | | | | R | | | | |
| 001 | ED/HD-SDR (16-bit) | Y | | | | | | | | CrCb | | | | | | | |
| 010 | ED/HD-DDR[4] | **ED/HD input format (0x33[2]) = 0** | | | | | | | | | | | | | | | |
| | 8-bit | YCrCb | | | | | | | | | | | | | | | |
| | | **ED/HD input format (0x33[2]) = 1** | | | | | | | | | | | | | | | |
| | 10-bit | YCrCb | | | | | | | | | | | | | | | |
| 111 | ED (at 54 MHz) | **ED/HD input format (0x33[2]) = 0** | | | | | | | | | | | | | | | |
| | 8-bit | YCrCb | | | | | | | | | | | | | | | |
| | | **ED/HD input format (0x33[2]) = 1** | | | | | | | | | | | | | | | |
| | 10-bit | YCrCb | | | | | | | | | | | | | | | |

[1] The input mode is determined by Subaddress 0x01, Bits[6:4].
[2] In SD mode, the width of the input data is determined by Subaddress 0x88, Bits[4:3].
[3] External synchronization signals must be used in this input mode. Embedded EAV/SAV timing codes are not supported.
[4] ED = enhanced definition = 525p and 625p.



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## ENHANCED DEFINITION/HIGH DEFINITION

### *Subaddress 0x01, Bits[6:4] = 001 or 010*

ED or HD YCrCb data can be input in a 4:2:2 format over an 8-/10-bit DDR bus or a 16-bit SDR bus.

The clock signal must be provided on the CLKIN pin. If required, external synchronization signals can be provided on the HSYNC and VSYNC pins. Embedded EAV/SAV timing codes are also supported.

### *16-Bit 4:2:2 YCrCb Mode (SDR)*

In 16-bit 4:2:2 YCrCb input mode, the Y pixel data is input on Pin P15 to Pin P8, with P8 being the LSB.

The CrCb pixel data is input on Pin P7 to Pin P0, with Pin P0 being the LSB.

### *8-/10-Bit 4:2:2 YCrCb Mode (DDR)*

In 8-/10-bit DDR 4:2:2 YCrCb input mode, the Y pixel data is input on Pin P15 to Pin P8/P6 on either the rising or falling edge of CLKIN. Pin P8/P6 is the LSB.

The CrCb pixel data is also input on Pin P15 to Pin P8/P6 on the opposite edge of CLKIN. P8/P6 is the LSB.

The 10-bit mode is enabled using Subaddress 0x33, Bit 2. Whether the Y data is clocked in on the rising or falling edge of CLKIN is determined by Subaddress 0x01, Bits[2:1] (see Figure 57 and Figure 58).

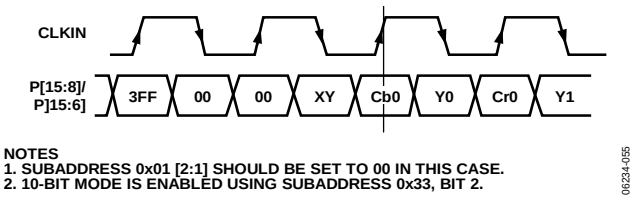


*Figure 57. ED/HD-DDR Input Sequence (EAV/SAV)—Option A*

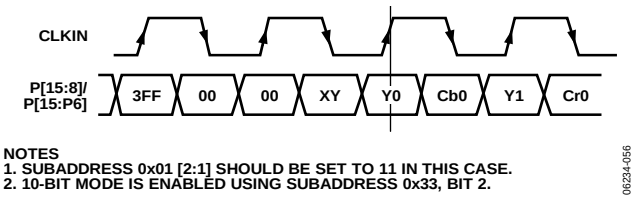


*Figure 58. ED/HD-DDR Input Sequence (EAV/SAV)—Option B*

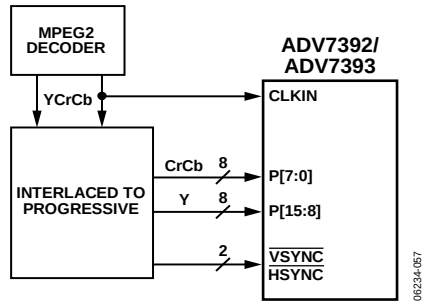


*Figure 59. ED/HD-SDR Example Application*

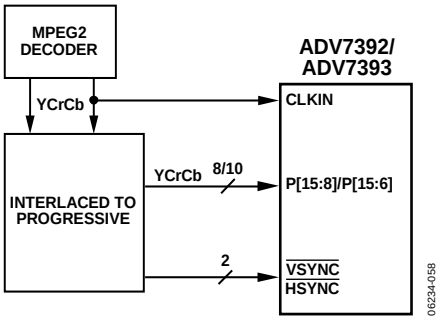


*Figure 60. ED/HD-DDR Example Application*

## ENHANCED DEFINITION (AT 54 MHz)

### *Subaddress 0x01, Bits[6:4] = 111*

ED YCrCb data can be input in an interleaved 4:2:2 format on an 8-/10-bit bus at a rate of 54 MHz.

A 54 MHz clock signal must be provided on the CLKIN pin. Embedded EAV/SAV timing codes are supported. External synchronization signals are not supported in this mode.

The interleaved pixel data is input on Pin P15 to Pin P8/P6, with Pin P8/P6 being the LSB.

The 10-bit mode is enabled using Subaddress 0x33, Bit 2.

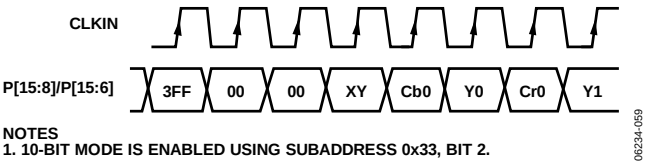


*Figure 61. ED (at 54 MHz) Input Sequence (EAV/SAV)*

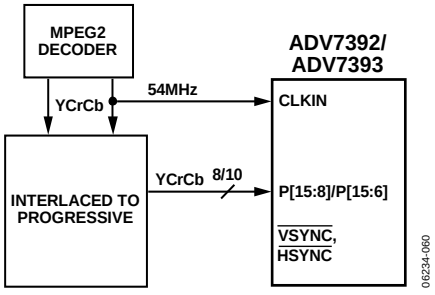


*Figure 62 ED (at 54 MHz) Example Application*



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# OUTPUT CONFIGURATION

The ADV7390/ADV7391/ADV7392/ADV7393 support a number of different output configurations. Table 37 to Table 39 list all possible output configurations.

**Table 37. SD Output Configurations**

| RGB/YPrPb Output Select[1] (Subaddress 0x02, Bit 5) | SD DAC Output 1 (Subaddress 0x82, Bit 1) | SD Luma/Chroma Swap (Subaddress 0x84, Bit 7) | DAC 1 | DAC 2 | DAC 3 |
|---|---|---|---|---|---|
| 0 | 0 | 0 | G | B | R |
| 1 | 0 | 0 | Y | Pb | Pr |
| 1 | 1 | 0 | CVBS | Luma | Chroma |
| 1 | 1 | 1 | CVBS | Chroma | Luma |

[1] If SD RGB output is selected, a color reversal is possible using Subaddress 0x86, Bit 7.

**Table 38. ED/HD Output Configurations**

| RGB/YPrPb Output Select (Subaddress 0x02, Bit 5) | ED/HD Color DAC Swap (Subaddress 0x35, Bit 3) | DAC 1 | DAC 2 | DAC 3 |
|---|---|---|---|---|
| 0 | 0 | G | B | R |
| 0 | 1 | G | R | B |
| 1 | 0 | Y | Pb | Pr |
| 1 | 1 | Y | Pr | Pb |

**Table 39. ED (at 54 MHz) Output Configurations**

| RGB/YPrPb Output Select (Subaddress 0x02, Bit 5) | ED/HD Color DAC Swap (Subaddress 0x35, Bit 3) | DAC 1 | DAC 2 | DAC 3 |
|---|---|---|---|---|
| 0 | 0 | G | B | R |
| 0 | 1 | G | R | B |
| 1 | 0 | Y | Pb | Pr |
| 1 | 1 | Y | Pr | Pb |



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# DESIGN FEATURES

## OUTPUT OVERSAMPLING

The ADV7390/ADV7391/ADV7392/ADV7393 include an on-chip phase-locked loop (PLL) that allows for oversampling of SD, ED, and HD video data. By default, the PLL is disabled. The PLL can be enabled using Subaddress 0x00, Bit 1 = 0.

Table 40 shows the various oversampling rates supported in the ADV7390/ADV7391/ADV7392/ADV7393.

### *External Sync Polarity*

For SD and ED/HD modes, the ADV7390/ADV7391/ADV7392/ADV7393 parts typically expect HS and VS to be low during their respective blanking periods. However, when the CEA861 compliance bit is enabled (0x39, Bit 5 for ED/HD modes and 0x86, Bit 3 for SD modes), the part expects the HS or VS to be active low or high depending on the input format selected (0x30, Bits[7:3]).

If a different polarity other than the default is required for ED/HD modes, 0x3A, Bits[2:0] can be used to invert PHSYNCB, PVSYNCB or PBLANKB individually regardless of whether CEA-861-B mode is enabled. It is not possible to invert S_HSYNC or S_VSYNC.

**Table 40. Output Oversampling Modes and Rates**

| Input Mode (0x01, Bits[6:4]) | | PLL and Oversampling Control (0x00, Bit 1) | SD/ED Oversample Rate Select (0x0D, Bit 3)[1] | HD Oversample Rate Select (0x31, Bit 1)[1] | Oversampling Mode and Rate |
|---|---|---|---|---|---|
| 000 | SD | 1 | X | X | SD (2×) |
| 000 | SD | 0 | 1 | X | SD (8×) |
| 000 | SD | 0 | 0 | X | SD (16×) |
| 001/010 | ED | 1 | X | X | ED (1×) |
| 001/010 | ED | 0 | 1 | X | ED (4×) |
| 001/010 | ED | 0 | 0 | X | ED (8×) |
| 001/010 | HD | 1 | X | X | HD (1×) |
| 001/010 | HD | 0 | X | 1 | HD (2×) |
| 001/010 | HD | 0 | X | 0 | HD (4×) |
| 111 | ED (at 54 MHz) | 1 | X | X | ED (at 54 MHz) (1×) |
| 111 | ED (at 54 MHz) | 0 | 1 | X | ED (at 54 MHz) (4×) |
| 111 | ED (at 54 MHz) | 0 | 0 | X | ED (at 54 MHz) (8×) |

[1] X = don't care



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## HD INTERLACE EXTERNAL HSYNC AND VSYNC CONSIDERATIONS

If the encoder revision code (Subaddress 0xBB, Bits[7:6]) = 01 or higher, the user should set Subaddress 0x02, Bit 1 to high. To ensure correct timing in HD interlace modes when using HSYNC and VSYNC synchronization signals. If this bit is set to low, the first active pixel on each line is masked in HD interlace modes and the Pr and Pb outputs are swapped when using the YCrCb 4:2:2 input format. Setting Subaddress 0x02, Bit 1 to low causes the encoder to behave in the same way as the first version of silicon (that is, this setting is backward compatible).

If the encoder revision code (Subaddress 0xBB, Bits[7:6]) = 00, the setting of Subaddress 0x02, Bit 1 has no effect. In this version of the encoder, the first active pixel is masked and the Pr and Pb outputs are swapped when using YCrCb 4:2:2 input format. To avoid these limitations, use the newer revision of silicon or use a different type of synchronization.

These considerations apply only to the HD interlace modes with external HSYNC and VSYNC synchronization (EAV/SAV mode is not affected and always has correct timing).

There is no negative effect in setting Subaddress 0x02, Bit 0 to high, and this bit can remain high for all the other video standards.

## ED/HD TIMING RESET

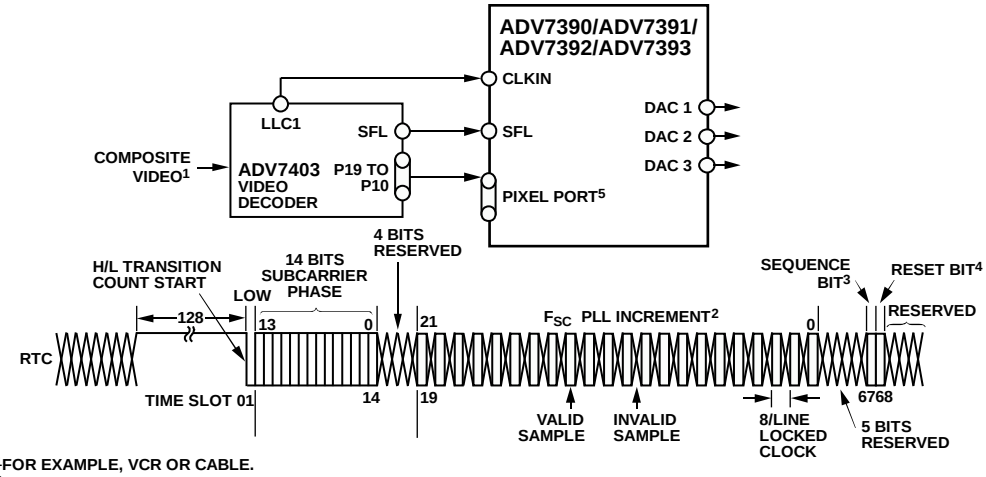
### *Subaddress 0x34, Bit 0*

An ED/HD timing reset is achieved by setting the ED/HD timing reset control bit (Subaddress 0x34, Bit 0) to 1. In this state, the horizontal and vertical counters remain reset. When this bit is set back to 0, the internal counters resume counting. This timing reset applies to the ED/HD timing counters only.

## SD SUBCARRIER FREQUENCY LOCK

### *Subcarrier Frequency Lock (SFL) Mode*

In subcarrier frequency lock (SFL) mode (Subaddress 0x84, Bits[2:1] = 11), the ADV7390/ADV7391/ADV7392/ADV7393 can be used to lock to an external video source. The SFL mode allows the ADV7390/ADV7391/ADV7392/ADV7393 to automatically alter the subcarrier frequency to compensate for line length variations. When the part is connected to a device such as an ADV7403 video decoder that outputs a digital data stream in the SFL format, the part automatically changes to the compensated subcarrier frequency on a line-by-line basis (see Figure 63). This digital data stream is 67 bits wide, and the subcarrier is contained in Bit 0 to Bit 21. Each bit is two clock cycles long.




1FOR EXAMPLE, VCR OR CABLE.
2$F_{SC}$ PLL INCREMENT IS 22 BITS LONG. VALUE LOADED INTO ADV7390/ADV7391/ADV7392/ADV7393 $F_{SC}$ DDS REGISTER IS $F_{SC}$ PLL INCREMENTS BITS[21:0] PLUS BITS[0:9] OF SUBCARRIER FREQUENCY REGISTERS.
3SEQUENCE BIT
PAL: 0 = LINE NORMAL, 1 = LINE INVERTED
NTSC: 0 = NO CHANGE
4RESET ADV7390/ADV7391/ADV7392/ADV7393 DDS.
5REFER TO THE ADV7390/ADV7391 AND ADV7392/ADV7393 INPUT CONFIGUR ATION TABLES FOR PIXEL DATA PIN ASSIGNMENTS.

06234-064

*Figure 63. SD Subcarrier Frequency Lock Timing and Connections Diagram (Subaddress 0x84, Bits [2:1] = 11)*



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## SD VCR FF/RW SYNC

### Subaddress 0x82, Bit 5

In DVD record applications where the encoder is used with a decoder, the VCR FF/RW sync control bit can be used for non-standard input video, that is, in fast forward or rewind modes.

In fast forward mode, the sync information at the start of a new field in the incoming video usually occurs before the correct number of lines/fields is reached. In rewind mode, this sync signal usually occurs after the total number of lines/fields is reached. Conventionally, this means that the output video has corrupted field signals because one signal is generated by the incoming video and another is generated when the internal line/field counters reach the end of a field.

When the VCR FF/RW sync control is enabled (Subaddress 0x82, Bit 5), the line/field counters are updated according to the incoming $\overline{\text{VSYNC}}$ signal and when the analog output matches the incoming $\overline{\text{VSYNC}}$ signal. This control is available in all slave-timing modes except Slave Mode 0.

## VERTICAL BLANKING INTERVAL

### Subaddress 0x31, Bit 4; Subaddress 0x83, Bit 4

The ADV7390/ADV7391/ADV7392/ADV7393 are able to accept input data that contains vertical blanking interval (VBI) data (such as CGMS, WSS, VITS) in SD, ED, and HD modes.

If VBI is disabled (Subaddress 0x31, Bit 4 for ED/HD; Subaddress 0x83, Bit 4 for SD), VBI data is not present at the output and the entire VBI is blanked. These control bits are valid in all master and slave timing modes.

For the SMPTE 293M (525p) standard, VBI data can be inserted on Line 13 to Line 42 of each frame or on Line 6 to Line 43 for the ITU-R BT.1358 (625p) standard. VBI data can be present on Line 10 to Line 20 for NTSC and on Line 7 to Line 22 for PAL.

In SD Timing Mode 0 (slave option), if VBI is enabled, the blanking bit in the EAV/SAV code is overwritten. It is possible to use VBI in this timing mode as well.

If CGMS is enabled and VBI is disabled, the CGMS data is, nevertheless, available at the output.

## SD SUBCARRIER FREQUENCY CONTROL

### Subaddress 0x8C to Subaddress 0x8F

The ADV7390/ADV7391/ADV7392/ADV7393 are able to generate the color subcarrier used in CVBS and S-Video (Y-C) outputs from the input pixel clock. Four 8-bit registers are used to set up the subcarrier frequency. The value of these registers is calculated using the following equation:

$$Subcarrier\ Frequency\ Register = \frac{Number\ of\ subcarrier\ periods\ in\ one\ video\ line}{Number\ of\ 27\ MHz\ clock\ cycles\ in\ one\ video\ line} \times 2^{32}$$

where the sum is rounded to the nearest integer.

For example, in NTSC mode:

$$Subcarrier\ Register\ Value = \left(\frac{227.5}{1716}\right) \times 2^{32} = 569408543$$

where:
*Subcarrier Register Value* = 569408543d = 0×21F07C1F
SD $F_{SC}$ Register 0: 0x1F
SD $F_{SC}$ Register 1: 0x7C
SD $F_{SC}$ Register 2: 0xF0
SD $F_{SC}$ Register 3: 0x21

### Programming the $F_{SC}$

The subcarrier frequency register value is divided into four $F_{SC}$ registers as shown in the previous example. The four subcarrier frequency registers must be updated sequentially, starting with Subcarrier Frequency Register 0 and ending with Subcarrier Frequency Register 3. The subcarrier frequency updates only after the last subcarrier frequency register byte is received by the ADV7390/ADV7391/ADV7392/ADV7393. The SD input standard autodetection feature must be disabled.

### Typical $F_{SC}$ Values

Table 41 outlines the values that should be written to the subcarrier frequency registers for NTSC and PAL B/D/G/H/I.

**Table 41. Typical $F_{SC}$ Values**

| Subaddress | Description | NTSC | PAL B/D/G/H/I |
|---|---|---|---|
| 0x8C | $F_{SC}0$ | 0x1F | 0xCB |
| 0x8D | $F_{SC}1$ | 0x7C | 0x8A |
| 0x8E | $F_{SC}2$ | 0xF0 | 0x09 |
| 0x8F | $F_{SC}3$ | 0x21 | 0x2A |

## SD NONINTERLACED MODE

### Subaddress 0x88, Bit 1

The ADV7390/ADV7391/ADV7392/ADV7393 support an SD noninterlaced mode. Using this mode, progressive inputs at twice the frame rate of NTSC and PAL (240p/59.94 Hz and 288p/50 Hz, respectively) can be input into the ADV7390/ADV7391/ADV7392/ADV7393. The SD noninterlaced mode can be enabled using Subaddress 0x88, Bit 1.

A 27 MHz clock signal must be provided on the CLKIN pin. Embedded EAV/SAV timing codes or external horizontal and vertical synchronization signals provided on the $\overline{\text{HSYNC}}$ and $\overline{\text{VSYNC}}$ pins can be used to synchronize the input pixel data.

All input configurations, output configurations, and features available in NTSC and PAL modes are available in SD noninterlaced mode. For 240p/59.94 Hz input, the ADV7390/ADV7391/ADV7392/ADV7393 should be configured for NTSC operation and Subaddress 0x88, Bit 1 should be set to 1.

For 288p/50 Hz input, the ADV7390/ADV7391/ADV7392/ADV7393 should be configured for PAL operation and Subaddress 0x88, Bit 1 should be set to 1.



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## SD SQUARE PIXEL MODE

### *Subaddress 0x82, Bit 4*

The ADV7390/ADV7391/ADV7392/ADV7393 support an SD square pixel mode (Subaddress 0x82, Bit 4). For NTSC operation, an input clock of 24.5454 MHz is required. The active resolution is 640 × 480. For PAL operation, an input clock of 29.5 MHz is required. The active resolution is 768 × 576.

For CVBS and S-Video (Y-C) outputs, the SD subcarrier frequency registers must be updated to reflect the input clock frequency used in SD square pixel mode. The SD input standard autodetection feature must be disabled in SD square pixel mode. In square pixel mode, the timing diagrams shown in Figure 64 and Figure 65 apply.

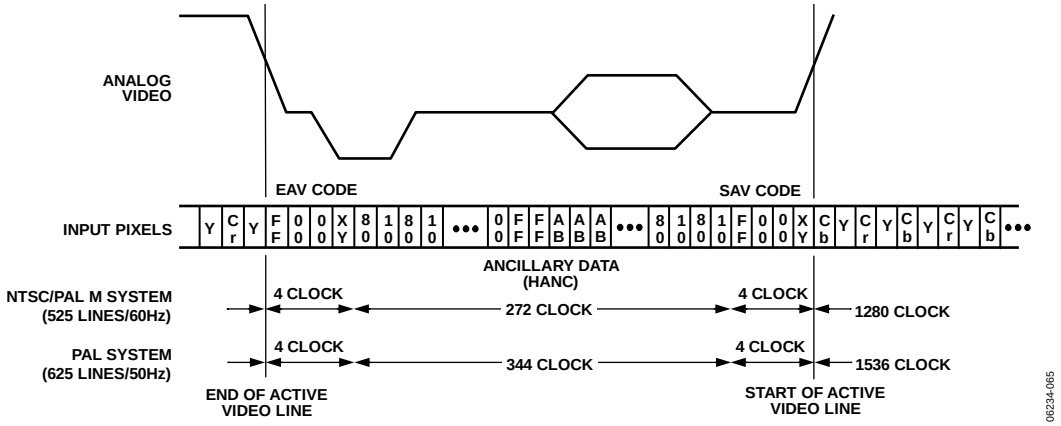


*Figure 64. Square Pixel Mode EAV/SAV Embedded Timing*

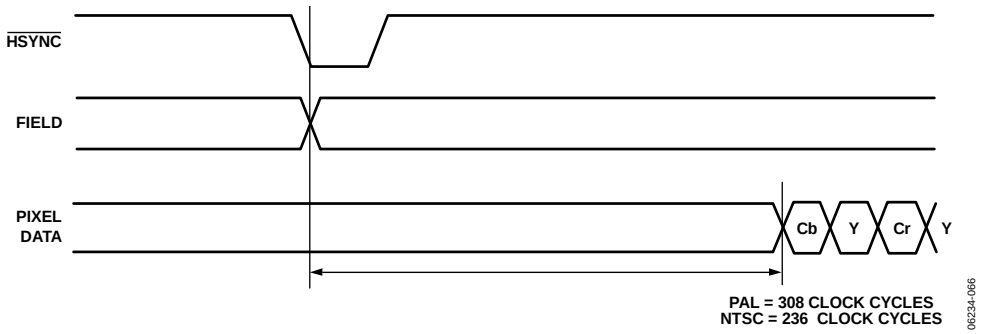


*Figure 65. Square Pixel Mode Active Pixel Timing*



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## FILTERS

Table 42 shows an overview of the programmable filters available on the ADV7390/ADV7391/ADV7392/ADV7393.

**Table 42. Selectable Filters**

| Filter | Subaddress |
|---|---|
| SD Luma LPF NTSC | 0x80 |
| SD Luma LPF PAL | 0x80 |
| SD Luma Notch NTSC | 0x80 |
| SD Luma Notch PAL | 0x80 |
| SD Luma SSAF | 0x80 |
| SD Luma CIF | 0x80 |
| SD Luma QCIF | 0x80 |
| SD Chroma 0.65 MHz | 0x80 |
| SD Chroma 1.0 MHz | 0x80 |
| SD Chroma 1.3 MHz | 0x80 |
| SD Chroma 2.0 MHz | 0x80 |
| SD Chroma 3.0 MHz | 0x80 |
| SD Chroma CIF | 0x80 |
| SD Chroma QCIF | 0x80 |
| SD PrPb SSAF | 0x82 |
| ED/HD Sinc Compensation Filter | 0x33 |
| ED/HD Chroma SSAF | 0x33 |

### *SD Internal Filter Response*

**Subaddress 0x80, Bits[7:2]; Subaddress 0x82, Bit 0**

The Y filter supports several different frequency responses, including two low-pass responses, two notch responses, an extended (SSAF) response with or without gain boost attenuation, a CIF response, and a QCIF response. The PrPb filter supports several different frequency responses, including six low-pass responses, a CIF response, and a QCIF response, as shown in Figure 38 and Figure 39.

If SD Luma SSAF gain is enabled (Subaddress 0x87, Bit 4), there are 13 response options in the range −4 dB to +4 dB. The desired response can be programmed using Subaddress 0xA2. Variation in frequency responses is shown in Figure 35 to Figure 37.

In addition to the chroma filters listed in Table 42, the ADV7390/ADV7391/ADV7392/ADV7393 contain an SSAF filter that is specifically designed for the color difference component outputs, Pr and Pb. This filter has a cutoff frequency of ~2.7 MHz and a gain of −40 dB at 3.8 MHz (see Figure 66). This filter can be controlled with Bit 0 of Sub-address 0x82, Bit 0.

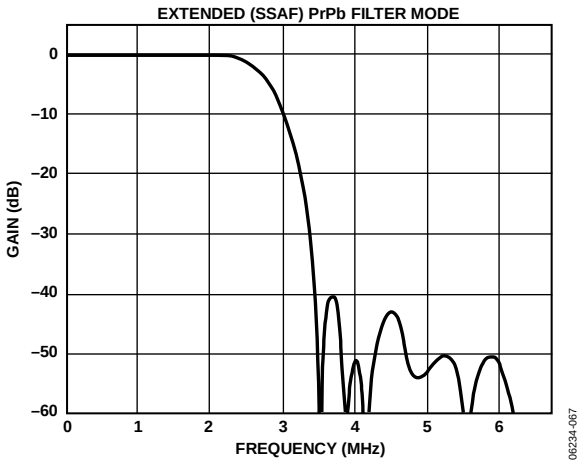


*Figure 66. PrPb SSAF Filter*

If this filter is disabled, one of the chroma filters shown in Table 43 can be selected and used for the CVBS or luma/chroma signal.

**Table 43. Internal Filter Specifications**

| Filter | Pass-Band Ripple (dB)[1] | 3 dB Bandwidth (MHz)[2] |
|---|---|---|
| Luma LPF NTSC | 0.16 | 4.24 |
| Luma LPF PAL | 0.1 | 4.81 |
| Luma Notch NTSC | 0.09 | 2.3/4.9/6.6 |
| Luma Notch PAL | 0.1 | 3.1/5.6/6.4 |
| Luma SSAF | 0.04 | 6.45 |
| Luma CIF | 0.127 | 3.02 |
| Luma QCIF | Monotonic | 1.5 |
| Chroma 0.65 MHz | Monotonic | 0.65 |
| Chroma 1.0 MHz | Monotonic | 1 |
| Chroma 1.3 MHz | 0.09 | 1.395 |
| Chroma 2.0 MHz | 0.048 | 2.2 |
| Chroma 3.0 MHz | Monotonic | 3.2 |
| Chroma CIF | Monotonic | 0.65 |
| Chroma QCIF | Monotonic | 0.5 |

[1] Pass-band ripple is the maximum fluctuation from the 0 dB response in the pass band, measured in decibels. The pass band is defined to have 0 Hz to fc (Hz) frequency limits for a low-pass filter and 0 Hz to f1 (Hz) and f2 (Hz) to infinity for a notch filter, where fc, f1, and f2 are the −3 dB points.
[2] 3 dB bandwidth refers to the −3 dB cutoff frequency.



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### *ED/HD Sinc Compensation Filter Response*

**Subaddress 0x33, Bit 3**

The ADV7390/ADV7391/ADV7392/ADV7393 include a filter designed to counter the effect of sinc roll-off in DAC 1, DAC 2, and DAC 3 while operating in ED/HD mode. This filter is enabled by default. It can be disabled using Subaddress 0x33, Bit 3. The benefit of the filter is illustrated in Figure 67 and Figure 68.

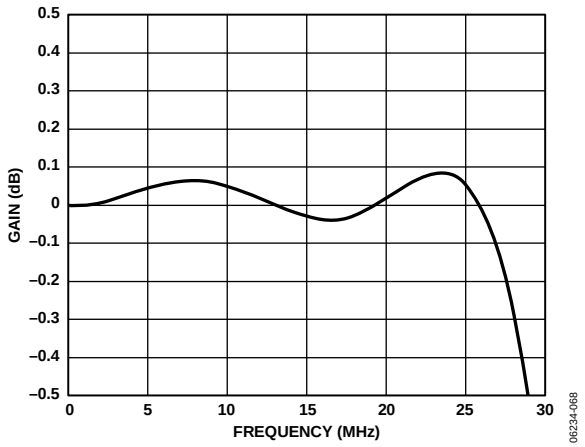


*Figure 67. ED/HD Sinc Compensation Filter Enabled*

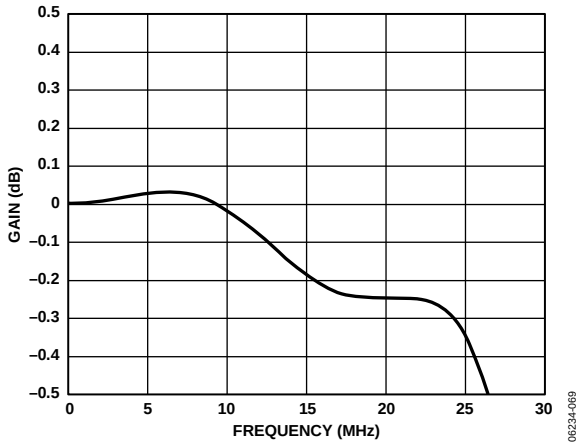


*Figure 68. ED/HD Sinc Compensation Filter Disabled*

## ED/HD TEST PATTERN COLOR CONTROLS

### *Subaddress 0x36 to Subaddress 0x38*

Three 8-bit registers at Subaddress 0x36 to Subaddress 0x38 are used to program the output color of the internal ED/HD test pattern generator (Subaddress 0x31, Bit 2 = 1), whether it be the lines of the crosshatch pattern or the uniform field test pattern. They are not functional as color controls for external pixel data input.

The values for the luma (Y) and color difference (Cr and Cb) signals used to obtain white, black, and saturated primary and complementary colors conform to the ITU-R BT.601-4 standard.

Table 44 shows sample color values that can be programmed into the color registers when the output standard selection is set to EIA770.2/EIA770.3 (Subaddress 0x30, Bits[1:0] = 00).

**Table 44. Sample Color Values for EIA770.2/EIA770.3 ED/HD Output Standard Selection**

| Sample Color | Y Value | | Cr Value | | Cb Value | |
|---|---|---|---|---|---|---|
| White | 235 | (0xEB) | 128 | (0x80) | 128 | (0x80) |
| Black | 16 | (0x10) | 128 | (0x80) | 128 | (0x80) |
| Red | 81 | (0x51) | 240 | (0xF0) | 90 | (0x5A) |
| Green | 145 | (0x91) | 34 | (0x22) | 54 | (0x36) |
| Blue | 41 | (0x29) | 110 | (0x6E) | 240 | (0xF0) |
| Yellow | 210 | (0xD2) | 146 | (0x92) | 16 | (0x10) |
| Cyan | 170 | (0xAA) | 16 | (0x10) | 166 | (0xA6) |
| Magenta | 106 | (0x6A) | 222 | (0xDE) | 202 | (0xCA) |

## COLOR SPACE CONVERSION MATRIX

### *Subaddress 0x03 to Subaddress 0x09*

The internal color space conversion (CSC) matrix automatically performs all color space conversions based on the input mode programmed in the mode select register (Subaddress 0x01, Bits[6:4]). Table 45 and Table 46 show the options available in this matrix.

An SD color space conversion from RGB-in to YPrPb-out is possible on the ADV7392/ADV7393. An ED/HD color space conversion from RGB-in to YPrPb-out is not possible.

**Table 45. SD Color Space Conversion Options**

| Input | Output[1] | YPrPb/RGB Out (Subaddress 0x02, Bit 5) | RGB In/YCrCb In (Subaddress 0x87, Bit 7) |
|---|---|---|---|
| YCrCb | YPrPb | 1 | 0 |
| YCrCb | RGB | 0 | 0 |
| RGB[2] | YPrPb | 1 | 1 |
| RGB[2] | RGB | 0 | 1 |

[1] CVBS/Y-C outputs are available for all CSC combinations.
[2] Available on the ADV7392/ADV7393 (40-pin devices) only.

**Table 46. ED/HD Color Space Conversion Options**

| Input | Output | YPrPb/RGB Out (Subaddress 0x02, Bit 5) |
|---|---|---|
| YCrCb | YPrPb | 1 |
| YCrCb | RGB | 0 |

### *SD Manual CSC Matrix Adjust Feature*

The SD manual CSC matrix adjust feature (available for the ADV7392 and ADV7393 only) provides custom coefficient manipulation for RGB to YPbPr conversion (for YPbPr to RGB conversion, this matrix adjustment is not available).

Normally, there is no need to modify the SD matrix coefficients because the CSC matrix automatically performs the color space conversion based on the output color space selected (see Table 46). Note that Bit 7 in subaddress 0x87 must be set to enable RGB input and, therefore, use the CSC manual adjustment.



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The SD CSC matrix scalar uses the following equations:

$$Y = (a1 \times R) + (a2 \times G) + (a3 \times B) + a4$$

$$Pr = (b1 \times R) + (b2 \times G) + (b3 \times B) + b4$$

$$Pb = (c1 \times R) + (c2 \times G) + (c3 \times B) + c4$$

The coefficients and their default values are located in the registers shown in Table 47.

**Table 47. SD Manual CSC Matrix Default Values**

| Coefficient | Subaddress | Default |
|---|---|---|
| a1 | 0xBD | 0x42 |
| a2 | 0xBE | 0x81 |
| a3 | 0xBF | 0x19 |
| a4 | 0xC0 | 0x10 |
| b1 | 0xC1 | 0x70 |
| b2 | 0xC2 | 0x5E |
| b3 | 0xC3 | 0x12 |
| b4 | 0xC4 | 0x80 |
| c1 | 0xC5 | 0x26 |
| c2 | 0xC6 | 0x4A |
| c3 | 0xC7 | 0x70 |
| c4 | 0xC8 | 0x80 |

### ED/HD Manual CSC Matrix Adjust Feature

The ED/HD manual CSC matrix adjust feature provides custom coefficient manipulation for color space conversions and is used in ED and HD modes only. The ED/HD manual CSC matrix adjust feature can be enabled using Subaddress 0x02, Bit 3.

Normally, there is no need to enable this feature because the CSC matrix automatically performs the color space conversion based on the input mode chosen (ED or HD) and the output color space selected (see Table 46). For this reason, the ED/HD manual CSC matrix adjust feature is disabled by default.

If RGB output is selected, the ED/HD CSC matrix scalar uses the following equations:

$$R = GY \times Y + RV \times Pr$$

$$G = GY \times Y - (GU \times Pb) - (GV \times Pr)$$

$$B = GY \times Y + BU \times Pb$$

Note that subtractions are implemented in the hardware.

If YPrPb output is selected, the following equations are used:

$$Y = GY \times Y$$

$$Pr = RV \times Pr$$

$$Pb = BU \times Pb$$

where:
*GY* = Subaddress 0x05, Bits[7:0] and Subaddress 0x03, Bits[1:0].
*GU* = Subaddress 0x06, Bits[7:0] and Subaddress 0x04, Bits[7:6].
*GV* = Subaddress 0x07, Bits[7:0] and Subaddress 0x04, Bits[5:4].
*BU* = Subaddress 0x08, Bits[7:0] and Subaddress 0x04, Bits[3:2].
*RV* = Subaddress 0x09, Bits[7:0] and Subaddress 0x04, Bits[1:0].

On power-up, the CSC matrix is programmed with the default values shown in Table 48.

**Table 48. ED/HD Manual CSC Matrix Default Values**

| Subaddress | Default |
|---|---|
| 0x03 | 0x03 |
| 0x04 | 0xF0 |
| 0x05 | 0x4E |
| 0x06 | 0x0E |
| 0x07 | 0x24 |
| 0x08 | 0x92 |
| 0x09 | 0x7C |

When the ED/HD manual CSC matrix adjust feature is enabled, the default coefficient values in Subaddress 0x03 to Subaddress 0x09 are correct for the HD color space only. The color components are converted according to the following 1080i and 720p standards (SMPTE 274M, SMPTE 296M):

$$R = Y + 1.575Pr$$

$$G = Y - 0.468Pr - 0.187Pb$$

$$B = Y + 1.855Pb$$

The conversion coefficients should be multiplied by 315 before being written to the ED/HD CSC matrix registers. This is reflected in the default values for GY = 0x13B, GU = 0x03B, GV = 0x093, BU = 0x248, and RV = 0x1F0.

If the ED/HD manual CSC matrix adjust feature is enabled and another input standard (such as ED) is used, the scale values for GY, GU, GV, BU, and RV must be adjusted according to this input standard color space. The user should consider that the color component conversion may use different scale values.

For example, SMPTE 293M uses the following conversion:

$$R = Y + 1.402Pr$$

$$G = Y - 0.714Pr - 0.344Pb$$

$$B = Y + 1.773Pb$$

The programmable CSC matrix is used for external ED/HD pixel data and is not functional when internal test patterns are enabled.

### Programming the CSC Matrix

If custom manipulation of the ED/HD CSC matrix coefficients is required for a YCrCb-to-RGB color space conversion, use the following procedure:

1. Enable the ED/HD manual CSC matrix adjust feature (Subaddress 0x02, Bit 3).
2. Set the output to RGB (Subaddress 0x02, Bit 5).
3. Disable sync on PrPb (Subaddress 0x35, Bit 2).
4. Enable sync on RGB (optional) (Subaddress 0x02, Bit 4).

The GY value controls the green signal output level, the BU value controls the blue signal output level, and the RV value controls the red signal output level.



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## SD LUMA AND COLOR SCALE CONTROL

### *Subaddress 0x9C to Subaddress 0x9F*

When enabled, the SD luma and color scale control feature can be used to scale the SD Y, Cb, and Cr output levels. This feature can be enabled using Subaddress 0x87, Bit 0. This feature affects all SD output signals, that is, CVBS, Y-C, YPrPb, and RGB.

When enabled, three 10-bit registers (SD Y scale, SD Cb scale, and SD Cr scale) control the scaling of the SD Y, Cb, and Cr output levels. The SD Y scale register contains the scaling factor used to scale the Y level from 0.0 to 1.5 times its initial level. The SD Cb scale and SD Cr scale registers contain the scaling factors to scale the Cb and Cr levels from 0.0 to 2.0 times their initial levels, respectively.

The values to be written to these 10-bit registers are calculated using the following equation:

*Y, Cb, or Cr Scale Value* = *Scale Factor* × 512

For example, if *Scale Factor* = 1.3

*Y, Cb, or Cr Scale Value* = 1.3 × 512 = 665.6

*Y, Cb, or Cr Scale Value* = 666 (rounded to the nearest integer)

*Y, Cb, or Cr Scale Value* = 1010011010b

Subaddress 0x9C, SD scale LSB = 0x2A
Subaddress 0x9D, SD Y scale register = 0xA6
Subaddress 0x9E, SD Cb scale register = 0xA6
Subaddress 0x9F, SD Cr scale register = 0xA6

It is recommended that the SD luma scale saturation feature (Subaddress 0x87, Bit 1) be enabled when scaling the Y output level to avoid excessive Y output levels.

## SD HUE ADJUST CONTROL

### *Subaddress 0xA0*

When enabled, the SD hue adjust control register (Subaddress 0xA0) is used to adjust the hue on the SD composite and chroma outputs. This feature can be enabled using Subaddress 0x87, Bit 2.

Subaddress 0xA0 contains the bits required to vary the hue of the video data, that is, the variance in phase of the subcarrier during active video with respect to the phase of the subcarrier during the color burst. The ADV7390/ADV7391/ADV7392/ADV7393 provide a range of ±22.5° in increments of 0.17578125°. For normal operation (zero adjustment), this register is set to 0x80. Value 0xFF and Value 0x00 represent the upper and lower limits, respectively, of the attainable adjustment in NTSC mode. Value 0xFF and Value 0x01 represent the upper and lower limits, respectively, of the attainable adjustment in PAL mode.

The hue adjust value is calculated using the following equation:

*Hue Adjust* (°) = 0.17578125° (*HCR*$_d$ − 128)

Where *HCR*$_d$ = the hue adjust control register (decimal).

For example, to adjust the hue by +4°, write 0x97 to the hue adjust control register.

$$\left(\frac{4}{0.17578125}\right) + 128 \approx 151d = 0x97$$

where the sum is rounded to the nearest integer.

To adjust the hue by −4°, write 0x69 to the hue adjust control register.

$$\left(\frac{-4}{0.17578125}\right) + 128 \approx 105d = 0x69$$

where the sum is rounded to the nearest integer.

## SD BRIGHTNESS DETECT

### *Subaddress 0xBA*

The ADV7390/ADV7391/ADV7392/ADV7393 allow monitoring of the brightness level of the incoming video data. This feature is used to monitor the average brightness of the incoming Y signal on a field-by-field basis. The information is read from the I²C and, based on this information, the color saturation, contrast, and brightness controls can be adjusted (for example, to compensate for very dark pictures).

The luma data is monitored in the active video area only. The average brightness I²C register is updated on the falling edge of every $\overline{\text{VSYNC}}$ signal. The SD brightness detect register (Subaddress 0xBA) is a read-only register.

## SD BRIGHTNESS CONTROL

### *Subaddress 0xA1, Bits[6:0]*

When this feature is enabled, the SD brightness/WSS control register (Subaddress 0xA1) is used to control brightness by adding a programmable setup level onto the scaled Y data. This feature can be enabled using Subaddress 0x87, Bit 3.

For NTSC with pedestal, the setup can vary from 0 IRE to 22.5 IRE. For NTSC without pedestal (see Figure 69) and for PAL, the setup can vary from −7.5 IRE to +15 IRE.

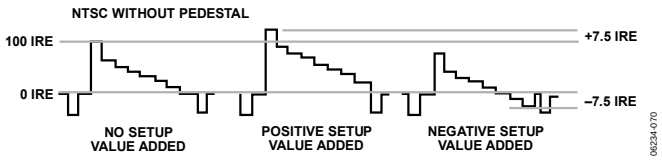


*Figure 69. Examples of Brightness Control Values*

The SD brightness control register is an 8-bit register. The seven LSBs of this 8-bit register are used to control the brightness level, which can be a positive or negative value.

For example, to add a +20 IRE brightness level to an NTSC signal with pedestal, write 0x28 to Subaddress 0xA1.

0 × (*SD Brightness Value*) =

0 × (*IRE Value* × 2.015631) =

0 × (20 × 2.015631) = 0 × (40.31262) ≈ 0x28



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To add a −7 IRE brightness level to a PAL signal, write 0x72 to Subaddress 0xA1.

0 × (*SD Brightness Value*) =

0 × (*IRE Value* × 2.075631) =

0 × (7 × 2.015631) = 0x(14.109417) ≈ 0001110b

0001110b *into twos complement* = 1110010b = 0x72

**Table 49. Sample Brightness Control Values[1]**

| Setup Level (NTSC) with Pedestal | Setup Level (NTSC) Without Pedestal | Setup Level (PAL) | Brightness Control Value |
|---|---|---|---|
| 22.5 IRE | 15 IRE | 15 IRE | 0x1E |
| 15 IRE | 7.5 IRE | 7.5 IRE | 0x0F |
| 7.5 IRE | 0 IRE | 0 IRE | 0x00 |
| 0 IRE | −7.5 IRE | −7.5 IRE | 0x71 |

[1] Values in the range of 0x3F to 0x44 may result in an invalid output signal.

## SD INPUT STANDARD AUTODETECTION

### *Subaddress 0x87, Bit 5*

The ADV7390/ADV7391/ADV7392/ADV7393 include an SD input standard autodetect feature that can be enabled by setting Subaddress 0x87, Bits[5:1].

When enabled, the ADV7390/ADV7391/ADV7392/ADV7393 can automatically identify an NTSC or a PAL B/D/G/H/I input stream. The ADV7390/ADV7391/ADV7392/ADV7393 automatically update the subcarrier frequency registers with the appropriate value for the identified standard. The ADV7390/ADV7391/ADV7392/ADV7393 are also configured to correctly encode the identified standard.

The SD standard bits (Subaddress 0x80, Bits[1:0]) and the subcarrier frequency registers are not updated to reflect the identified standard. All registers retain their default or user-defined values.

## DOUBLE BUFFERING

### *Subaddress 0x33, Bit 7 for ED/HD; Subaddress 0x88, Bit 2 for SD*

Double-buffered registers are updated once per field. Double buffering improves overall performance because modifications to register settings are not be made during active video but take effect prior to the start of the active video on the next field.

Using Subaddress 0x33, Bit 7, double buffering can be activated on the following ED/HD registers: the ED/HD Gamma A and Gamma B curves and ED/HD CGMS registers.

Using Subaddress 0x88, Bit 2, double buffering can be activated on the following SD registers: the SD Gamma A and Gamma B curves, SD Y scale, SD Cr scale, SD Cb scale, SD brightness, SD closed captioning, and SD Macrovision Bits[5:0] (Subaddress 0xE0, Bits[5:0]).

## PROGRAMMABLE DAC GAIN CONTROL

### *Subaddress 0x0B*

It is possible to adjust the DAC output signal gain up or down from its absolute level. This is illustrated in Figure 70.

DAC 1 to DAC 3 are controlled by Register 0x0B.

In Case A of Figure 70, the video output signal is gained. The absolute level of the sync tip and the blanking level increase with respect to the reference video output signal. The overall gain of the signal is increased from the reference signal.

In Case B of Figure 70, the video output signal is reduced. The absolute level of the sync tip and the blanking level decrease with respect to the reference video output signal. The overall gain of the signal is reduced from the reference signal.

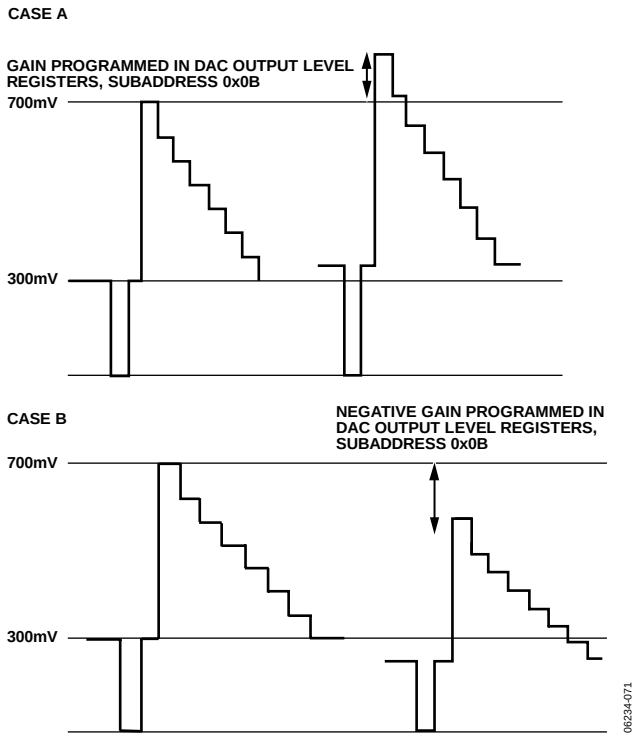


*Figure 70. Programmable DAC Gain—Positive and Negative Gain*

The range of this feature is specified for ±7.5% of the nominal output from the DACs. For example, if the output current of the DAC is 4.33 mA, the DAC gain control feature can change this output current from 4.008 mA (−7.5%) to 4.658 mA (+7.5%).



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The reset value of the control registers is 0x00; that is, nominal DAC current is output. Table 50 is an example of how the output current of the DACs varies for a nominal 4.33 mA output current.

**Table 50. DAC Gain Control**

| Subaddress 0x0B | DAC Current (mA) | % Gain | Note |
|---|---|---|---|
| 0100 0000 (0x40) | 4.658 | 7.5000% | |
| 0011 1111 (0x3F) | 4.653 | 7.3820% | |
| 0011 1110 (0x3E) | 4.648 | 7.3640% | |
| ... | ... | ... | |
| ... | ... | ... | |
| 0000 0010 (0x02) | 4.43 | 0.0360% | |
| 0000 0001 (0x01) | 4.38 | 0.0180% | |
| 0000 0000 (0x00) | 4.33 | 0.0000% | Reset value, nominal |
| 1111 1111 (0xFF) | 4.25 | −0.0180% | |
| 1111 1110 (0xFE) | 4.23 | −0.0360% | |
| ... | ... | ... | |
| ... | ... | ... | |
| 1100 0010 (0xC2) | 4.018 | −7.3640% | |
| 1100 0001 (0xC1) | 4.013 | −7.3820% | |
| 1100 0000 (0xC0) | 4.008 | −7.5000% | |

## GAMMA CORRECTION

### *Subaddress 0x44 to Subaddress 0x57 for ED/HD; Subaddress 0xA6 to Subaddress 0xB9 for SD*

Generally, gamma correction is applied to compensate for the nonlinear relationship between signal input and output brightness level (as perceived on a CRT). It can also be applied wherever nonlinear processing is used.

Gamma correction uses the function

$$Signal_{OUT} = (Signal_{IN})^{\gamma}$$

where γ is the gamma correction factor.

Gamma correction is available for SD and ED/HD video. For both variations, there are twenty 8-bit registers. They are used to program Gamma Correction Curve A and Gamma Correction Curve B.

ED/HD gamma correction is enabled using Subaddress 0x35, Bit 5. ED/HD Gamma Correction Curve A is programmed at Subaddress 0x44 to Subaddress 0x4D, and ED/HD Gamma Correction Curve B is programmed at Subaddress 0x4E to Subaddress 0x57.

SD gamma correction is enabled using Subaddress 0x88, Bit 6. SD Gamma Correction Curve A is programmed at Subaddress 0xA6 to Subaddress 0xAF, and SD Gamma Correction Curve B is programmed at Subaddress 0xB0 to Subaddress 0xB9.

Gamma correction is performed on the luma data only. The user can choose one of two correction curves, Curve A or Curve B. Only one of these curves can be used at a time. For ED/HD gamma correction, curve selection is controlled using Subaddress 0x35, Bit 4. For SD gamma correction, curve selection is controlled using Subaddress 0x88, Bit 7.

The shape of the gamma correction curve is controlled by defining the curve response at 10 different locations along the curve. By altering the response at these locations, the shape of the gamma correction curve can be modified. Between these points, linear interpolation is used to generate intermediate values. Considering the curve to have a total length of 256 points, the 10 programmable locations are at the following points: 24, 32, 48, 64, 80, 96, 128, 160, 192, and 224. The following locations are fixed and cannot be changed: 0, 16, 240, and 255.

From the curve locations, 16 to 240, the values at the programmable locations and, therefore, the response of the gamma correction curve, should be calculated to produce the following result:

$$x_{DESIRED} = (x_{INPUT})^{\gamma}$$

where:
$x_{DESIRED}$ is the desired gamma corrected output.
$x_{INPUT}$ is the linear input signal.
$\gamma$ is the gamma correction factor.

To program the gamma correction registers, calculate the 10 programmable curve values using the following formula:

$$\gamma_n = \left(\left(\frac{n-16}{240-16}\right)^{\gamma} \times (240-16)\right) + 16$$

where:
$\gamma_n$ is the value to be written into the gamma correction register for point $n$ on the gamma correction curve.
$n$ = 24, 32, 48, 64, 80, 96, 128, 160, 192, or 224.
$\gamma$ is the gamma correction factor.

For example, setting γ = 0.5 for all programmable curve data points results in the following $y_n$ values:

$y_{24} = [(8/224)^{0.5} \times 224] + 16 = 58$

$y_{32} = [(16/224)^{0.5} \times 224] + 16 = 76$

$y_{48} = [(32/224)^{0.5} \times 224] + 16 = 101$

$y_{64} = [(48/224)^{0.5} \times 224] + 16 = 120$

$y_{80} = [(64/224)^{0.5} \times 224] + 16 = 136$

$y_{96} = [(80/224)^{0.5} \times 224] + 16 = 150$

$y_{128} = [(112/224)^{0.5} \times 224] + 16 = 174$

$y_{160} = [(144/224)^{0.5} \times 224] + 16 = 195$

$y_{192} = [(176/224)^{0.5} \times 224] + 16 = 214$

$y_{224} = [(208/224)^{0.5} \times 224] + 16 = 232$

where the sum of each equation is rounded to the nearest integer.



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The gamma curves in Figure 71 and Figure 72 are examples only; any user-defined curve in the range from 16 to 240 is acceptable.

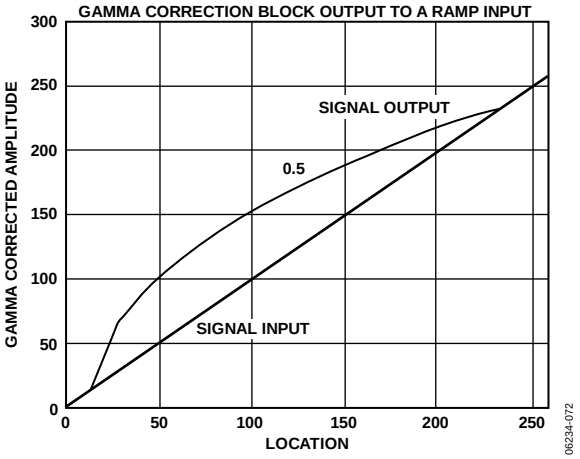


*Figure 71. Signal Input (Ramp) and Signal Output for Gamma 0.5*

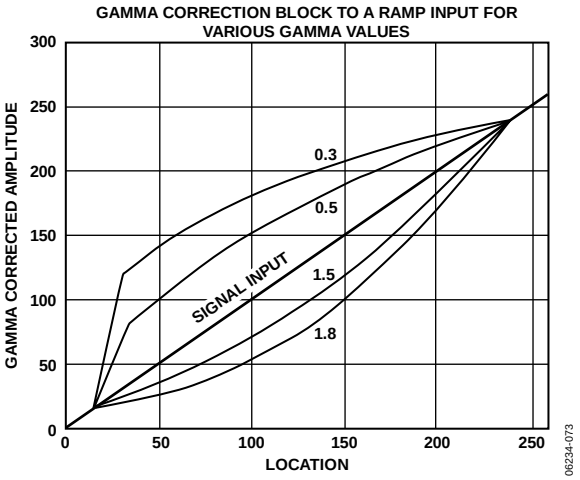


*Figure 72. Signal Input (Ramp) and Selectable Output Curves*

## ED/HD SHARPNESS FILTER AND ADAPTIVE FILTER CONTROLS

### *Subaddress 0x40; Subaddress 0x58 to Subaddress 0x5D*

There are three filter modes available on the ADV7390/ADV7391/ADV7392/ADV7393: sharpness filter mode and two adaptive filter modes.

### *ED/HD Sharpness Filter Mode*

To enhance or attenuate the Y signal in the frequency ranges shown in Figure 73, the ED/HD sharpness filter must be enabled (Subaddress 0x31, Bit 7 = 1) and the ED/HD adaptive filter must be disabled (Subaddress 0x35, Bit 7 = 0).

To select one of the 256 individual responses, the corresponding gain values, ranging from −8 to +7 for each filter, must be programmed into the ED/HD sharpness filter gain register at Subaddress 0x40.

### *ED/HD Adaptive Filter Mode*

In ED/HD adaptive filter mode, the following registers are used:

- ED/HD Adaptive Filter Threshold A
- ED/HD Adaptive Filter Threshold B
- ED/HD Adaptive Filter Threshold C
- ED/HD Adaptive Filter Gain 1
- ED/HD Adaptive Filter Gain 2
- ED/HD Adaptive Filter Gain 3
- ED/HD sharpness filter gain

To activate the adaptive filter control, the ED/HD sharpness filter and the ED/HD adaptive filter must be enabled (Subaddress 0x31, Bit 7 = 1, and Subaddress 0x35, Bit 7 = 1, respectively).

The derivative of the incoming signal is compared to the three programmable threshold values: ED/HD adaptive filter (Threshold A, Threshold B, and Threshold C) registers (Subaddress 0x5B, Subaddress 0x5C, and Subaddress 0x5D). The recommended threshold range is 16 to 235, although any value in the range of 0 to 255 can be used.

The edges can then be attenuated with the settings in the ED/HD adaptive filter (Gain 1, Gain 2, and Gain 3) registers (Subaddress 0x58, Subaddress 0x59 and Subaddress 0x5A), and the ED/HD sharpness filter gain register (Subaddress 0x40).

There are two adaptive filter modes available. The mode is selected using the ED/HD adaptive filter mode control (Subaddress 0x35, Bit 6) as follows:

- Mode A is used when the ED/HD adaptive filter mode control is set to 0. In this case, Filter B (LPF) is used in the adaptive filter block. In addition, only the programmed values for Gain B in the ED/HD sharpness filter gain register and ED/HD adaptive filter (Gain 1, Gain 2, and Gain 3) registers are applied when needed. The Gain A values are fixed and cannot be changed.
- Mode B is used when ED/HD adaptive filter mode control is set to 1. In this mode, a cascade of Filter A and Filter B is used. Both settings for Gain A and Gain B in the ED/HD sharpness filter gain register and ED/HD adaptive filter (Gain 1, Gain 2, and Gain 3) registers become active when needed.



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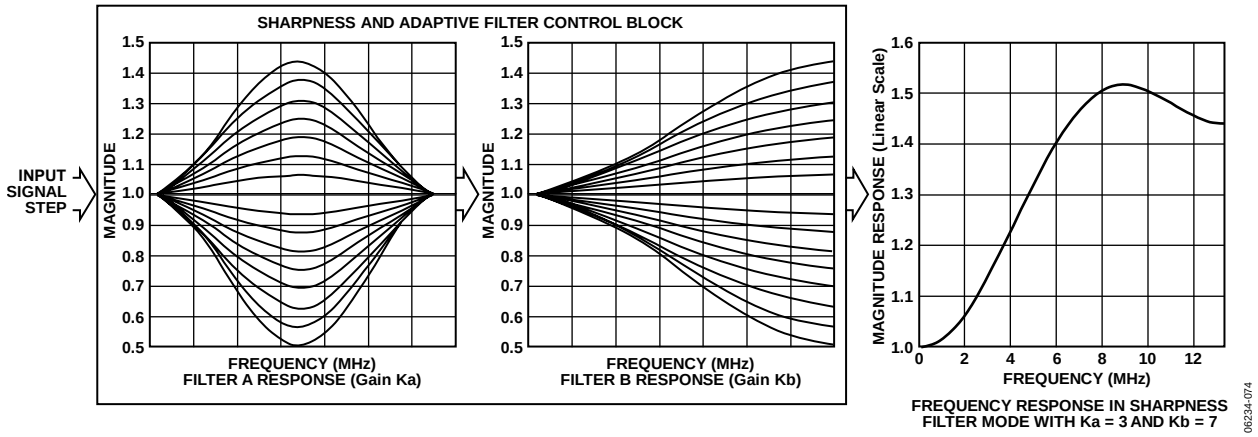
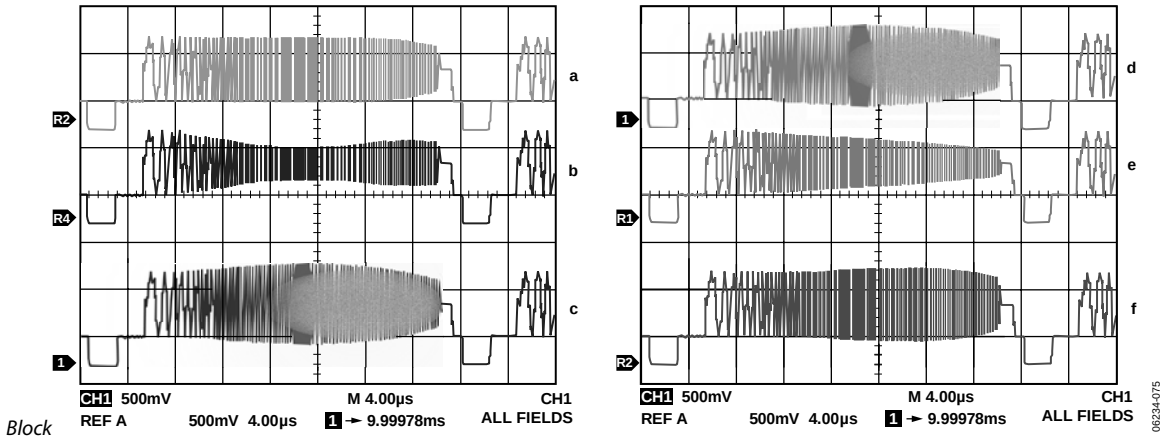



*Figure 73. ED/HD Sharpness and Adaptive Filter Control*




Block

*Figure 74. ED/HD Sharpness Filter Control with Different Gain Settings for ED/HD Sharpness Filter Gain Values*

## ED/HD SHARPNESS FILTER AND ADAPTIVE FILTER APPLICATION EXAMPLES

### *Sharpness Filter Application*

The ED/HD sharpness filter can be used to enhance or attenuate the Y video output signal. The register settings in Table 51 are used to achieve the results shown in Figure 74. Input data is generated by an external signal source.

**Table 51. ED/HD Sharpness Control Settings for Figure 74**

| Subaddress | Register Setting | Reference[1] |
|---|---|---|
| 0x00 | 0xFC | |
| 0x01 | 0x10 | |
| 0x02 | 0x20 | |
| 0x30 | 0x00 | |
| 0x31 | 0x81 | |
| 0x40 | 0x00 | a |
| 0x40 | 0x08 | b |
| 0x40 | 0x04 | c |
| 0x40 | 0x40 | d |
| 0x40 | 0x80 | e |
| 0x40 | 0x22 | f |

[1] See Figure 74.

### *Adaptive Filter Control Application*

The register settings in Table 52 are used to obtain the results shown in Figure 76, that is, to remove the ringing on the input Y signal, as shown in Figure 75. Input data is generated by an external signal source.

**Table 52. Register Settings for Figure 76**

| Subaddress | Register Setting |
|---|---|
| 0x00 | 0xFC |
| 0x01 | 0x38 |
| 0x02 | 0x20 |
| 0x30 | 0x00 |
| 0x31 | 0x81 |
| 0x35 | 0x80 |
| 0x40 | 0x00 |
| 0x58 | 0xAC |
| 0x59 | 0x9A |
| 0x5A | 0x88 |
| 0x5B | 0x28 |
| 0x5C | 0x3F |
| 0x5D | 0x64 |



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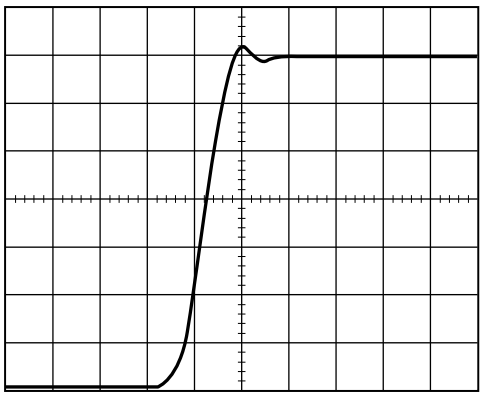


Figure 75. Input Signal to ED/HD Adaptive Filter

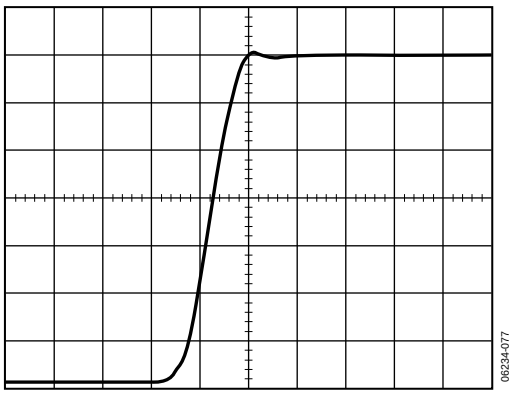


Figure 76. Output Signal from ED/HD Adaptive Filter (Mode A)

When the adaptive filter mode is changed to Mode B (Subaddress 0x35, Bit 6), the output shown in Figure 77 can be obtained.

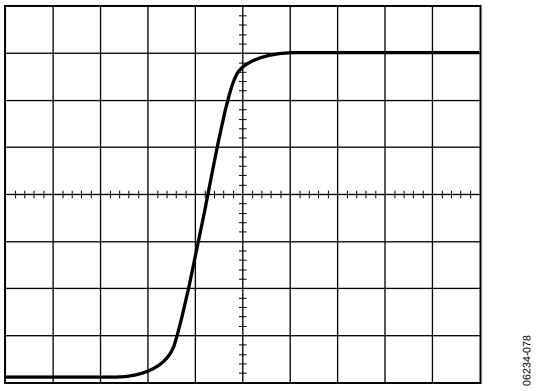


Figure 77. Output Signal from ED/HD Adaptive Filter (Mode B)

## SD DIGITAL NOISE REDUCTION

### *Subaddress 0xA3 to Subaddress 0xA5*

Digital noise reduction (DNR) is applied to the Y data only. A filter block selects the high frequency, low amplitude components of the incoming signal (DNR input select). The absolute value of the filter output is compared to a programmable threshold value (DNR threshold control). There are two DNR modes available: DNR mode and DNR sharpness mode.

In DNR mode, if the absolute value of the filter output is smaller than the threshold, it is assumed to be noise. A programmable amount (coring gain border, coring gain data) of this noise signal is subtracted from the original signal. In DNR sharpness mode, if the absolute value of the filter output is less than the programmed threshold, it is assumed to be noise as before. However, if the level exceeds the threshold, now being identified as a valid signal, a fraction of the signal (coring gain border, coring gain data) is added to the original signal to boost high frequency components and sharpen the video image.

In MPEG systems, it is common to process the video information in blocks of 8 pixels × 8 pixels for MPEG2 systems or 16 pixels × 16 pixels for MPEG1 systems (block size control). DNR can be applied to the resulting block transition areas known to contain noise. Generally, the block transition area contains two pixels. It is possible to define this area to contain four pixels (border area).

It is also possible to compensate for variable block positioning or differences in YCrCb pixel timing with the use of the DNR block offset.

The digital noise reduction registers are three 8-bit registers. They are used to control the DNR processing.

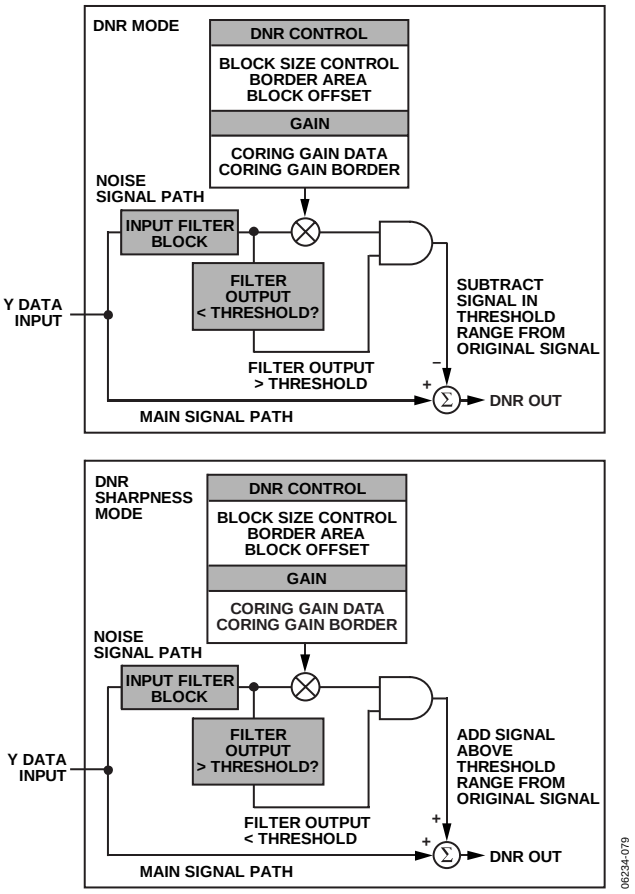


Figure 78. SD DNR Block Diagram



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### Coring Gain Border—Subaddress 0xA3, Bits[3:0]

These four bits are assigned to the gain factor applied to border areas. In DNR mode, the range of gain values is 0 to 1 in increments of 1/8. This factor is applied to the DNR filter output that lies below the set threshold range. The result is then subtracted from the original signal.

In DNR sharpness mode, the range of gain values is 0 to 0.5 in increments of 1/16. This factor is applied to the DNR filter output that lies above the threshold range. The result is added to the original signal.

### Coring Gain Data—Subaddress 0xA3, Bits[7:4]

These four bits are assigned to the gain factor applied to the luma data inside the MPEG pixel block. In DNR mode, the range of gain values is 0 to 1 in increments of 1/8. This factor is applied to the DNR filter output that lies below the set threshold range. The result is then subtracted from the original signal.

In DNR sharpness mode, the range of gain values is 0 to 0.5 in increments of 1/16. This factor is applied to the DNR filter output that lies above the threshold range. The result is added to the original signal.

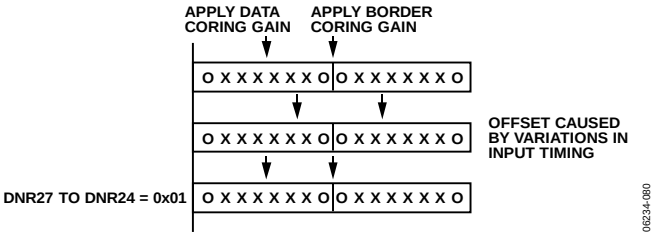


Figure 79. SD DNR Offset Control

### DNR Threshold—Subaddress 0xA4, Bits[5:0]

These six bits are used to define the threshold value in the range of 0 to 63. The range is an absolute value.

### Border Area—Subaddress 0xA4, Bit 6

When this bit is set to Logic 1, the block transition area can be defined to consist of four pixels. If this bit is set to Logic 0, the border transition area consists of two pixels, where one pixel refers to two clock cycles at 27 MHz.

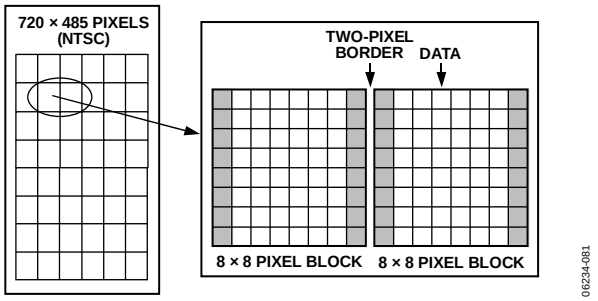


Figure 80. SD DNR Border Area

### Block Size—Subaddress 0xA4, Bit 7

This bit is used to select the size of the data blocks to be processed. Setting the block size control function to Logic 1 defines a 16 pixel × 16 pixel data block, and Logic 0 defines an 8 pixel × 8 pixel data block, where one pixel refers to two clock cycles at 27 MHz.

### DNR Input Select—Subaddress 0xA5, Bits[2:0]

These three bits are assigned to select the filter that is applied to the incoming Y data. The signal that lies in the pass band of the selected filter is the signal processed by DNR. Figure 81 shows the filter responses selectable with this control.

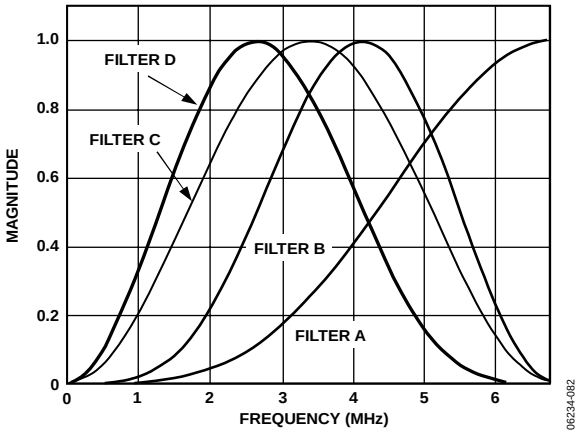


Figure 81. SD DNR Input Select

### DNR Mode—Subaddress 0xA5, Bit 3

This bit controls the DNR mode selected. Logic 0 selects DNR mode; Logic 1 selects DNR sharpness mode.

DNR works on the principle of defining low amplitude, high frequency signals as probable noise and subtracting this noise from the original signal.

In DNR mode, it is possible to subtract a fraction of the signal that lies below the set threshold, assumed to be noise, from the original signal. The threshold is set in DNR Register 1.

When DNR sharpness mode is enabled, it is possible to add a fraction of the signal that lies above the set threshold to the original signal because this data is assumed to be valid data and not noise. The overall effect is that the signal is boosted (similar to using the extended SSAF filter).

### Block Offset Control—Subaddress 0xA5, Bits[7:4]

Four bits are assigned to this control, which allows a shift in the data block of 15 pixels maximum. The coring gain positions are fixed. The block offset shifts the data in steps of one pixel such that the border coring gain factors can be applied at the same position regardless of variations in input timing of the data.



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## SD ACTIVE VIDEO EDGE CONTROL

### *Subaddress 0x82, Bit 7*

The ADV7390/ADV7391/ADV7392/ADV7393 are able to control fast rising and falling signals at the start and end of active video to minimize ringing.

When the active video edge control feature is enabled (Subaddress 0x82, Bit 7 = 1), the first three pixels and the last three pixels of the active video on the luma channel are scaled so that maximum transitions on these pixels are not possible.

At the start of active video, the first three pixels are multiplied by 1/8, 1/2, and 7/8, respectively. Approaching the end of active video, the last three pixels are multiplied by 7/8, 1/2, and 1/8, respectively. All other active video pixels pass through unprocessed.

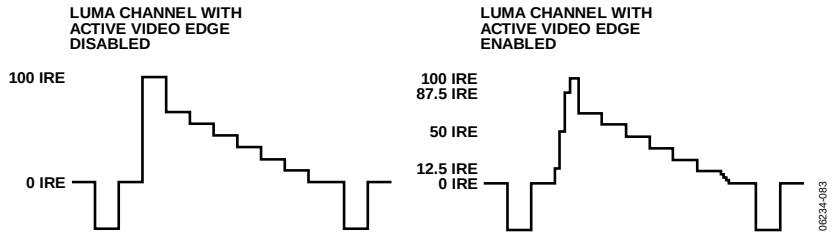


*Figure 82. Example of Active Video Edge Functionality*

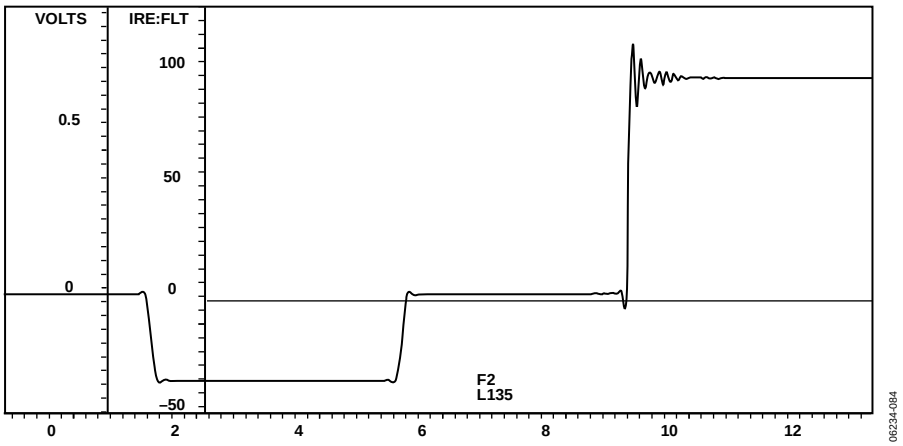


*Figure 83. Example of Video Output with Subaddress 0x82, Bit 7 = 0*

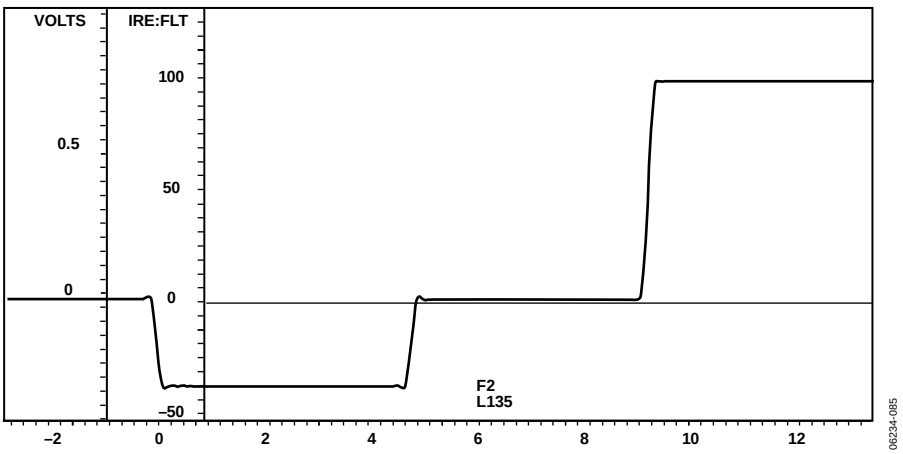


*Figure 84. Example of Video Output with Subaddress 0x82, Bit 7 = 1*



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## EXTERNAL HORIZONTAL AND VERTICAL SYNCHRONIZATION CONTROL

For timing synchronization purposes, the ADV7390/ADV7391/ADV7392/ADV7393 are able to accept either EAV/SAV time codes embedded in the input pixel data or external synchronization signals provided on the HSYNC and VSYNC pins (see Table 53). It is also possible to output synchronization signals on the HSYNC and VSYNC pins (see Table 54 to Table 56).

**Table 53. Timing Synchronization Signal Input Options**

| Signal | Pin | Condition |
|---|---|---|
| SD HSYNC In | HSYNC | SD slave timing (Mode 1, Mode 2, or Mode 3) selected (Subaddress 0x8A[2:0])[1] |
| SD VSYNC/FIELD In | VSYNC | SD slave timing (Mode 1, Mode 2, or Mode 3) selected (Subaddress 0x8A[2:0])[1] |
| ED/HD HSYNC In | HSYNC | ED/HD timing synchronization inputs enabled (Subaddress 0x30, Bit 2 = 0) |
| ED/HD VSYNC/FIELD In | VSYNC | ED/HD timing synchronization inputs enabled (Subaddress 0x30, Bit 2 = 0) |

[1] SD and ED/HD timing synchronization outputs must also be disabled (Subaddress 0x02[7:6] = 00).

**Table 54. Timing Synchronization Signal Output Options**

| Signal | Pin | Condition |
|---|---|---|
| SD HSYNC Out | HSYNC | SD timing synchronization outputs enabled (Subaddress 0x02, Bit 6 = 1)[1] |
| SD VSYNC/FIELD Out | VSYNC | SD timing synchronization outputs enabled (Subaddress 0x02, Bit 6 = 1)[1] |
| ED/HD HSYNC Out | HSYNC | ED/HD timing synchronization outputs enabled (Subaddress 0x02, Bit 7 = 1)[2] |
| ED/HD VSYNC/FIELD Out | VSYNC | ED/HD timing synchronization outputs enabled (Subaddress 0x02, Bit 7 = 1)[2] |

[1] ED/HD timing synchronization outputs must also be disabled (Subaddress 0x02, Bit 7 = 0).
[2] ED/HD timing synchronization inputs must also be disabled; that is, embedded EAV/SAV timing codes must be enabled (Subaddress 0x30, Bit 2 = 1).

**Table 55. HSYNC Output Control[1, 2]**

| ED/HD Input Sync Format (Subaddress 0x30, Bit 2) | ED/HD HSYNC Control (Subaddress 0x34, Bit 1) | ED/HD Sync Output Enable (Subaddress 0x02, Bit 7) | SD Sync Output Enable (Subaddress 0x02, Bit 6) | Signal on HSYNC Pin | Duration |
|---|---|---|---|---|---|
| X | X | 0 | 0 | Tristate | N/A |
| X | X | 0 | 1 | Pipelined SD HSYNC | See the SD Timing section. |
| 0 | 0 | 1 | X | Pipelined ED/HD HSYNC | As per HSYNC timing. |
| 1 | 0 | 1 | X | Pipelined ED/HD HSYNC based on AV Code H bit | Same as line blanking interval. |
| X | 1 | 1 | X | Pipelined ED/HD HSYNC based on horizontal counter | Same as embedded HSYNC. |

[1] In all ED/HD standards where there is an HSYNC output, the start of the HSYNC pulse is aligned with the falling edge of the embedded HSYNC in the output video.
[2] X = don't care.

**Table 56. VSYNC Output Control[1, 2]**

| ED/HD Input Sync Format (Subaddress 0x30, Bit 2) | ED/HD VSYNC Control (Subaddress 0x34, Bit 2) | ED/HD Sync Output Enable (Subaddress 0x02, Bit 7) | SD Sync Output Enable (Subaddress 0x02, Bit 6) | Video Standard | Signal on VSYNC Pin | Duration |
|---|---|---|---|---|---|---|
| x | x | 0 | 0 | x | Tristate | N/A |
| x | x | 0 | 1 | Interlaced | Pipelined SD VSYNC/field | See the SD Timing section. |
| 0 | 0 | 1 | x | x | Pipelined ED/HD VSYNC or field signal | As per VSYNC or field signal timing. |
| 1 | 0 | 1 | x | All HD interlaced standards | Pipelined field signal based on AV Code F bit | Field. |
| 1 | 0 | 1 | x | All ED/HD progressive standards | Pipelined VSYNC based on AV Code V bit | Vertical blanking interval. |



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| ED/HD Input Sync Format (Subaddress 0x30, Bit 2) | ED/HD $\overline{\text{VSYNC}}$ Control (Subaddress 0x34, Bit 2) | ED/HD Sync Output Enable (Subaddress 0x02, Bit 7) | SD Sync Output Enable (Subaddress 0x02, Bit 6) | Video Standard | Signal on $\overline{\text{VSYNC}}$ Pin | Duration |
|---|---|---|---|---|---|---|
| X | 1 | 1 | X | All ED/HD standards except 525p | Pipelined ED/HD $\overline{\text{VSYNC}}$ based on the vertical counter | Aligned with serration lines. |
| X | 1 | 1 | X | 525p | Pipelined ED/HD $\overline{\text{VSYNC}}$ based on the vertical counter | Vertical blanking interval. |

[1] In all ED/HD standards where there is a $\overline{\text{VSYNC}}$ output, the start of the $\overline{\text{VSYNC}}$ pulse is aligned with the falling edge of the embedded $\overline{\text{VSYNC}}$ in the output video.
[2] X = don't care.

## LOW POWER MODE

### *Subaddress 0x0D, Bits[2:0]*

For power-sensitive applications, the ADV7390/ADV7391/ADV7392/ADV7393 support an Analog Devices, Inc., proprietary low power mode of operation. To use this low power mode, the DACs must be operating in full-drive mode ($R_{SET}$ = 510 Ω, $R_L$ = 37.5 Ω). Low power mode is not available in low-drive mode ($R_{SET}$ = 4.12 kΩ, $R_L$ = 300 Ω). Low power mode can be independently enabled or disabled on each DAC using Subaddress 0x0D, Bits[2:0]. Low power mode is disabled by default on all DACs.

In low-power mode, DAC current consumption is content dependent and, on a typical video stream, it can be reduced by as much as 40%. For applications requiring the highest possible video performance, low power mode should be disabled.

## CABLE DETECTION

### *Subaddress 0x10, Bits[1:0]*

The ADV7390/ADV7391/ADV7392/ADV7393 include an Analog Devices proprietary cable detection feature. The cable detection feature is available on DAC 1 and DAC 2 when operating in full-drive mode ($R_{SET}$ = 510 Ω, $R_L$ = 37.5 Ω, assuming a connected cable). The feature is not available in low-drive mode ($R_{SET}$ = 4.12 kΩ, $R_L$ = 300 Ω). For a DAC to be monitored, the DAC must be powered up in Subaddress 0x00.

The cable detection feature can be used with all SD, ED, and HD video standards. It is available for all output configurations, that is, CVBS, Y-C, YPrPb, and RGB output configurations.

For CVBS/Y-C output configurations, both DAC 1 and DAC 2 are monitored; that is, the CVBS and Y-C luma outputs are monitored. For YPrPb and RGB output configurations, only DAC 1 is monitored; that is, the luma or green output is monitored.

Once per frame, the ADV7390/ADV7391/ADV7392/ADV7393 monitor DAC 1 and/or DAC 2, updating Subaddress 0x10, Bit 0 and/or Bit 1, respectively. If a cable is detected on one of the DACs, the relevant bit is set to 0. If not, the bit is set to 1.

## DAC AUTOPOWER-DOWN

### *Subaddress 0x10, Bit 4*

For power-sensitive applications, a DAC autopower-down feature can be enabled using Subaddress 0x10, Bit 4. This feature is available only when the cable detection feature is enabled.

With this feature enabled, the cable detection circuitry monitors DAC 1 and/or DAC 2 once per frame and, if they are unconnected, automatically powers down some or all of the DACs. Which DAC or DACs are powered down depends on the selected output configuration. For CVBS/Y-C output configurations, if DAC 1 is unconnected, only DAC 1 powers down. If DAC 2 is unconnected, DAC 2 and DAC 3 power down.

For YPrPb and RGB output configurations, if DAC 1 is unconnected, all three DACs are powered down. DAC 2 is not monitored for YPrPb and RGB output configurations.

Once per frame, DAC 1 and/or DAC 2 is monitored. If a cable is detected, the appropriate DAC or DACs remain powered up for the duration of the frame. If no cable is detected, the appropriate DAC or DACs power down until the next frame, when the process is repeated.

## SLEEP MODE

### *Subaddress 0x00, Bit 0*

In sleep mode, most of the digital I/O pins of the ADV7390/ADV7391/ADV7392/ADV7393 are disabled. For inputs, this means that the external data is ignored, and internally the logic normally driven by a given input is just tied low or high. This includes CLKIN.

For digital output pins, this means that the pin goes into tristate (high impedance) mode.

There are some exceptions to allow the user to continue to communicate with the part via $I^2C$: the $\overline{\text{RESET}}$, ALSB, SDA and SCL pins are kept alive.

Most of the analogue circuitry is powered down when in sleep mode. In addition, the cable detect feature no longer works as the DACs are powered down.

Sleep mode is enabled using Subaddress 0x00, Bit 0.



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## PIXEL AND CONTROL PORT READBACK

### *Subaddress 0x13, Subaddress 0x14, Subaddress 0x16*

The ADV7390/ADV7391/ADV7392/ADV7393 support the readback of most digital inputs via the I²C MPU port. This feature is useful for board-level connectivity testing with upstream devices.

The pixel port (P[15:0] or P[7:0]), $\overline{\text{HSYNC}}$, $\overline{\text{VSYNC}}$, and SFL are available for readback via the MPU port. The readback registers are located at Subaddress 0x13, Subaddress 0x14, and Subaddress 0x16.

When using this feature, apply a clock signal to the CLKIN pin to register the levels applied to the input pins. The SD input mode (Subaddress 0x01, Bits[6:4] = 000) must be selected when using this feature.

## RESET MECHANISMS

### *Subaddress 0x17, Bit 1*

A hardware reset is activated with a high-to-low transition on the $\overline{\text{RESET}}$ pin in accordance with the timing specifications. This resets all registers to their default values. After a hardware reset, the MPU port is configured for I²C operation. For correct device operation, a hardware reset is necessary after power-up.

The ADV7390/ADV7391/ADV7392/ADV7393 also have a software reset accessible via the I²C MPU port. A software reset is activated by writing a 1 to Subaddress 0x17, Bit 1. This resets all registers to their default values. This bit is self-clearing; that is, after a 1 has been written to the bit, the bit automatically returns to 0.

A hardware reset is necessary after power-up for correct device operation. If no hardware reset functionality is required by the application, the $\overline{\text{RESET}}$ pin can be connected to an RC network to provide the hardware reset necessary after power-up. After power-up, the time constant of the RC network holds the $\overline{\text{RESET}}$ pin low long enough to cause a reset to take place. All subsequent resets can be done via software.

## SD TELETEXT INSERTION

### *Subaddress 0xC9 to Subaddress 0xCE*

The ADV7390/ADV7391/ADV7392/ADV7393 support the insertion of teletext data, using a two pin interface, when operating in PAL mode. Teletext insertion is enabled using Subaddress 0xC9, Bit 0.

In accordance with the PAL WST teletext standard, teletext data should be inserted into the ADV7390/ADV7391/ADV7392/ADV7393 at a rate of 6.9375 Mbps. On the ADV7390/ADV7391, the teletext data is inserted on the $\overline{\text{VSYNC}}$ pin. On the ADV7392/ADV7393, the teletext data can be inserted on the $\overline{\text{VSYNC}}$ or P0 pin (selectable through Subaddress 0xC9, Bit 2).

When teletext insertion is enabled, a teletext request signal is output from the ADV7390/ADV7391/ADV7392/ADV7393 to indicate when teletext data should be inserted. The teletext request signal is output on the SFL pin. The position (relative to the teletext data) and width of the request signal are configurable using Subaddress 0xCA. The request signal can operate in either a line or bit mode. The request signal mode is controlled using Subaddress 0xC9, Bit 1.

To account for the noninteger relationship between the teletext insertion rate (6.9375 Mbps) and the pixel clock (27 MHz), a teletext insertion protocol is implemented in the ADV7390/ADV7391/ADV7392/ADV7393. At a rate of 6.9375 Mbps, the time taken for the insertion of 37 teletext bits equates to 144 pixel clock cycles (at 27 MHz). For every 37 teletext bits inserted into the ADV7390/ADV7391/ADV7392/ADV7393, the 10th, 19th, 28th, and 37th bits are carried for three pixel clock cycles, and the remainder are carried for four pixel clock cycles (totaling 144 pixel clock cycles). The teletext insertion protocol repeats every 37 teletext bits or 144 pixel clock cycles until all 360 teletext bits are inserted.

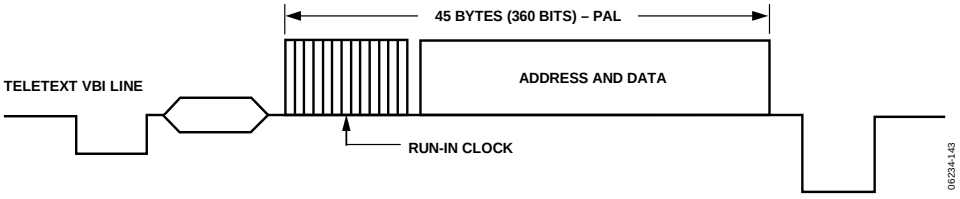


*Figure 85. Teletext VBI Line*



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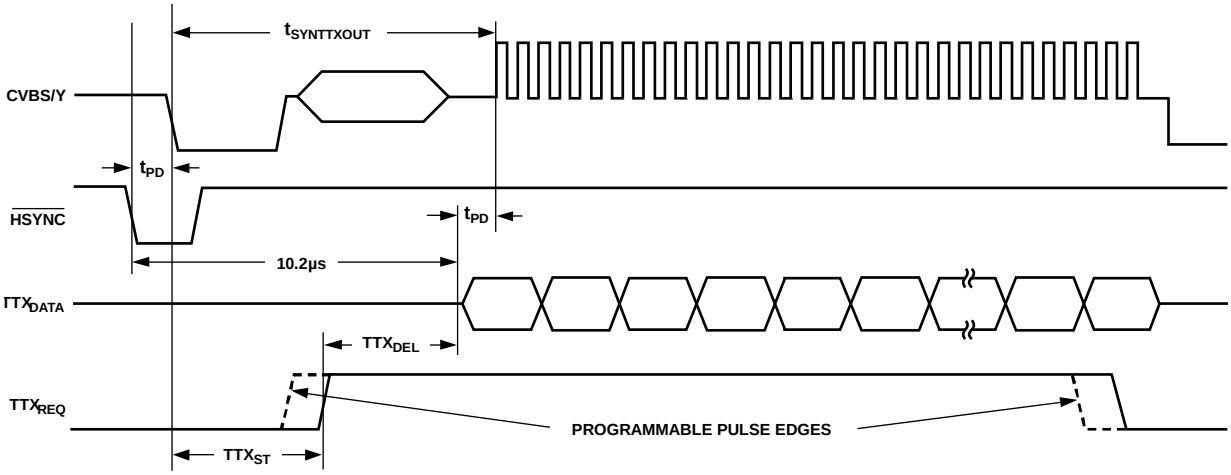


$t_{SYNTTXOUT}$ = 10.2µs.
$t_{PD}$ = PIPELINE DELAY THROUGH ADV7390/ADV7391/ADV7392/ADV7393.
$TTX_{DEL}$ = $TTX_{REQ}$ TO $TTX_{DATA}$ (PROGRAMMABLE RANGE = 4 BITS [0 TO 15 PIXEL CLOCK CYCLES]).

*Figure 86. Teletext Functionality Diagram*



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# PRINTED CIRCUIT BOARD LAYOUT AND DESIGN

## UNUSED PINS

If the $\overline{\text{HSYNC}}$ and $\overline{\text{VSYNC}}$ pins are not used, they should be tied to $V_{DD_IO}$ through a pull-up resistor (10 kΩ or 4.7 kΩ). Any other unused digital inputs should be tied to ground. Unused digital output pins should be left floating. DAC outputs can either be left floating or connected to GND. Disabling these outputs is recommended.

## DAC CONFIGURATIONS

The ADV7390/ADV7391/ADV7392/ADV7393 contain three DACs. All three DACs can be configured to operate in full-drive mode. Full-drive mode is defined as 34.7 mA full-scale current into a 37.5 Ω load, $R_L$. Full drive is the recommended mode of operation for the DACs.

Alternatively, all three DACs can be configured to operate in low-drive mode. Low-drive mode is defined as 4.33 mA full-scale current into a 300 Ω load, $R_L$.

The ADV7390/ADV7391/ADV7392/ADV7393 contain an $R_{SET}$ pin. A resistor connected between the $R_{SET}$ pin and AGND is used to control the full-scale output current and, therefore, the output voltage levels of DAC 1, DAC 2, and DAC 3. For full-drive operation, $R_{SET}$ must have a value of 510 Ω and RL must have a value of 37.5 Ω. For low drive operation, $R_{SET}$ must have a value of 4.12 kΩ, and $R_L$ must have a value of 300 Ω. The resistor connected to the $R_{SET}$ pin should have a 1% tolerance.

The ADV7390/ADV7391/ADV7392/ADV7393 contain a compensation pin, COMP. A 2.2 nF compensation capacitor should be connected from the COMP pin to $V_{AA}$.

## VIDEO OUTPUT BUFFER AND OPTIONAL OUTPUT FILTER

An output buffer is necessary on any DAC that operates in low-drive mode ($R_{SET}$ = 4.12 kΩ, $R_L$ = 300 Ω). Analog Devices produces a range of op amps suitable for this application, for example, the AD8061. For more information about line driver buffering circuits, see the relevant op amp data sheet.

An optional reconstruction (anti-imaging) low-pass filter (LPF) may be required on the ADV7390/ADV7391/ADV7392/ADV7393 DAC outputs. The filter specifications vary with the application. The use of 16× (SD), 8× (ED), or 4× (HD) oversampling can remove the requirement for a reconstruction filter altogether.

For applications requiring an output buffer and reconstruction filter, the ADA4430-1 and ADA4411-3 integrated video filter buffers should be considered.

**Table 57. ADV7390/ADV7391/ADV7392/ADV7393 Output Rates**

| Input Mode (Subaddress 0x01, Bits[6:4]) | Oversampling | Output Rate (MHz) | |
|---|---|---|---|
| SD | Off | 27 | (2×) |
| | On | 108 | (8×) |
| | On | 216 | (16×) |
| ED | Off | 27 | (1×) |
| | On | 108 | (4×) |
| | On | 216 | (8×) |
| HD | Off | 74.25 | (1×) |
| | On | 148.5 | (2×) |
| | On | 297 | (4×) |

**Table 58. Output Filter Requirements**

| Application | Oversampling | Cutoff Frequency (MHz) | Attenuation −50 dB at (MHz) |
|---|---|---|---|
| SD | 2× | > 6.5 | 20.5 |
| | 8× | > 6.5 | 101.5 |
| | 16× | > 6.5 | 209.5 |
| ED | 1× | > 12.5 | 14.5 |
| | 4× | > 12.5 | 95.5 |
| | 8× | > 12.5 | 203.5 |
| HD | 1× | > 30 | 44.25 |
| | 2× | > 30 | 118.5 |
| | 4× | > 30 | 267 |

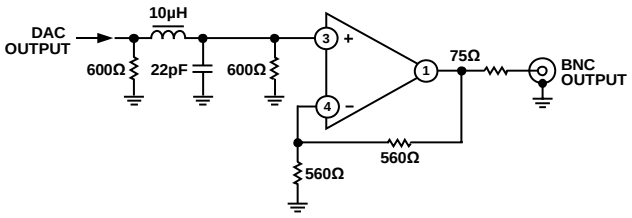


*Figure 87. Example of Output Filter for SD, 16× Oversampling*

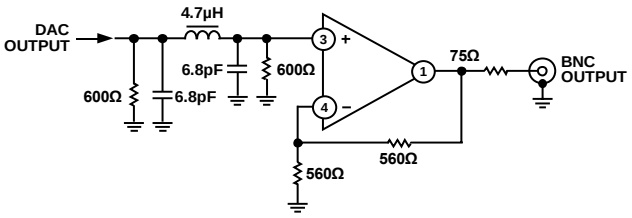


*Figure 88. Example of Output Filter for ED, 8× Oversampling*

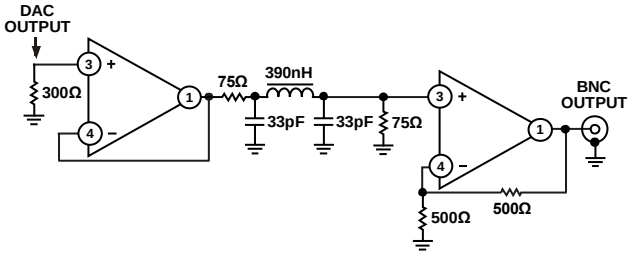


*Figure 89. Example of Output Filter for HD, 4× Oversampling*



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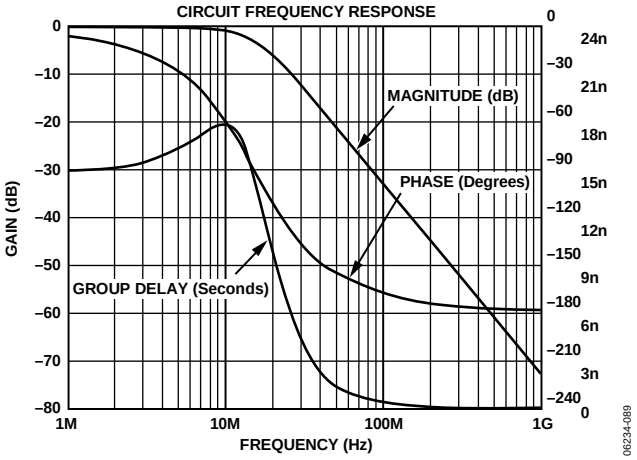


*Figure 90. Output Filter Plot for SD, 16× Oversampling*

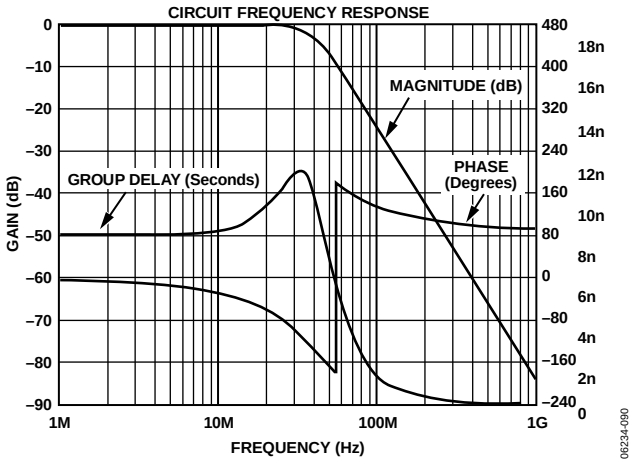


*Figure 91. Output Filter Plot for ED, 8× Oversampling*

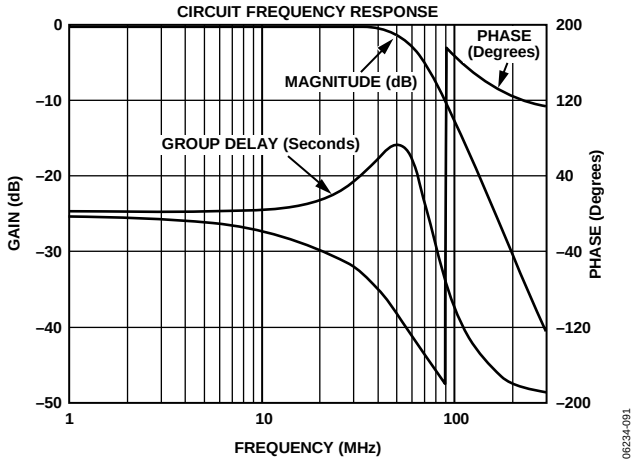


*Figure 92. Output Filter Plot for HD, 4× Oversampling*

## PRINTED CIRCUIT BOARD (PCB) LAYOUT

The ADV7390/ADV7391/ADV7392/ADV7393 are highly integrated circuits containing both precision analog and high speed digital circuitry. It is designed to minimize interference effects on the integrity of the analog circuitry by the high speed digital circuitry. It is imperative that these same design and layout techniques be applied to the system-level design so that optimal performance is achieved.

The layout should be optimized for lowest noise on the ADV7390/ADV7391/ADV7392/ADV7393 power and ground planes by shielding the digital inputs and providing good power supply decoupling.

It is recommended to use a 4-layer printed circuit board with ground and power planes separating the signal trace layer and the solder side layer.

### *Component Placement*

Component placement should be carefully considered to separate noisy circuits, such as clock signals and high speed digital circuitry, from analog circuitry.

The external loop filter components and components connected to the COMP and $R_{SET}$ pins should be placed as close as possible to, and on the same side of the PCB as, the ADV7390/ADV7391/ADV7392/ADV7393. Adding vias to the PCB to get the components closer to the ADV7390/ADV7391/ADV7392/ADV7393 is not recommended.

It is recommended that the ADV7390/ADV7391/ADV7392/ADV7393 be placed as close as possible to the output connector, with the DAC output traces as short as possible.

The termination resistors on the DAC output traces should be placed as close as possible to and on the same side of the PCB as the ADV7390/ADV7391/ADV7392/ADV7393. The termination resistors should overlay the PCB ground plane.

External filter and buffer components connected to the DAC outputs should be placed as close as possible to the ADV7390/ADV7391/ADV7392/ADV7393 to minimize the possibility of noise pickup from neighboring circuitry and to minimize the effect of trace capacitance on output bandwidth. This is particularly important when operating in low-drive mode ($R_{SET}$ = 4.12 kΩ, $R_L$ = 300 Ω).

### *Power Supplies*

It is recommended that a separate regulated supply be provided for each power domain ($V_{AA}$, $V_{DD}$, $V_{DD_IO}$, and $PV_{DD}$). For optimal performance, linear regulators rather than switch mode regulators should be used. If switch mode regulators must be used, care must be taken with regard to the quality of the output voltage in terms of ripple and noise. This is particularly true for the $V_{AA}$ and $PV_{DD}$ power domains. Each power supply should be individually connected to the system power supply at a single point through a suitable filtering device, such as a ferrite bead.



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### *Power Supply Decoupling*

It is recommended that each power supply pin be decoupled with 10 nF and 0.1 µF ceramic capacitors. The $V_{AA}$, $PV_{DD}$, $V_{DD_IO}$, and both $V_{DD}$ pins should be individually decoupled to ground. The decoupling capacitors should be placed as close as possible to the ADV7390/ADV7391/ADV7392/ADV7393 with the capacitor leads kept as short as possible to minimize lead inductance.

A 1 µF tantalum capacitor is recommended across the $V_{AA}$ supply in addition to the 10 nF and 0.1 µF ceramic capacitors.

### *Power Supply Sequencing*

The ADV7390/ADV7391/ADV7392/ADV7393 are robust to all power supply sequencing combinations. Any sequence can be used. However, all power supplies should settle to their nominal voltages within one second.

### *Digital Signal Interconnect*

The digital signal traces should be isolated as much as possible from the analog outputs and other analog circuitry. Digital signal traces should not overlay the $V_{AA}$ or $PV_{DD}$ power plane.

Due to the high clock rates used, avoid long clock traces to the ADV7390/ADV7391/ADV7392/ADV7393 to minimize noise pickup.

Any pull-up termination resistors for the digital inputs should be connected to the $V_{DD_IO}$ power supply.

### *Analog Signal Interconnect*

DAC output traces should be treated as transmission lines with appropriate measures taken to ensure optimal performance (for example, impedance matched traces). The DAC output traces should be kept as short as possible. The termination resistors on the DAC output traces should be placed as close as possible to, and on the same side of the PCB as, the ADV7390/ADV7391/ADV7392/ADV7393.

To avoid crosstalk between the DAC outputs, it is recommended that as much space as possible be left between the traces connected to the DAC output pins. Adding ground traces between the DAC output traces is also recommended.

## ADDITIONAL LAYOUT CONSIDERATIONS FOR THE WLCSP PACKAGE

Due to the high pad density and 0.5 mm pitch of the WLCSP, it is not recommended that connections to inner bumps be routed on the top PCB layer only.

The traces (track and space) must fit within the limits of the solder mask openings. Routing all traces on the top surface layer of the board, while possible, is usually not a feasible solution due to the limitations of the geometries imposed by the board fabrication technology. Given a pitch of 0.5 mm with a typical solder mask opening diameter of 0.35 mm, there is only a 0.15 mm distance between the solder mask openings.

An alternative to routing on the top surface is to route out on buried layers. To achieve this, the pads are connected to the lower layers using microvias. See the AN-617 Application Note, *MicroCSP Wafer Level Chip Scale Package* for additional details about the board layout for the WLCSP package.



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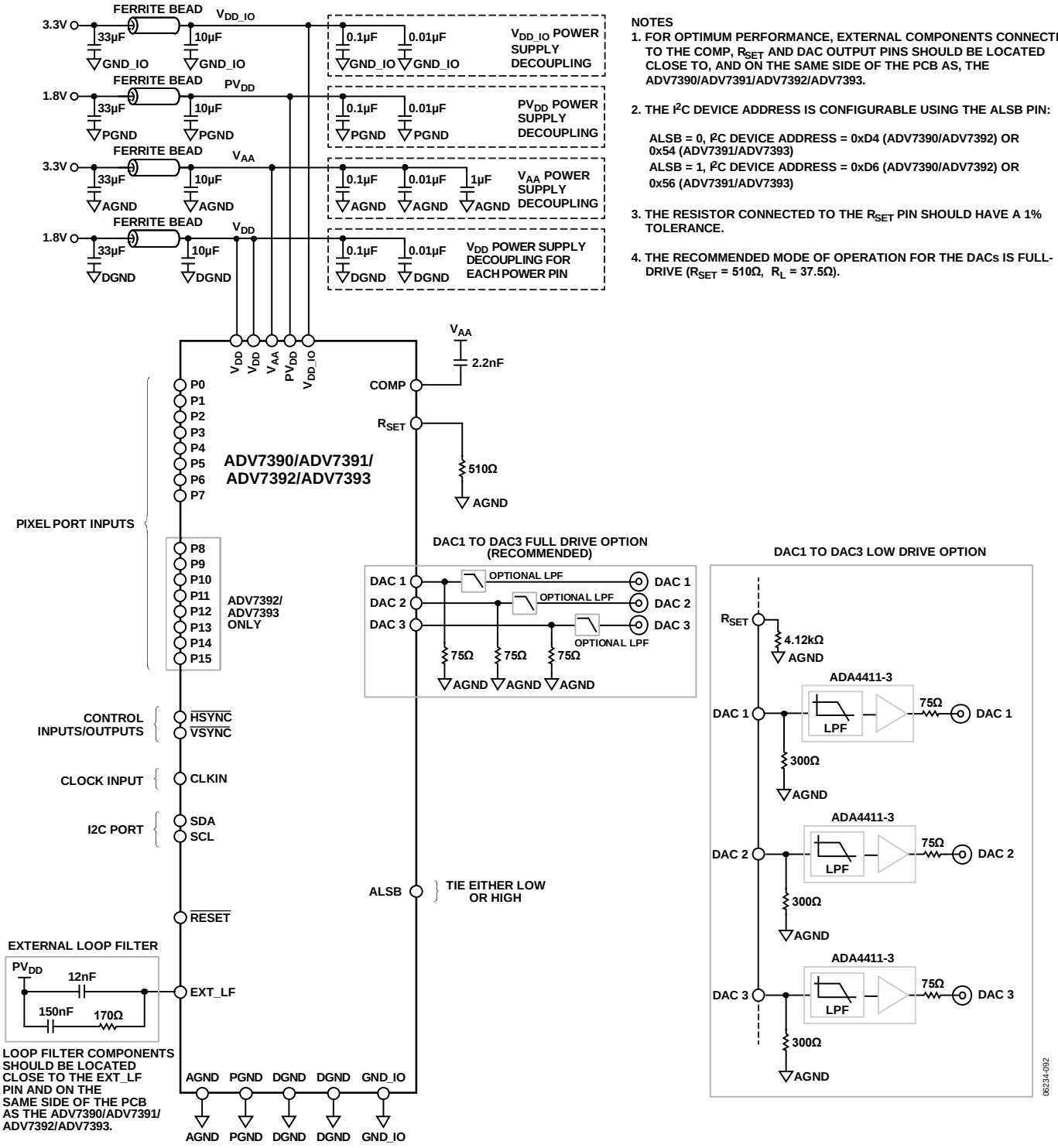
## TYPICAL APPLICATIONS CIRCUITS




NOTES

1. FOR OPTIMUM PERFORMANCE, EXTERNAL COMPONENTS CONNECTED TO THE COMP, $R_{SET}$ AND DAC OUTPUT PINS SHOULD BE LOCATED CLOSE TO, AND ON THE SAME SIDE OF THE PCB AS, THE ADV7390/ADV7391/ADV7392/ADV7393.
2. THE $I^2C$ DEVICE ADDRESS IS CONFIGURABLE USING THE ALSB PIN:

   ALSB = 0, $I^2C$ DEVICE ADDRESS = 0xD4 (ADV7390/ADV7392) OR 0x54 (ADV7391/ADV7393)
   ALSB = 1, $I^2C$ DEVICE ADDRESS = 0xD6 (ADV7390/ADV7392) OR 0x56 (ADV7391/ADV7393)
3. THE RESISTOR CONNECTED TO THE $R_{SET}$ PIN SHOULD HAVE A 1% TOLERANCE.
4. THE RECOMMENDED MODE OF OPERATION FOR THE DACs IS FULL-DRIVE ($R_{SET}$ = 510Ω, $R_L$ = 37.5Ω).

*Figure 93. ADV7390/ADV7391/ADV7392/ADV7393 (LFCSP) Typical Applications Circuit*



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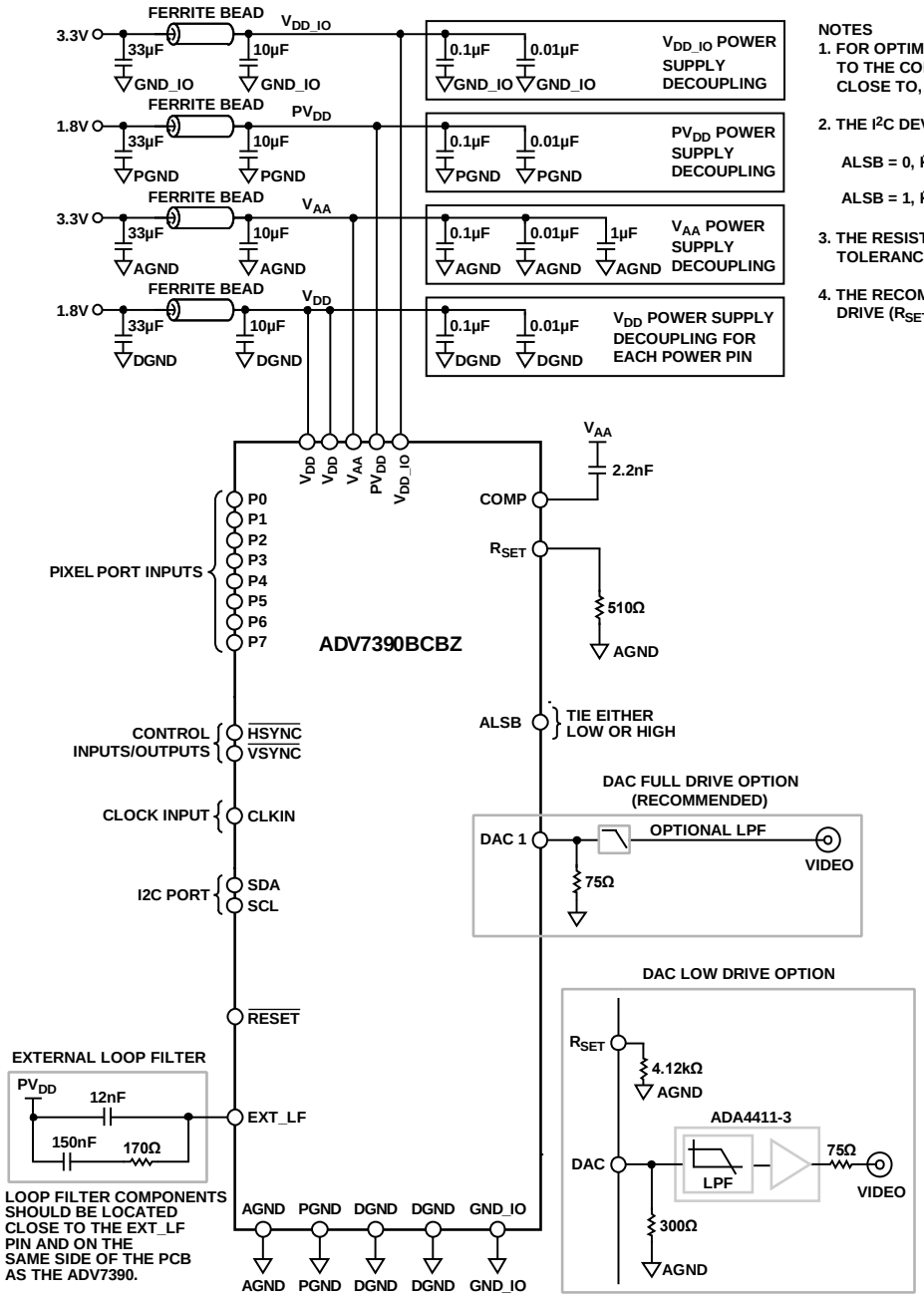


NOTES
1. FOR OPTIMUM PERFORMANCE, EXTERNAL COMPONENTS CONNECTED TO THE COMP, $R_{SET}$ AND DAC OUTPUT PINS SHOULD BE LOCATED CLOSE TO, AND ON THE SAME SIDE OF THE PCB AS, THE ADV7390.
2. THE $I^2C$ DEVICE ADDRESS IS CONFIGURABLE USING THE ALSB PIN:
   ALSB = 0, $I^2C$ DEVICE ADDRESS = 0xD4
   ALSB = 1, $I^2C$ DEVICE ADDRESS = 0xD6
3. THE RESISTOR CONNECTED TO THE $R_{SET}$ PIN SHOULD HAVE A 1% TOLERANCE.
4. THE RECOMMENDED MODE OF OPERATION FOR THE DACs IS FULL-DRIVE ($R_{SET}$ = 510Ω, $R_L$ = 37.5Ω).

*Figure 94. ADV7390BCBZ-A (WLCSP) Typical Applications Circuit*



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# COPY GENERATION MANAGEMENT SYSTEM

## SD CGMS

### *Subaddress 0x99 to Subaddress 0x9B*

The ADV7390/ADV7391/ADV7392/ADV7393 support a copy generation management system (CGMS) that conforms to the EIAJ CPR-1204 and ARIB TR-B15 standards. CGMS data is transmitted on Line 20 of odd fields and Line 283 of even fields. Subaddress 0x99, Bits[6:5] control whether CGMS data is output on odd or even fields or both.

SD CGMS data can be transmitted only when the ADV7390/ADV7391/ADV7392/ADV7393 are configured in NTSC mode. The CGMS data is 20 bits long. The CGMS data is preceded by a reference pulse of the same amplitude and duration as a CGMS bit (see Figure 95).

## ED CGMS

### *Subaddress 0x41 to Subaddress 0x43; Subaddress 0x5E to Subaddress 0x6E*

#### 525p Mode

The ADV7390/ADV7391/ADV7392/ADV7393 support a copy generation management system (CGMS) in 525p mode in accordance with EIAJ CPR-1204-1.

When ED CGMS is enabled (Subaddress 0x32, Bit 6 = 1), 525p CGMS data is inserted on Line 41. The 525p CGMS data registers are at Subaddress 0x41, Subaddress 0x42, and Subaddress 0x43.

The ADV7390/ADV7391/ADV7392/ADV7393 also support CGMS Type B packets in 525p mode in accordance with CEA-805-A.

When ED CGMS Type B is enabled (Subaddress 0x5E, Bit 0 = 1), 525p CGMS Type B data is inserted on Line 40. The 525p CGMS Type B data registers are at Subaddress 0x5E to Subaddress 0x6E.

#### 625p Mode

The ADV7390/ADV7391/ADV7392/ADV7393 support a copy generation management system (CGMS) in 625p mode in accordance with IEC 62375 (2004).

When ED CGMS is enabled (Subaddress 0x32, Bit 6 = 1), 625p CGMS data is inserted on Line 43. The 625p CGMS data registers are at Subaddress 0x42 and Subaddress 0x43.

## HD CGMS

### *Subaddress 0x41 to Subaddress 0x43; Subaddress 0x5E to Subaddress 0x6E*

The ADV7390/ADV7391/ADV7392/ADV7393 support a copy generation management system (CGMS) in HD mode (720p and 1080i) in accordance with EIAJ CPR-1204-2.

When HD CGMS is enabled (Subaddress 0x32, Bit 6 = 1), 720p CGMS data is applied to Line 24 of the luminance vertical blanking interval.

When HD CGMS is enabled (Subaddress 0x32, Bit 6 = 1), 1080i CGMS data is applied to Line 19 and Line 582 of the luminance vertical blanking interval.

The HD CGMS data registers are at Subaddress 0x41, Subaddress 0x42, and Subaddress 0x43.

The ADV7390/ADV7391/ADV7392/ADV7393 also support CGMS Type B packets in HD mode (720p and 1080i) in accordance with CEA-805-A.

When HD CGMS Type B is enabled (Subaddress 0x5E, Bit 0 = 1), 720p CGMS data is applied to Line 23 of the luminance vertical blanking interval.

When HD CGMS Type B is enabled (Subaddress 0x5E, Bit 0 = 1), 1080i CGMS data is applied to Line 18 and Line 581 of the luminance vertical blanking interval.

The HD CGMS Type B data registers are at Subaddress 0x5E to Subaddress 0x6E.

## CGMS CRC FUNCTIONALITY

If SD CGMS CRC (Subaddress 0x99, Bit 4) or ED/HD CGMS CRC (Subaddress 0x32, Bit 7) is enabled, the upper six CGMS data bits (C19 to C14) that comprise the 6-bit CRC check sequence are automatically calculated on the ADV7390/ADV7391/ADV7392/ADV7393. This calculation is based on the lower 14 bits (C13 to C0) of the data in the CGMS data registers, and the result is output with the remaining 14 bits to form the complete 20 bits of the CGMS data. The calculation of the CRC sequence is based on the polynomial $x^6 + x + 1$ with a preset value of 111111.

If SD CGMS CRC or ED/HD CGMS CRC is disabled, all 20 bits (C19 to C0) are output directly from the CGMS registers (CRC must be calculated by the user manually).

If ED/HD CGMS Type B CRC (Subaddress 0x5E, Bit 1) is enabled, the upper six CGMS Type B data bits (P122 to P127) that comprise the 6-bit CRC check sequence are automatically calculated on the ADV7390/ADV7391/ADV7392/ADV7393. This calculation is based on the lower 128 bits (H0 to H5 and P0 to P121) of the data in the CGMS Type B data registers. The result is output with the remaining 128 bits to form the complete 134 bits of the CGMS Type B data. The calculation of the CRC sequence is based on the polynomial $x^6 + x + 1$ with a preset value of 111111.

If ED/HD CGMS Type B CRC is disabled, all 134 bits (H0 to H5 and P0 to P127) are output directly from the CGMS Type B registers (CRC must be calculated by the user manually).



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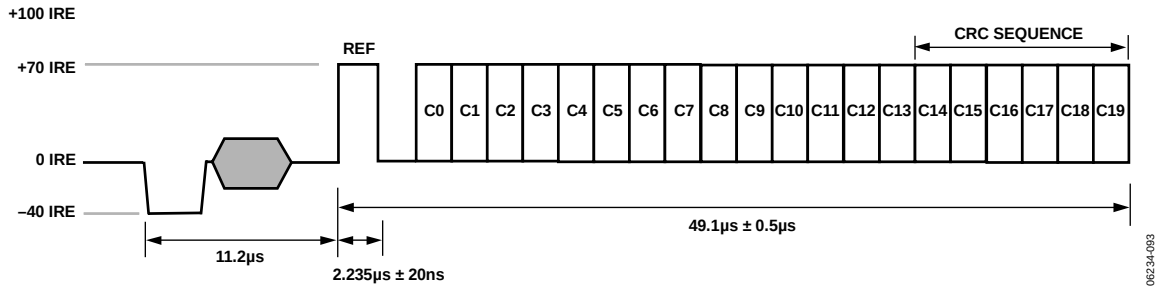


*Figure 95. Standard Definition CGMS Waveform*

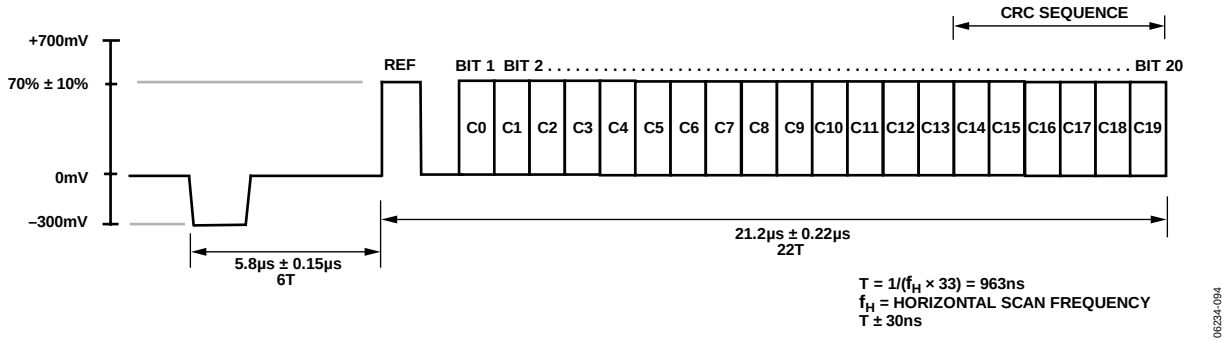


*Figure 96. Enhanced Definition (525p) CGMS Waveform*

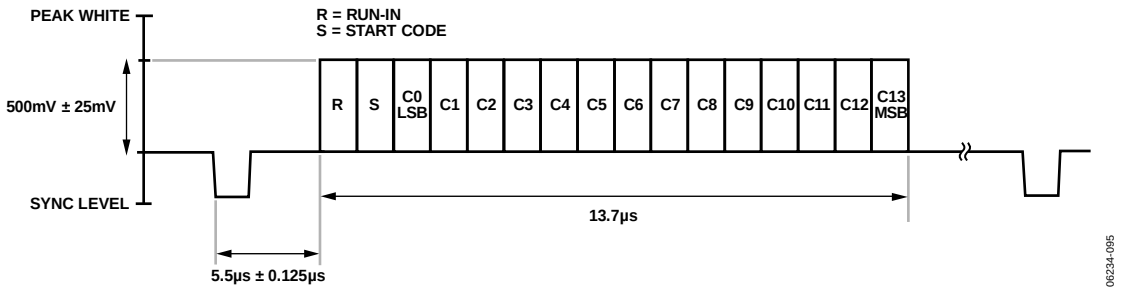


*Figure 97. Enhanced Definition (625p) CGMS Waveform*

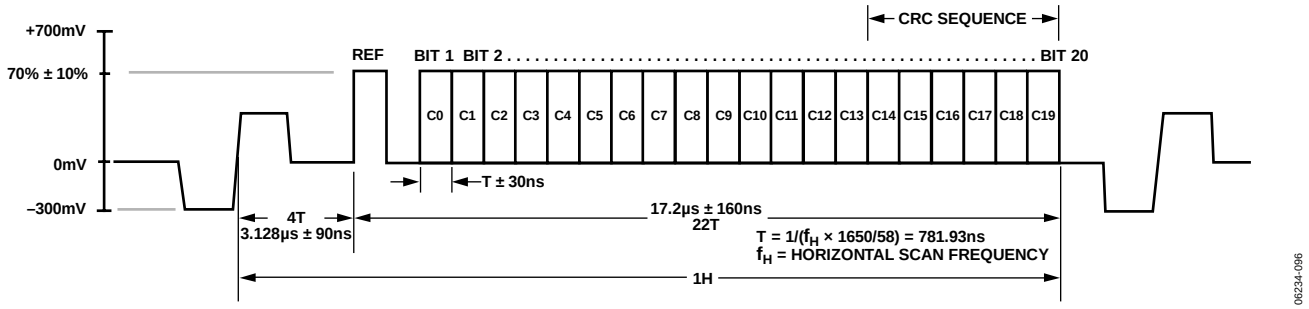


*Figure 98. High Definition (720p) CGMS Waveform*



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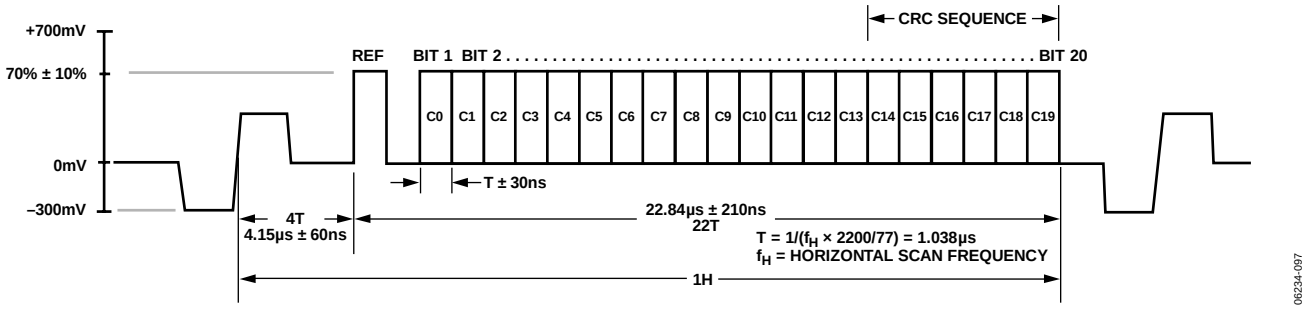
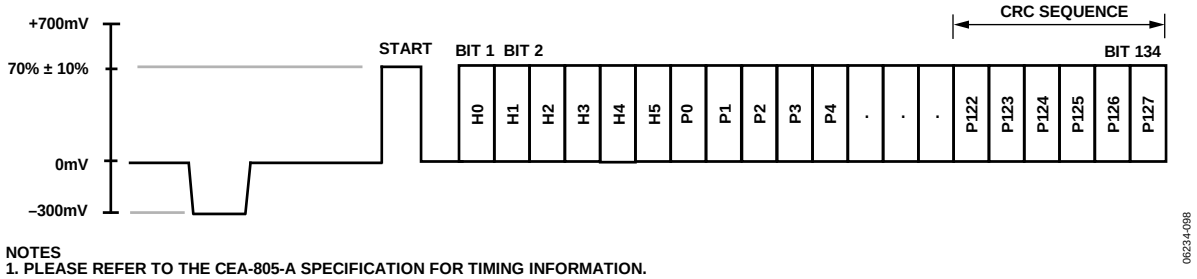
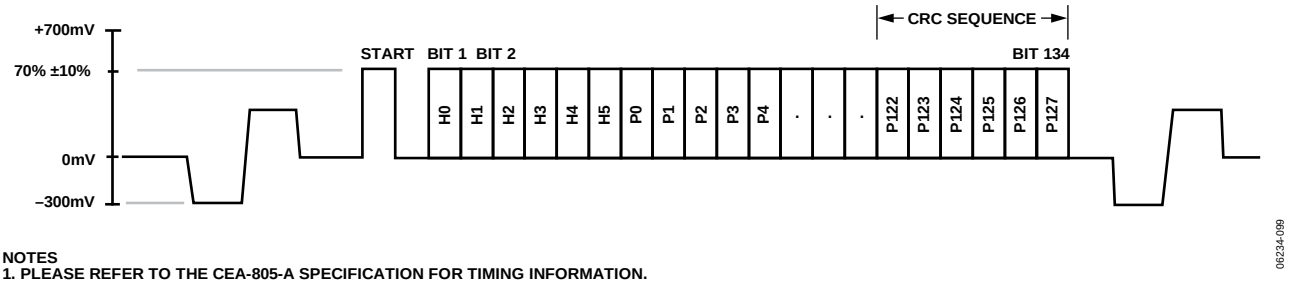



*Figure 99. High Definition (1080i) CGMS Waveform*




NOTES
1. PLEASE REFER TO THE CEA-805-A SPECIFICATION FOR TIMING INFORMATION.

*Figure 100. Enhanced Definition (525p) CGMS Type B Waveform*




NOTES
1. PLEASE REFER TO THE CEA-805-A SPECIFICATION FOR TIMING INFORMATION.

*Figure 101. High Definition (720p and 1080i) CGMS Type B Waveform*



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# SD WIDE SCREEN SIGNALING

***Subaddress 0x99, Subaddress 0x9A, Subaddress 0x9B***

The ADV7390/ADV7391/ADV7392/ADV7393 support wide screen signaling (WSS) con-forming to the ETSI 300 294 standard. WSS data is transmitted on Line 23. WSS data can be transmitted only when the device is configured in PAL mode. The WSS data is 14 bits long. The function of each of these bits is shown in Table 59. The WSS data is preceded by a run-in sequence and a start code (see Figure 102). The latter portion of Line 23 (after 42.5 µs from the falling edge of HSYNC) is available for the insertion of video. WSS data transmission on Line 23 can be enabled using Subaddress 0x99, Bit 7. It is possible to blank the WSS portion of Line 23 with Subaddress 0xA1, Bit 7.

**Table 59. Function of WSS Bits**

| | Bit Number | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Bit Description** | **13** | **12** | **11** | **10** | **9** | **8** | **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** | **Setting** |
| Aspect Ratio, Format, Position | | | | | | | | | | | 1 | 0 | 0 | 0 | 4:3, full format, N/A |
| | | | | | | | | | | | 0 | 0 | 0 | 1 | 14:9, letterbox, center |
| | | | | | | | | | | | 0 | 0 | 1 | 0 | 14:9, letterbox, top |
| | | | | | | | | | | | 1 | 0 | 1 | 1 | 16:9, letterbox, center |
| | | | | | | | | | | | 0 | 1 | 0 | 0 | 16:9, letterbox, top |
| | | | | | | | | | | | 1 | 1 | 0 | 1 | >16:9, letterbox, center |
| | | | | | | | | | | | 1 | 1 | 1 | 0 | 14:9, full format, center |
| | | | | | | | | | | | 0 | 1 | 1 | 1 | 16:0, N/A, N/A |
| Mode | | | | | | | | | | 0 | | | | | Camera mode |
| | | | | | | | | | | 1 | | | | | Film mode |
| Color Encoding | | | | | | | | | 0 | | | | | | Normal PAL |
| | | | | | | | | | 1 | | | | | | Motion Adaptive ColorPlus |
| Helper Signals | | | | | | | | 0 | | | | | | | Not present |
| | | | | | | | | 1 | | | | | | | Present |
| Reserved | | | | | | | 0 | | | | | | | | N/A |
| Teletext Subtitles | | | | | | 0 | | | | | | | | | No |
| | | | | | | 1 | | | | | | | | | Yes |
| Open Subtitles | | | | 0 | 0 | | | | | | | | | | No |
| | | | | 0 | 1 | | | | | | | | | | Subtitles in active image area |
| | | | | 1 | 0 | | | | | | | | | | Subtitles out of active image area |
| | | | | 1 | 1 | | | | | | | | | | Reserved |
| Surround Sound | | | 0 | | | | | | | | | | | | No |
| | | | 1 | | | | | | | | | | | | Yes |
| Copyright | | 0 | | | | | | | | | | | | | No copyright asserted or unknown |
| | | 1 | | | | | | | | | | | | | Copyright asserted |
| Copy Protection | 0 | | | | | | | | | | | | | | Copying not restricted |
| | 1 | | | | | | | | | | | | | | Copying restricted |

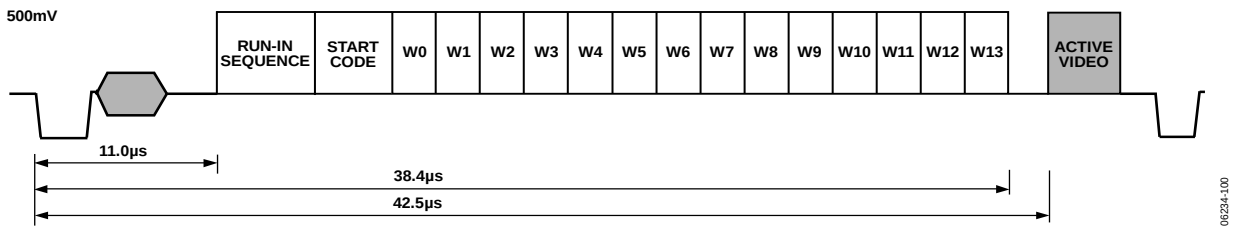


*Figure 102. WSS Waveform Diagram*



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# SD CLOSED CAPTIONING

### *Subaddress 0x91 to Subaddress 0x94*

The ADV7390/ADV7391/ADV7392/ADV7393 support closed captioning conforming to the standard television synchronizing waveform for color trans-mission. When enabled, closed captioning is transmitted during the blanked active line time of Line 21 of the odd fields and Line 284 of the even fields. Closed captioning can be enabled using Subaddress 0x83, Bits[6:5].

Closed captioning consists of a seven-cycle sinusoidal burst that is frequency- and phase-locked to the caption data. After the clock run-in signal, the blanking level is held for two data bits and is followed by a Logic 1 start bit. Sixteen bits of data follow the start bit. The data consists of two 8-bit bytes (seven data bits and one odd parity bit per byte). The data for these bytes is stored in SD closed captioning registers (Subaddress 0x93 to Subaddress 0x94).

The ADV7390/ADV7391/ADV7392/ADV7393 also support the extended closed captioning operation, which is active during even fields and encoded on Line 284. The data for this operation is stored in SD closed captioning registers (Subaddress 0x91 to Subaddress 0x92).

The ADV7390/ADV7391/ADV7392/ADV7393 automatically generate all clock run-in signals and timing that support closed captioning on Line 21 and Line 284. All pixels inputs are ignored on Line 21 and Line 284 if closed captioning is enabled.

The FCC Code of Federal Regulations (CFR) Title 47 Section 15.119 and EIA-608 describe the closed captioning information for Line 21 and Line 284.

The ADV7390/ADV7391/ADV7392/ADV7393 use a single buffering method. This means that the closed captioning buffer is only 1-byte deep. Therefore, there is no frame delay in outputting the closed captioning data, unlike other 2-byte deep buffering systems. The data must be loaded one line before it is output on Line 21 and Line 284. A typical implementation of this method is to use $\overline{\text{VSYNC}}$ to interrupt a microprocessor, which in turn loads the new data (two bytes) in every field. If no new data is required for transmission, 0s must be inserted in both data registers; this is called nulling. It is also important to load control codes, all of which are double bytes, on Line 21. Otherwise, a TV does not recognize them. If there is a message such as "Hello World" that has an odd number of characters, it is important to add a blank character at the end to make sure that the end-of-caption, 2-byte control code lands in the same field.

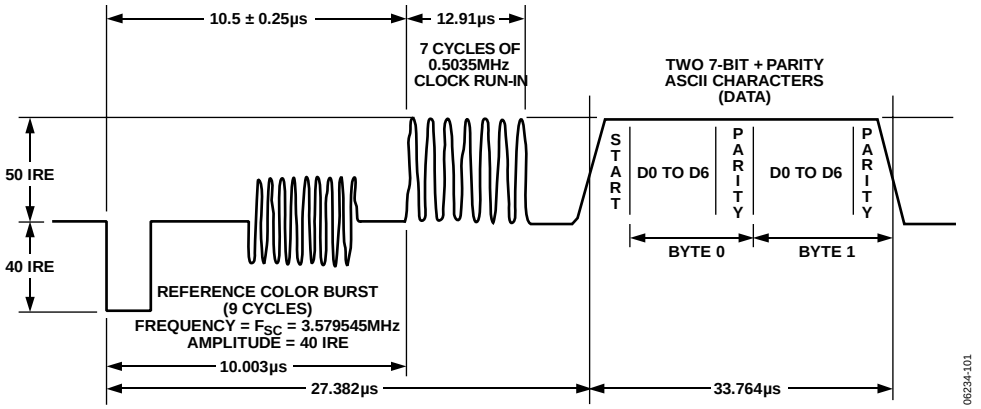


*Figure 103. SD Closed Captioning Waveform, NTSC*



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# INTERNAL TEST PATTERN GENERATION

## SD TEST PATTERNS

The ADV7390/ADV7391/ADV7392/ADV7393 are able to internally generate SD color bar and black bar test patterns. For this function, a 27 MHz clock signal must be applied to the CLKIN pin.

The register settings in Table 60 are used to generate an SD NTSC 75% color bar test pattern. All other registers are set as normal/default. Component YPrPb output is available on DAC 1 to DAC 3. On power-up, the subcarrier frequency registers default to the appropriate values for NTSC.

**Table 60. SD NTSC Color Bar Test Pattern Register Writes**

| Subaddress | Setting |
|---|---|
| 0x00 | 0x1C |
| 0x82 | 0xC9 |
| 0x84 | 0x40 |

For CVBS and S-Video (Y/C) output, 0xCB instead of 0xC9 should be written to Subaddress 0x82.

For component RGB output rather than YPrPb output, 0 should be written to Subaddress 0x02, Bit 5.

To generate an SD NTSC black bar test pattern, the settings shown in Table 60 should be used with an additional write of 0x24 to Subaddress 0x02.

For PAL output of either test pattern, the same settings are used except that Subaddress 0x80 is programmed to 0x11, and the subcarrier frequency ($F_{SC}$) registers are programmed as shown in Table 61.

**Table 61. PAL $F_{SC}$ Register Writes**

| Subaddress | Description | Setting |
|---|---|---|
| 0x8C | $F_{SC}0$ | 0xCB |
| 0x8D | $F_{SC}1$ | 0x8A |
| 0x8E | $F_{SC}2$ | 0x09 |
| 0x8F | $F_{SC}3$ | 0x2A |

Note that, when programming the $F_{SC}$ registers, the user must write the values in the sequence $F_{SC}0$, $F_{SC}1$, $F_{SC}2$, $F_{SC}3$. The full $F_{SC}$ value to be written is only accepted after the $F_{SC}3$ write is complete.

## ED/HD TEST PATTERNS

The ADV7390/ADV7391/ADV7392/ADV7393 are able to internally generate ED/HD color bar, black bar, and hatch test patterns. For ED test patterns, a 27 MHz clock signal must be applied to the CLKIN pin. For HD test patterns, a 74.25 MHz clock signal must be applied to the CLKIN pin.

The register settings in Table 62 are used to generate an ED 525p hatch test pattern. All other registers are set as normal/default. Component YPrPb output is available on DAC 1 to DAC 3. For component RGB output rather than YPrPb output, 0 should be written to Subaddress 0x02, Bit 5.

**Table 62. ED 525p Hatch Test Pattern Register Writes**

| Subaddress | Setting |
|---|---|
| 0x00 | 0x1C |
| 0x01 | 0x10 |
| 0x31 | 0x05 |

To generate an ED 525p black bar test pattern, the settings shown in Table 62 should be used with an additional write of 0x24 to Subaddress 0x02.

To generate an ED 525p flat field test pattern, the settings shown in Table 62 should be used, except that 0x0D should be written to Subaddress 0x31.

The Y, Cr, and Cb levels for the hatch and flat field test patterns can be controlled using Subaddress 0x36, Subaddress 0x37, and Subaddress 0x38, respectively.

For ED/HD standards other than 525p, the settings shown in Table 62 (and subsequent comments) are used, except that Subaddress 0x30, Bits[7:3] are updated as appropriate.



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# SD TIMING

### *Mode 0 (CCIR-656)—Slave Option (Subaddress 0x8A = X X X X X 0 0 0)*

The ADV7390/ADV7391/ADV7392/ADV7393 are controlled by the SAV (start of active video) and EAV (end of active video) time codes embedded in the pixel data. All timing information is transmitted using a 4-byte synchronization pattern. A synchronization pattern is sent immediately before and after each line during active picture and retrace. If the $\overline{\text{VSYNC}}$ and $\overline{\text{HSYNC}}$ pins are not used, they should be tied to $V_{DD_IO}$ when using this mode.

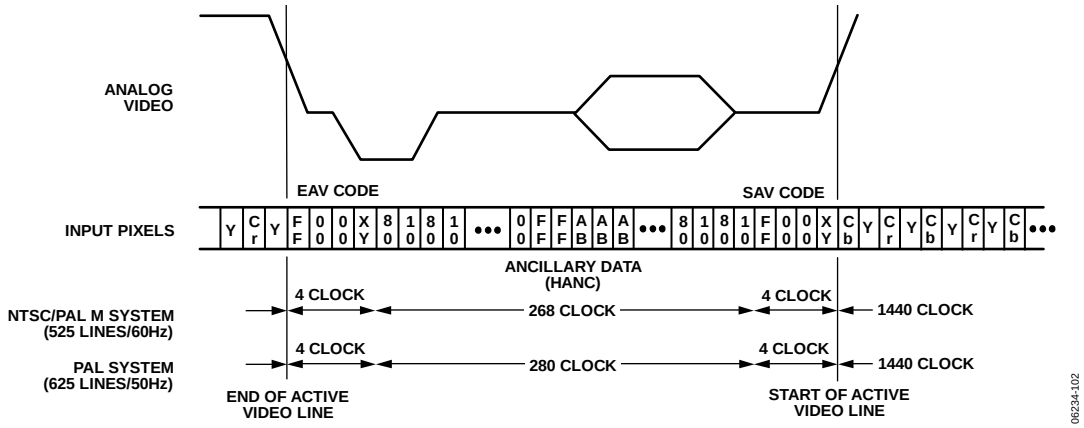


*Figure 104. SD Timing Mode 0, Slave Option*

### *Mode 0 (CCIR-656)—Master Option (Subaddress 0x8A = X X X X X 0 0 1)*

The ADV7390/ADV7391/ADV7392/ADV7393 generate H and F signals required for the SAV and EAV time codes in the CCIR-656 standard. The H bit is output on $\overline{\text{HSYNC}}$ and the F bit is output on $\overline{\text{VSYNC}}$.

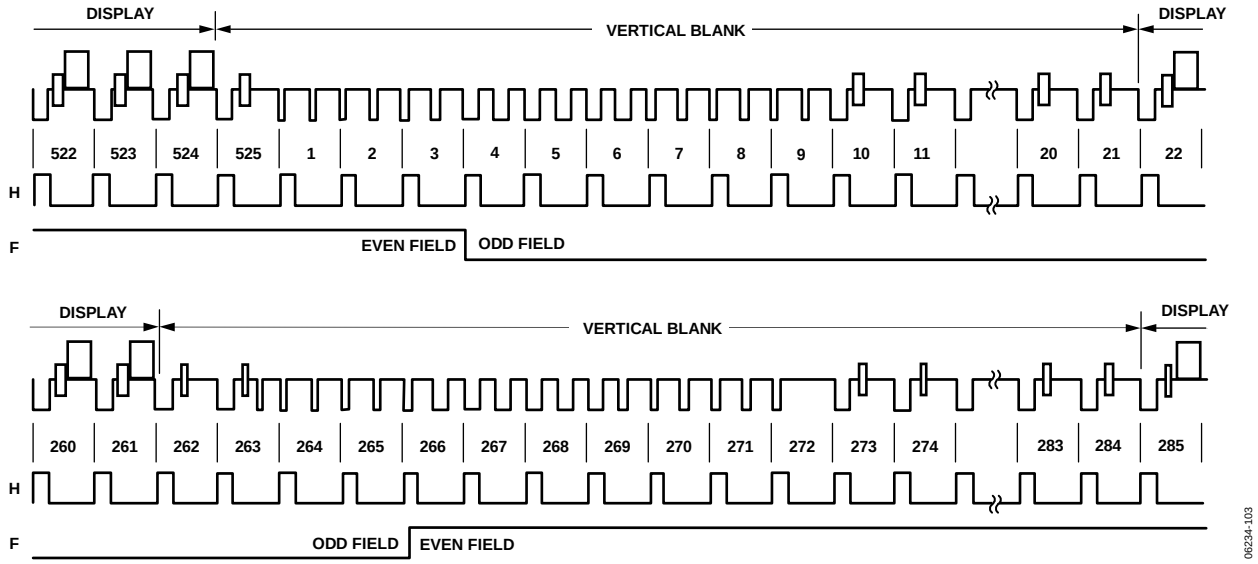


*Figure 105. SD Timing Mode 0, Master Option, NTSC*



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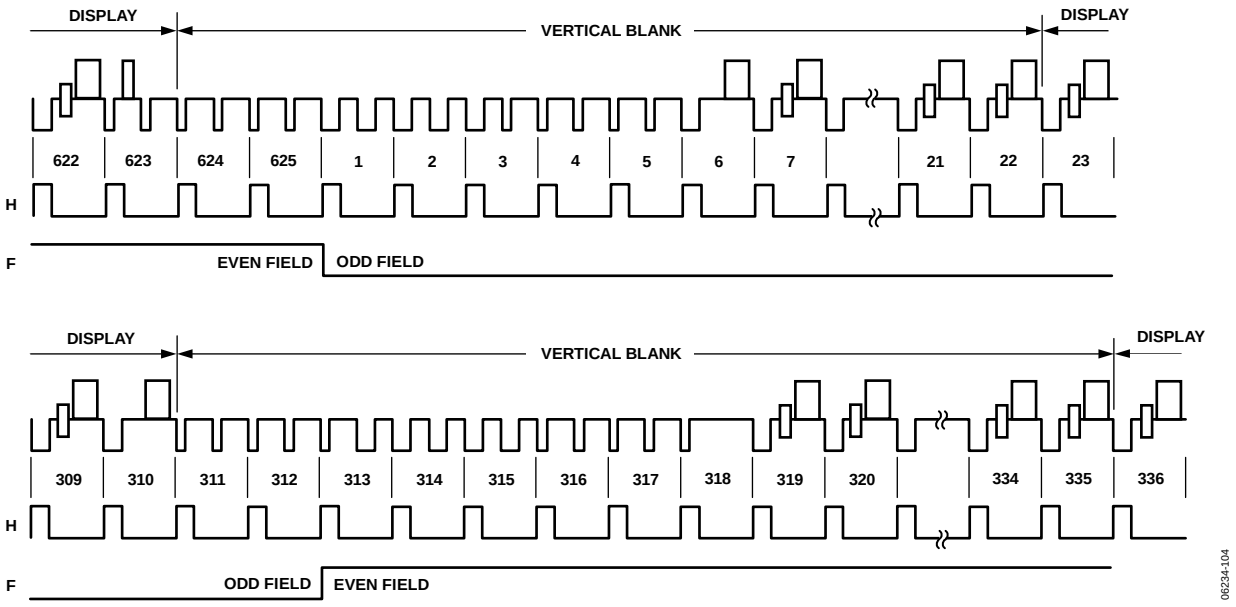


*Figure 106. SD Timing Mode 0, Master Option, PAL*

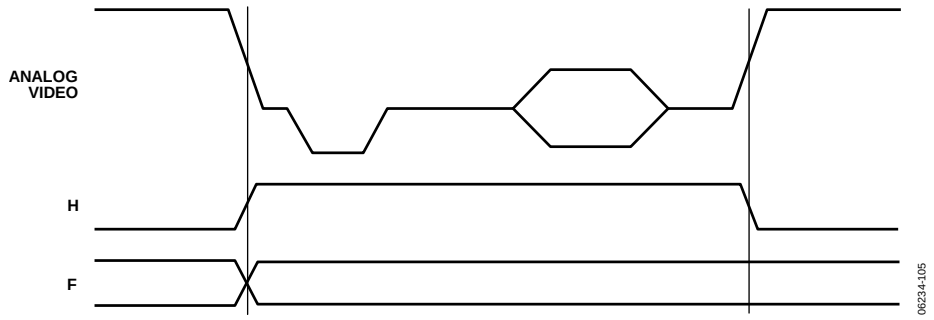


*Figure 107. SD Timing Mode 0, Master Option, Data Transitions*

### *Mode 1—Slave Option (Subaddress 0x8A = X X X X X 0 1 0)*

In this mode, the ADV7390/ADV7391/ADV7392/ADV7393 accept horizontal synchronization and odd/even field signals. When $\overline{\text{HSYNC}}$ is low, a transition of the field input indicates a new frame, that is, vertical retrace. $\overline{\text{HSYNC}}$ and FIELD are input on the $\overline{\text{HSYNC}}$ and $\overline{\text{VSYNC}}$ pins, respectively.

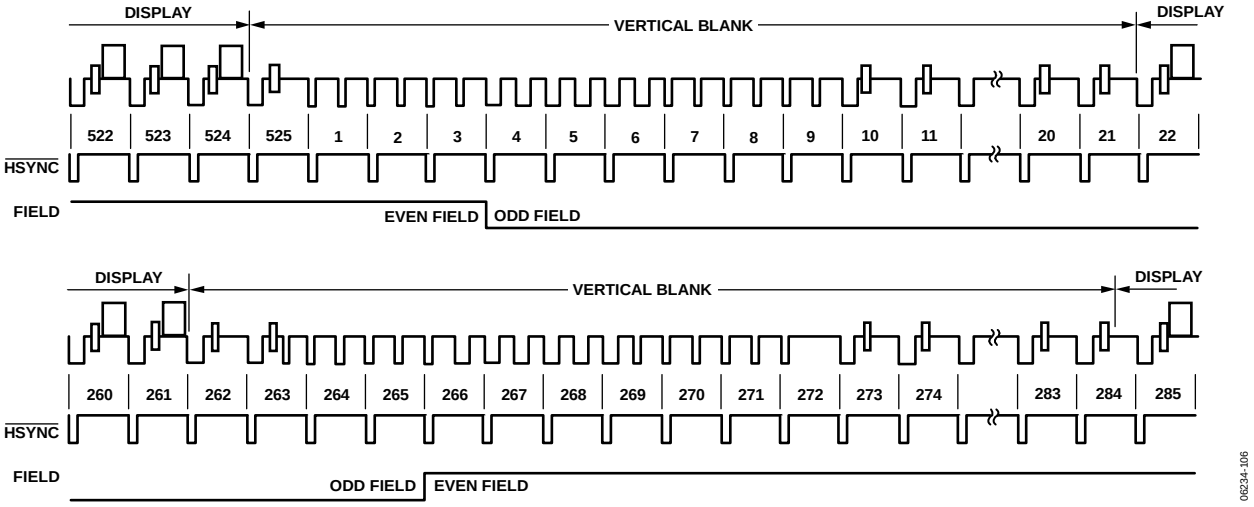


*Figure 108. SD Timing Mode 1, Slave Option, NTSC*



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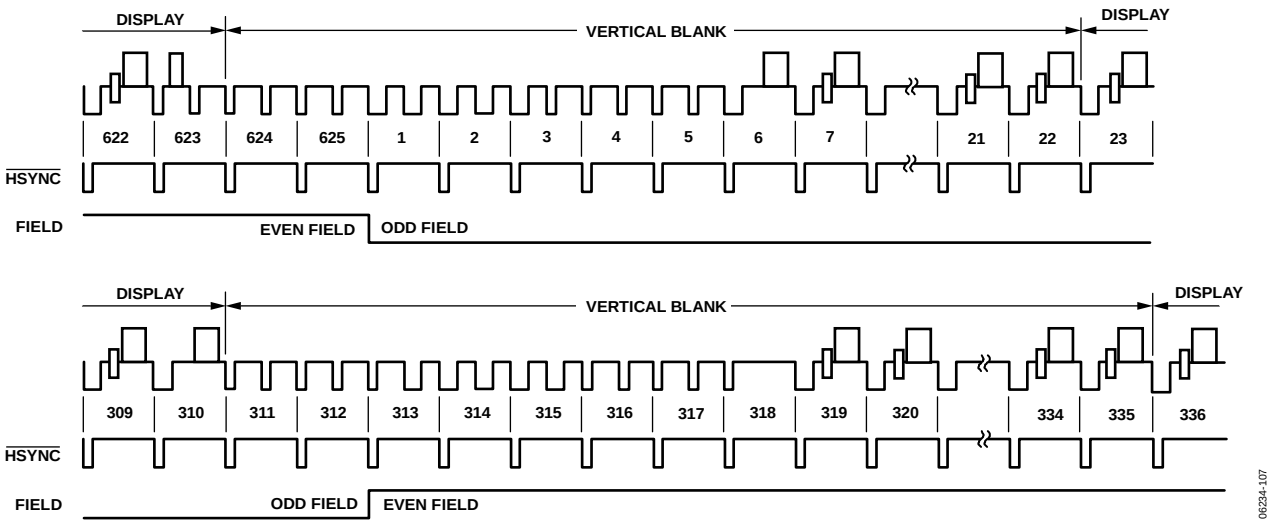


*Figure 109. SD Timing Mode 1, Slave Option, PAL*

### *Mode 1—Master Option (Subaddress 0x8A = X X X X X 0 1 1)*

In this mode, the ADV7390/ADV7391/ADV7392/ADV7393 can generate horizontal synchronization and odd/even field signals. When $\overline{\text{HSYNC}}$ is low, a transition of the field input indicates a new frame, that is, vertical retrace. The ADV7390/ADV7391/ADV7392/ADV7393 automatically blank all normally blank lines as required by the CCIR-624 standard. Pixel data is latched on the rising clock edge following the timing signal transitions. $\overline{\text{HSYNC}}$ and FIELD are output on the $\overline{\text{HSYNC}}$ and $\overline{\text{VSYNC}}$ pins, respectively.

*Figure 110. SD Timing Mode 1, Odd/Even Field Transitions (Master/Slave)*

### *Mode 2— Slave Option (Subaddress 0x8A = X X X X X 1 0 0)*

In this mode, the ADV7390/ADV7391/ADV7392/ADV7393 accept horizontal and vertical synchronization signals. A coincident low transition of both $\overline{\text{HSYNC}}$ and $\overline{\text{VSYNC}}$ inputs indicates the start of an odd field. A $\overline{\text{VSYNC}}$ low transition when $\overline{\text{HSYNC}}$ is high indicates the start of an even field. The ADV7390/ADV7391/ADV7392/ADV7393 automatically blank all normally blank lines as required by the CCIR-624 standard. $\overline{\text{HSYNC}}$ and $\overline{\text{VSYNC}}$ are input on the $\overline{\text{HSYNC}}$ and $\overline{\text{VSYNC}}$ pins, respectively.



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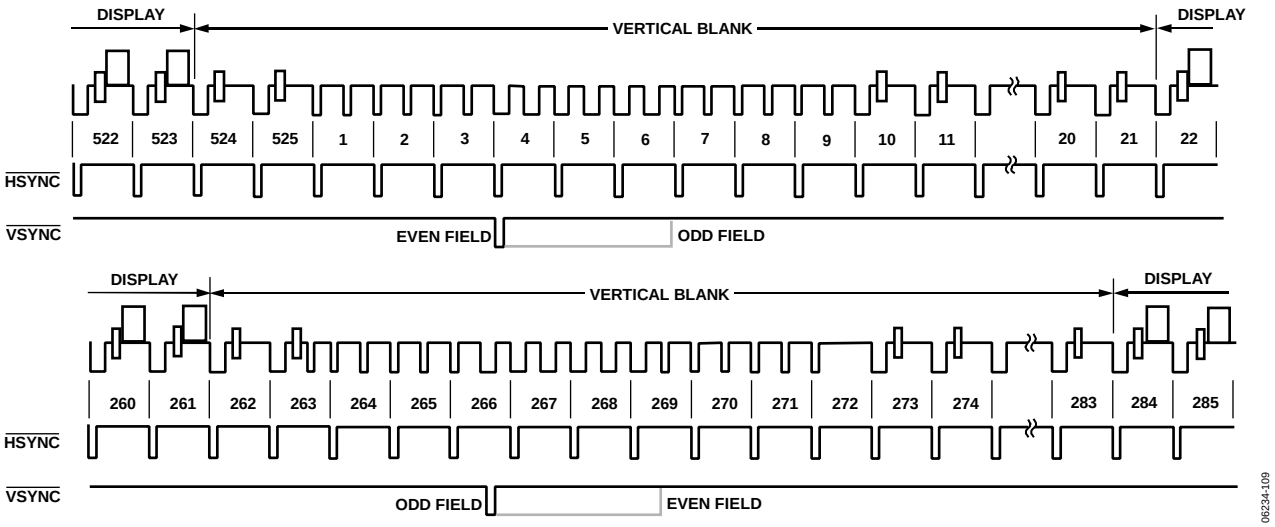


*Figure 111. SD Timing Mode 2, Slave Option, NTSC*

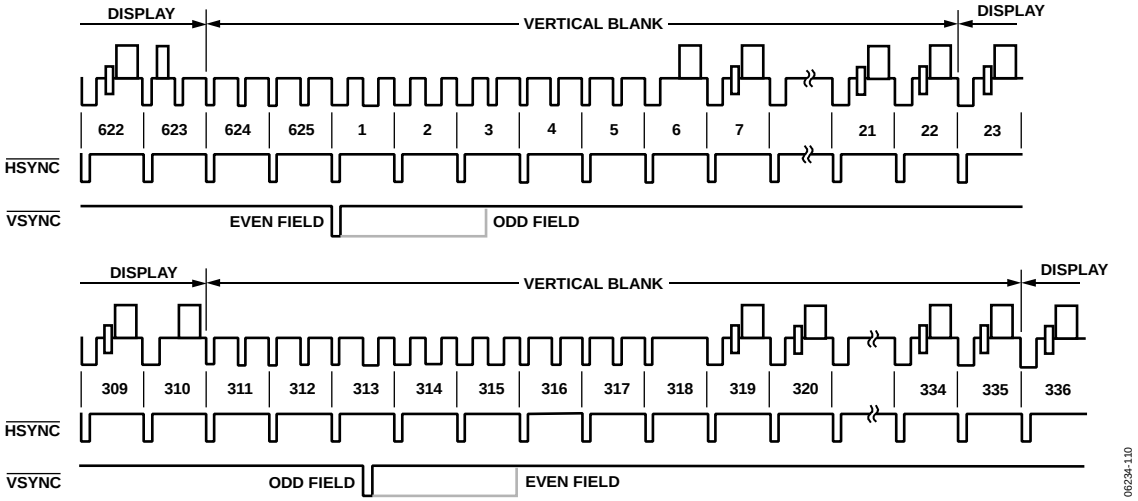


*Figure 112. SD Timing Mode 2, Slave Option, PAL*

### *Mode 2—Master Option (Subaddress 0x8A = X X X X X 1 0 1)*

In this mode, the ADV7390/ADV7391/ADV7392/ADV7393 can generate horizontal and vertical synchronization signals. A coincident low transition of both $\overline{\text{HSYNC}}$ and $\overline{\text{VSYNC}}$ inputs indicates the start of an odd field. A $\overline{\text{VSYNC}}$ low transition when $\overline{\text{HSYNC}}$ is high indicates the start of an even field. The ADV7390/ADV7391/ADV7392/ADV7393 automatically blank all normally blank lines as required by the CCIR-624 standard. $\overline{\text{HSYNC}}$ and $\overline{\text{VSYNC}}$ are output on the $\overline{\text{HSYNC}}$ and $\overline{\text{VSYNC}}$ pins, respectively.

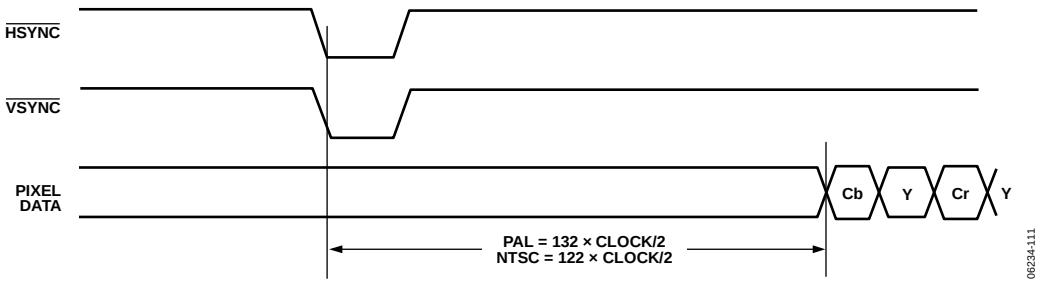


*Figure 113. SD Timing Mode 2, Even-to-Odd Field Transition (Master/Slave)*



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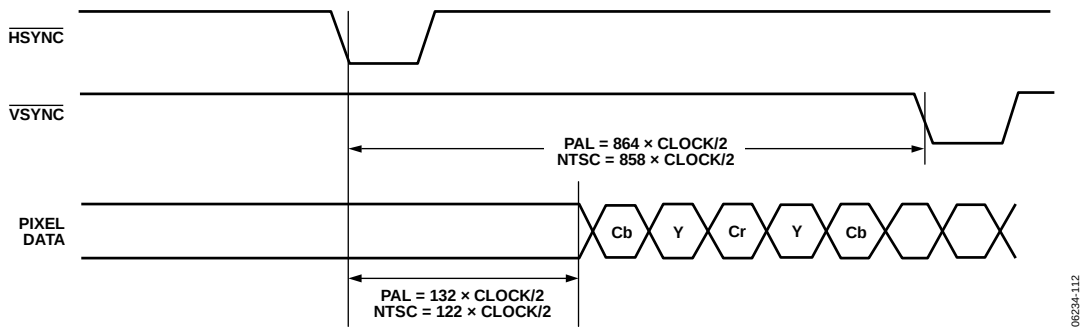


*Figure 114. SD Timing Mode 2, Odd-to-Even Field Transition (Master/Slave)*

### *Mode 3—Master/Slave Option (Subaddress 0x8A = X X X X X 1 1 0 or X X X X X 1 1 1)*

In this mode, the ADV7390/ADV7391/ADV7392/ADV7393 accept or generates horizontal synchronization and odd/even field signals. When $\overline{\text{HSYNC}}$ is high, a transition of the field input indicates a new frame, that is, vertical retrace. The ADV7390/ADV7391/ADV7392/ADV7393 automatically blank all normally blank lines as required by the CCIR-624 standard. $\overline{\text{HSYNC}}$ and $\overline{\text{VSYNC}}$ are output in master mode and input in slave mode on the $\overline{\text{HSYNC}}$ and $\overline{\text{VSYNC}}$ pins, respectively.

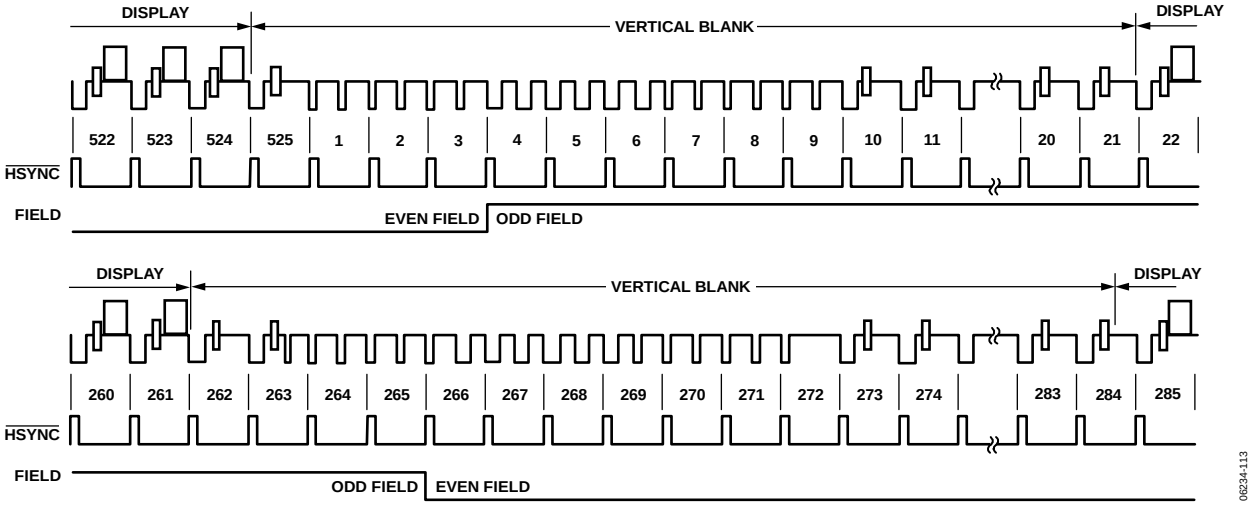


*Figure 115. SD Timing Mode 3, NTSC*

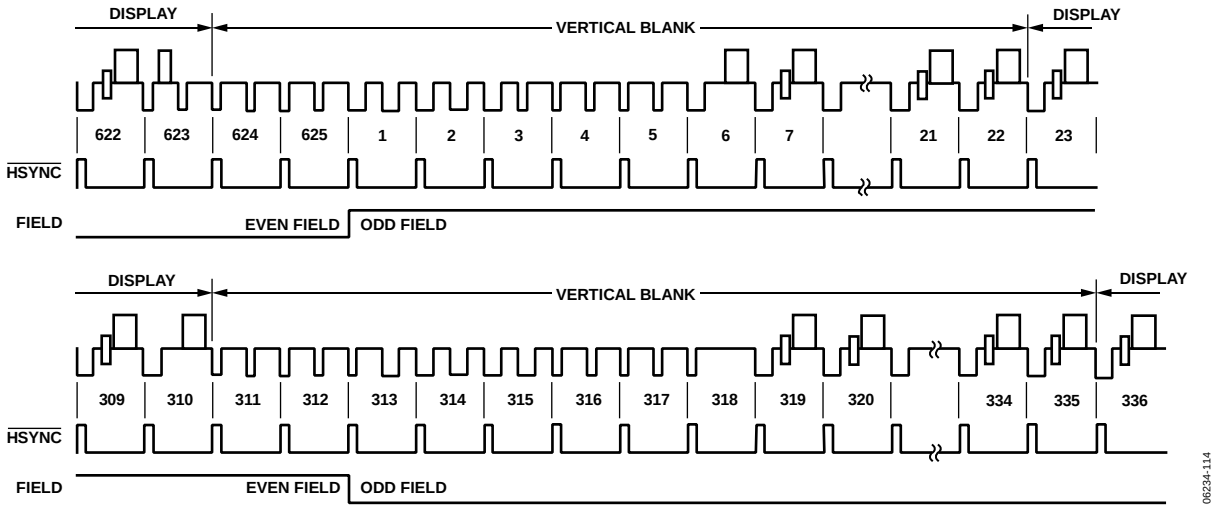


*Figure 116. SD Timing Mode 3, PAL*



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## HD TIMING

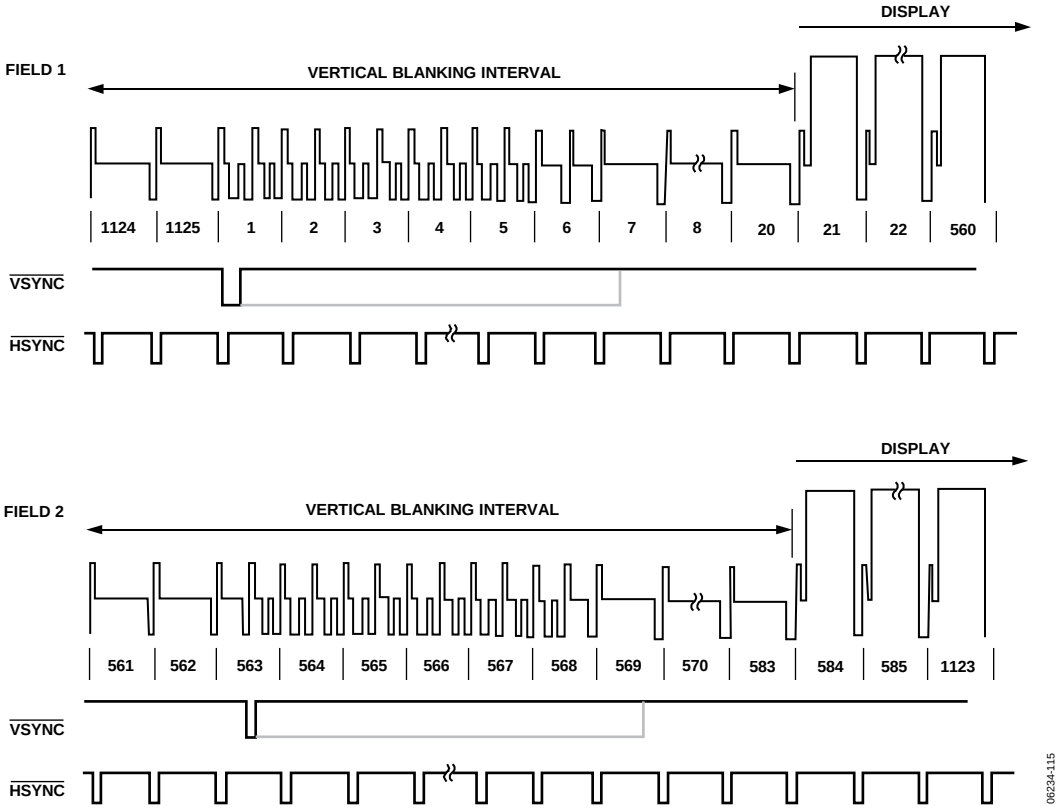


*Figure 117. 1080i $\overline{HSYNC}$ and $\overline{VSYNC}$ Input Timing*



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# VIDEO OUTPUT LEVELS

## SD YPrPb OUTPUT LEVELS—SMPTE/EBU N10

***Pattern: 100% Color Bars***

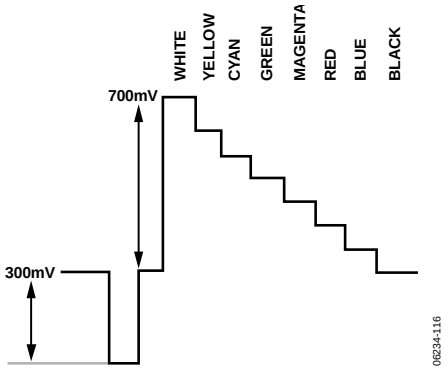


*Figure 118. Y Levels—NTSC*

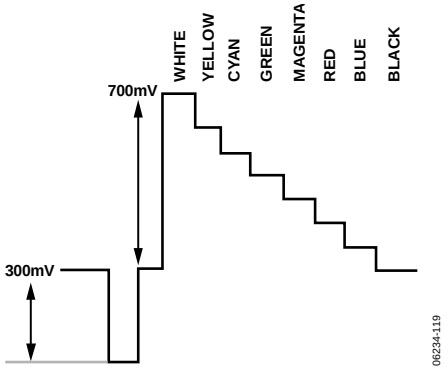


*Figure 121. Y Levels—PAL*

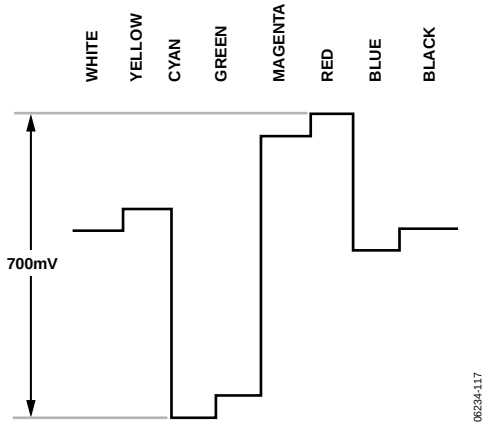


*Figure 119. Pr Levels—NTSC*

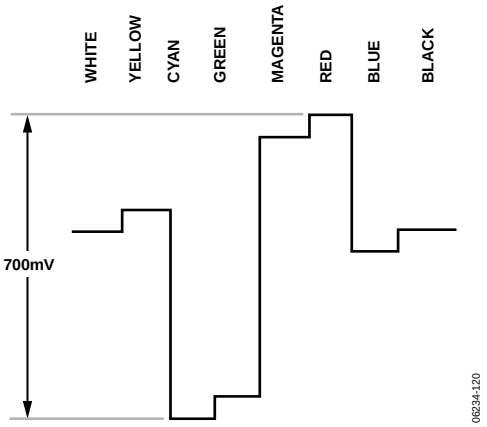


*Figure 122. Pr Levels—PAL*

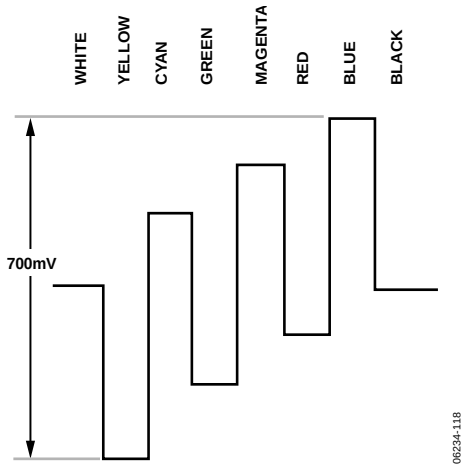


*Figure 120. Pb Levels—NTSC*

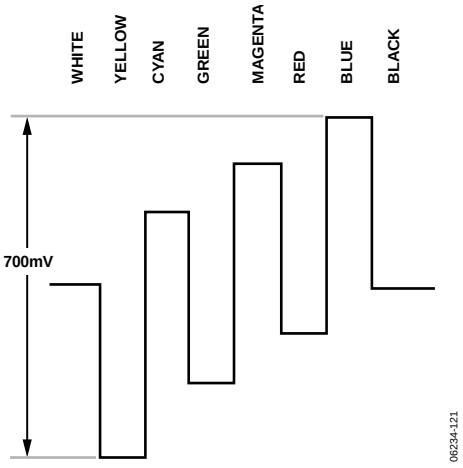


*Figure 123. Pb Levels—PAL*



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## ED/HD YPrPb OUTPUT LEVELS

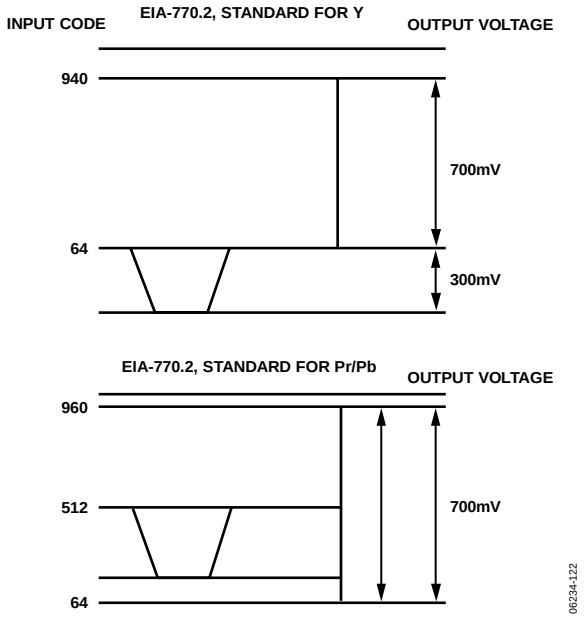


*Figure 124. EIA-770.2 Standard Output Signals (525p/625p)*

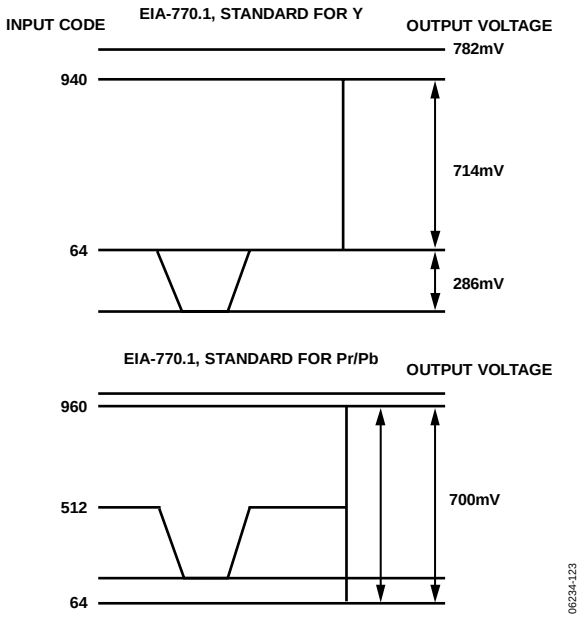


*Figure 125. EIA-770.1 Standard Output Signals (525p/625p)*

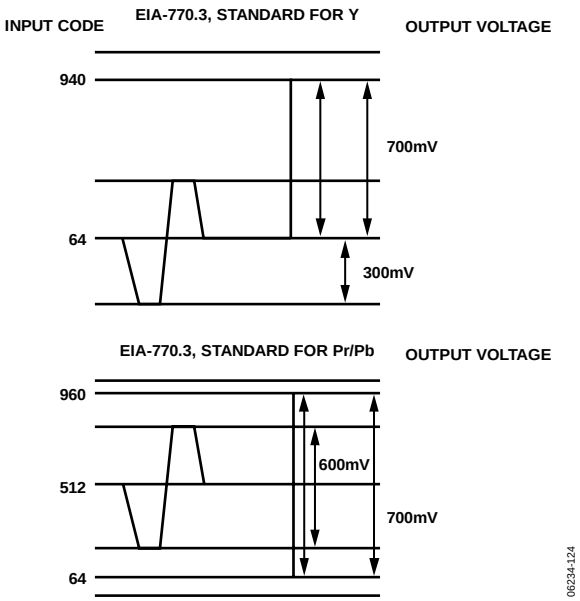


*Figure 126. EIA-770.3 Standard Output Signals (1080i/720p)*

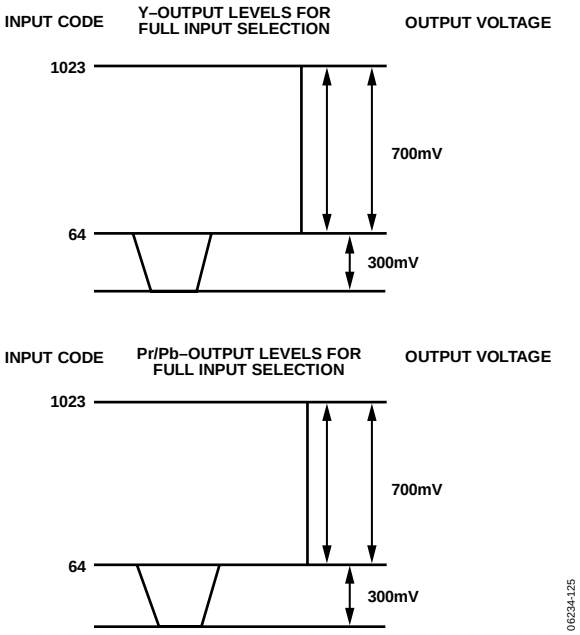


*Figure 127. Output Levels for Full Input Selection*



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## SD/ED/HD RGB OUTPUT LEVELS

***Pattern: 100%/75% Color Bars***

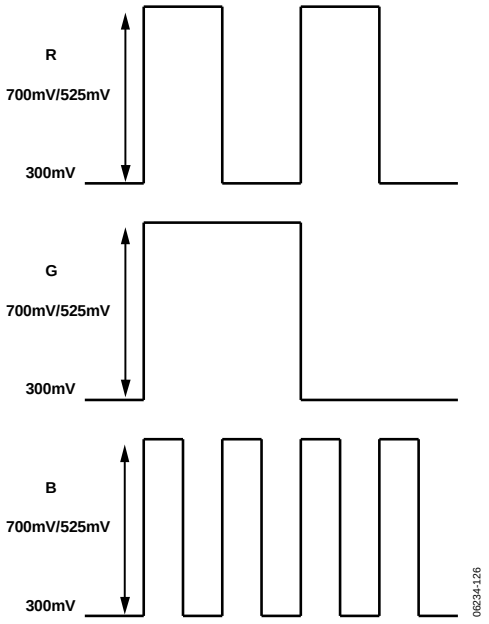


*Figure 128. SD/ED RGB Output Levels—RGB Sync Disabled*

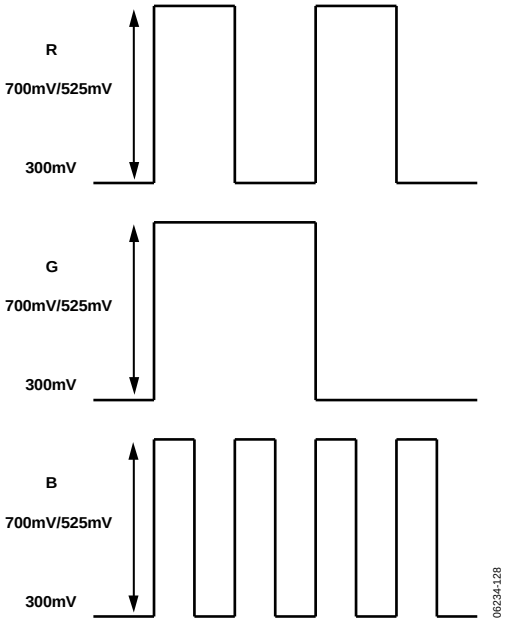


*Figure 130. HD RGB Output Levels—RGB Sync Disabled*

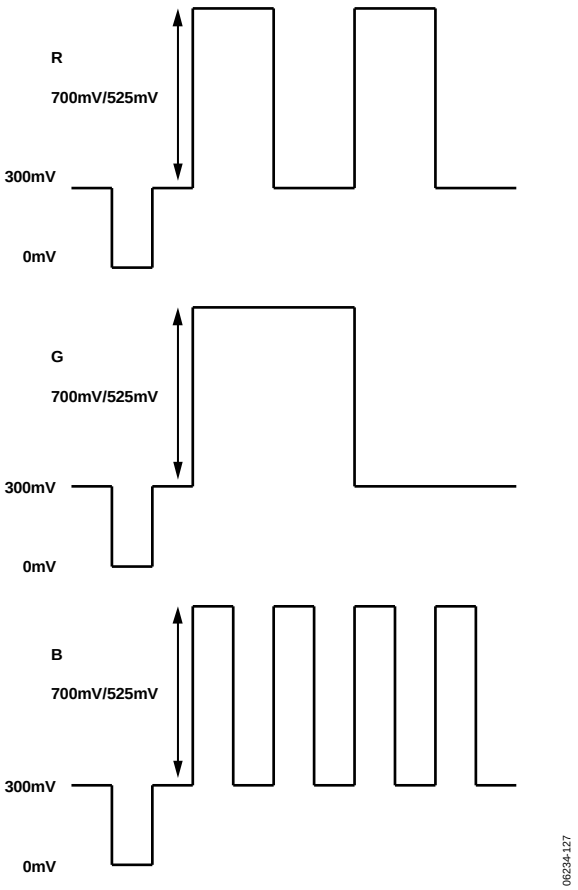


*Figure 129. SD/ED RGB Output Levels—RGB Sync Enabled*

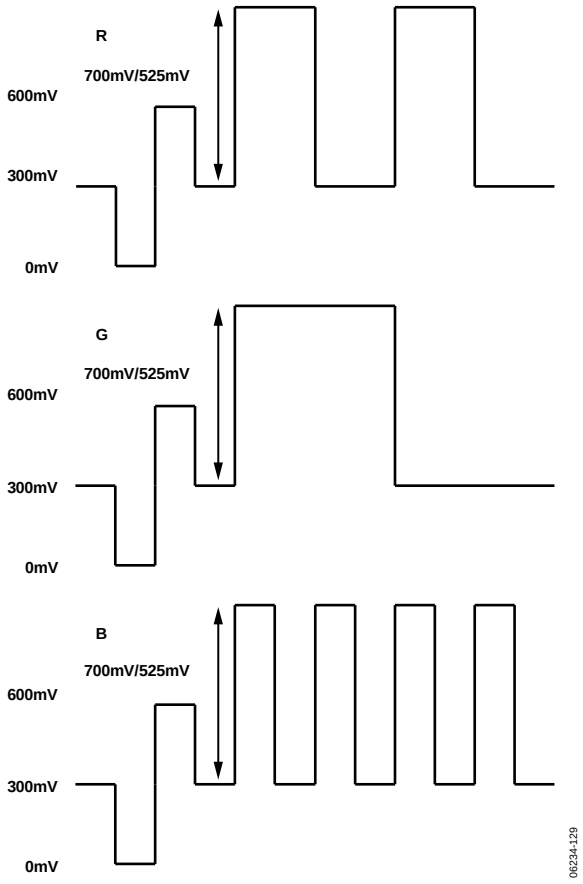


*Figure 131. HD RGB Output Levels—RGB Sync Enabled*



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## SD OUTPUT PLOTS

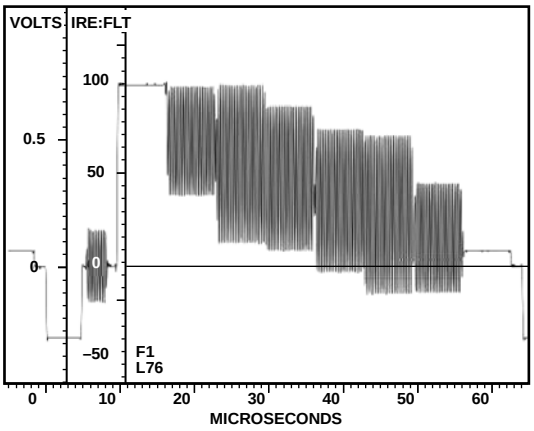


Figure 132. NTSC Color Bars (75%)

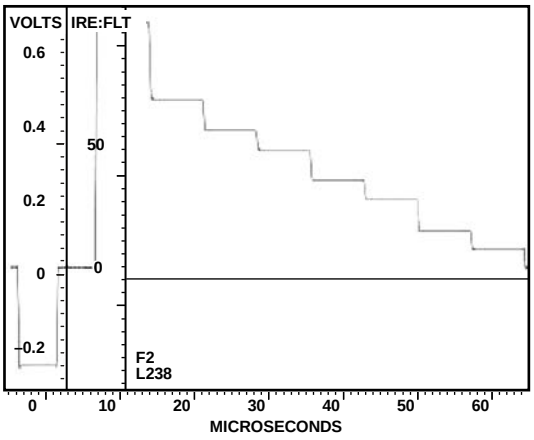


Figure 133. NTSC Luma

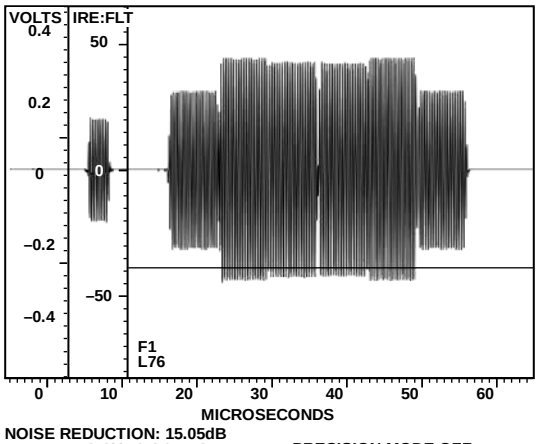


Figure 134. NTSC Chroma

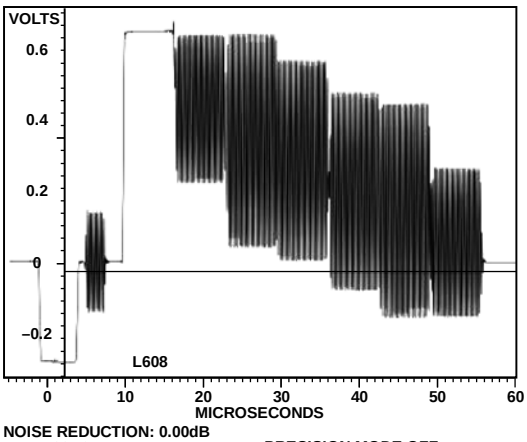


Figure 135. PAL Color Bars (75%)

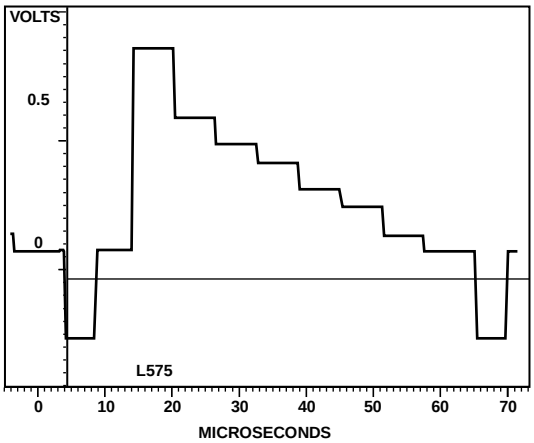


Figure 136. PAL Luma

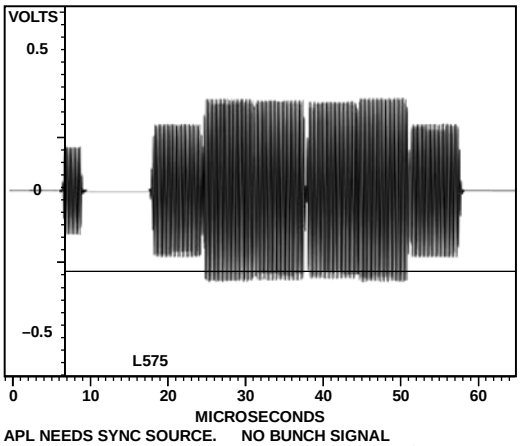


Figure 137. PAL Chroma



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# VIDEO STANDARDS

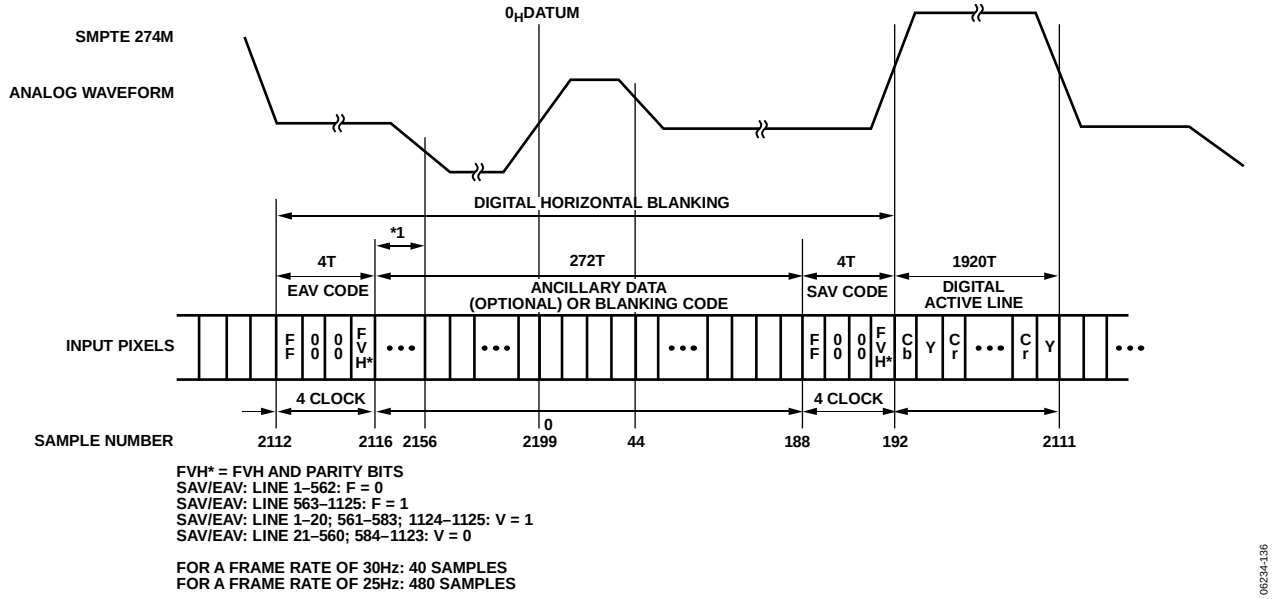


*Figure 138. EAV/SAV Input Data Timing Diagram (SMPTE 274M)*

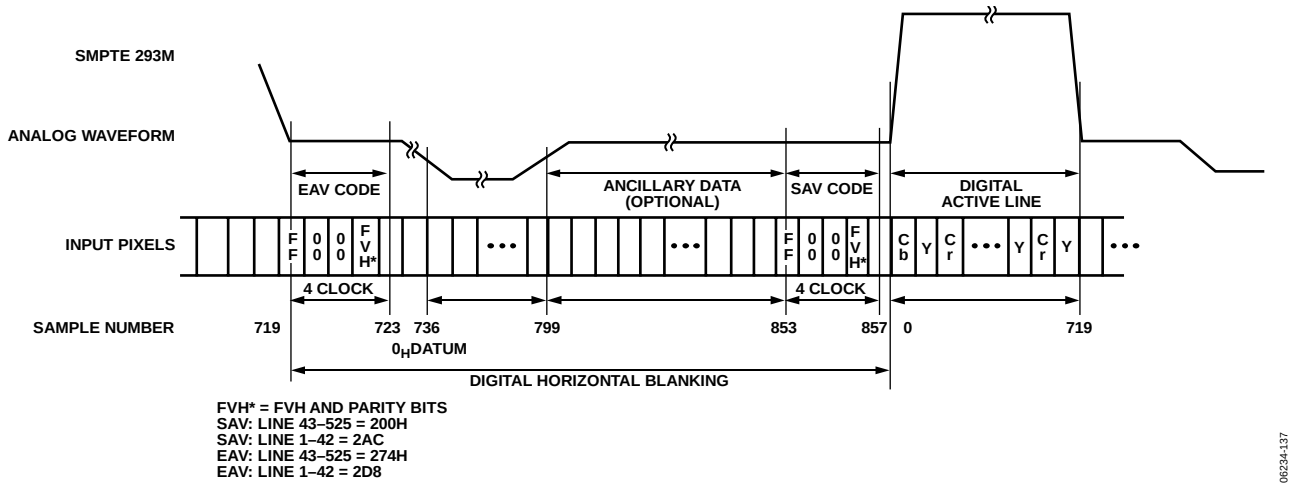


*Figure 139. EAV/SAV Input Data Timing Diagram (SMPTE 293M)*

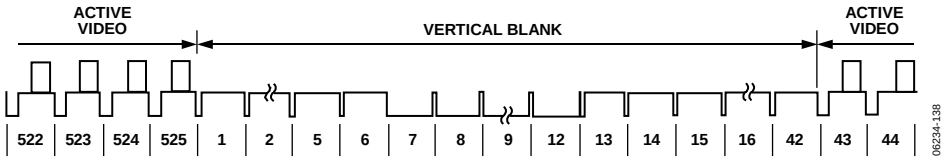


*Figure 140. SMPTE 293M (525p)*



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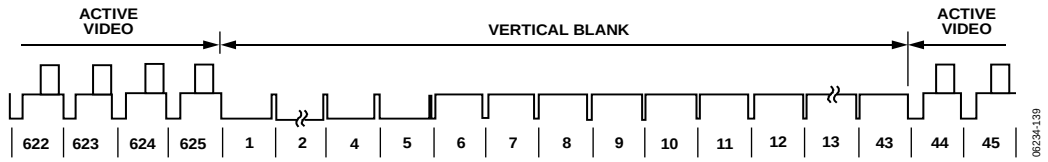


*Figure 141. ITU-R BT.1358 (625p)*

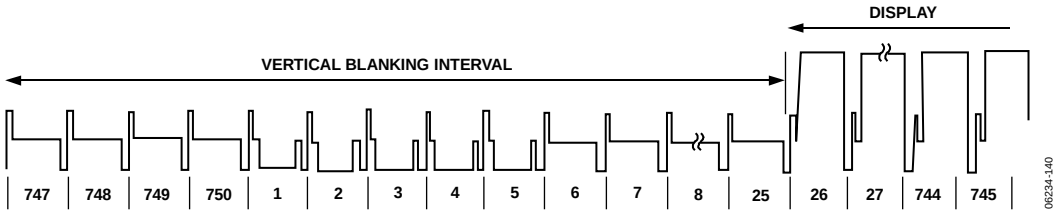


*Figure 142. SMPTE 296M (720p)*

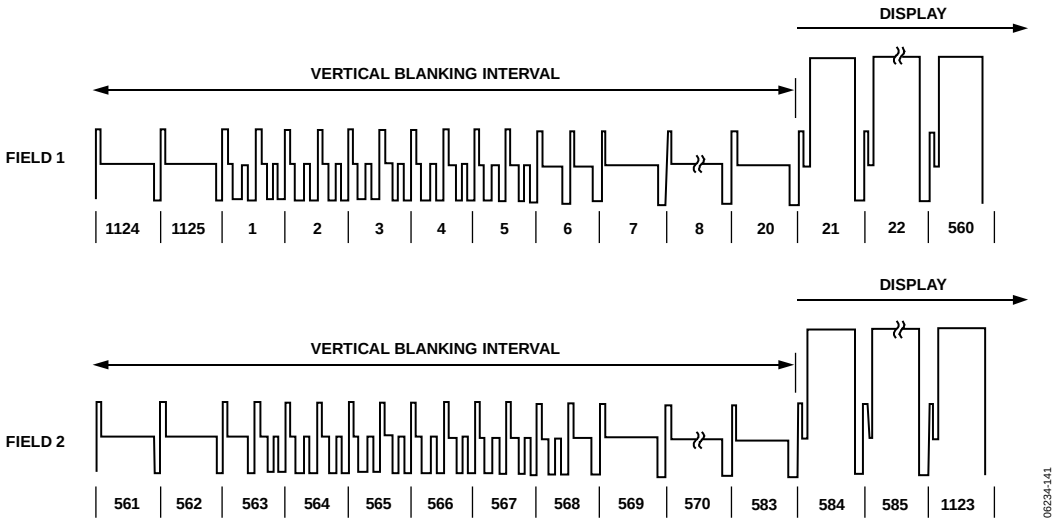


*Figure 143. SMPTE 274M (1080i)*



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# CONFIGURATION SCRIPTS

The scripts listed in the following pages can be used to configure the ADV7390/ADV7391/ADV7392/ADV7393 for basic operation. Certain features are enabled by default. If required for a specific application, additional features can be enabled. Table 63 lists the scripts available for SD modes of operation. Similarly, Table 98 and Table 115 list the scripts available for ED and HD modes of operation, respectively. For all scripts, only the necessary register writes are included. All other registers are assumed to have their default values. The WLCSP package supports only scripts in Table 65, Table 79, Table 82, and Table 96. In those scripts, Subaddress 0x00 must be set to 0x10.

## STANDARD DEFINITION

**Table 63. SD Configuration Scripts**

| Input Format | Input Data Width[1] | Synchronization Format | Input Color Space | Output Color Space | Table Number |
|---|---|---|---|---|---|
| 525i (NTSC) | 8-bit SDR | EAV/SAV | YCrCb | YPrPb | Table 64 |
| 525i (NTSC) | 8-bit SDR | EAV/SAV | YCrCb | CVBS/Y-C (S-Video) | Table 65 |
| 525i (NTSC) | 8-bit SDR | $\overline{\text{HSYNC}}$/$\overline{\text{VSYNC}}$ | YCrCb | YPrPb | Table 66 |
| 525i (NTSC) | 8-bit SDR | EAV/SAV | YCrCb | RGB | Table 67 |
| 525i (NTSC) | 8-bit SDR | $\overline{\text{HSYNC}}$/$\overline{\text{VSYNC}}$ | YCrCb | RGB | Table 68 |
| 525i (NTSC) | 10-bit SDR | EAV/SAV | YCrCb | YPrPb | Table 69 |
| 525i (NTSC) | 10-bit SDR | $\overline{\text{HSYNC}}$/$\overline{\text{VSYNC}}$ | YCrCb | YPrPb | Table 70 |
| 525i (NTSC) | 10-bit SDR | $\overline{\text{HSYNC}}$/$\overline{\text{VSYNC}}$ | YCrCb | CVBS/Y-C (S-Video) | Table 71 |
| 525i (NTSC) | 10-bit SDR | EAV/SAV | YCrCb | RGB | Table 72 |
| 525i (NTSC) | 10-bit SDR | $\overline{\text{HSYNC}}$/$\overline{\text{VSYNC}}$ | YCrCb | RGB | Table 73 |
| 525i (NTSC) | 16-bit SDR | $\overline{\text{HSYNC}}$/$\overline{\text{VSYNC}}$ | YCrCb | YPrPb | Table 74 |
| 525i (NTSC) | 16-bit SDR | $\overline{\text{HSYNC}}$/$\overline{\text{VSYNC}}$ | YCrCb | RGB | Table 75 |
| 525i (NTSC) | 16-bit SDR | $\overline{\text{HSYNC}}$/$\overline{\text{VSYNC}}$ | RGB | YPrPb | Table 76 |
| 525i (NTSC) | 16-bit SDR | $\overline{\text{HSYNC}}$/$\overline{\text{VSYNC}}$ | RGB | CVBS/Y-C (S-Video) | Table 77 |
| 525i (NTSC) | 16-bit SDR | $\overline{\text{HSYNC}}$/$\overline{\text{VSYNC}}$ | RGB | RGB | Table 78 |
| NTSC Sq. Pixel | 8-bit SDR | EAV/SAV | YCrCb | CVBS/Y-C (S-Video) | Table 79 |
| NTSC Sq. Pixel | 16-bit SDR | $\overline{\text{HSYNC}}$/$\overline{\text{VSYNC}}$ | RGB | CVBS/Y-C (S-Video) | Table 80 |
| 625i (PAL) | 8-bit SDR | EAV/SAV | YCrCb | YPrPb | Table 81 |
| 625i (PAL) | 8-bit SDR | EAV/SAV | YCrCb | CVBS/Y-C (S-Video) | Table 82 |
| 625i (PAL) | 8-bit SDR | $\overline{\text{HSYNC}}$/$\overline{\text{VSYNC}}$ | YCrCb | YPrPb | Table 83 |
| 625i (PAL) | 8-bit SDR | EAV/SAV | YCrCb | RGB | Table 84 |
| 625i (PAL) | 8-bit SDR | $\overline{\text{HSYNC}}$/$\overline{\text{VSYNC}}$ | YCrCb | RGB | Table 85 |
| 625i (PAL) | 10-bBit SDR | EAV/SAV | YCrCb | YPrPb | Table 86 |
| 625i (PAL) | 10-bit SDR | $\overline{\text{HSYNC}}$/$\overline{\text{VSYNC}}$ | YCrCb | YPrPb | Table 87 |
| 625i (PAL) | 10-bit SDR | $\overline{\text{HSYNC}}$/$\overline{\text{VSYNC}}$ | YCrCb | CVBS/Y-C (S-Video) | Table 88 |
| 625i (PAL) | 10-bit SDR | EAV/SAV | YCrCb | RGB | Table 89 |
| 625i (PAL) | 10-bit SDR | $\overline{\text{HSYNC}}$/$\overline{\text{VSYNC}}$ | YCrCb | RGB | Table 90 |
| 625i (PAL) | 16-bit SDR | $\overline{\text{HSYNC}}$/$\overline{\text{VSYNC}}$ | YCrCb | YPrPb | Table 91 |
| 625i (PAL) | 16-bit SDR | $\overline{\text{HSYNC}}$/$\overline{\text{VSYNC}}$ | YCrCb | RGB | Table 92 |
| 625i (PAL) | 16-bit SDR | $\overline{\text{HSYNC}}$/$\overline{\text{VSYNC}}$ | RGB | YPrPb | Table 93 |
| 625i (PAL) | 16-bit SDR | $\overline{\text{HSYNC}}$/$\overline{\text{VSYNC}}$ | RGB | CVBS/Y-C (S-Video) | Table 94 |
| 625i (PAL) | 16-bit SDR | $\overline{\text{HSYNC}}$/$\overline{\text{VSYNC}}$ | RGB | RGB | Table 95 |
| PAL Sq. Pixel | 8-bit SDR | EAV/SAV | YCrCb | CVBS/Y-C (S-Video) | Table 96 |
| PAL Sq. Pixel | 16-bit SDR | $\overline{\text{HSYNC}}$/$\overline{\text{VSYNC}}$ | RGB | CVBS/Y-C (S-Video) | Table 97 |

[1] SDR = single data rate.



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**Table 64. 8-Bit 525i YCrCb In (EAV/SAV), YPrPb Out**

| Subaddress | Setting | Description |
|---|---|---|
| 0x17 | 0x02 | Software reset. |
| 0x00 | 0x1C | All DACs enabled. PLL enabled (16×). |
| 0x01 | 0x00 | SD input mode. |
| 0x80 | 0x10 | NTSC standard. SSAF luma filter enabled.<br>1.3 MHz chroma filter enabled. |
| 0x82 | 0xC9 | Pixel data valid. YPrPb out. SSAF PrPb filter enabled. Active video edge control enabled. Pedestal enabled. |

**Table 65. 8-Bit 525i YCrCb In (EAV/SAV), CVBS/Y-C Out**

| Subaddress | Setting | Description |
|---|---|---|
| 0x17 | 0x02 | Software reset |
| 0x00 | 0x1C | All DACs enabled. PLL enabled (16×). |
| | 0x10 | WLCSP required. |
| 0x01 | 0x00 | SD input mode. |
| 0x80 | 0x10 | NTSC standard. SSAF luma filter enabled. 1.3 MHz chroma filter enabled. |
| 0x82 | 0xCB | Pixel data valid. CVBS/Y-C (S-Video) out. SSAF PrPb filter enabled. Active video edge control enabled. Pedestal enabled. |

**Table 66. 8-Bit 525i YCrCb In, YPrPb Out**

| Subaddress | Setting | Description |
|---|---|---|
| 0x17 | 0x02 | Software reset. |
| 0x00 | 0x1C | All DACs enabled. PLL enabled (16×). |
| 0x01 | 0x00 | SD input mode. |
| 0x80 | 0x10 | NTSC standard. SSAF luma filter enabled. 1.3 MHz chroma filter enabled. |
| 0x82 | 0xC9 | Pixel data valid. YPrPb out. SSAF PrPb filter enabled. Active video edge control enabled. Pedestal enabled. |
| 0x8A | 0x0C | Timing Mode 2 (slave). $\overline{\text{HSYNC}}$/$\overline{\text{VSYNC}}$ synchronization. |

**Table 67. 8-Bit 525i YCrCb In (EAV/SAV), RGB Out**

| Subaddress | Setting | Description |
|---|---|---|
| 0x17 | 0x02 | Software reset. |
| 0x00 | 0x1C | All DACs enabled. PLL enabled (16×). |
| 0x01 | 0x00 | SD input mode. |
| 0x02 | 0x10 | RGB output enabled. RGB output sync enabled. |
| 0x80 | 0x10 | NTSC standard. SSAF luma filter enabled. 1.3 MHz chroma filter enabled. |
| 0x82 | 0xC9 | Pixel data valid. RGB out. SSAF PrPb filter enabled. Active video edge control enabled. Pedestal enabled. |

**Table 68. 8-Bit 525i YCrCb In, RGB Out**

| Subaddress | Setting | Description |
|---|---|---|
| 0x17 | 0x02 | Software reset. |
| 0x00 | 0x1C | All DACs enabled. PLL enabled (16×). |
| 0x01 | 0x00 | SD input mode. |
| 0x02 | 0x10 | RGB output enabled. RGB output sync enabled. |
| 0x80 | 0x10 | NTSC standard. SSAF luma filter enabled. 1.3 MHz chroma filter enabled. |
| 0x82 | 0xC9 | Pixel data valid. RGB out. SSAF PrPb filter enabled. Active video edge control enabled. Pedestal enabled. |
| 0x8A | 0x0C | Timing Mode 2 (slave). $\overline{\text{HSYNC}}$/$\overline{\text{VSYNC}}$ synchronization. |

**Table 69. 10-Bit 525i YCrCb In (EAV/SAV), YPrPb Out**

| Subaddress | Setting | Description |
|---|---|---|
| 0x17 | 0x02 | Software reset. |
| 0x00 | 0x1C | All DACs enabled. PLL enabled (16×). |
| 0x01 | 0x00 | SD input mode. |
| 0x80 | 0x10 | NTSC standard. SSAF luma filter enabled. 1.3 MHz chroma filter enabled. |
| 0x82 | 0xC9 | Pixel data valid. YPrPb out. SSAF PrPb filter enabled. Active video edge control enabled. Pedestal enabled. |
| 0x88 | 0x10 | 10-bit input enabled. |

**Table 70. 10-Bit 525i YCrCb In, YPrPb Out**

| Subaddress | Setting | Description |
|---|---|---|
| 0x17 | 0x02 | Software reset. |
| 0x00 | 0x1C | All DACs enabled. PLL enabled (16×). |
| 0x01 | 0x00 | SD input mode. |
| 0x80 | 0x10 | NTSC standard. SSAF luma filter enabled. 1.3 MHz chroma filter enabled. |
| 0x82 | 0xC9 | Pixel data valid. YPrPb out. SSAF PrPb filter enabled. Active video edge control enabled. Pedestal enabled. |
| 0x88 | 0x10 | 10-bit input enabled. |
| 0x8A | 0x0C | Timing Mode 2 (slave). $\overline{\text{HSYNC}}$/$\overline{\text{VSYNC}}$ synchronization. |



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**Table 71. 10-Bit 525i YCrCb In, CVBS/Y-C Out**

| Subaddress | Setting | Description |
|---|---|---|
| 0x17 | 0x02 | Software reset. |
| 0x00 | 0x1C | All DACs enabled. PLL enabled (16×). |
| 0x01 | 0x00 | SD input mode. |
| 0x80 | 0x10 | NTSC standard. SSAF luma filter enabled. 1.3 MHz chroma filter enabled. |
| 0x82 | 0xCB | Pixel data valid. CVBS/Y-C (S-Video) out. SSAF PrPb filter enabled. Active video edge control enabled. Pedestal enabled. |
| 0x88 | 0x10 | 10-bit input enabled. |
| 0x8A | 0x0C | Timing Mode 2 (slave). $\overline{\text{HSYNC}}$/$\overline{\text{VSYNC}}$ synchronization. |

**Table 72. 10-Bit 525i YCrCb In (EAV/SAV), RGB Out**

| Subaddress | Setting | Description |
|---|---|---|
| 0x17 | 0x02 | Software reset. |
| 0x00 | 0x1C | All DACs enabled. PLL enabled (16×). |
| 0x01 | 0x00 | SD input mode. |
| 0x02 | 0x10 | RGB output enabled. RGB output sync enabled. |
| 0x80 | 0x10 | NTSC standard. SSAF luma filter enabled. 1.3 MHz chroma filter enabled. |
| 0x82 | 0xC9 | Pixel data valid. RGB out. SSAF PrPb filter enabled. Active video edge control enabled. Pedestal enabled. |
| 0x88 | 0x10 | 10-bit input enabled. |

**Table 73. 10-Bit 525i YCrCb In, RGB Out**

| Subaddress | Setting | Description |
|---|---|---|
| 0x17 | 0x02 | Software reset. |
| 0x00 | 0x1C | All DACs enabled. PLL enabled (16×). |
| 0x01 | 0x00 | SD input mode. |
| 0x02 | 0x10 | RGB output enabled. RGB output sync enabled. |
| 0x80 | 0x10 | NTSC standard. SSAF luma filter enabled. 1.3 MHz chroma filter enabled. |
| 0x82 | 0xC9 | Pixel data valid. RGB out. SSAF PrPb filter enabled. Active video edge control enabled. Pedestal enabled. |
| 0x88 | 0x10 | 10-bit input enabled. |
| 0x8A | 0x0C | Timing Mode 2 (slave). $\overline{\text{HSYNC}}$/$\overline{\text{VSYNC}}$ synchronization. |

**Table 74. 16-Bit 525i YCrCb In, YPrPb Out**

| Subaddress | Setting | Description |
|---|---|---|
| 0x17 | 0x02 | Software reset. |
| 0x00 | 0x1C | All DACs enabled. PLL enabled (16×). |
| 0x01 | 0x00 | SD input mode. |
| 0x80 | 0x10 | NTSC standard. SSAF luma filter enabled. 1.3 MHz chroma filter enabled. |
| 0x82 | 0xC9 | Pixel data valid. YPrPb out. SSAF PrPb filter enabled. Active video edge control enabled. Pedestal enabled. |
| 0x88 | 0x10 | 16-bit RGB input enabled. |
| 0x8A | 0x0C | Timing Mode 2 (slave). $\overline{\text{HSYNC}}$/$\overline{\text{VSYNC}}$ synchronization. |

**Table 75. 16-Bit 525i YCrCb In, RGB Out**

| Subaddress | Setting | Description |
|---|---|---|
| 0x17 | 0x02 | Software reset |
| 0x00 | 0x1C | All DACs enabled. PLL enabled (16×). |
| 0x01 | 0x00 | SD input mode. |
| 0x02 | 0x10 | RGB output enabled. RGB output sync enabled. |
| 0x80 | 0x10 | NTSC standard. SSAF luma filter enabled. 1.3 MHz chroma filter enabled. |
| 0x82 | 0xC9 | Pixel data valid. RGB out. SSAF PrPb filter enabled. Active video edge control enabled. Pedestal enabled. |
| 0x88 | 0x10 | 16-bit RGB input enabled. |
| 0x8A | 0x0C | Timing Mode 2 (slave). $\overline{\text{HSYNC}}$/$\overline{\text{VSYNC}}$ synchronization. |

**Table 76. 16-Bit 525i RGB In, YPrPb Out**

| Subaddress | Setting | Description |
|---|---|---|
| 0x17 | 0x02 | Software reset. |
| 0x00 | 0x1C | All DACs enabled. PLL enabled (16×). |
| 0x01 | 0x00 | SD input mode. |
| 0x80 | 0x10 | NTSC standard. SSAF luma filter enabled. 1.3 MHz chroma filter enabled. |
| 0x82 | 0xC9 | Pixel data valid. YPrPb out. SSAF PrPb filter enabled. Active video edge control enabled. Pedestal enabled. |
| 0x87 | 0x80 | RGB input enabled. |
| 0x88 | 0x10 | 16-bit RGB input enabled. |
| 0x8A | 0x0C | Timing Mode 2 (slave). $\overline{\text{HSYNC}}$/$\overline{\text{VSYNC}}$ synchronization. |



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**Table 77. 16-Bit 525i RGB In, CVBS/Y-C Out**

| Subaddress | Setting | Description |
|---|---|---|
| 0x17 | 0x02 | Software reset. |
| 0x00 | 0x1C | All DACs enabled. PLL enabled (16×). |
| 0x01 | 0x00 | SD input mode. |
| 0x80 | 0x10 | NTSC standard. SSAF luma filter enabled. 1.3 MHz chroma filter enabled. |
| 0x82 | 0xCB | Pixel data valid. CVBS/Y-C (S-Video) out. SSAF PrPb filter enabled. Active video edge control enabled. Pedestal enabled. |
| 0x87 | 0x80 | RGB input enabled. |
| 0x88 | 0x10 | 16-bit RGB input enabled. |
| 0x8A | 0x0C | Timing Mode 2 (slave). $\overline{\text{HSYNC}}$/$\overline{\text{VSYNC}}$ synchronization. |

**Table 78. 16-Bit 525i RGB In, RGB Out**

| Subaddress | Setting | Description |
|---|---|---|
| 0x17 | 0x02 | Software reset. |
| 0x00 | 0x1C | All DACs enabled. PLL enabled (16×). |
| 0x01 | 0x00 | SD input mode. |
| 0x02 | 0x10 | RGB output enabled. RGB output sync enabled. |
| 0x80 | 0x10 | NTSC standard. SSAF luma filter enabled. 1.3 MHz chroma filter enabled. |
| 0x82 | 0xC9 | Pixel data valid. RGB out. SSAF PrPb filter enabled. Active video edge control enabled. Pedestal enabled. |
| 0x87 | 0x80 | RGB input enabled. |
| 0x88 | 0x10 | 16-bit RGB input enabled. |
| 0x8A | 0x0C | Timing Mode 2 (slave). $\overline{\text{HSYNC}}$/$\overline{\text{VSYNC}}$ synchronization. |

**Table 79. 8-Bit NTSC Square Pixel YCrCb In (EAV/SAV), CVBS/Y-C Out**

| Subaddress | Setting | Description |
|---|---|---|
| 0x17 | 0x02 | Software reset |
| 0x00 | 0x1C | All DACs enabled. PLL enabled (16×). |
| | 0x10 | WLCSP required. |
| 0x01 | 0x00 | SD input mode. |
| 0x80 | 0x10 | NTSC standard. SSAF luma filter enabled. 1.3 MHz chroma filter enabled. |
| 0x82 | 0xDB | Pixel data valid. CVBS/Y-C (S-Video) out. SSAF PrPb filter enabled. Active video edge control enabled. Pedestal enabled. Square pixel mode enabled. |
| 0x8C | 0x55 | Subcarrier frequency register values for CVBS and/or S-Video (Y-C) output in NTSC square pixel mode (24.5454 MHz input clock). |
| 0x8D | 0x55 | |
| 0x8E | 0x55 | |
| 0x8F | 0x25 | |

**Table 80. 16-Bit NTSC Square Pixel RGB In, CVBS/Y-C Out**

| Subaddress | Setting | Description |
|---|---|---|
| 0x17 | 0x02 | Software reset. |
| 0x00 | 0x1C | All DACs enabled. PLL enabled (16×). |
| 0x01 | 0x00 | SD input mode. |
| 0x80 | 0x10 | NTSC standard. SSAF luma filter enabled. 1.3 MHz chroma filter enabled. |
| 0x82 | 0xDB | Pixel data valid. CVBS/Y-C (S-Video) out. SSAF PrPb filter enabled. Active video edge control enabled. Pedestal enabled. Square pixel mode enabled. |
| 0x87 | 0x80 | RGB input enabled. |
| 0x88 | 0x10 | 16-bit RGB input enabled. |
| 0x8A | 0x0C | Timing Mode 2 (slave). $\overline{\text{HSYNC}}$/$\overline{\text{VSYNC}}$ synchronization. |
| 0x8C | 0x55 | Subcarrier frequency register values for CVBS and/or S-Video (Y-C) output in NTSC square pixel mode (24.5454 MHz input clock). |
| 0x8D | 0x55 | |
| 0x8E | 0x55 | |
| 0x8F | 0x25 | |

**Table 81. 8-Bit 625i YCrCb In (EAV/SAV), YPrPb Out**

| Subaddress | Setting | Description |
|---|---|---|
| 0x17 | 0x02 | Software reset. |
| 0x00 | 0x1C | All DACs enabled. PLL enabled (16×). |
| 0x01 | 0x00 | SD input mode. |
| 0x80 | 0x11 | PAL standard. SSAF luma filter enabled. 1.3 MHz chroma filter enabled. |
| 0x82 | 0xC1 | Pixel data valid. YPrPb out. SSAF PrPb filter enabled. Active video edge control enabled. |

**Table 82. 8-Bit 625i YCrCb In (EAV/SAV), CVBS/Y-C Out**

| Subaddress | Setting | Description |
|---|---|---|
| 0x17 | 0x02 | Software reset. |
| 0x00 | 0x1C | All DACs enabled. PLL enabled (16×). |
| | 0x10 | WLCSP required. |
| 0x01 | 0x00 | SD input mode. |
| 0x80 | 0x11 | PAL standard. SSAF luma filter enabled. 1.3 MHz chroma filter enabled. |
| 0x82 | 0xC3 | Pixel data valid. CVBS/Y-C (S-Video) out. SSAF PrPb filter enabled. Active video edge control enabled. |
| 0x8C | 0xCB | Subcarrier frequency register values for CVBS and/or S-Video (Y-C) output in PAL mode (27 MHz input clock). |
| 0x8D | 0x8A | |
| 0x8E | 0x09 | |
| 0x8F | 0x2A | |



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**Table 83. 8-Bit 625i YCrCb In, YPrPb Out**

| Subaddress | Setting | Description |
|---|---|---|
| 0x17 | 0x02 | Software reset. |
| 0x00 | 0x1C | All DACs enabled. PLL enabled (16×). |
| 0x01 | 0x00 | SD input mode. |
| 0x80 | 0x11 | PAL standard. SSAF luma filter enabled. 1.3 MHz chroma filter enabled. |
| 0x82 | 0xC1 | Pixel data valid. YPrPb out. SSAF PrPb filter enabled. Active video edge control enabled. |
| 0x8A | 0x0C | Timing Mode 2 (slave). $\overline{\text{HSYNC}}$/$\overline{\text{VSYNC}}$ synchronization. |

**Table 84. 8-Bit 625i YCrCb In (EAV/SAV), RGB Out**

| Subaddress | Setting | Description |
|---|---|---|
| 0x17 | 0x02 | Software reset. |
| 0x00 | 0x1C | All DACs enabled. PLL enabled (16×). |
| 0x01 | 0x00 | SD input mode. |
| 0x02 | 0x10 | RGB output enabled. RGB output sync enabled. |
| 0x80 | 0x11 | PAL standard. SSAF luma filter enabled. 1.3 MHz chroma filter enabled. |
| 0x82 | 0xC1 | Pixel data valid. RGB out. SSAF PrPb filter enabled. Active video edge control enabled. |

**Table 85. 8-Bit 625i YCrCb In, RGB Out**

| Subaddress | Setting | Description |
|---|---|---|
| 0x17 | 0x02 | Software reset. |
| 0x00 | 0x1C | All DACs enabled. PLL enabled (16×). |
| 0x01 | 0x00 | SD input mode. |
| 0x02 | 0x10 | RGB output enabled. RGB output sync enabled. |
| 0x80 | 0x11 | PAL standard. SSAF luma filter enabled. 1.3 MHz chroma filter enabled. |
| 0x82 | 0xC1 | Pixel data valid. RGB out. SSAF PrPb filter enabled. Active video edge control enabled. |
| 0x8A | 0x0C | Timing Mode 2 (slave). $\overline{\text{HSYNC}}$/$\overline{\text{VSYNC}}$ synchronization. |

**Table 86. 10-Bit 625i YCrCb In (EAV/SAV), YPrPb Out**

| Subaddress | Setting | Description |
|---|---|---|
| 0x17 | 0x02 | Software reset. |
| 0x00 | 0x1C | All DACs enabled. PLL enabled (16×). |
| 0x01 | 0x00 | SD input mode. |
| 0x80 | 0x11 | PAL standard. SSAF luma filter enabled. 1.3 MHz chroma filter enabled. |
| 0x82 | 0xC1 | Pixel data valid. YPrPb out. SSAF PrPb filter enabled. Active video edge control enabled. |
| 0x88 | 0x10 | 10-bit input enabled. |

**Table 87. 10-Bit 625i YCrCb In, YPrPb Out**

| Subaddress | Setting | Description |
|---|---|---|
| 0x17 | 0x02 | Software reset. |
| 0x00 | 0x1C | All DACs enabled. PLL enabled (16×). |
| 0x01 | 0x00 | SD input mode. |
| 0x80 | 0x11 | PAL standard. SSAF luma filter enabled. 1.3 MHz chroma filter enabled. |
| 0x82 | 0xC1 | Pixel data valid. YPrPb out. SSAF PrPb filter enabled. Active video edge control enabled. |
| 0x88 | 0x10 | 10-bit input enabled. |
| 0x8A | 0x0C | Timing Mode 2 (slave). $\overline{\text{HSYNC}}$/$\overline{\text{VSYNC}}$ synchronization. |

**Table 88. 10-Bit 625i YCrCb In, CVBS/Y-C Out**

| Subaddress | Setting | Description |
|---|---|---|
| 0x17 | 0x02 | Software reset. |
| 0x00 | 0x1C | All DACs enabled. PLL enabled (16×). |
| 0x01 | 0x00 | SD input mode. |
| 0x80 | 0x11 | PAL standard. SSAF luma filter enabled. 1.3 MHz chroma filter enabled. |
| 0x82 | 0xC3 | Pixel Data Valid. CVBS/Y-C (S-Video) Out. SSAF PrPb filter enabled. Active video edge control enabled. |
| 0x88 | 0x10 | 10-bit input enabled. |
| 0x8A | 0x0C | Timing Mode 2 (slave). $\overline{\text{HSYNC}}$/$\overline{\text{VSYNC}}$ synchronization. |
| 0x8C | 0xCB | Subcarrier frequency register values for CVBS and/or S-Video (Y-C) output in PAL mode (27 MHz input clock). |
| 0x8D | 0x8A | |
| 0x8E | 0x09 | |
| 0x8F | 0x2A | |

**Table 89. 10-Bit 625i YCrCb In (EAV/SAV), RGB Out**

| Subaddress | Setting | Description |
|---|---|---|
| 0x17 | 0x02 | Software reset. |
| 0x00 | 0x1C | All DACs enabled. PLL enabled (16×). |
| 0x01 | 0x00 | SD input mode. |
| 0x02 | 0x10 | RGB output enabled. RGB output sync enabled. |
| 0x80 | 0x11 | PAL standard. SSAF luma filter enabled. 1.3 MHz chroma filter enabled. |
| 0x82 | 0xC1 | Pixel data valid. RGB out. SSAF PrPb filter enabled. Active video edge control enabled. |
| 0x88 | 0x10 | 10-bit input enabled. |



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**Table 90. 10-Bit 625i YCrCb In, RGB Out**

| Subaddress | Setting | Description |
|---|---|---|
| 0x17 | 0x02 | Software reset. |
| 0x00 | 0x1C | All DACs enabled. PLL enabled (16×). |
| 0x01 | 0x00 | SD input mode. |
| 0x02 | 0x10 | RGB output enabled. RGB output sync enabled. |
| 0x80 | 0x11 | PAL standard. SSAF luma filter enabled. 1.3 MHz chroma filter enabled. |
| 0x82 | 0xC1 | Pixel data valid. RGB out. SSAF PrPb filter enabled. Active video edge control enabled. |
| 0x88 | 0x10 | 10-bit input enabled. |
| 0x8A | 0x0C | Timing Mode 2 (slave). $\overline{\text{HSYNC}}$/$\overline{\text{VSYNC}}$ synchronization. |

**Table 91. 16-Bit 625i YCrCb In, YPrPb Out**

| Subaddress | Setting | Description |
|---|---|---|
| 0x17 | 0x02 | Software reset. |
| 0x00 | 0x1C | All DACs enabled. PLL enabled (16×). |
| 0x01 | 0x00 | SD input mode. |
| 0x80 | 0x11 | PAL standard. SSAF luma filter enabled. 1.3 MHz chroma filter enabled. |
| 0x82 | 0xC1 | Pixel data valid. YPrPb out. SSAF PrPb filter enabled. Active video edge control enabled. |
| 0x88 | 0x10 | 16-bit RGB input enabled. |
| 0x8A | 0x0C | Timing Mode 2 (slave). $\overline{\text{HSYNC}}$/$\overline{\text{VSYNC}}$ synchronization. |

**Table 92. 16-Bit 625i YCrCb In, RGB Out**

| Subaddress | Setting | Description |
|---|---|---|
| 0x17 | 0x02 | Software reset. |
| 0x00 | 0x1C | All DACs enabled. PLL enabled (16×). |
| 0x01 | 0x00 | SD input mode. |
| 0x02 | 0x10 | RGB output enabled. RGB output sync enabled. |
| 0x80 | 0x11 | PAL standard. SSAF luma filter enabled. 1.3 MHz chroma filter enabled. |
| 0x82 | 0xC1 | Pixel data valid. RGB out. SSAF PrPb filter enabled. Active video edge control enabled. |
| 0x88 | 0x10 | 16-bit RGB input enabled. |
| 0x8A | 0x0C | Timing Mode 2 (slave). $\overline{\text{HSYNC}}$/$\overline{\text{VSYNC}}$ synchronization. |

**Table 93. 16-Bit 625i RGB In, YPrPb Out**

| Subaddress | Setting | Description |
|---|---|---|
| 0x17 | 0x02 | Software reset. |
| 0x00 | 0x1C | All DACs enabled. PLL enabled (16×). |
| 0x01 | 0x00 | SD input mode. |
| 0x80 | 0x11 | PAL standard. SSAF luma filter enabled. 1.3 MHz chroma filter enabled. |
| 0x82 | 0xC1 | Pixel data valid. YPrPb out. SSAF PrPb filter enabled. Active video edge control enabled. |
| 0x87 | 0x80 | RGB input enabled. |
| 0x88 | 0x10 | 16-bit RGB input enabled. |
| 0x8A | 0x0C | Timing Mode 2 (slave). $\overline{\text{HSYNC}}$/$\overline{\text{VSYNC}}$ synchronization. |

**Table 94. 16-Bit 625i RGB In, CVBS/Y-C Out**

| Subaddress | Setting | Description |
|---|---|---|
| 0x17 | 0x02 | Software reset. |
| 0x00 | 0x1C | All DACs enabled. PLL enabled (16×). |
| 0x01 | 0x00 | SD input mode. |
| 0x80 | 0x11 | PAL standard. SSAF luma filter enabled. 1.3 MHz chroma filter enabled. |
| 0x82 | 0xC3 | Pixel data valid. CVBS/Y-C (S-Video) out. SSAF PrPb filter enabled. Active video edge control enabled. |
| 0x87 | 0x80 | RGB input enabled. |
| 0x88 | 0x10 | 16-bit RGB input enabled. |
| 0x8A | 0x0C | Timing Mode 2 (slave). $\overline{\text{HSYNC}}$/$\overline{\text{VSYNC}}$ synchronization. |
| 0x8C | 0xCB | Subcarrier frequency register values for CVBS and/or S-Video (Y-C) output in PAL mode (27 MHz input clock). |
| 0x8D | 0x8A | |
| 0x8E | 0x09 | |
| 0x8F | 0x2A | |

**Table 95. 16-Bit 625i RGB In, RGB Out**

| Subaddress | Setting | Description |
|---|---|---|
| 0x17 | 0x02 | Software reset. |
| 0x00 | 0x1C | All DACs enabled. PLL enabled (16×). |
| 0x01 | 0x00 | SD input mode. |
| 0x02 | 0x10 | RGB output enabled. RGB output sync enabled. |
| 0x80 | 0x11 | PAL standard. SSAF luma filter enabled. 1.3 MHz chroma filter enabled. |
| 0x82 | 0xC1 | Pixel data valid. RGB out. SSAF PrPb filter enabled. Active video edge control enabled. |
| 0x87 | 0x80 | RGB input enabled. |
| 0x88 | 0x10 | 16-bit RGB input enabled. |
| 0x8A | 0x0C | Timing Mode 2 (slave). $\overline{\text{HSYNC}}$/$\overline{\text{VSYNC}}$ synchronization. |



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**Table 96. 8-Bit PAL Square Pixel YCrCb In (EAV/SAV), CVBS/Y-C Out**

| Subaddress | Setting | Description |
|---|---|---|
| 0x17 | 0x02 | Software reset. |
| 0x00 | 0x1C | All DACs enabled. PLL enabled (16×). |
| | 0x10 | WLCSP required. |
| 0x01 | 0x00 | SD input mode. |
| 0x80 | 0x11 | PAL standard. SSAF luma filter enabled. 1.3 MHz chroma filter enabled. |
| 0x82 | 0xD3 | Pixel data valid. CVBS/Y-C (S-Video) out. SSAF PrPb filter enabled. Active video edge control enabled. Square pixel mode enabled. |
| 0x8C | 0x0C | Subcarrier frequency register values for CVBS and/or S-Video (Y-C) output in PAL square pixel mode (29.5 MHz input clock). |
| 0x8D | 0x8C | |
| 0x8E | 0x79 | |
| 0x8F | 0x26 | |

**Table 97. 16-Bit PAL Square Pixel RGB In, CVBS/Y-C Out**

| Subaddress | Setting | Description |
|---|---|---|
| 0x17 | 0x02 | Software reset. |
| 0x00 | 0x1C | All DACs enabled. PLL enabled (16×). |
| 0x01 | 0x00 | SD input mode. |
| 0x80 | 0x11 | PAL standard. SSAF luma filter enabled. 1.3 MHz chroma filter enabled. |
| 0x82 | 0xD3 | Pixel data valid. CVBS/Y-C (S-Video) out. SSAF PrPb filter enabled. Active video edge control enabled. Square pixel mode enabled. |
| 0x87 | 0x80 | RGB input enabled. |
| 0x88 | 0x10 | 16-bit RGB input enabled. |
| 0x8A | 0x0C | Timing Mode 2 (slave). $\overline{\text{HSYNC}}$/$\overline{\text{VSYNC}}$ synchronization. |
| 0x8C | 0x0C | Subcarrier frequency register values for CVBS and/or S-Video (Y-C) output in PAL square pixel mode (29.5 MHz input clock). |
| 0x8D | 0x8C | |
| 0x8E | 0x79 | |
| 0x8F | 0x26 | |



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## ENHANCED DEFINITION

**Table 98. ED Configuration Scripts**

| Input Format | Input Data Width | Synchronization Format | Input Color Space | Output Color Space | Table Number |
|---|---|---|---|---|---|
| 525p | 8-bit DDR | EAV/SAV | YCrCb | YPrPb | Table 107 |
| 525p | 8-bit DDR | EAV/SAV | YCrCb | RGB | Table 109 |
| 525p | 10-bit DDR | EAV/SAV | YCrCb | YPrPb | Table 108 |
| 525p | 10-bit DDR | EAV/SAV | YCrCb | RGB | Table 110 |
| 525p | 16-bit SDR | EAV/SAV | YCrCb | YPrPb | Table 99 |
| 525p | 16-bit SDR | $\overline{\text{HSYNC}}$/$\overline{\text{VSYNC}}$ | YCrCb | YPrPb | Table 100 |
| 525p | 16-bit SDR | EAV/SAV | YCrCb | RGB | Table 101 |
| 525p | 16-bit SDR | $\overline{\text{HSYNC}}$/$\overline{\text{VSYNC}}$ | YCrCb | RGB | Table 102 |
| 625p | 8-bit DDR | EAV/SAV | YCrCb | YPrPb | Table 111 |
| 625p | 8-bit DDR | EAV/SAV | YCrCb | RGB | Table 113 |
| 625p | 10-bit DDR | EAV/SAV | YCrCb | YPrPb | Table 112 |
| 625p | 10-bit DDR | EAV/SAV | YCrCb | RGB | Table 114 |
| 625p | 16-bit SDR | EAV/SAV | YCrCb | YPrPb | Table 103 |
| 625p | 16-bit SDR | $\overline{\text{HSYNC}}$/$\overline{\text{VSYNC}}$ | YCrCb | YPrPb | Table 104 |
| 625p | 16-bit SDR | EAV/SAV | YCrCb | RGB | Table 105 |
| 625p | 16-bit SDR | $\overline{\text{HSYNC}}$/$\overline{\text{VSYNC}}$ | YCrCb | RGB | Table 106 |

**Table 99. 16-Bit 525p YCrCb In (EAV/SAV), YPrPb Out**

| Subaddress | Setting | Description |
|---|---|---|
| 0x17 | 0x02 | Software reset. |
| 0x00 | 0x1C | All DACs enabled. PLL enabled (8×). |
| 0x01 | 0x10 | ED-SDR input mode. |
| 0x30 | 0x04 | 525p at 59.94 Hz. EAV/SAV synchronization. EIA-770.2 output levels. |
| 0x31 | 0x01 | Pixel data valid. |

**Table 100. 16-Bit 525p YCrCb In, YPrPb Out**

| Subaddress | Setting | Description |
|---|---|---|
| 0x17 | 0x02 | Software reset. |
| 0x00 | 0x1C | All DACs enabled. PLL enabled (8×). |
| 0x01 | 0x10 | ED-SDR input mode. |
| 0x30 | 0x00 | 525p at 59.94 Hz. $\overline{\text{HSYNC}}$/$\overline{\text{VSYNC}}$ synchronization. EIA-770.2 output levels. |
| 0x31 | 0x01 | Pixel data valid. |

**Table 101. 16-Bit 525p YCrCb In (EAV/SAV), RGB Out**

| Subaddress | Setting | Description |
|---|---|---|
| 0x17 | 0x02 | Software reset. |
| 0x00 | 0x1C | All DACs enabled. PLL enabled (8×). |
| 0x01 | 0x10 | ED-SDR input mode. |
| 0x02 | 0x10 | RGB output enabled. RGB output sync enabled. |
| 0x30 | 0x04 | 525p at 59.94 Hz. EAV/SAV synchronization. EIA-770.2 output levels. |
| 0x31 | 0x01 | Pixel data valid. |

**Table 102. 16-Bit 525p YCrCb In, RGB Out**

| Subaddress | Setting | Description |
|---|---|---|
| 0x17 | 0x02 | Software reset. |
| 0x00 | 0x1C | All DACs enabled. PLL enabled (8×). |
| 0x01 | 0x10 | ED-SDR input mode. |
| 0x02 | 0x10 | RGB output enabled. RGB output sync enabled. |
| 0x30 | 0x00 | 525p at 59.94 Hz. $\overline{\text{HSYNC}}$/$\overline{\text{VSYNC}}$ synchronization. EIA-770.2 output levels. |
| 0x31 | 0x01 | Pixel data valid. |

**Table 103. 16-Bit 625p YCrCb In (EAV/SAV), YPrPb Out**

| Subaddress | Setting | Description |
|---|---|---|
| 0x17 | 0x02 | Software reset. |
| 0x00 | 0x1C | All DACs enabled. PLL enabled (8×). |
| 0x01 | 0x10 | ED-SDR input mode. |
| 0x30 | 0x1C | 625p at 50 Hz. EAV/SAV synchronization. EIA-770.2 output levels. |
| 0x31 | 0x01 | Pixel data valid. |

**Table 104. 16-Bit 625p YCrCb In, YPrPb Out**

| Subaddress | Setting | Description |
|---|---|---|
| 0x17 | 0x02 | Software reset. |
| 0x00 | 0x1C | All DACs enabled. PLL enabled (8×). |
| 0x01 | 0x10 | ED-SDR input mode. |
| 0x30 | 0x18 | 625p at 50 Hz. $\overline{\text{HSYNC}}$/$\overline{\text{VSYNC}}$ synchronization. EIA-770.2 output levels. |
| 0x31 | 0x01 | Pixel data valid. |



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**Table 105. 16-Bit 625p YCrCb In (EAV/SAV), RGB Out**

| Subaddress | Setting | Description |
|---|---|---|
| 0x17 | 0x02 | Software reset. |
| 0x00 | 0x1C | All DACs enabled. PLL enabled (8×). |
| 0x01 | 0x10 | ED-SDR input mode. |
| 0x02 | 0x10 | RGB output enabled. RGB output sync enabled. |
| 0x30 | 0x1C | 625p at 50 Hz. EAV/SAV synchronization. EIA-770.2 output levels. |
| 0x31 | 0x01 | Pixel data valid. |

**Table 106. 16-Bit 625p YCrCb In, RGB Out**

| Subaddress | Setting | Description |
|---|---|---|
| 0x17 | 0x02 | Software reset. |
| 0x00 | 0x1C | All DACs enabled. PLL enabled (8×). |
| 0x01 | 0x10 | ED-SDR input mode. |
| 0x02 | 0x10 | RGB output enabled. RGB output sync enabled. |
| 0x30 | 0x18 | 625p at 50 Hz. $\overline{\text{HSYNC}}$/$\overline{\text{VSYNC}}$ synchronization. EIA-770.2 output levels. |
| 0x31 | 0x01 | Pixel data valid. |

**Table 107. 8-Bit 525p YCrCb In (EAV/SAV), YPrPb Out**

| Subaddress | Setting | Description |
|---|---|---|
| 0x17 | 0x02 | Software reset. |
| 0x00 | 0x1C | All DACs enabled. PLL enabled (8×). |
| 0x01 | 0x20 | ED-DDR input mode. Luma data clocked on falling edge of CLKIN. |
| 0x30 | 0x04 | 525p at 59.94 Hz. EAV/SAV synchronization. EIA-770.2 output levels. |
| 0x31 | 0x01 | Pixel data valid. |

**Table 108. 10-Bit 525p YCrCb In (EAV/SAV), YPrPb Out**

| Subaddress | Setting | Description |
|---|---|---|
| 0x17 | 0x02 | Software reset. |
| 0x00 | 0x1C | All DACs enabled. PLL enabled (8×). |
| 0x01 | 0x20 | ED-DDR input mode. Luma data clocked on falling edge of CLKIN. |
| 0x30 | 0x04 | 525p at 59.94 Hz. EAV/SAV synchronization. EIA-770.2 output levels. |
| 0x31 | 0x01 | Pixel data valid. |
| 0x33 | 0x6C | 10-bit input enabled. |

**Table 109. 8-Bit 525p YCrCb In (EAV/SAV), RGB Out**

| Subaddress | Setting | Description |
|---|---|---|
| 0x17 | 0x02 | Software reset. |
| 0x00 | 0x1C | All DACs enabled. PLL enabled (8×). |
| 0x01 | 0x20 | ED-DDR input mode. Luma data clocked on falling edge of CLKIN. |
| 0x02 | 0x10 | RGB output enabled. RGB output sync enabled. |
| 0x30 | 0x04 | 525p at 59.94 Hz. EAV/SAV synchronization. EIA-770.2 output levels. |
| 0x31 | 0x01 | Pixel data valid. |

**Table 110. 10-Bit 525p YCrCb In (EAV/SAV), RGB Out**

| Subaddress | Setting | Description |
|---|---|---|
| 0x17 | 0x02 | Software reset. |
| 0x00 | 0x1C | All DACs enabled. PLL enabled (8×). |
| 0x01 | 0x20 | ED-DDR input mode. Luma data clocked on falling edge of CLKIN. |
| 0x02 | 0x10 | RGB output enabled. RGB output sync enabled. |
| 0x30 | 0x04 | 525p at 59.94 Hz. EAV/SAV synchronization. EIA-770.2 output levels. |
| 0x31 | 0x01 | Pixel data valid. |
| 0x33 | 0x6C | 10-bit input enabled. |

**Table 111. 8-Bit 625p YCrCb In (EAV/SAV), YPrPb Out**

| Subaddress | Setting | Description |
|---|---|---|
| 0x17 | 0x02 | Software reset. |
| 0x00 | 0x1C | All DACs enabled. PLL enabled (8×). |
| 0x01 | 0x20 | ED-DDR input mode. Luma data clocked on falling edge of CLKIN. |
| 0x30 | 0x1C | 625p at 50 Hz. EAV/SAV synchronization. EIA-770.2 output levels. |
| 0x31 | 0x01 | Pixel data valid. |

**Table 112. 10-Bit 625p YCrCb In (EAV/SAV), YPrPb Out**

| Subaddress | Setting | Description |
|---|---|---|
| 0x17 | 0x02 | Software reset. |
| 0x00 | 0x1C | All DACs enabled. PLL enabled (8×). |
| 0x01 | 0x20 | ED-DDR input mode. Luma data clocked on falling edge of CLKIN. |
| 0x30 | 0x1C | 625p at 50 Hz. EAV/SAV synchronization. EIA-770.2 output levels. |
| 0x31 | 0x01 | Pixel data valid. |
| 0x33 | 0x6C | 10-bit input enabled. |



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**Table 113. 8-Bit 625p YCrCb In (EAV/SAV), RGB Out**

| Subaddress | Setting | Description |
|---|---|---|
| 0x17 | 0x02 | Software reset. |
| 0x00 | 0x1C | All DACs enabled. PLL enabled (8×). |
| 0x01 | 0x20 | ED-DDR input mode. Luma data clocked on falling edge of CLKIN. |
| 0x02 | 0x10 | RGB output enabled. RGB output sync enabled. |
| 0x30 | 0x1C | 625p at 50 Hz. EAV/SAV synchronization. EIA-770.2 output levels. |
| 0x31 | 0x01 | Pixel data valid. |

**Table 114. 10-Bit 625p YCrCb In (EAV/SAV), RGB Out**

| Subaddress | Setting | Description |
|---|---|---|
| 0x17 | 0x02 | Software reset. |
| 0x00 | 0x1C | All DACs enabled. PLL enabled (8×). |
| 0x01 | 0x20 | ED-DDR input mode. Luma data clocked on falling edge of CLKIN. |
| 0x02 | 0x10 | RGB output enabled. RGB output sync enabled. |
| 0x30 | 0x1C | 625p at 50 Hz. EAV/SAV synchronization. EIA-770.2 output levels. |
| 0x31 | 0x01 | Pixel data valid. |
| 0x33 | 0x6C | 10-bit input enabled. |

## HIGH DEFINITION

**Table 115. HD Configuration Scripts**

| Input Format | Input Data Width | Synchronization Format | Input Color Space | Output Color Space | Table Number |
|---|---|---|---|---|---|
| 720p | 8-bit DDR | EAV/SAV | YCrCb | YPrPb | Table 124 |
| 720p | 8-bit DDR | EAV/SAV | YCrCb | RGB | Table 126 |
| 720p | 10-bit DDR | EAV/SAV | YCrCb | YPrPb | Table 125 |
| 720p | 10-bit DDR | EAV/SAV | YCrCb | RGB | Table 127 |
| 720p | 16-bit SDR | EAV/SAV | YCrCb | YPrPb | Table 116 |
| 720p | 16-bit SDR | $\overline{\text{HSYNC}}$/$\overline{\text{VSYNC}}$ | YCrCb | YPrPb | Table 117 |
| 720p | 16-bit SDR | EAV/SAV | YCrCb | RGB | Table 118 |
| 720p | 16-bit SDR | $\overline{\text{HSYNC}}$/$\overline{\text{VSYNC}}$ | YCrCb | RGB | Table 119 |
| 1080i | 8-bit DDR | EAV/SAV | YCrCb | YPrPb | Table 128 |
| 1080i | 8-bit DDR | EAV/SAV | YCrCb | RGB | Table 130 |
| 1080i | 10-bit DDR | EAV/SAV | YCrCb | YPrPb | Table 129 |
| 1080i | 10-bit DDR | EAV/SAV | YCrCb | RGB | Table 131 |
| 1080i | 16-bit SDR | EAV/SAV | YCrCb | YPrPb | Table 120 |
| 1080i | 16-bit SDR | $\overline{\text{HSYNC}}$/$\overline{\text{VSYNC}}$ | YCrCb | YPrPb | Table 121 |
| 1080i | 16-bit SDR | EAV/SAV | YCrCb | RGB | Table 122 |
| 1080i | 16-bit SDR | $\overline{\text{HSYNC}}$/$\overline{\text{VSYNC}}$ | YCrCb | RGB | Table 123 |



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**Table 116. 16-Bit 720p YCrCb In (EAV/SAV), YPrPb Out**

| Subaddress | Setting | Description |
|---|---|---|
| 0x17 | 0x02 | Software reset. |
| 0x00 | 0x1C | All DACs enabled. PLL enabled (4×). |
| 0x01 | 0x10 | HD-SDR input mode. |
| 0x30 | 0x2C | 720p at 60 Hz/59.94 Hz. EAV/SAV synchronization. EIA-770.3 output levels. |
| 0x31 | 0x01 | Pixel data valid. 4× oversampling. |

**Table 117. 16-Bit 720p YCrCb In, YPrPb Out**

| Subaddress | Setting | Description |
|---|---|---|
| 0x17 | 0x02 | Software reset. |
| 0x00 | 0x1C | All DACs enabled. PLL enabled (4×). |
| 0x01 | 0x10 | HD-SDR input mode. |
| 0x30 | 0x28 | 720p at 60 Hz/59.94 Hz. $\overline{\text{HSYNC}}$/$\overline{\text{VSYNC}}$ synchronization. EIA-770.3 output levels. |
| 0x31 | 0x01 | Pixel data valid. 4× oversampling. |

**Table 118. 16-Bit 720p YCrCb In (EAV/SAV), RGB Out**

| Subaddress | Setting | Description |
|---|---|---|
| 0x17 | 0x02 | Software reset. |
| 0x00 | 0x1C | All DACs enabled. PLL enabled (4×). |
| 0x01 | 0x10 | HD-SDR input mode. |
| 0x02 | 0x10 | RGB output enabled. RGB output sync enabled. |
| 0x30 | 0x2C | 720p at 60 Hz/59.94 Hz. EAV/SAV synchronization. EIA-770.3 output levels. |
| 0x31 | 0x01 | Pixel data valid. 4× oversampling. |

**Table 119. 16-Bit 720p YCrCb In, RGB Out**

| Subaddress | Setting | Description |
|---|---|---|
| 0x17 | 0x02 | Software reset. |
| 0x00 | 0x1C | All DACs enabled. PLL enabled (4×). |
| 0x01 | 0x10 | HD-SDR input mode. |
| 0x02 | 0x10 | RGB output enabled. RGB output sync enabled. |
| 0x30 | 0x28 | 720p at 60 Hz/59.94 Hz. $\overline{\text{HSYNC}}$/$\overline{\text{VSYNC}}$ synchronization. EIA-770.3 output levels. |
| 0x31 | 0x01 | Pixel data valid. 4× oversampling. |

**Table 120. 16-Bit 1080i YCrCb In (EAV/SAV), YPrPb Out**

| Subaddress | Setting | Description |
|---|---|---|
| 0x17 | 0x02 | Software reset. |
| 0x00 | 0x1C | All DACs enabled. PLL enabled (4×). |
| 0x01 | 0x10 | HD-SDR input mode. |
| 0x30 | 0x6C | 1080i at 30 Hz/29.97 Hz. EAV/SAV synchronization. EIA-770.3 output levels. |
| 0x31 | 0x01 | Pixel data valid. 4× oversampling. |

**Table 121. 16-Bit 1080i YCrCb In, YPrPb Out**

| Subaddress | Setting | Description |
|---|---|---|
| 0x17 | 0x02 | Software reset. |
| 0x00 | 0x1C | All DACs enabled. PLL enabled (4×). |
| 0x01 | 0x10 | HD-SDR input mode. |
| 0x30 | 0x18 | 1080i at 30 Hz/29.97 Hz. $\overline{\text{HSYNC}}$/$\overline{\text{VSYNC}}$ synchronization. EIA-770.3 output levels. |
| 0x31 | 0x01 | Pixel data valid. 4× oversampling. |

**Table 122. 16-Bit 1080i YCrCb In (EAV/SAV), RGB Out**

| Subaddress | Setting | Description |
|---|---|---|
| 0x17 | 0x02 | Software reset. |
| 0x00 | 0x1C | All DACs enabled. PLL enabled (4×). |
| 0x01 | 0x10 | HD-SDR input mode. |
| 0x02 | 0x10 | RGB output enabled. RGB output sync enabled. |
| 0x30 | 0x6C | 1080i at 30 Hz/29.97 Hz. EAV/SAV synchronization. EIA-770.3 output levels. |
| 0x31 | 0x01 | Pixel data valid. 4× oversampling. |

**Table 123. 16-Bit 1080i YCrCb In, RGB Out**

| Subaddress | Setting | Description |
|---|---|---|
| 0x17 | 0x02 | Software reset. |
| 0x00 | 0x1C | All DACs enabled. PLL enabled (4×). |
| 0x01 | 0x10 | HD-SDR input mode. |
| 0x02 | 0x10 | RGB output enabled. RGB output sync enabled. |
| 0x30 | 0x18 | 1080i at 30 Hz/29.97 Hz. $\overline{\text{HSYNC}}$/$\overline{\text{VSYNC}}$ synchronization. EIA-770.3 output levels. |
| 0x31 | 0x01 | Pixel data valid. 4× oversampling. |

**Table 124. 8-Bit 720p YCrCb In (EAV/SAV), YPrPb Out**

| Subaddress | Setting | Description |
|---|---|---|
| 0x17 | 0x02 | Software reset. |
| 0x00 | 0x1C | All DACs enabled. PLL enabled (4×). |
| 0x01 | 0x20 | HD-DDR input mode. Luma data clocked on falling edge of CLKIN. |
| 0x30 | 0x2C | 720p at 60 Hz/59.94 Hz. EAV/SAV synchronization. EIA-770.3 output levels. |
| 0x31 | 0x01 | Pixel data valid. 4× oversampling. |

**Table 125. 10-Bit 720p YCrCb In (EAV/SAV), YPrPb Out**

| Subaddress | Setting | Description |
|---|---|---|
| 0x17 | 0x02 | Software reset. |
| 0x00 | 0x1C | All DACs enabled. PLL enabled (4×). |
| 0x01 | 0x20 | HD-DDR input mode. Luma data clocked on falling edge of CLKIN. |
| 0x30 | 0x2C | 720p at 60 Hz/59.94 Hz. EAV/SAV synchronization. EIA-770.3 output levels. |
| 0x31 | 0x01 | Pixel data valid. 4× oversampling. |
| 0x33 | 0x6C | 10-bit input enabled. |



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**Table 126. 8-Bit 720p YCrCb In (EAV/SAV), RGB Out**

| Subaddress | Setting | Description |
|---|---|---|
| 0x17 | 0x02 | Software reset. |
| 0x00 | 0x1C | All DACs enabled. PLL enabled (4×). |
| 0x01 | 0x20 | HD-DDR input mode. Luma data clocked on falling edge of CLKIN. |
| 0x02 | 0x10 | RGB output enabled. RGB output sync enabled. |
| 0x30 | 0x2C | 720p at 60 Hz/59.94 Hz. EAV/SAV synchronization. EIA-770.3 output levels. |
| 0x31 | 0x01 | Pixel data valid. 4× oversampling. |

**Table 127. 10-Bit 720p YCrCb In (EAV/SAV), RGB Out**

| Subaddress | Setting | Description |
|---|---|---|
| 0x17 | 0x02 | Software reset. |
| 0x00 | 0x1C | All DACs enabled. PLL enabled (4×). |
| 0x01 | 0x20 | HD-DDR input mode. Luma data clocked on falling edge of CLKIN. |
| 0x02 | 0x10 | RGB output enabled. RGB output sync enabled. |
| 0x30 | 0x2C | 720p at 60 Hz/59.94 Hz. EAV/SAV synchronization. EIA-770.3 output levels. |
| 0x31 | 0x01 | Pixel data valid. 4× oversampling. |
| 0x33 | 0x6C | 10-bit input enabled. |

**Table 128. 8-Bit 1080i YCrCb In (EAV/SAV), YPrPb Out**

| Subaddress | Setting | Description |
|---|---|---|
| 0x17 | 0x02 | Software reset. |
| 0x00 | 0x1C | All DACs enabled. PLL enabled (4×). |
| 0x01 | 0x20 | HD-DDR input mode. Luma data clocked on falling edge of CLKIN. |
| 0x30 | 0x6C | 1080i at 30 Hz/29.97 Hz. EAV/SAV synchronization. EIA-770.3 output levels. |
| 0x31 | 0x01 | Pixel data valid. 4× oversampling. |

**Table 129. 10-Bit 1080i YCrCb In (EAV/SAV), YPrPb Out**

| Subaddress | Setting | Description |
|---|---|---|
| 0x17 | 0x02 | Software reset. |
| 0x00 | 0x1C | All DACs enabled. PLL enabled (4×). |
| 0x01 | 0x20 | HD-DDR input mode. Luma data clocked on falling edge of CLKIN. |
| 0x30 | 0x6C | 1080i at 30 Hz/29.97 Hz. EAV/SAV synchronization. EIA-770.3 output levels. |
| 0x31 | 0x01 | Pixel data valid. 4× oversampling. |
| 0x33 | 0x6C | 10-bit input enabled. |

**Table 130. 8-Bit 1080i YCrCb In (EAV/SAV), RGB Out**

| Subaddress | Setting | Description |
|---|---|---|
| 0x17 | 0x02 | Software reset. |
| 0x00 | 0x1C | All DACs enabled. PLL enabled (4×). |
| 0x01 | 0x20 | HD-DDR input mode. Luma data clocked on falling edge of CLKIN. |
| 0x02 | 0x10 | RGB output enabled. RGB output sync enabled. |
| 0x30 | 0x6C | 1080i at 30 Hz/29.97 Hz. EAV/SAV synchronization. EIA-770.3 output levels. |
| 0x31 | 0x01 | Pixel data valid. 4× oversampling. |

**Table 131. 10-Bit 1080i YCrCb In (EAV/SAV), RGB Out**

| Subaddress | Setting | Description |
|---|---|---|
| 0x17 | 0x02 | Software reset. |
| 0x00 | 0x1C | All DACs enabled. PLL enabled (4×). |
| 0x01 | 0x20 | HD-DDR input mode. Luma data clocked on falling edge of CLKIN. |
| 0x02 | 0x10 | RGB output enabled. RGB output sync enabled. |
| 0x30 | 0x6C | 1080i @ 30 Hz/29.97 Hz. EAV/SAV synchronization. EIA-770.3 output levels. |
| 0x31 | 0x01 | Pixel data valid. 4× oversampling. |
| 0x33 | 0x6C | 10-bit input enabled. |



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# ADV7390/ADV7391/ADV7392/ADV7393 EVALUATION BOARD

To accommodate evaluation of the ADV7390/ADV7391/ADV7392/ADV7393, Analog Devices provides a two-board solution. The ADV7390/ADV7391/ADV7392/ADV7393 evaluation platform front-end board contains an Analog Devices decoder (ADV7403) and an FPGA. The back-end board (where the actual ADV7390/ADV7391/ADV7392/ADV7393 are attached) is connected to the front-end board through a connector.

These two boards allow the user to perform a complete evaluation of the part, although it is also possible to order only the back-end board. Note that these two boards must be ordered separately.

For more information about the evaluation boards, see the evaluation board documentation available on the Analog Devices product web page.

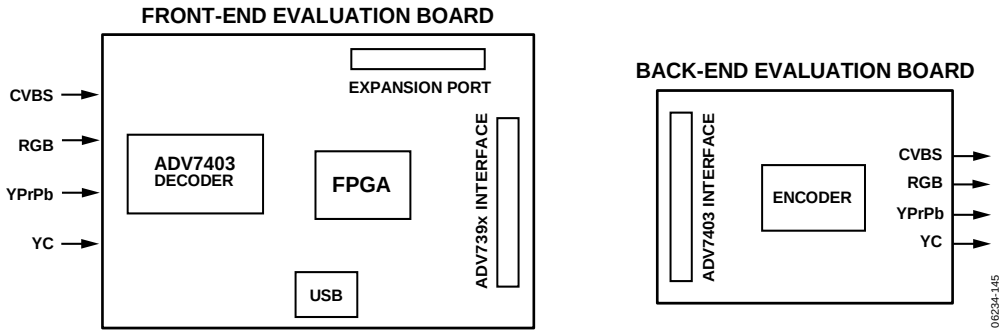


*Figure 144. ADV7390/ADV7391/ADV7392/ADV7393 Front-End and Back-End Evaluation Boards*



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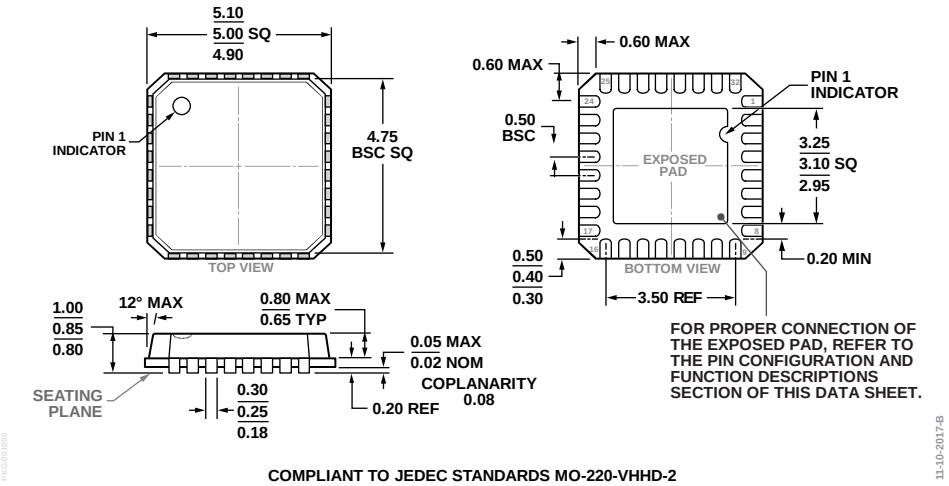
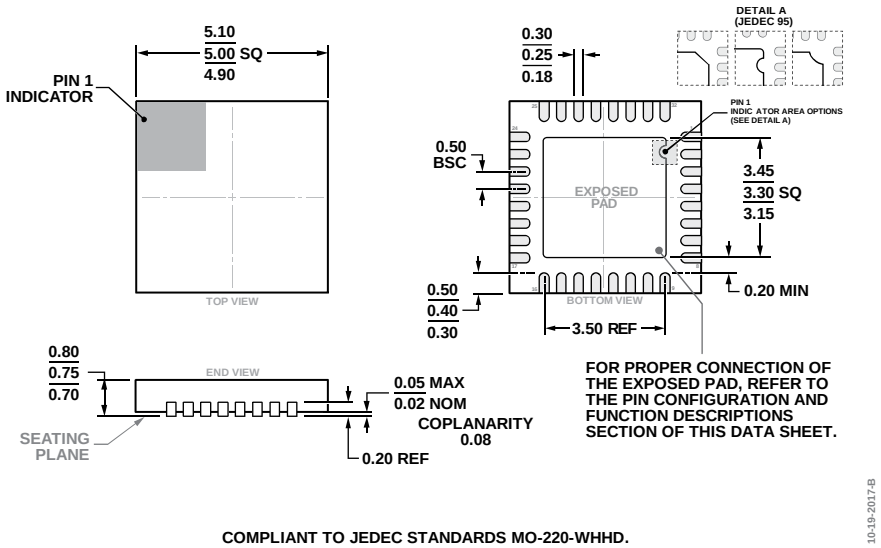
# OUTLINE DIMENSIONS




COMPLIANT TO JEDEC STANDARDS MO-220-VHHD-2

*Figure 145. 32-Lead Lead Frame Chip Scale Package [LFCSP]*
*5 mm × 5 mm Body and 0.85 mm Package Height*
*(CP-32-2)*
*Dimensions shown in millimeters*




COMPLIANT TO JEDEC STANDARDS MO-220-WHHD.

*Figure 146. 32-Lead Lead Frame Chip Scale Package [LFCSP]*
*5 mm × 5 mm Body and 0.75 mm Package Height*
*(CP-32-13)*
*Dimensions shown in millimeters*



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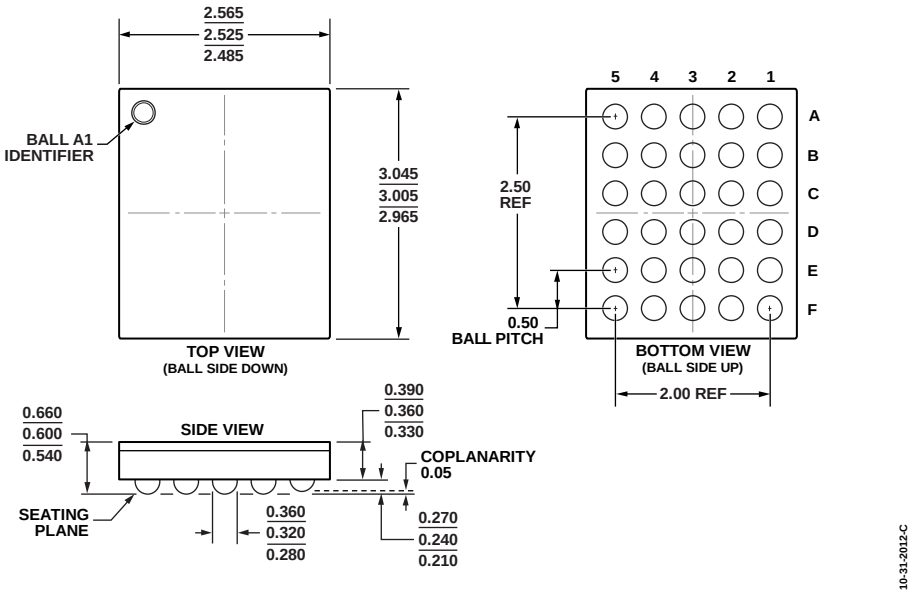
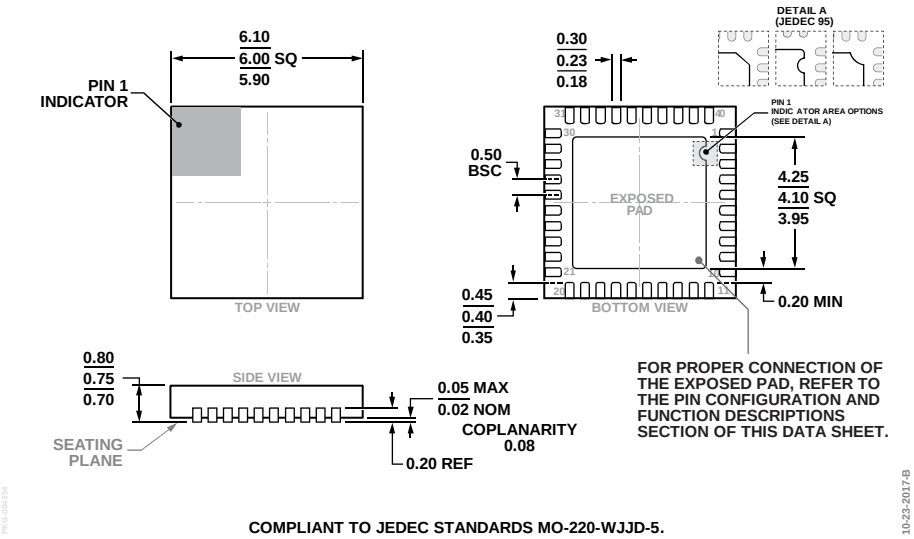



*Figure 147. 30-Ball Wafer Level Chip Scale Package [WLCSP]*
*(CB-30-3)*
*Dimensions shown in millimeters*




**COMPLIANT TO JEDEC STANDARDS MO-220-WJJD-5.**

*Figure 148. 40-Lead Lead Frame Chip Scale Package [LFCSP]*
*6 mm × 6 mm Body and 0.75 mm Package Height*
*(CP-40-9)*
*Dimensions shown in millimeters*



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## ORDERING GUIDE

| Model[1, 2] | Temperature Range | Macrovision[3] Antitaping | Package Description | Package Option |
|---|---|---|---|---|
| ADV7390BCPZ | −40°C to +85°C | Yes | 32-Lead Lead Frame Chip Scale Package [LFCSP] | CP-32-2 |
| ADV7390BCPZ-REEL | −40°C to +85°C | Yes | 32-Lead Lead Frame Chip Scale Package [LFCSP] | CP-32-2 |
| ADV7390WBCPZ | −40°C to +105°C | Yes | 32-Lead Lead Frame Chip Scale Package [LFCSP] | CP-32-13 |
| ADV7390WBCPZ-RL | −40°C to +105°C | Yes | 32-Lead Lead Frame Chip Scale Package [LFCSP] | CP-32-13 |
| ADV7390BCBZ-A-RL | −40°C to +85°C | Yes | 30-Ball Wafer Level Chip Scale Package [WLCSP] | CB-30-3 |
| ADV7391BCPZ | −40°C to +85°C | No | 32-Lead Lead Frame Chip Scale Package [LFCSP] | CP-32-2 |
| ADV7391BCPZ-REEL | −40°C to +85°C | No | 32-Lead Lead Frame Chip Scale Package [LFCSP] | CP-32-2 |
| ADV7391WBCPZ | −40°C to +105°C | No | 32-Lead Lead Frame Chip Scale Package [LFCSP] | CP-32-13 |
| ADV7391WBCPZ-RL | −40°C to +105°C | No | 32-Lead Lead Frame Chip Scale Package [LFCSP] | CP-32-13 |
| ADV7392BCPZ | −40°C to +85°C | Yes | 40-Lead Lead Frame Chip Scale Package [LFCSP] | CP-40-9 |
| ADV7392BCPZ-REEL | −40°C to +85°C | Yes | 40-Lead Lead Frame Chip Scale Package [LFCSP] | CP-40-9 |
| ADV7392BCPZ-3REEL | −40°C to +85°C | Yes | 40-Lead Lead Frame Chip Scale Package [LFCSP] | CP-40-9 |
| ADV7392WBCPZ | −40°C to +105°C | Yes | 40-Lead Lead Frame Chip Scale Package [LFCSP] | CP-40-9 |
| ADV7392WBCPZ-REEL | −40°C to +105°C | Yes | 40-Lead Lead Frame Chip Scale Package [LFCSP] | CP-40-9 |
| ADV7393BCPZ | −40°C to +85°C | No | 40-Lead Lead Frame Chip Scale Package [LFCSP] | CP-40-9 |
| ADV7393BCPZ-REEL | −40°C to +85°C | No | 40-Lead Lead Frame Chip Scale Package [LFCSP] | CP-40-9 |
| ADV7393WBCPZ | −40°C to +105°C | No | 40-Lead Lead Frame Chip Scale Package [LFCSP] | CP-40-9 |
| ADV7393WBCPZ-REEL | −40°C to +105°C | No | 40-Lead Lead Frame Chip Scale Package [LFCSP] | CP-40-9 |
| EVAL-ADV739xFEZ | | Not available | ADV739x Evaluation Platform Front-End Board | |
| EVAL-ADV7390EBZ | | Yes | ADV7390 Evaluation Board | |
| EVAL-ADV7391EBZ | | No | ADV7391 Evaluation Board | |
| EVAL-ADV7392EBZ | | Yes | ADV7392 Evaluation Board | |
| EVAL-ADV7393EBZ | | No | ADV7393 Evaluation Board | |

[1] Z = RoHS Compliant Part.
[2] W = Qualified for Automotive Applications.
[3] Macrovision-enabled ICs require the buyer to be an approved licensee (authorized buyer) of ICs that are able to output Macrovision Rev 7.1.L1-compliant video.

## AUTOMOTIVE PRODUCTS

The ADV7390W, ADV7391W, ADV7392W, and ADV7393W models are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that these automotive models may have specifications that differ from the commercial models; therefore, designers should review the Specifications section of this data sheet carefully. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

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