TABLE OF CONTENTS

REVISION HISTORY

2/09—Rev. 0 to Rev. A

10/05—Revision 0: Initial Version

SPECIFICATIONS

DUAL SUPPLY

V_{DD} = 15 V ± 10%, V_{SS} = −15 V± 10%, GND = 0 V, unless otherwise noted.

Table 1.

Parameter	Y Version[1] 25°C	Y Version[1] −40°C to +105°C	Unit	Test Conditions/Comments
ANALOG SWITCH				
Analog Signal Range		V_{DD} to V_{SS}	V	
On Resistance (R_{ON})	130	230	Ω typ	V_S = ±10 V, I_S = −1 mA; see Figure 10
	200		Ω max	V_{DD} = +13.5 V, V_{SS} = −13.5 V
On Resistance Match Between Channels (ΔR_{ON})	5		Ω typ	V_S = ±10 V, I_S = −1 mA
	10		Ω max	
On Resistance Flatness ($R_{FLAT(ON)}$)	25		Ω typ	V_S = −5 V/0 V/+5 V; I_S = −1 mA
	65		Ω max	
LEAKAGE CURRENTS				V_{DD} = +16.5 V, V_{SS} = −16.5 V
Source Off Leakage, I_S (Off)	±10		nA typ	V_S = ±10 V, V_D = ∓10 V; see Figure 11
Drain Off Leakage, I_D (Off)	±10		nA typ	V_S = ±10 V, V_D = ∓10 V; see Figure 11
Channel On Leakage, I_D, I_S (On)	±10		nA typ	V_S = V_D = ±10 V; see Figure 12
DIGITAL INPUTS				
Input High Voltage, V_{INH}		2.0	V min	
Input Low Voltage, V_{INL}		0.8	V max	
Input Current, I_{INL} or I_{INH}	0.005		μA typ	V_{IN} = V_{INL} or V_{INH}
		±0.1	μA max	
Digital Input Capacitance, C_{IN}	2.5		pF typ	
DYNAMIC CHARACTERISTICS[2]				
t_{ON}	105		ns typ	R_L = 300 Ω, C_L = 35 pF
	125	180	ns max	V_S = 10 V; see Figure 13
t_{OFF}	40		ns typ	R_L = 300 Ω, C_L = 35 pF
	50	60	ns max	V_S = 10 V; see Figure 13
Break-Before-Make Time Delay, t_D	25		ns typ	R_L = 300 Ω, C_L = 35 pF
(ADG1313 Only)		10	ns min	V_{S1} = V_{S2} = 10 V; see Figure 14
Charge Injection	2		pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF; see Figure 15
Off Isolation	80		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 16
Channel-to-Channel Crosstalk	90		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 17
−3 dB Bandwidth	600		MHz typ	R_L = 50 Ω, C_L = 5 pF; see Figure 18
C_S (Off)	5		pF typ	
C_D (Off)	5		pF typ	
C_D, C_S (On)	10		pF typ	
POWER REQUIREMENTS				V_{DD} = +16.5 V, V_{SS} = −16.5 V
I_{DD}	0.001		μA typ	Digital inputs = 0 V or V_{DD}
		1.0	μA max	
I_{DD}	220		μA typ	Digital inputs = 5 V
		380	μA max	
I_{SS}	0.001		μA typ	Digital inputs = 0 V or V_{DD}
		1.0	μA max	
I_{SS}	0.001		μA typ	Digital inputs = 5 V
		1.0	μA max	

[1] Temperature range for Y Version is −40°C to +105°C.
[2] Guaranteed by design, not subject to production test.

SINGLE SUPPLY

V_{DD} = 12 V ± 10%, V_{SS} = 0 V, GND = 0 V, unless otherwise noted.

Table 2.

Parameter	Y Version[1] 25°C	−40°C to +105°C	Unit	Test Conditions/Comments
ANALOG SWITCH				
Analog Signal Range		0 V to V_{DD}	V	
On Resistance (R_{ON})	325	520	Ω typ	V_S = 0 V – 10 V, I_S = −1 mA; see Figure 10
	500		Ω max	V_{DD} = 10.8 V, V_{SS} = 0 V
On Resistance Match Between Channels (ΔR_{ON})	10		Ω typ	V_S = 0 V – 10 V, I_S = −1 mA
	15		Ω max	
On Resistance Flatness ($R_{FLAT(ON)}$)	65		Ω typ	V_S = 3 V/6 V/9 V, I_S = −1 mA
LEAKAGE CURRENTS				V_{DD} = 13.2 V, V_{SS} = 0 V
Source Off Leakage, I_S (Off)	±10		nA typ	V_S = 1 V/10 V, V_D = 10 V/1 V; see Figure 11
Drain Off Leakage, I_D (Off)	±10		nA typ	V_S = 1 V/10 V, V_D = 10 V/1 V see Figure 11
Channel On Leakage, I_D, I_S (On)	±10		nA typ	V_S = V_D = 1 V or 10 V; se e Figure 12
DIGITAL INPUTS				
Input High Voltage, V_{INH}		2.0	V min	
Input Low Voltage, V_{INL}		0.8	V max	
Input Current, I_{INL} or I_{INH}	0.001		μA typ	V_{IN} = V_{INL} or V_{INH}
		±0.1	μA max	
Digital Input Capacitance, C_{IN}	3		pF typ	
DYNAMIC CHARACTERISTICS[2]				
t_{ON}	120		ns typ	R_L = 300 Ω, C_L = 35 pF
	155	210	ns max	V_S = 8 V; see Figure 13
t_{OFF}	45		ns typ	R_L = 300 Ω, C_L = 35 pF
	65	80	ns max	V_S = 8 V; see Figure 13
Break-Before-Make Time Delay, t_D	50		ns typ	R_L = 300 Ω, C_L = 35 pF
(ADG1313 Only)		10	ns min	V_{S1} = V_{S2} = 8 V; see Figure 14
Charge Injection	2		pC typ	V_S = 6 V, R_S = 0 Ω, C_L = 1 nF; see Figure 15
Off Isolation	80		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 16
Channel-to-Channel Crosstalk	90		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 17
−3 dB Bandwidth	500		MHz typ	R_L = 50 Ω, C_L = 5 pF; see Figure 18
C_S (Off)	5		pF typ	
C_D (Off)	5		pF typ	
C_D, C_S (On)	10		pF typ	
POWER REQUIREMENTS				V_{DD} = 13.2 V
I_{DD}	0.001		μA typ	Digital inputs = 0 V or V_{DD}
		1.0	μA max	
I_{DD}	220		μA typ	Digital inputs = 5 V
		380	μA max	

[1] Temperature range for Y Version is −40°C to +105°C.
[2] Guaranteed by design, not subject to production test.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
V_{DD} to V_{SS}	35 V
V_{DD} to GND	−0.3 V to +25 V
V_{SS} to GND	+0.3 V to −25 V
Analog Inputs[1]	V_{SS} − 0.3 V to V_{DD} + 0.3 V or 30 mA, whichever occurs first
Digital Inputs[1]	GND − 0.3 V to V_{DD} + 0.3 V or 30 mA, whichever occurs first
Peak Current, S or D	100 mA (pulsed at 1 ms, 10% duty cycle max)
Continuous Current per Channel, S or D	25 mA
Operating Temperature Range	
Automotive	−40°C to +105°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
16-Lead TSSOP, θ_{JA} Thermal Impedance (4-layer board)	112°C/W
16-Lead SOIC, θ_{JA} Thermal Impedance	77°C/W
Reflow Soldering Peak Temperature, Pb free	260°C

[1] Overvoltages at IN, S, or D are clamped by internal diodes. Current should be limited to the maximum ratings given.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 4. ADG1311/ADG1312 Truth Table

ADG1311 INx	ADG1312 INx	Switch Condition
0	1	On
1	0	Off

Table 5. ADG1313 Truth Table

ADG1313 INx	Switch 1, 4	Switch 2, 3
0	Off	On
1	On	Off

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

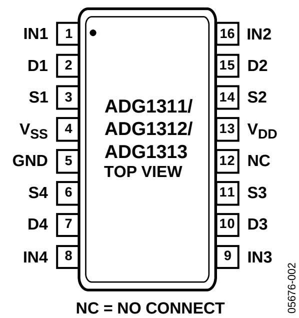


Figure 2. SOIC/TSSOP Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	IN1	Logic Control Input.
2	D1	Drain Terminal. Can be an input or output.
3	S1	Source Terminal. Can be an input or output.
4	V_{SS}	Most Negative Power Supply Potential.
5	GND	Ground (0 V) Reference.
6	S4	Source Terminal. Can be an input or output.
7	D4	Drain Terminal. Can be an input or output.
8	IN4	Logic Control Input.
9	IN3	Logic Control Input.
10	D3	Drain Terminal. Can be an input or output.
11	S3	Source Terminal. Can be an input or output.
12	NC	No Connection.
13	V_{DD}	Most Positive Power Supply Potential.
14	S2	Source Terminal. Can be an input or output.
15	D2	Drain Terminal. Can be an input or output.
16	IN2	Logic Control Input.

TERMINOLOGY

I_{DD}
The positive supply current.

I_{SS}
The negative supply current.

V_D (V_S)
The analog voltage on Terminal D and Terminal S.

R_{ON}
The ohmic resistance between D and S.

$R_{FLAT(ON)}$
Flatness is defined as the difference between the maximum and minimum value of on resistance, as measured over the specified analog signal range.

I_S (Off)
The source leakage current with the switch off.

I_D (Off)
The drain leakage current with the switch off.

I_D, I_S (On)
The channel leakage current with the switch on.

V_{INL}
The maximum input voltage for Logic 0.

V_{INH}
The minimum input voltage for Logic 1.

I_{INL} (I_{INH})
The input current of the digital input.

C_S (Off)
The off switch source capacitance, measured with reference to ground.

C_D (Off)
The off switch drain capacitance, measured with reference to ground.

C_D, C_S (On)
The on switch capacitance, measured with reference to ground.

C_{IN}
The digital input capacitance.

t_{ON}
The delay between applying the digital control input and the output switching on. See Figure 13.

t_{OFF}
The delay between applying the digital control input and the output switching off. See Figure 13.

Charge Injection
A measure of the glitch impulse transferred from the digital input to the analog output during switching.

Off Isolation
A measure of unwanted signal coupling through an off switch.

Crosstalk
A measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance.

Bandwidth
The frequency at which the output is attenuated by 3 dB.

On Response
The frequency response of the on switch.

Insertion Loss
The loss due to the on resistance of the switch.

TYPICAL PERFORMANCE CHARACTERISTICS

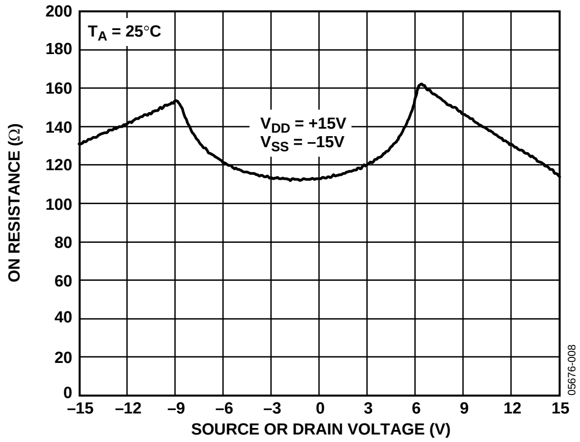


Figure 3. On Resistance as a Function of V_D (V_S) for Dual Supply

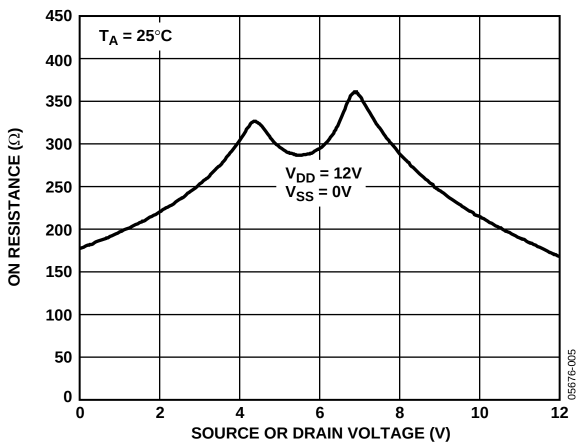


Figure 4. On Resistance as a Function of V_D (V_S) for Single Supply

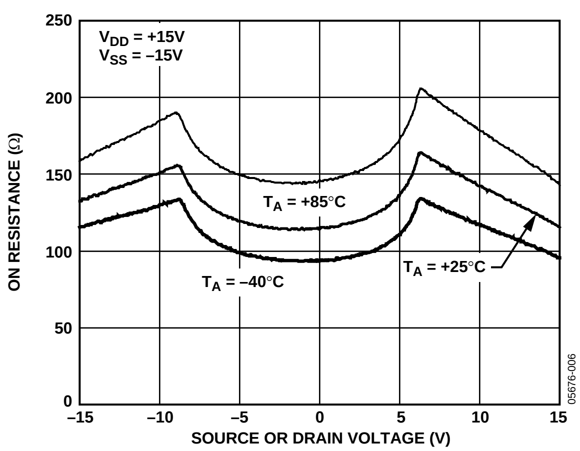


Figure 5. On Resistance as a Function of V_D (V_S) for Different Temperatures, Dual Supply

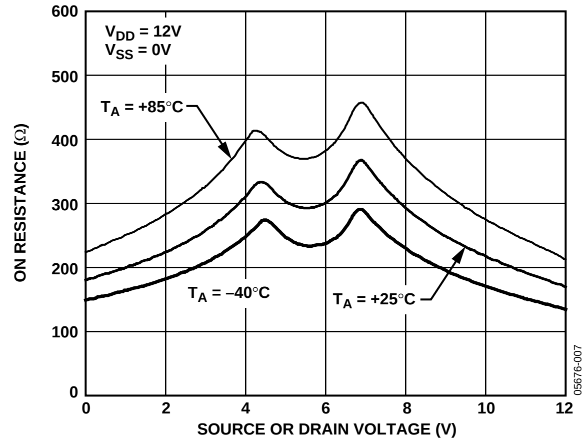


Figure 6. On Resistance as a Function of V_D (V_S) for Different Temperatures, Single Supply

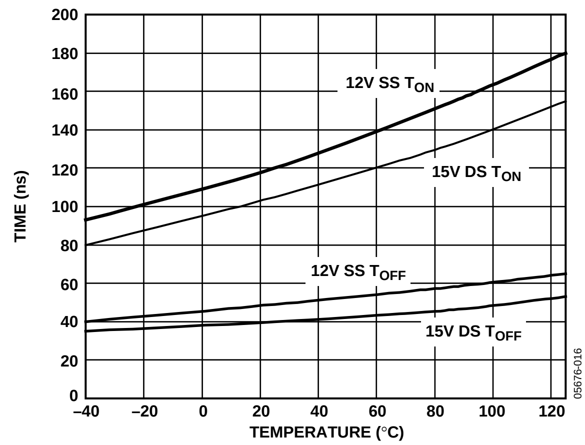


Figure 7. T_{ON}/T_{OFF} Times vs. Temperature

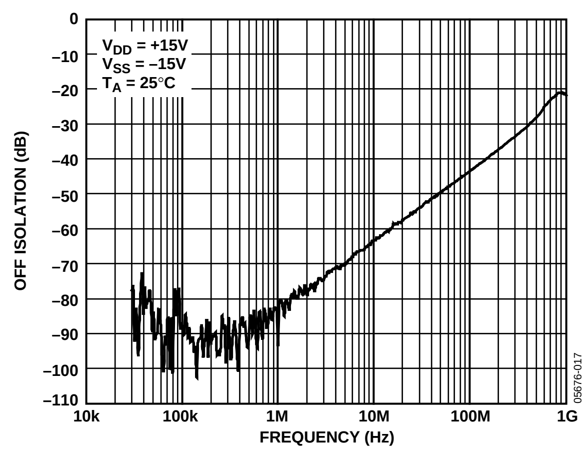


Figure 8. Off Isolation vs. Frequency

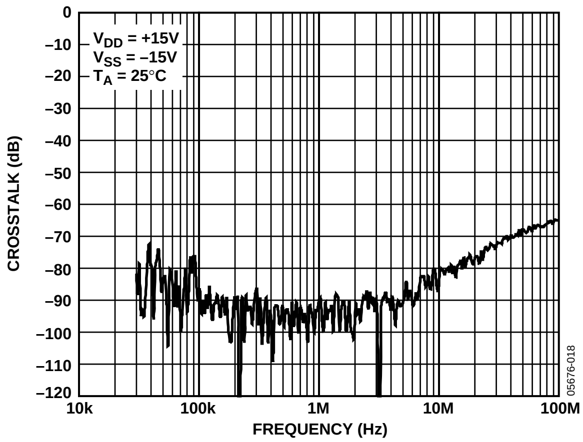


Figure 9. Crosstalk vs. Frequency

TEST CIRCUITS

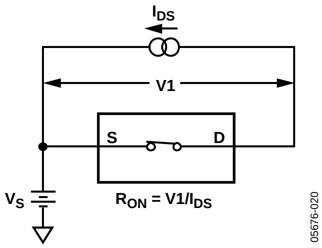


Figure 10. On Resistance

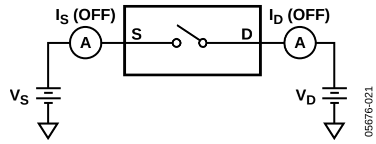


Figure 11. Off Leakage

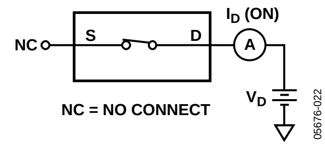


Figure 12. On Leakage

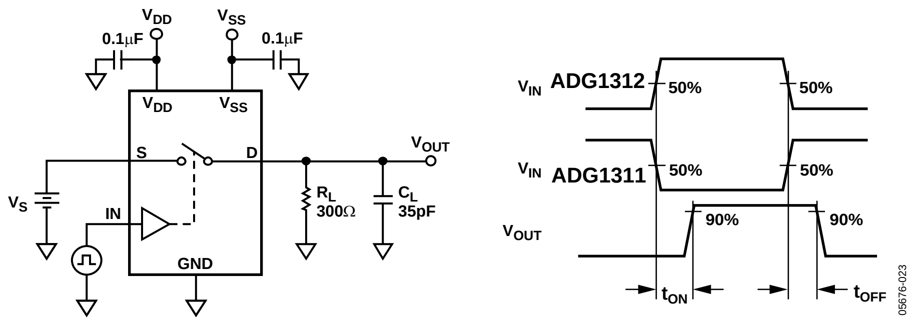


Figure 13. Switching Times

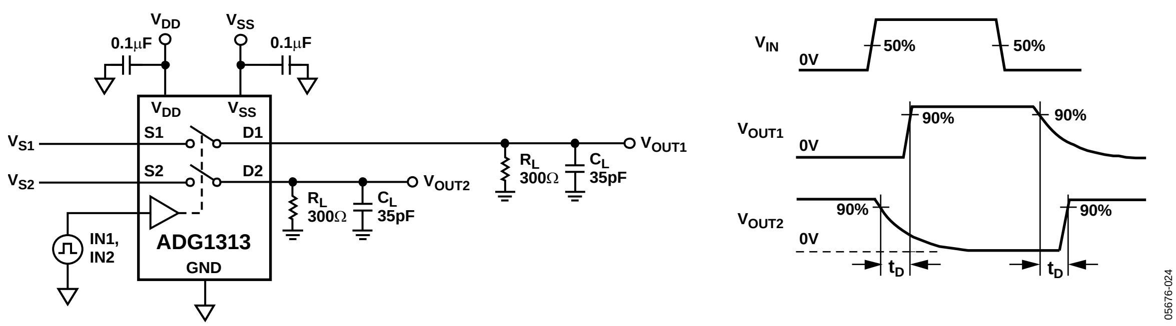


Figure 14. Break-Before-Make Time Delay

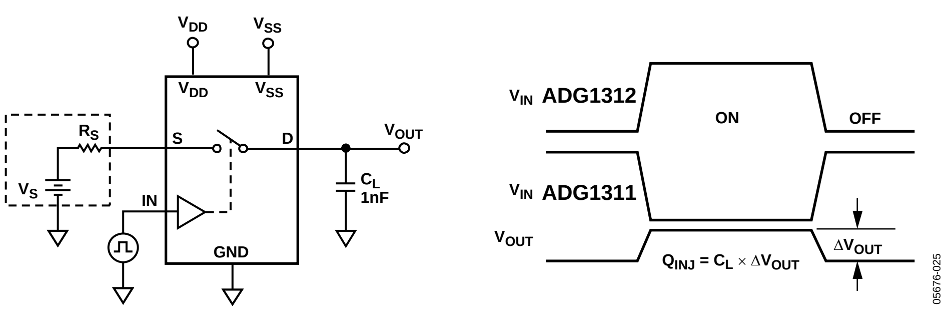


Figure 15. Charge Injection

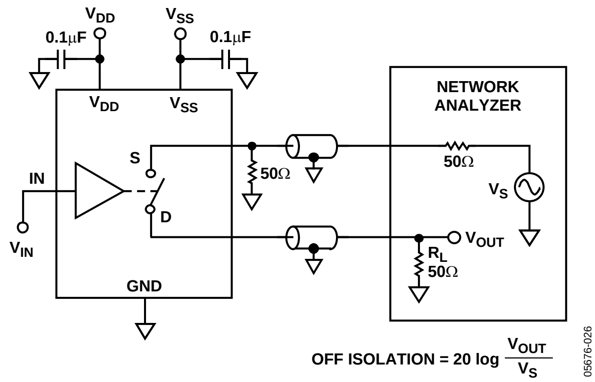


Figure 16. Off Isolation

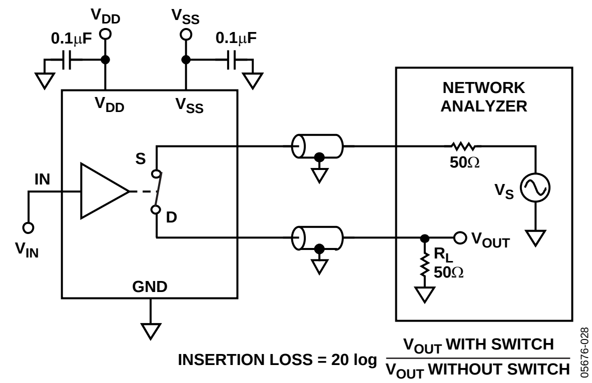


Figure 18. Bandwidth

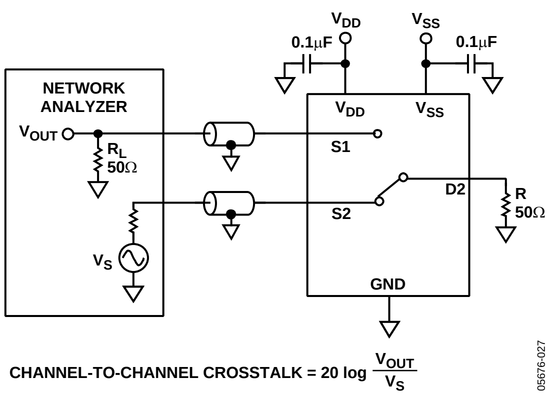
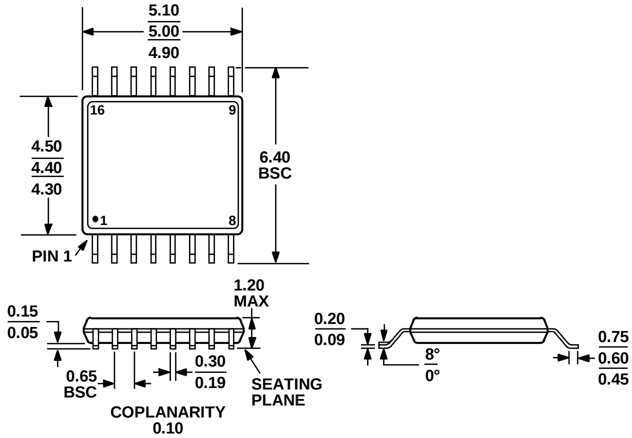


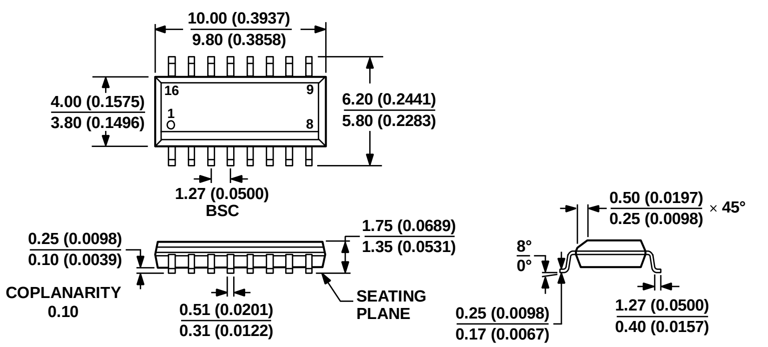
Figure 17. Channel-to-Channel Crosstalk

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-153-AB

Figure 19. 16-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-16)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MS-012-AC

CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

060606-A

Figure 20. 16-Lead Standard Small Outline Package [SOIC_N]
Narrow Body (R-16)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADG1311YRUZ[1]	−40°C to +105°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG1311YRUZ-REEL7[1]	−40°C to +105°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG1311YRZ[1]	−40°C to +105°C	16-Lead Narrow Body Small Outline Package [SOIC_N]	R-16
ADG1311YRZ-REEL7[1]	−40°C to +105°C	16-Lead Narrow Body Small Outline Package [SOIC_N]	R-16
ADG1312YRUZ[1]	−40°C to +105°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG1312YRUZ-REEL7[1]	−40°C to +105°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG1312YRZ[1]	−40°C to +105°C	16-Lead Narrow Body Small Outline Package [SOIC_N]	R-16
ADG1312YRZ-REEL7[1]	−40°C to +105°C	16-Lead Narrow Body Small Outline Package [SOIC_N]	R-16
ADG1313YRUZ[1]	−40°C to +105°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG1313YRUZ-REEL7[1]	−40°C to +105°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG1313YRZ[1]	−40°C to +105°C	16-Lead Narrow Body Small Outline Package [SOIC_N]	R-16
ADG1313YRZ-REEL7[1]	−40°C to +105°C	16-Lead Narrow Body Small Outline Package [SOIC_N]	R-16

[1] Z = RoHS Compliant Part.

D05676-0-2/09(A)

www.analog.com