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## REVISION HISTORY

**5/2016—Rev. 0 to Rev. A**

Changed ADA4939 to ADA4939-1/ADA4939-2, CP-16-2 to CP-16-21, and CP-24-1 to CP-24-10 ... Throughout
Changes to Figure 5, Figure 6, Table 9, and Table 10 ... 8
Changes to Figure 54 ... 23
Updated Outline Dimensions ... 24
Changes to Ordering Guide ... 24

**5/2008—Revision 0: Initial Version**

# SPECIFICATIONS

## 5 V OPERATION

$T_A$ = 25°C, $+V_S$ = 5 V, $-V_S$ = 0 V, $V_{OCM}$ = $+V_S/2$, $R_F$ = 402 Ω, $R_G$ = 200 Ω, $R_T$ = 60.4 Ω (when used), $R_{L, dm}$ = 1 kΩ, unless otherwise noted. All specifications refer to single-ended input and differential outputs, unless otherwise noted. Refer to Figure 42 for signal definitions.

### *±$D_{IN}$ to $V_{OUT, dm}$ Performance*

**Table 1.**

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| DYNAMIC PERFORMANCE | | | | | |
| −3 dB Small Signal Bandwidth | $V_{OUT, dm}$ = 0.1 V p-p | | 1400 | | MHz |
| Bandwidth for 0.1 dB Flatness | $V_{OUT, dm}$ = 0.1 V p-p, ADA4939-1 | | 300 | | MHz |
| | $V_{OUT, dm}$ = 0.1 V p-p, ADA4939-2 | | 90 | | MHz |
| Large Signal Bandwidth | $V_{OUT, dm}$ = 2 V p-p | | 1400 | | MHz |
| Slew Rate | $V_{OUT, dm}$ = 2 V p-p, 25% to 75% | | 6800 | | V/µs |
| Overdrive Recovery Time | $V_{IN}$ = 0 V to 1.5 V step, G = 3.16 | | <1 | | ns |
| NOISE/HARMONIC PERFORMANCE | See Figure 41 for distortion test circuit | | | | |
| Second Harmonic | $V_{OUT, dm}$ = 2 V p-p, 10 MHz | | −102 | | dBc |
| | $V_{OUT, dm}$ = 2 V p-p, 70 MHz | | −83 | | dBc |
| | $V_{OUT, dm}$ = 2 V p-p, 100 MHz | | −77 | | dBc |
| Third Harmonic | $V_{OUT, dm}$ = 2 V p-p, 10 MHz | | −101 | | dBc |
| | $V_{OUT, dm}$ = 2 V p-p, 70 MHz | | −97 | | dBc |
| | $V_{OUT, dm}$ = 2 V p-p, 100 MHz | | −91 | | dBc |
| IMD | $f_1$ = 70 MHz, $f_2$ = 70.1 MHz, $V_{OUT, dm}$ = 2 V p-p | | −95 | | dBc |
| | $f_1$ = 140 MHz, $f_2$ = 140.1 MHz, $V_{OUT, dm}$ = 2 V p-p | | −89 | | dBc |
| Voltage Noise (RTI) | f = 100 kHz | | 2.3 | | nV/√Hz |
| Input Current Noise | f = 100 kHz | | 6 | | pA/√Hz |
| Crosstalk | f = 100 MHz, ADA4939-2 | | −80 | | dB |
| INPUT CHARACTERISTICS | | | | | |
| Offset Voltage | $V_{OS, dm} = V_{OUT, dm}/2$, $V_{DIN+} = V_{DIN-}$ = 2.5 V | −3.4 | ±0.5 | +2.8 | mV |
| | $T_{MIN}$ to $T_{MAX}$ variation | | ±2.0 | | µV/°C |
| Input Bias Current | | −26 | −10 | +2.2 | µA |
| | $T_{MIN}$ to $T_{MAX}$ variation | | ±0.5 | | µA/°C |
| Input Offset Current | | −11.2 | +0.5 | +11.2 | µA |
| Input Resistance | Differential | | 180 | | kΩ |
| | Common mode | | 450 | | kΩ |
| Input Capacitance | | | 1 | | pF |
| Input Common-Mode Voltage | | 1.1 | | 3.9 | V |
| CMRR | $\Delta V_{OUT, dm}/\Delta V_{IN, cm}$, $\Delta V_{IN, cm}$ = ±1 V | | −83 | −77 | dB |
| OUTPUT CHARACTERISTICS | | | | | |
| Output Voltage Swing | Maximum $\Delta V_{OUT}$; single-ended output, $R_F = R_G$ = 10 kΩ | 0.9 | | 4.1 | V |
| Linear Output Current | | | 100 | | mA |
| Output Balance Error | $\Delta V_{OUT, cm}/\Delta V_{OUT, dm}$, $\Delta V_{OUT, dm}$ = 1 V, 10 MHz, see Figure 40 for test circuit | | −64 | | dB |

### $V_{OCM}$ to $V_{OUT, cm}$ Performance

**Table 2.**

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $V_{OCM}$ DYNAMIC PERFORMANCE | | | | | |
| −3 dB Bandwidth | | | 670 | | MHz |
| Slew Rate | $V_{IN}$ = 1.5 V to 3.5 V, 25% to 75% | | 2500 | | V/µs |
| Input Voltage Noise (RTI) | f = 100 kHz | | 7.5 | | nV/√Hz |
| $V_{OCM}$ INPUT CHARACTERISTICS | | | | | |
| Input Voltage Range | | 1.3 | | 3.5 | V |
| Input Resistance | | 8.3 | 9.7 | 11.5 | kΩ |
| Input Offset Voltage | $V_{OS, cm} = V_{OUT, cm}$, $V_{DIN+} = V_{DIN-} = +V_S/2$ | −3.7 | ±0.5 | +3.7 | mV |
| $V_{OCM}$ CMRR | $\Delta V_{OUT, dm}/\Delta V_{OCM}$, $\Delta V_{OCM}$ = ±1 V | | −90 | −73 | dB |
| Gain | $\Delta V_{OUT, cm}/\Delta V_{OCM}$, $\Delta V_{OCM}$ = ±1 V | 0.97 | 0.98 | 0.99 | V/V |

### General Performance

**Table 3.**

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| POWER SUPPLY | | | | | |
| Operating Range | | 3.0 | | 5.25 | V |
| Quiescent Current per Amplifier | | 35.1 | 36.5 | 37.7 | mA |
| | $T_{MIN}$ to $T_{MAX}$ variation | | 16 | | µA/°C |
| | Powered down | 0.26 | 0.32 | 0.38 | mA |
| Power Supply Rejection Ratio | $\Delta V_{OUT, dm}/\Delta V_S$, $\Delta V_S$ = 1 V | | −90 | −80 | dB |
| POWER-DOWN ($\overline{PD}$) | | | | | |
| $\overline{PD}$ Input Voltage | Powered down | | ≤1 | | V |
| | Enabled | | ≥2 | | V |
| Turn-Off Time | | | 500 | | ns |
| Turn-On Time | | | 100 | | ns |
| $\overline{PD}$ Pin Bias Current per Amplifier | | | | | |
| Enabled | $\overline{PD}$ = 5 V | | 30 | | µA |
| Disabled | $\overline{PD}$ = 0 V | | −200 | | µA |
| OPERATING TEMPERATURE RANGE | | −40 | | +105 | °C |

## 3.3 V OPERATION

$T_A$ = 25°C, $+V_S$ = 3.3 V, $-V_S$ = 0 V, $V_{OCM}$ = $+V_S$/2, $R_F$ = 402 Ω, $R_G$ = 200 Ω, $R_T$ = 60.4 Ω (when used), $R_{L, dm}$ = 1 kΩ, unless otherwise noted. All specifications refer to single-ended input and differential outputs, unless otherwise noted. Refer to Figure 42 for signal definitions.

### *±$D_{IN}$ to $V_{OUT, dm}$ Performance*

**Table 4.**

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| DYNAMIC PERFORMANCE | | | | | |
| −3 dB Small Signal Bandwidth | $V_{OUT, dm}$ = 0.1 V p-p | | 1400 | | MHz |
| Bandwidth for 0.1 dB Flatness | $V_{OUT, dm}$ = 0.1 V p-p, ADA4939-1 | | 300 | | MHz |
| | $V_{OUT, dm}$ = 0.1 V p-p, ADA4939-2 | | 90 | | MHz |
| Large Signal Bandwidth | $V_{OUT, dm}$ = 2 V p-p | | 1400 | | MHz |
| Slew Rate | $V_{OUT, dm}$ = 2 V p-p, 25% to 75% | | 5000 | | V/µs |
| Overdrive Recovery Time | $V_{IN}$ = 0 V to 1.0 V step, G = 3.16 | | <1 | | ns |
| NOISE/HARMONIC PERFORMANCE | See Figure 41 for distortion test circuit | | | | |
| Second Harmonic | $V_{OUT, dm}$ = 2 V p-p, 10 MHz | | −100 | | dBc |
| | $V_{OUT, dm}$ = 2 V p-p, 70 MHz | | −90 | | dBc |
| | $V_{OUT, dm}$ = 2 V p-p, 100 MHz | | −83 | | dBc |
| Third Harmonic | $V_{OUT, dm}$ = 2 V p-p, 10 MHz | | −94 | | dBc |
| | $V_{OUT, dm}$ = 2 V p-p, 70 MHz | | −82 | | dBc |
| | $V_{OUT, dm}$ = 2 V p-p, 100 MHz | | −75 | | dBc |
| IMD | $f_1$ = 70 MHz, $f_2$ = 70.1 MHz, $V_{OUT, dm}$ = 2 V p-p | | −87 | | dBc |
| | $f_1$ = 140 MHz, $f_2$ = 140.1 MHz, $V_{OUT, dm}$ = 2 V p-p | | −70 | | dBc |
| Voltage Noise (RTI) | f = 100 kHz | | 2.3 | | nV/√Hz |
| Input Current Noise | f = 100 kHz | | 6 | | pA/√Hz |
| Crosstalk | f = 100 MHz, ADA4939-2 | | −80 | | dB |
| INPUT CHARACTERISTICS | | | | | |
| Offset Voltage | $V_{OS, dm} = V_{OUT, dm}/2$, $V_{DIN+} = V_{DIN-} = +V_S/2$ | −3.5 | ±0.5 | +3.5 | mV |
| | $T_{MIN}$ to $T_{MAX}$ variation | | ±2.0 | | µV/°C |
| Input Bias Current | | −26 | −10 | +2.2 | µA |
| | $T_{MIN}$ to $T_{MAX}$ variation | | ±0.5 | | µA/°C |
| Input Offset Current | | −11.2 | ±0.4 | +11.2 | |
| Input Resistance | Differential | | 180 | | kΩ |
| | Common mode | | 450 | | kΩ |
| Input Capacitance | | | 1 | | pF |
| Input Common-Mode Voltage | | 0.9 | | 2.4 | V |
| CMRR | $\Delta V_{OUT, dm}/\Delta V_{IN, cm}$, $\Delta V_{IN, cm}$ = ±1 V | | −85 | −75 | dB |
| OUTPUT CHARACTERISTICS | | | | | |
| Output Voltage Swing | Maximum $\Delta V_{OUT}$, single-ended output, $R_F = R_G$ = 10 kΩ | 0.8 | | 2.5 | V |
| Linear Output Current | | | 75 | | mA |
| Output Balance Error | $\Delta V_{OUT, cm}/\Delta V_{OUT, dm}$, $\Delta V_{OUT, dm}$ = 1 V, f = 10 MHz, see Figure 40 for test circuit | | −61 | | dB |

### $V_{OCM}$ to $V_{OUT, cm}$ Performance

**Table 5.**

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $V_{OCM}$ DYNAMIC PERFORMANCE | | | | | |
| −3 dB Bandwidth | | | 560 | | MHz |
| Slew Rate | $V_{IN}$ = 0.9 V to 2.4 V, 25% to 75% | | 1250 | | V/µs |
| Input Voltage Noise (RTI) | f = 100 kHz | | 7.5 | | nV/√Hz |
| $V_{OCM}$ INPUT CHARACTERISTICS | | | | | |
| Input Voltage Range | | 1.3 | | 1.9 | V |
| Input Resistance | | 8.3 | 9.7 | 11.2 | kΩ |
| Input Offset Voltage | $V_{OS, cm} = V_{OUT, cm}$, $V_{DIN+} = V_{DIN-}$ = 1.67 V | −3.7 | ±0.5 | +3.7 | mV |
| $V_{OCM}$ CMRR | $\Delta V_{OUT, dm}/\Delta V_{OCM}$, $\Delta V_{OCM}$ = ±1 V | | −75 | −73 | dB |
| Gain | $\Delta V_{OUT, cm}/\Delta V_{OCM}$, $\Delta V_{OCM}$ = ±1 V | 0.97 | 0.98 | 0.99 | V/V |

### General Performance

**Table 6.**

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| POWER SUPPLY | | | | | |
| Operating Range | | 3.0 | | 5.25 | V |
| Quiescent Current per Amplifier | | 32.8 | 34.5 | 36.0 | mA |
| | $T_{MIN}$ to $T_{MAX}$ variation | | 16 | | µA/°C |
| | Powered down | 0.16 | 0.20 | 0.26 | mA |
| Power Supply Rejection Ratio | $\Delta V_{OUT, dm}/\Delta V_S$, $\Delta V_S$ = 1 V | | −84 | −72 | dB |
| POWER-DOWN ($\overline{PD}$) | | | | | |
| $\overline{PD}$ Input Voltage | Powered down | | ≤1 | | V |
| | Enabled | | ≥2 | | V |
| Turn-Off Time | | | 500 | | ns |
| Turn-On Time | | | 100 | | ns |
| $\overline{PD}$ Pin Bias Current per Amplifier | | | | | |
| Enabled | $\overline{PD}$ = 3.3 V | | 26 | | µA |
| Disabled | $\overline{PD}$ = 0 V | | −137 | | µA |
| OPERATING TEMPERATURE RANGE | | −40 | | +105 | °C |

# ABSOLUTE MAXIMUM RATINGS

**Table 7.**

| Parameter | Rating |
|---|---|
| Supply Voltage | 5.5 V |
| Power Dissipation | See Figure 4 |
| Input Current, +IN, –IN, $\overline{PD}$ | ±5 mA |
| Storage Temperature Range | –65°C to +125°C |
| Operating Temperature Range | |
| ADA4939-1 | –40°C to +105°C |
| ADA4939-2 | –40°C to +105°C |
| Lead Temperature (Soldering, 10 sec) | 300°C |
| Junction Temperature | 150°C |

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

## THERMAL RESISTANCE

$\theta_{JA}$ is specified for the device (including exposed pad) soldered to a high thermal conductivity 2s2p circuit board, as described in EIA/JESD 51-7.

**Table 8. Thermal Resistance**

| Package Type | $\theta_{JA}$ | Unit |
|---|---|---|
| ADA4939-1, 16-Lead LFCSP (Exposed Pad) | 98 | °C/W |
| ADA4939-2, 24-Lead LFCSP (Exposed Pad) | 67 | °C/W |

## MAXIMUM POWER DISSIPATION

The maximum safe power dissipation for the ADA4939-1/ ADA4939-2 package is limited by the associated rise in junction temperature ($T_J$) on the die. At approximately 150°C, which is the glass transition temperature, the plastic changes its properties. Even temporarily exceeding this temperature limit can change the stresses that the package exerts on the die, permanently shifting the parametric performance of the ADA4939-1/ ADA4939-2. Exceeding a junction temperature of 150°C for an extended period can result in changes in the silicon devices, potentially causing failure.

The power dissipated in the package ($P_D$) is the sum of the quiescent power dissipation and the power dissipated in the package due to the load drive. The quiescent power is the voltage between the supply pins ($V_S$) times the quiescent current ($I_S$). The power dissipated due to the load drive depends upon the particular application. Calculate the power due to the load drive by multiplying the load current by the associated voltage drop across the device. RMS voltages and currents must be used in these calculations.

Airflow increases heat dissipation, effectively reducing $\theta_{JA}$. In addition, more metal directly in contact with the package leads/ exposed pad from metal traces, through holes, ground, and power planes reduces $\theta_{JA}$.

Figure 4 shows the maximum safe power dissipation in the package vs. the ambient temperature for the single 16-lead LFCSP (98°C/W) and the dual 24-lead LFCSP (67°C/W) on a JEDEC standard 4-layer board with the exposed pad soldered to a PCB pad that is connected to a solid plane.

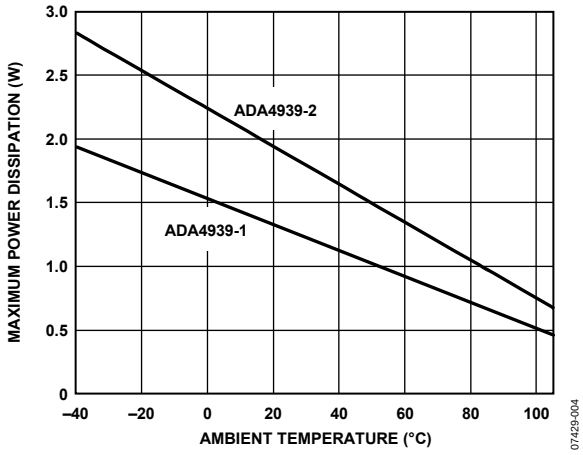


*Figure 4. Maximum Power Dissipation vs. Ambient Temperature for a 4-Layer Board*

## ESD CAUTION

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

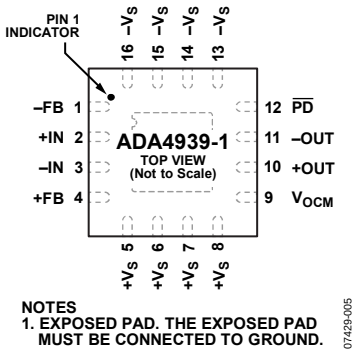


*Figure 5. ADA4939-1 Pin Configuration*

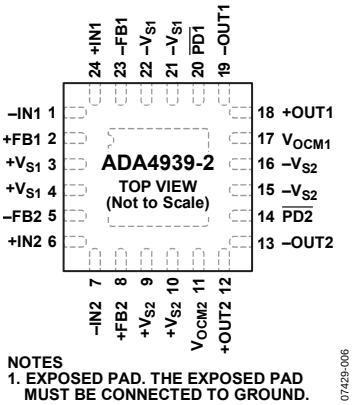


*Figure 6. ADA4939-2 Pin Configuration*

**Table 9. ADA4939-1 Pin Function Descriptions**

| Pin No. | Mnemonic | Description |
|---|---|---|
| 1 | –FB | Negative Output for Feedback Component Connection |
| 2 | +IN | Positive Input Summing Node |
| 3 | –IN | Negative Input Summing Node |
| 4 | +FB | Positive Output for Feedback Component Connection |
| 5 to 8 | $+V_S$ | Positive Supply Voltage |
| 9 | $V_{OCM}$ | Output Common-Mode Voltage |
| 10 | +OUT | Positive Output for Load Connection |
| 11 | –OUT | Negative Output for Load Connection |
| 12 | $\overline{PD}$ | Power-Down Pin |
| 13 to 16 | $-V_S$ | Negative Supply Voltage |
| | EPAD | Exposed Pad. The exposed pad must be connected to ground. |

**Table 10. ADA4939-2 Pin Function Descriptions**

| Pin No. | Mnemonic | Description |
|---|---|---|
| 1 | –IN1 | Negative Input Summing Node 1 |
| 2 | +FB1 | Positive Output Feedback 1 |
| 3, 4 | $+V_{S1}$ | Positive Supply Voltage 1 |
| 5 | –FB2 | Negative Output Feedback 2 |
| 6 | +IN2 | Positive Input Summing Node 2 |
| 7 | –IN2 | Negative Input Summing Node 2 |
| 8 | +FB2 | Positive Output Feedback 2 |
| 9, 10 | $+V_{S2}$ | Positive Supply Voltage 2 |
| 11 | $V_{OCM2}$ | Output Common-Mode Voltage 2 |
| 12 | +OUT2 | Positive Output 2 |
| 13 | –OUT2 | Negative Output 2 |
| 14 | $\overline{PD2}$ | Power-Down Pin 2 |
| 15, 16 | $-V_{S2}$ | Negative Supply Voltage 2 |
| 17 | $V_{OCM1}$ | Output Common-Mode Voltage 1 |
| 18 | +OUT1 | Positive Output 1 |
| 19 | –OUT1 | Negative Output 1 |
| 20 | $\overline{PD1}$ | Power-Down Pin 1 |
| 21, 22 | $-V_{S1}$ | Negative Supply Voltage 1 |
| 23 | –FB1 | Negative Output Feedback 1 |
| 24 | +IN1 | Positive Input Summing Node 1 |
| | EPAD | Exposed Pad. The exposed pad must be connected to ground. |

# TYPICAL PERFORMANCE CHARACTERISTICS

$T_A$ = 25°C, $+V_S$ = 5 V, $-V_S$ = 0 V, $V_{OCM}$ = $+V_S$ /2, $R_G$ = 200 Ω, $R_F$ = 402 Ω, $R_T$ = 60.4 Ω, G = 1, $R_{L, dm}$ = 1 kΩ, unless otherwise noted. Refer to Figure 39 for test setup. Refer to Figure 42 for signal definitions.

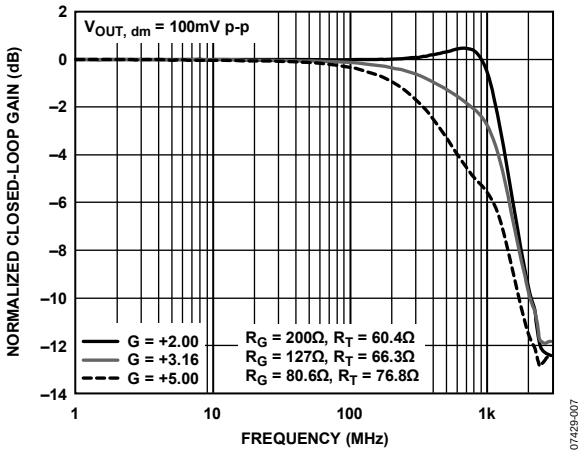


Figure 7. Small Signal Frequency Response for Various Gains

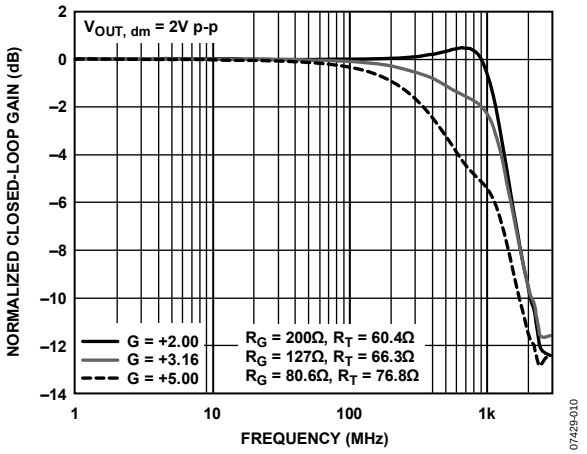


Figure 10. Large Signal Frequency Response for Various Gains

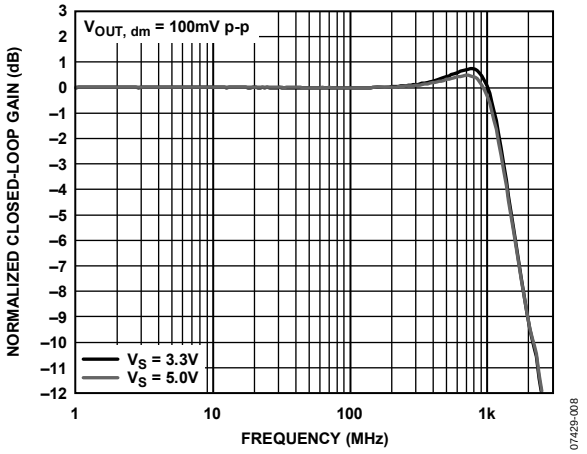


Figure 8. Small Signal Frequency Response for Various Supplies

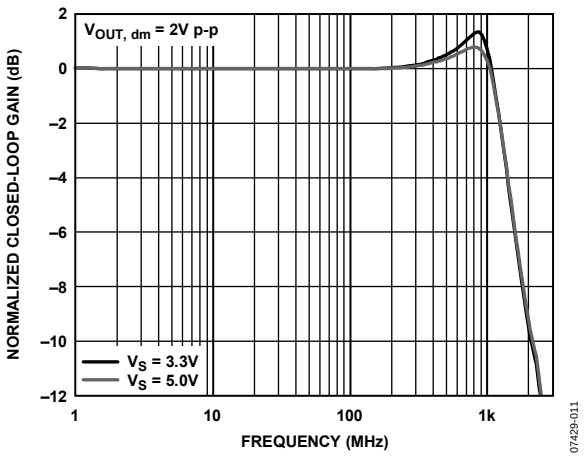


Figure 11. Large Signal Frequency Response for Various Supplies

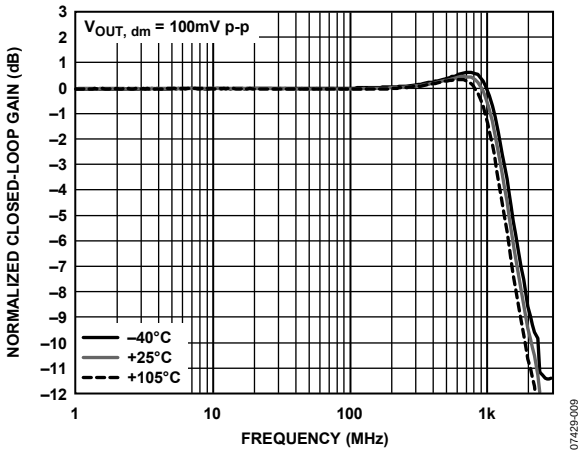


Figure 9. Small Signal Frequency Response for Various Temperatures

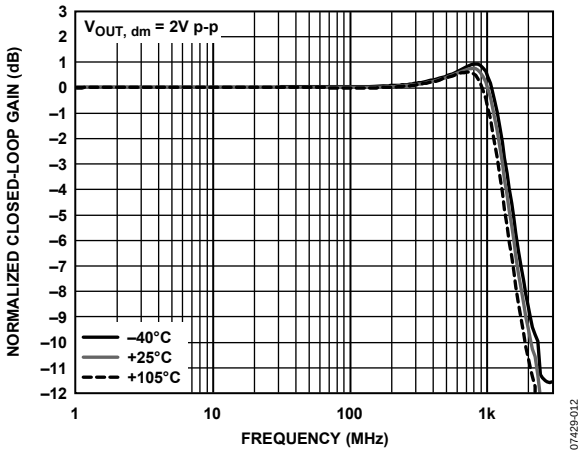


Figure 12. Large Signal Frequency Response for Various Temperatures

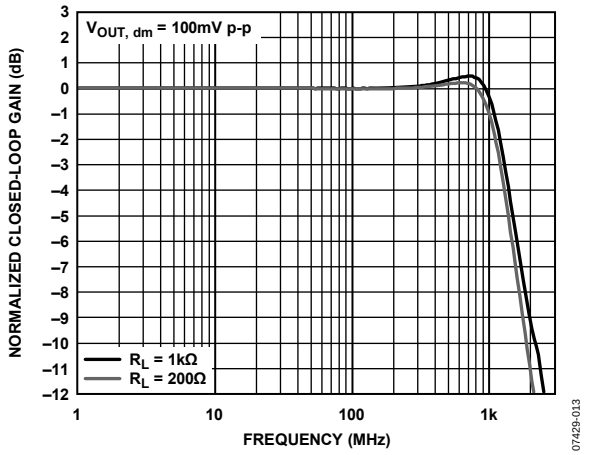


Figure 13. Small Signal Frequency Response for Various Loads

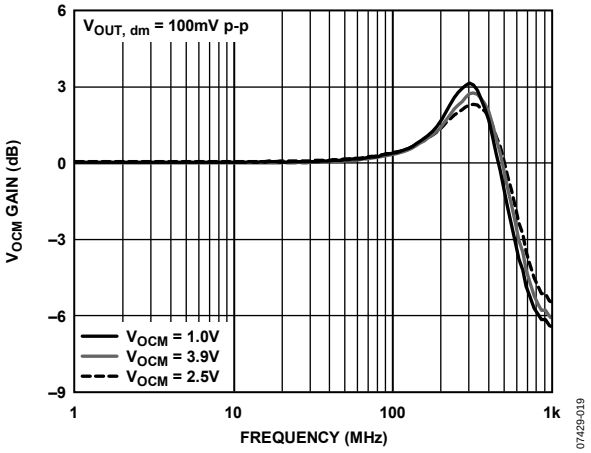


Figure 14. $V_{OCM}$ Small Signal Frequency Response at Various DC Levels

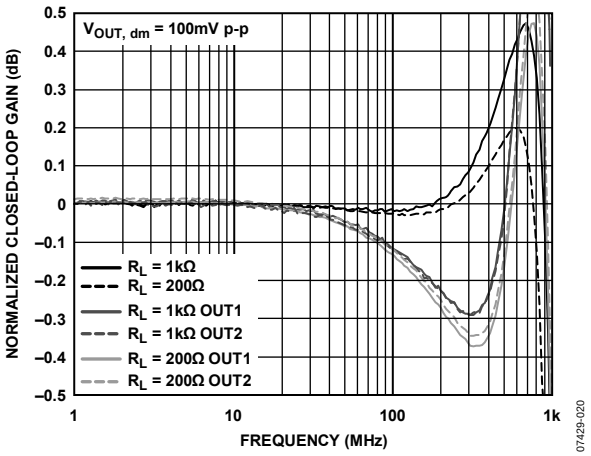


Figure 15. 0.1 dB Flatness Small Signal Response for Various Loads

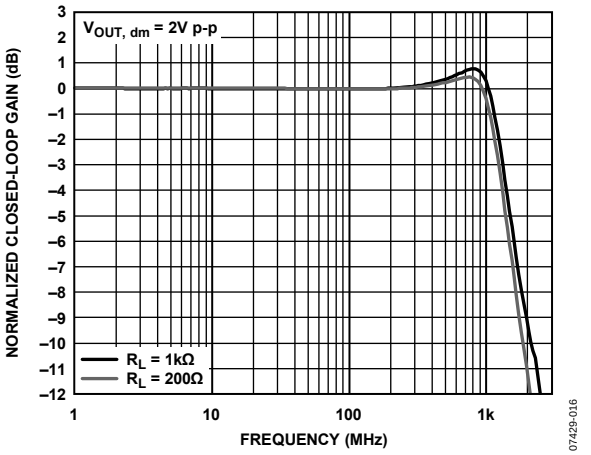


Figure 16. Large Signal Frequency Response for Various Loads

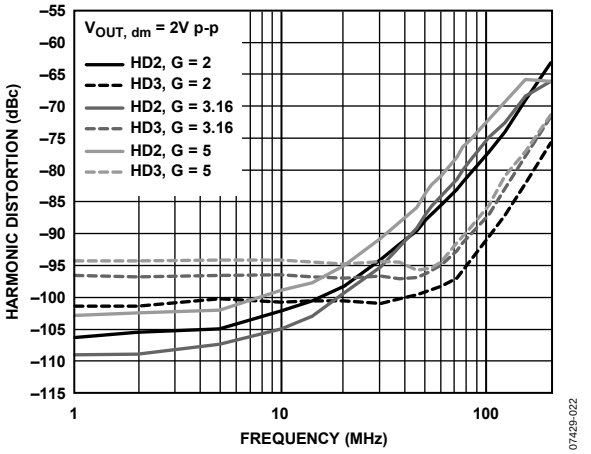


Figure 17. Harmonic Distortion vs. Frequency at Various Gains

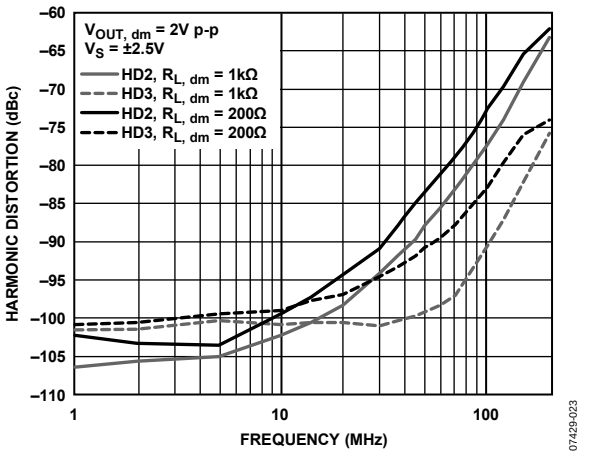


Figure 18. Harmonic Distortion vs. Frequency at Various Loads

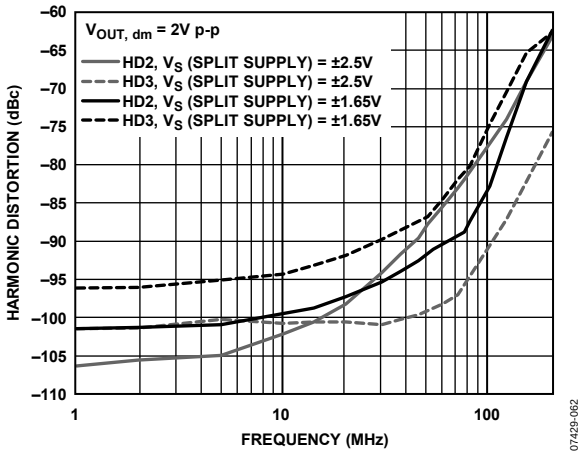


Figure 19. Harmonic Distortion vs. Frequency at Various Supplies

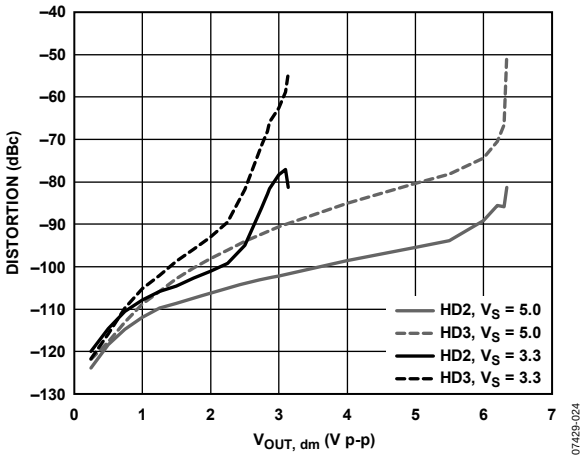


Figure 22. Harmonic Distortion vs. $V_{OUT, dm}$ and Supply Voltage, f = 10 MHz

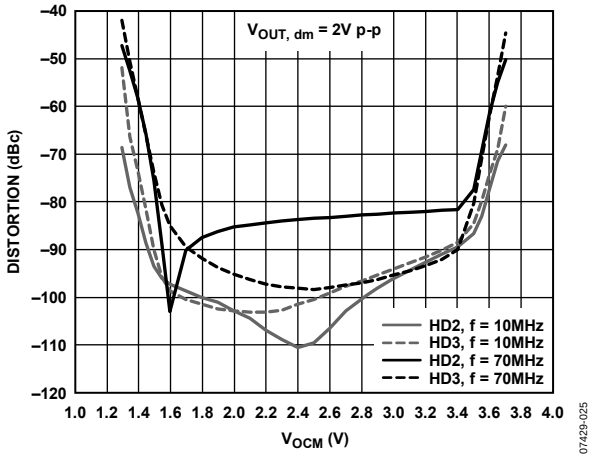


Figure 20. Harmonic Distortion vs. $V_{OCM}$ at Various Frequencies

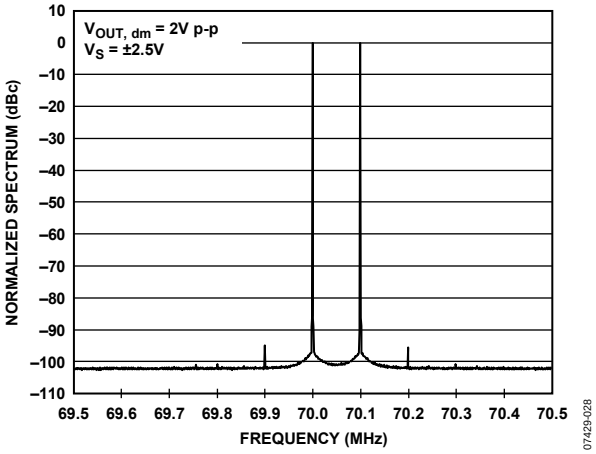


Figure 23. 70 MHz Intermodulation Distortion

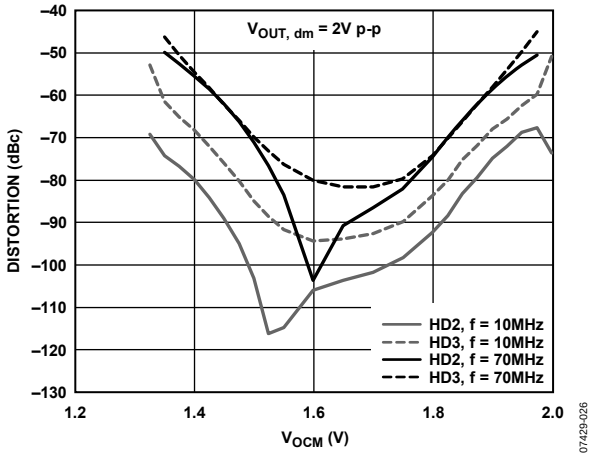


Figure 21. Harmonic Distortion vs. $V_{OCM}$ at Various Frequencies

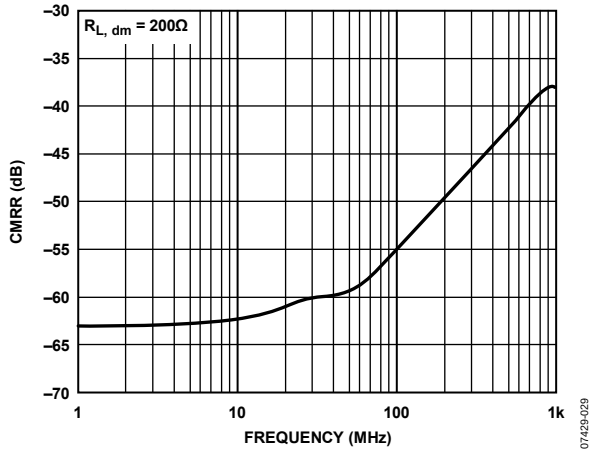


Figure 24. CMRR vs. Frequency

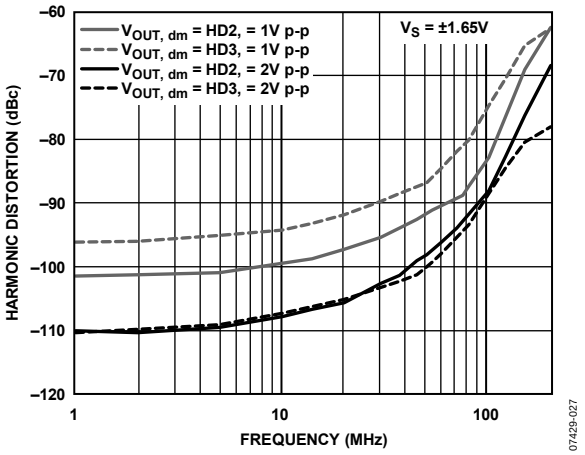


Figure 25. Harmonic Distortion vs. Frequency at Various Output Voltages

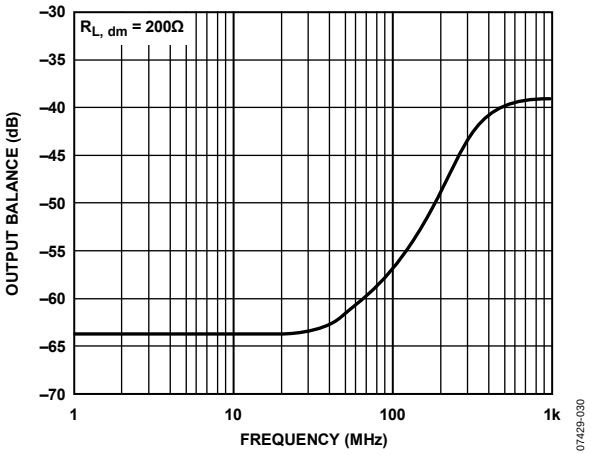


Figure 28. Output Balance vs. Frequency

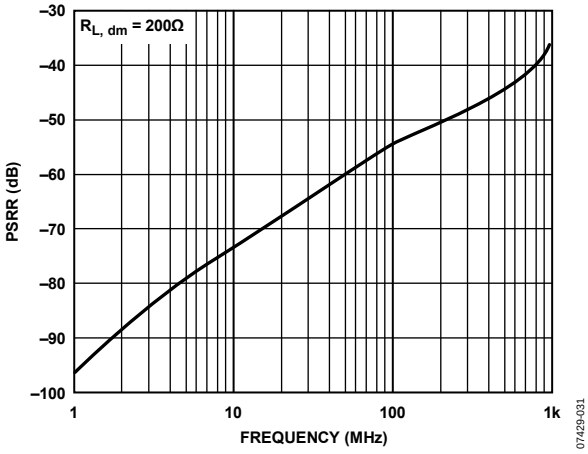


Figure 26. PSRR vs. Frequency, $R_L$ = 200 Ω

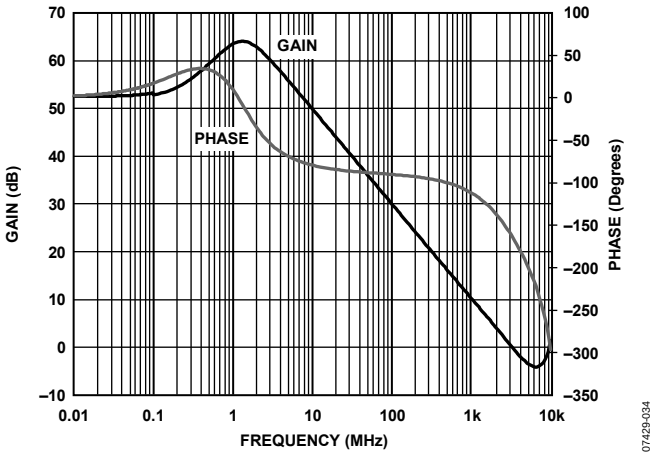


Figure 29. Open-Loop Gain and Phase vs. Frequency

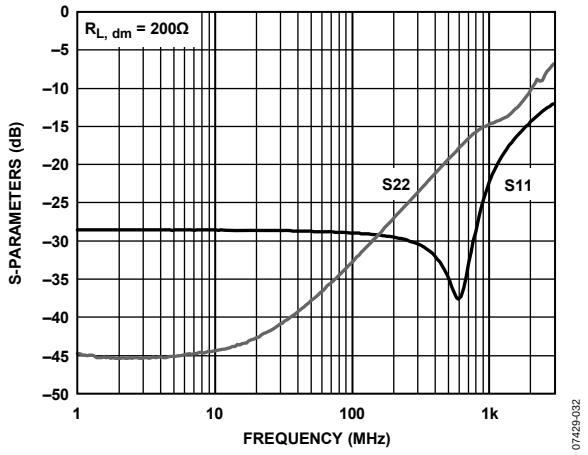


Figure 27. Return Loss (S11, S22) vs. Frequency

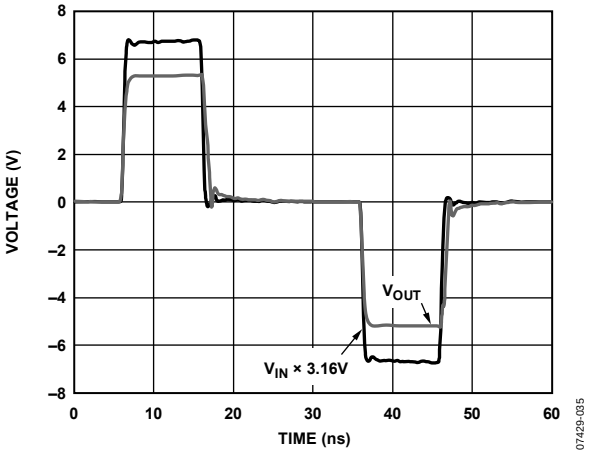


Figure 30. Overdrive Recovery, G = 3.16

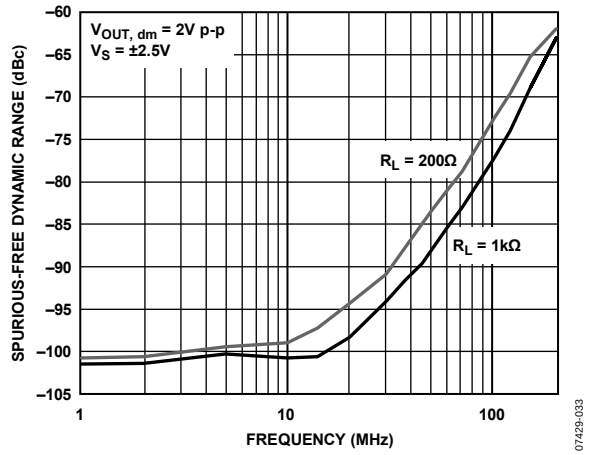


Figure 31. Spurious-Free Dynamic Range vs. Frequency at Various Loads

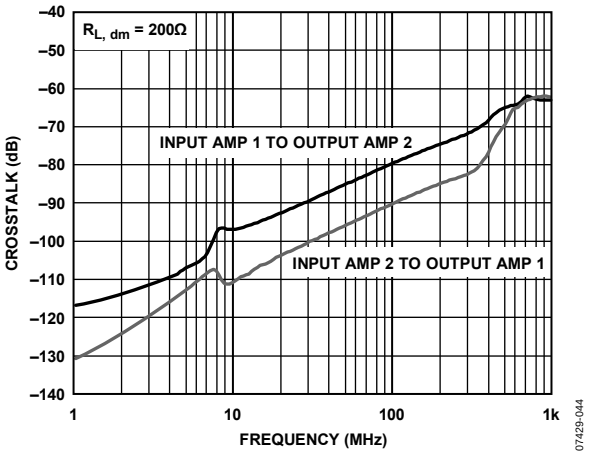


Figure 34. Crosstalk vs. Frequency for ADA4939-2

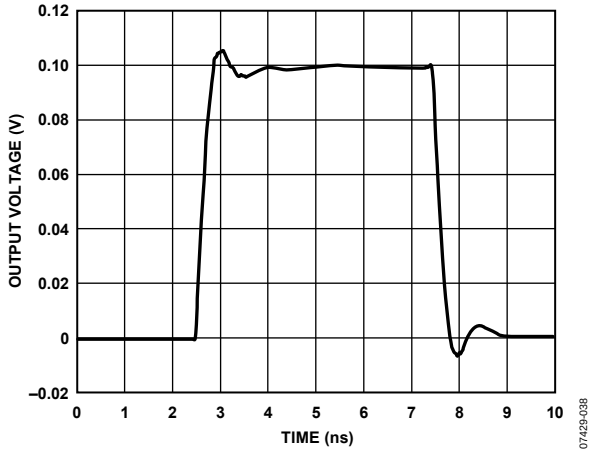


Figure 32. Small Signal Pulse Response

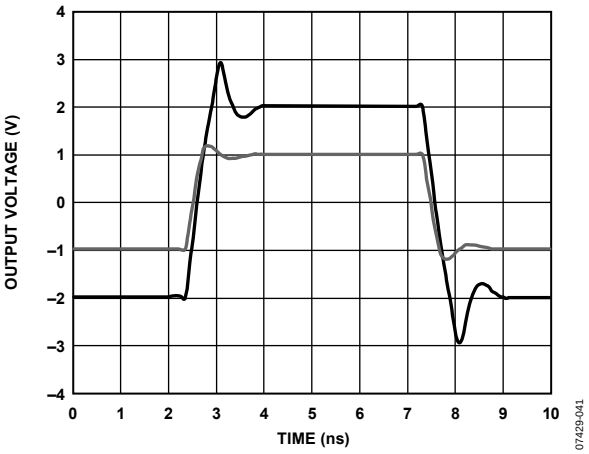


Figure 35. Large Signal Pulse Response

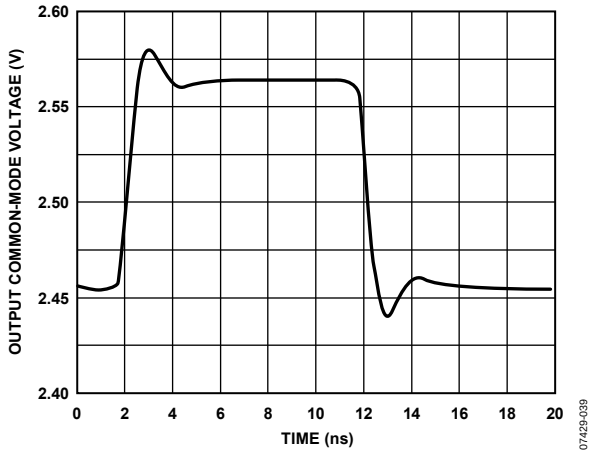


Figure 33. $V_{OCM}$ Small Signal Pulse Response

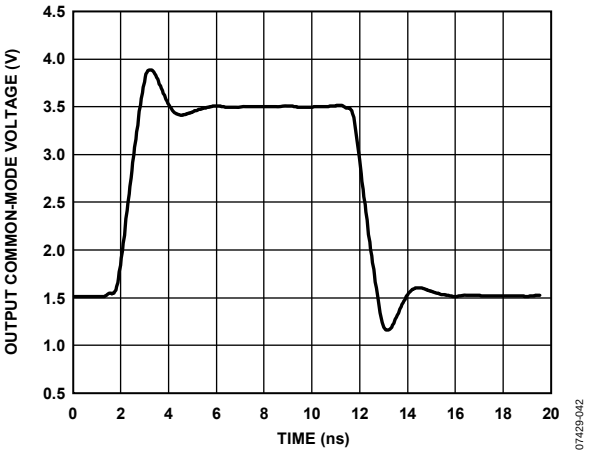


Figure 36. $V_{OCM}$ Large Signal Pulse Response

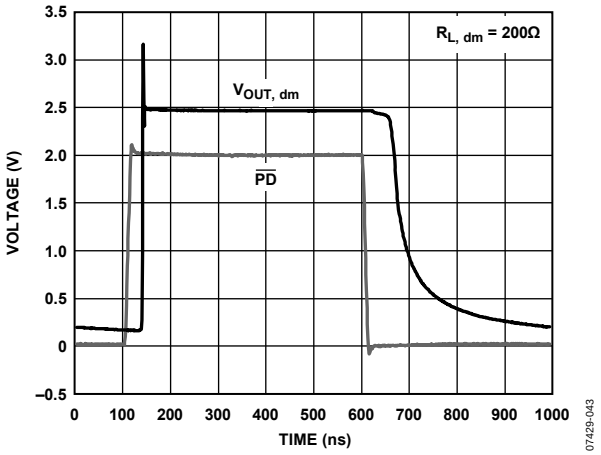


Figure 37. $\overline{PD}$ Response Time

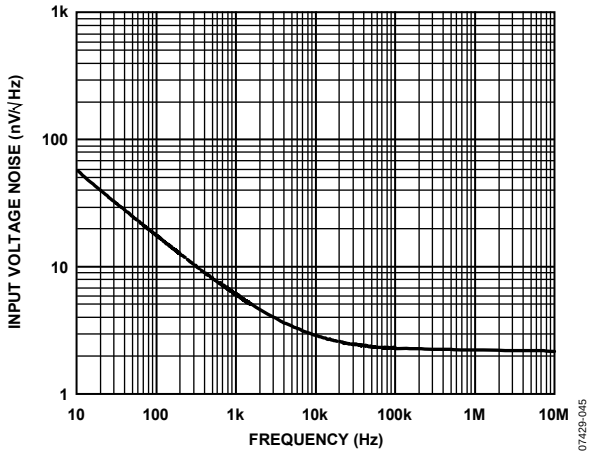


Figure 38. Voltage Noise Spectral Density, RTI

# TEST CIRCUITS

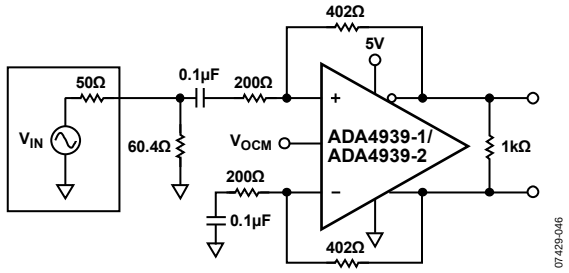


*Figure 39. Equivalent Basic Test Circuit, G = 2*

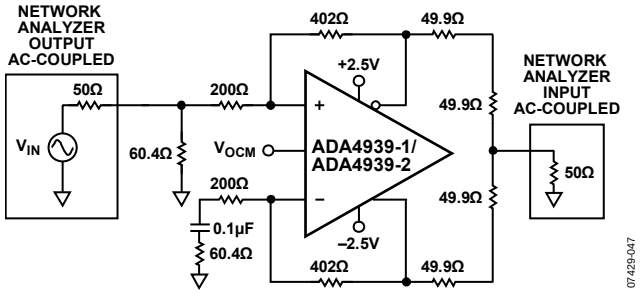


*Figure 40. Test Circuit for Output Balance, CMRR*

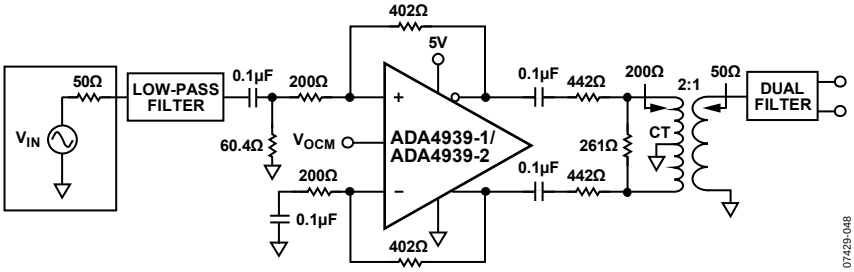


*Figure 41. Test Circuit for Distortion Measurements*

# OPERATIONAL DESCRIPTION

## DEFINITION OF TERMS

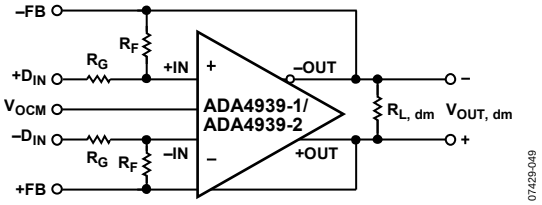


*Figure 42. Circuit Definitions*

### *Differential Voltage*

Differential voltage refers to the difference between two node voltages. For example, the output differential voltage (or equivalently, output differential-mode voltage) is defined as

$$V_{OUT,\,dm} = (V_{+OUT} - V_{-OUT})$$

where $V_{+OUT}$ and $V_{-OUT}$ refer to the voltages at the +OUT and −OUT terminals with respect to a common reference.

### *Common-Mode Voltage*

Common-mode voltage refers to the average of two node voltages. The output common-mode voltage is defined as

$$V_{OUT,\,cm} = (V_{+OUT} + V_{-OUT})/2$$

### *Balance*

Output balance is a measure of how close the differential signals are to being equal in amplitude and opposite in phase. Output balance is most easily determined by placing a well-matched resistor divider between the differential voltage nodes and comparing the magnitude of the signal at the divider midpoint with the magnitude of the differential signal (see Figure 39). By this definition, output balance is the magnitude of the output common-mode voltage divided by the magnitude of the output differential mode voltage.

$$Output\ Balance\ Error = \left| \frac{V_{OUT,\,cm}}{V_{OUT,\,dm}} \right|$$

# THEORY OF OPERATION

The ADA4939-1/ADA4939-2 differ from conventional op amps in that they have two outputs whose voltages move in opposite directions and an additional input, $V_{OCM}$. Like op amps, they rely on high open-loop gain and negative feedback to force these outputs to the desired voltages. The ADA4939-1/ADA4939-2 behave much like standard voltage feedback op amps and facilitate single-ended-to-differential conversions, common-mode level shifting, and amplifications of differential signals. Like op amps, the ADA4939-1/ADA4939-2 have high input impedance and low output impedance. Because they use voltage feedback, the ADA4939-1/ADA4939-2 manifest a nominally constant gain-bandwidth product.

Two feedback loops are employed to control the differential and common-mode output voltages. The differential feedback, set with external resistors, controls only the differential output voltage. The common-mode feedback controls only the common-mode output voltage. This architecture makes it easy to set the output common-mode level to any arbitrary value within the specified limits. The output common-mode voltage is forced by the internal common-mode feedback loop to be equal to the voltage applied to the $V_{OCM}$ input.

The internal common-mode feedback loop produces outputs that are highly balanced over a wide frequency range without requiring tightly matched external components. This results in differential outputs that are very close to the ideal of being identical in amplitude and are exactly 180° apart in phase.

## ANALYZING AN APPLICATION CIRCUIT

The ADA4939-1/ADA4939-2 use high open-loop gain and negative feedback to force their differential and common-mode output voltages in such a way as to minimize the differential and common-mode error voltages. The differential error voltage is defined as the voltage between the differential inputs labeled +IN and −IN (see Figure 42). For most purposes, this voltage is zero. Similarly, the difference between the actual output common-mode voltage and the voltage applied to $V_{OCM}$ is also zero. Starting from these two assumptions, any application circuit can be analyzed.

## SETTING THE CLOSED-LOOP GAIN

The differential-mode gain of the circuit in Figure 42 can be determined by

$$\left|\frac{V_{OUT,dm}}{V_{IN,dm}}\right| = \frac{R_F}{R_G}$$

This presumes that the input resistors ($R_G$) and feedback resistors ($R_F$) on each side are equal.

## STABLE FOR GAINS ≥2

The ADA4939-1/ADA4939-2 frequency response exhibits excessive peaking for differential gains <2; therefore, operate the devioce with differential gains ≥2.

## ESTIMATING THE OUTPUT NOISE VOLTAGE

To estimate the differential output noise of the ADA4939-1/ADA4939-2 use the noise model shown in Figure 43. The input-referred noise voltage density, $v_{nIN}$, is modeled as a differential input, and the noise currents, $i_{nIN-}$ and $i_{nIN+}$, appear between each input and ground. The output voltage due to $v_{nIN}$ is obtained by multiplying $v_{nIN}$ by the noise gain, $G_N$ (defined in the $G_N$ equation that follows). The noise currents are uncorrelated with the same mean-square value, and each produces an output voltage that is equal to the noise current multiplied by the associated feedback resistance. The noise voltage density at the $V_{OCM}/V_{OCMx}$ pin is $v_{nCM}$. When the feedback networks have the same feedback factor, as in most cases, the output noise due to $v_{nCM}$ is common-mode. Each of the four resistors contributes $(4kTR_{xx})^{1/2}$. The noise from the feedback resistors appears directly at the output, and the noise from the gain resistors appears at the output multiplied by $R_{Fx}/R_{Gx}$. Table 11 summarizes the input noise sources, the multiplication factors, and the output-referred noise density terms.

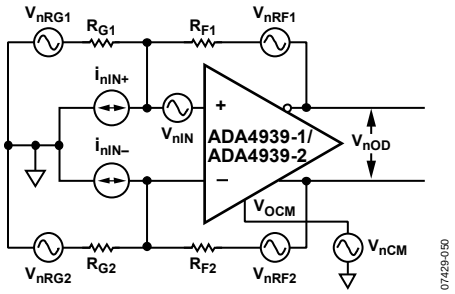


*Figure 43. Noise Model*

**Table 11. Output Noise Voltage Density Calculations for Matched Feedback Networks**

| Input Noise Contribution | Input Noise Term | Input Noise Voltage Density | Output Multiplication Factor | Differential Output Noise Voltage Density Term |
|---|---|---|---|---|
| Differential Input | $v_{nIN}$ | $v_{nIN}$ | $G_N$ | $v_{nO1} = G_N(v_{nIN})$ |
| Inverting Input | $i_{nIN}$ | $i_{nIN} \times (R_{F2})$ | 1 | $v_{nO2} = (i_{nIN})(R_{F2})$ |
| Noninverting Input | $i_{nIN}$ | $i_{nIN} \times (R_{F1})$ | 1 | $v_{nO3} = (i_{nIN})(R_{F1})$ |
| $V_{OCM}$ Input | $v_{nCM}$ | $v_{nCM}$ | 0 | $v_{nO4} = 0$ |
| Gain Resistor $R_{G1}$ | $v_{nRG1}$ | $(4kTR_{G1})^{1/2}$ | $R_{F1}/R_{G1}$ | $v_{nO5} = (R_{F1}/R_{G1})(4kTR_{G1})^{1/2}$ |
| Gain Resistor $R_{G2}$ | $v_{nRG2}$ | $(4kTR_{G2})^{1/2}$ | $R_{F2}/R_{G2}$ | $v_{nO6} = (R_{F2}/R_{G2})(4kTR_{G2})^{1/2}$ |
| Feedback Resistor $R_{F1}$ | $v_{nRF1}$ | $(4kTR_{F1})^{1/2}$ | 1 | $v_{nO7} = (4kTR_{F1})^{1/2}$ |
| Feedback Resistor $R_{F2}$ | $v_{nRF2}$ | $(4kTR_{F2})^{1/2}$ | 1 | $v_{nO8} = (4kTR_{F2})^{1/2}$ |

**Table 12. Differential Input, DC-Coupled**

| Nominal Gain (dB) | $R_F$ (Ω) | $R_G$ (Ω) | $R_{IN, dm}$ (Ω) | Differential Output Noise Density (nV/√Hz) |
|---|---|---|---|---|
| 6 | 402 | 200 | 400 | 9.7 |
| 10 | 402 | 127 | 254 | 12.4 |
| 14 | 402 | 80.6 | 161 | 16.6 |

**Table 13. Single-Ended Ground-Referenced Input, DC-Coupled, $R_S$ = 50 Ω**

| Nominal Gain (dB) | $R_F$ (Ω) | $R_{G1}$ (Ω) | $R_T$ (Ω) | $R_{IN, cm}$ (Ω) | $R_{G2}$ (Ω)[1] | Differential Output Noise Density (nV/√Hz) |
|---|---|---|---|---|---|---|
| 6 | 402 | 200 | 60.4 | 301 | 228 | 9.1 |
| 10 | 402 | 127 | 66.5 | 205 | 155 | 11.1 |
| 14 | 402 | 80.6 | 76.8 | 138 | 111 | 13.5 |

[1] $R_{G2} = R_{G1} + (R_S||R_T)$.

Similar to the case of a conventional op amp, the output noise voltage densities can be estimated by multiplying the input-referred terms at +IN and −IN by the appropriate output factor,

where:

$G_N = \frac{2}{(\beta_1 + \beta_2)}$ is the circuit noise gain.

$\beta_1 = \frac{R_{G1}}{R_{F1} + R_{G1}}$ and $\beta_2 = \frac{R_{G2}}{R_{F2} + R_{G2}}$ are the feedback factors.

When the feedback factors are matched, $R_{F1}/R_{G1} = R_{F2}/R_{G2}$, β1 = β2 = β, and the noise gain becomes

$$G_N = \frac{1}{\beta} = 1 + \frac{R_F}{R_G}$$

Note that the output noise from $V_{OCM}$ goes to zero in this case. The total differential output noise density, $v_{nOD}$, is the root-sum-square of the individual output noise terms.

$$v_{nOD} = \sqrt{\sum_{i=1}^{8} v_{nOi}^2}$$

Table 12 and Table 13 list several common gain settings, associated resistor values, input impedance, and output noise density for both balanced and unbalanced input configurations.

## IMPACT OF MISMATCHES IN THE FEEDBACK NETWORKS

As previously mentioned, even if the external feedback networks ($R_F/R_G$) are mismatched, the internal common-mode feedback loop still forces the outputs to remain balanced. The amplitudes of the signals at each output remain equal and 180° out of phase. The input-to-output differential mode gain varies proportionately to the feedback mismatch, but the output balance is unaffected.

The gain from the $V_{OCM}/V_{OCMx}$ pin to $V_{O, dm}$ is equal to

$$2(\beta1 - \beta2)/(\beta1 + \beta2)$$

When β1 = β2, this term goes to zero and there is no differential output voltage due to the voltage on the $V_{OCM}$ input (including noise). The extreme case occurs when one loop is open and the other has 100% feedback; in this case, the gain from $V_{OCM}$ input to $V_{O, dm}$ is either +2 or −2, depending on which loop is closed. The feedback loops are nominally matched to within 1% in most applications, and the output noise and offsets due to the $V_{OCM}$ input are negligible. If the loops are intentionally mismatched by a large amount, it is necessary to include the gain term from $V_{OCM}$ to $V_{O, dm}$ and account for the extra noise. For example, if β1 = 0.5 and β2 = 0.25, the gain from $V_{OCM}$ to $V_{O, dm}$ is 0.67. If the $V_{OCM}/V_{OCMx}$ pin is set to 2.5 V, a differential offset voltage is present at the output of (2.5 V)(0.67) = 1.67 V. The differential output noise contribution is (7.5 nV/√Hz)(0.67) = 5 nV/√Hz. Both of these results are undesirable in most applications; therefore, it is best to use nominally matched feedback factors.

Mismatched feedback networks also result in a degradation of the ability of the circuit to reject input common-mode signals, much the same as for a four-resistor difference amplifier made from a conventional op amp.

As a practical summarization of the above issues, resistors of 1% tolerance produce a worst-case input CMRR of approximately 40 dB, a worst-case differential-mode output offset of 25 mV due to a 2.5 V $V_{OCM}$ input, negligible $V_{OCM}$ noise contribution, and no significant degradation in output balance error.

## CALCULATING THE INPUT IMPEDANCE FOR AN APPLICATION CIRCUIT

The effective input impedance of a circuit depends on whether the amplifier is being driven by a single-ended or differential signal source. For balanced differential input signals, as shown in Figure 44, the input impedance ($R_{IN, dm}$) between the inputs ($+D_{IN}$ and $-D_{IN}$) is simply $R_{IN, dm} = 2 \times R_G$.

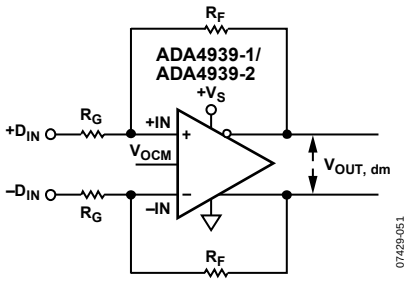


*Figure 44. ADA4939-1/ADA4939-2 Configured for Balanced (Differential) Inputs*

For an unbalanced, single-ended input signal (see Figure 45), the input impedance is

$$R_{IN, SE} = \left( \frac{R_G}{1 - \frac{R_F}{2 \times (R_G + R_F)}} \right)$$

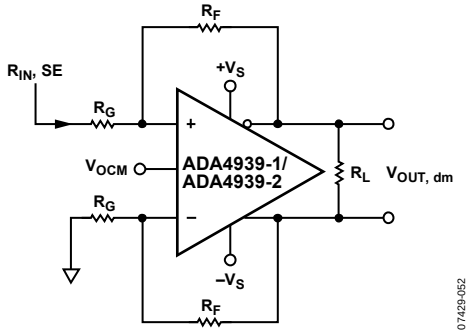


*Figure 45. ADA4939-1/ADA4939-2 with Unbalanced (Single-Ended) Input*

The input impedance of the circuit is effectively higher than it would be for a conventional op amp connected as an inverter because a fraction of the differential output voltage appears at the inputs as a common-mode signal, partially bootstrapping the voltage across the input resistor $R_G$. The common-mode voltage at the amplifier input terminals can be easily determined by noting that the voltage at the inverting input is equal to the noninverting output voltage divided down by the voltage divider formed by $R_F$ and $R_G$ in the lower loop. This voltage is present at both input terminals due to negative voltage feedback and is in phase with the input signal, thus reducing the effective voltage across $R_G$ in the upper loop and partially bootstrapping $R_G$.

### *Terminating a Single-Ended Input*

This section deals with how to properly terminate a single-ended input to the ADA4939-1/ADA4939-2 with a gain of 2, $R_F$ = 400 Ω, and $R_G$ = 200 Ω. An example using an input source with a terminated output voltage of 1 V p-p and source resistance of 50 Ω illustrates the four simple steps that must be followed. Note that, because the terminated output voltage of the source is 1 V p-p, the open circuit output voltage of the source is 2 V p-p. The source shown in Figure 46 indicates this open-circuit voltage.

1. The input impedance must be calculated using the formula

$$R_{IN} = \left( \frac{R_G}{1 - \frac{R_F}{2 \times (R_G + R_F)}} \right) = \left( \frac{200}{1 - \frac{400}{2 \times (200 + 400)}} \right) = 300\Omega$$

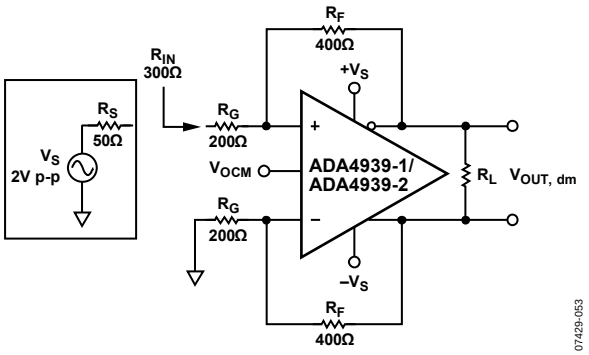


*Figure 46. Calculating Single-Ended Input Impedance $R_{IN}$*

2. To match the 50 Ω source resistance, the termination resistor, $R_T$, is calculated using $R_T||300\ \Omega = 50\ \Omega$. The closest standard 1% value for $R_T$ is 60.4 Ω.

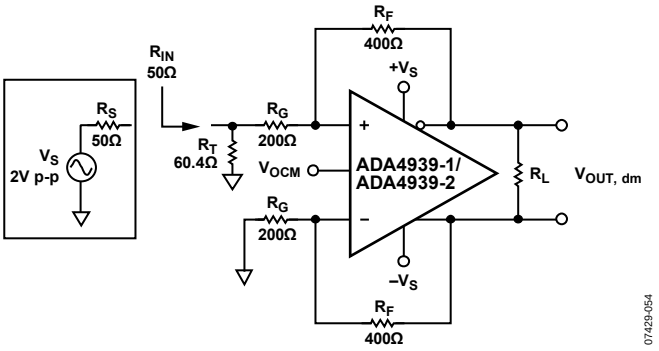


*Figure 47. Adding Termination Resistor $R_T$*

3. Figure 47 shows that the effective $R_G$ in the upper feedback loop is now greater than the $R_G$ in the lower loop due to the addition of the termination resistors. To compensate for the imbalance of the gain resistors, a correction resistor ($R_{TS}$) is added in series with $R_G$ in the lower loop. $R_{TS}$ is equal to the Thevenin equivalent of the source resistance $R_S$ and the termination resistance $R_T$ and is equal to $R_S||R_T$.

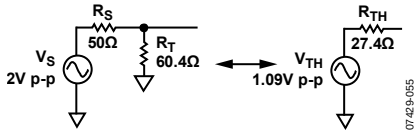


*Figure 48. Calculating the Thevenin Equivalent*

$R_{TS} = R_{TH} = R_S||R_T = 27.4\ \Omega$. Note that $V_{TH}$ is greater than 1 V p-p, which was obtained with $R_T = 50\ \Omega$. The modified circuit with the Thevenin equivalent of the terminated source and $R_{TS}$ in the lower feedback loop is shown in Figure 49.

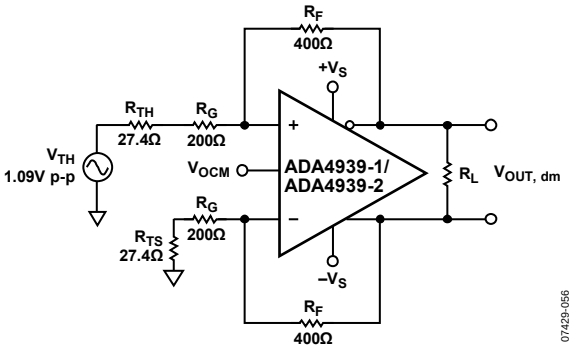


*Figure 49. Thevenin Equivalent and Matched Gain Resistors*

Figure 49 presents a tractable circuit with matched feedback loops that can be easily evaluated.

It is useful to point out two effects that occur with a terminated input. The first is that the value of $R_G$ is increased in both loops, lowering the overall closed-loop gain. The second is that $V_{TH}$ is a little larger than 1 V p-p, as it would be if $R_T = 50\ \Omega$. These two effects have opposite impacts on the output voltage, and for large resistor values in the feedback loops (~1 kΩ), the effects essentially cancel each other out. For small $R_F$ and $R_G$, however, the diminished closed-loop gain is not canceled completely by the increased $V_{TH}$. This can be seen by evaluating Figure 49.

The desired differential output in this example is 2 V p-p because the terminated input signal was 1 V p-p and the closed-loop gain = 2. The actual differential output voltage, however, is equal to (1.09 V p-p)(400/227.4) = 1.92 V p-p. To obtain the desired output voltage of 2 V p-p, a final gain adjustment can be made by increasing $R_F$ without modifying any of the input circuitry (see Step 4).

4. The feedback resistor value is modified as a final gain adjustment to obtain the desired output voltage.

To make the output voltage $V_{OUT} = 2$ V p-p, calculate $R_F$ by

$$R_F = \frac{(Desired\ V_{OUT,dm})(R_G + R_{TS})}{V_{TH}} = \frac{(2V_{P-P})(227.4\Omega)}{1.09V_{P-P}} = 417\Omega$$

The closest standard 1 % values to 417 Ω are 412 Ω and 422 Ω. Choosing 422 Ω gives a differential output voltage of 2.02 V p-p.

The final circuit is shown in Figure 50.

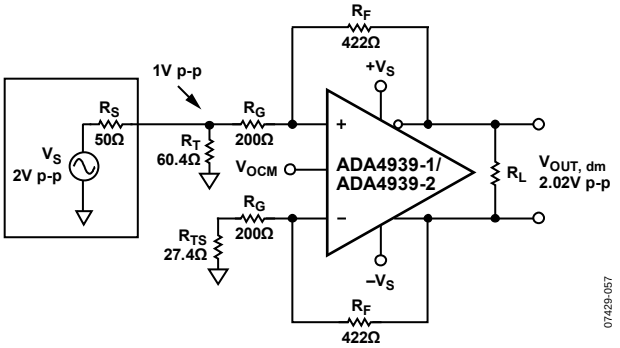


*Figure 50. Terminated Single-Ended-to-Differential System with G = 2*

## INPUT COMMON-MODE VOLTAGE RANGE

The ADA4939-1/ADA4939-2 input common-mode range is centered between the two supply rails, in contrast to other ADC drivers with level-shifted input ranges, such as the ADA4937-1/ADA4937-2. The centered input common-mode range is best suited to ac-coupled, differential-to-differential and dual supply applications.

For 5 V single-supply operation, the input common-mode range at the summing nodes of the amplifier is specified as 1.1 V to 3.9 V and is specified as 0.9 V to 2.4 V with a 3.3 V supply. To avoid nonlinearities, the voltage swing at the +IN and −IN terminals must be confined to these ranges.

## INPUT AND OUTPUT CAPACITIVE AC COUPLING

Input ac coupling capacitors can be inserted between the source and $R_G$. This ac coupling blocks the flow of the dc common-mode feedback current and causes the ADA4939-1/ADA4939-2 dc input common-mode voltage to equal the dc output common-mode voltage. These ac coupling capacitors must be placed in both loops to keep the feedback factors matched.

Output ac coupling capacitors can be placed in series between each output and its respective load. See Figure 54 for an example that uses input and output capacitive ac coupling.

## MINIMUM $R_G$ VALUE OF 50 Ω

Due to the wide bandwidth of the ADA4939-1/ADA4939-2, the value of $R_G$ must be greater than or equal to 50 Ω to provide sufficient damping in the amplifier front end. In the terminated case, $R_G$ includes the Thevenin resistance of the source and load terminations.

## SETTING THE OUTPUT COMMON-MODE VOLTAGE

The $V_{OCM}/V_{OCMx}$ pin of the ADA4939-1/ADA4939-2 is internally biased with a voltage divider comprising two 20 kΩ resistors at a voltage approximately equal to the midsupply point, $[(+V_S) + (-V_S)]/2$. Because of this internal divider, the $V_{OCM}/V_{OCMx}$ pin sources and sinks current, depending on the externally applied voltage and its associated source resistance. Relying on the internal bias results in an output common-mode voltage that is within about 100 mV of the expected value.

In cases where more accurate control of the output common-mode level is required, it is recommended that an external source or resistor divider be used with source resistance less than 100 Ω. The output common-mode offset listed in the Specifications section assumes that the $V_{OCM}$ input is driven by a low impedance voltage source.

It is also possible to connect the $V_{OCM}$ input to a common-mode level (CML) output of an ADC. However, care must be taken to ensure that the output has sufficient drive capability. The input impedance of the $V_{OCM}/V_{OCMx}$ pin is approximately 10 kΩ. If multiple ADA4939-1/ADA4939-2 devices share one reference output, it is recommended that a buffer be used.

# LAYOUT, GROUNDING, AND BYPASSING

As a high speed device, the ADA4939-1 is sensitive to the PCB environment in which it operates. Realizing its superior performance requires attention to the details of high speed PCB design. This section shows a detailed example of how the ADA4939-1 was addressed.

The first requirement is a solid ground plane that covers as much of the board area around the ADA4939-1 as possible. However, the area near the feedback resistors ($R_F$), gain resistors ($R_G$), and the input summing nodes (Pin 2 and Pin 3) must be cleared of all ground and power planes (see Figure 51). Clearing the ground and power planes minimizes any stray capacitance at these nodes and prevents peaking of the response of the amplifier at high frequencies.

The thermal resistance, $\theta_{JA}$, is specified for the device, including the exposed pad, soldered to a high thermal conductivity four-layer circuit board, as described in EIA/JESD 51-7.

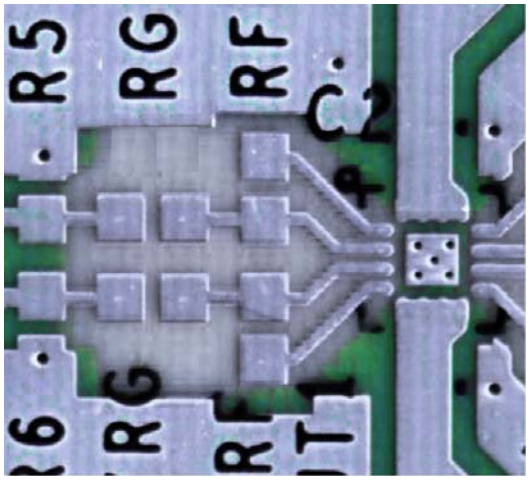


*Figure 51. Ground and Power Plane Voiding in Vicinity of $R_F$ and $R_G$*

Bypass the power supply pins as close to the device as possible and directly to a nearby ground plane. Use high frequency ceramic chip capacitors. It is recommended to use two parallel bypass capacitors (1000 pF and 0.1 µF) for each supply. Place the 1000 pF capacitor closer to the device. Further away, provide low frequency bypassing, using 10 µF tantalum capacitors from each supply to ground.

Ensure that signal routing is short and direct to avoid parasitic effects. Wherever complementary signals exist, provide a symmetrical layout to maximize balanced performance. When routing differential signals over a long distance, ensure that the PCB traces are close together, and twist any differential wiring such that the loop area is minimized which reduces radiated energy and makes the circuit less susceptible to interference.

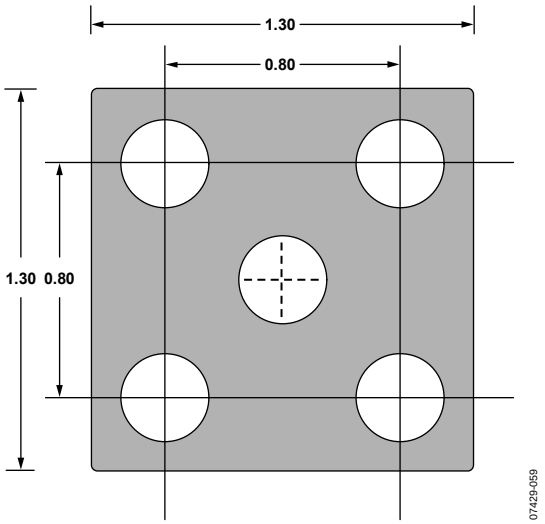


*Figure 52. Recommended PCB Thermal Attach Pad Dimensions (Millimeters)*

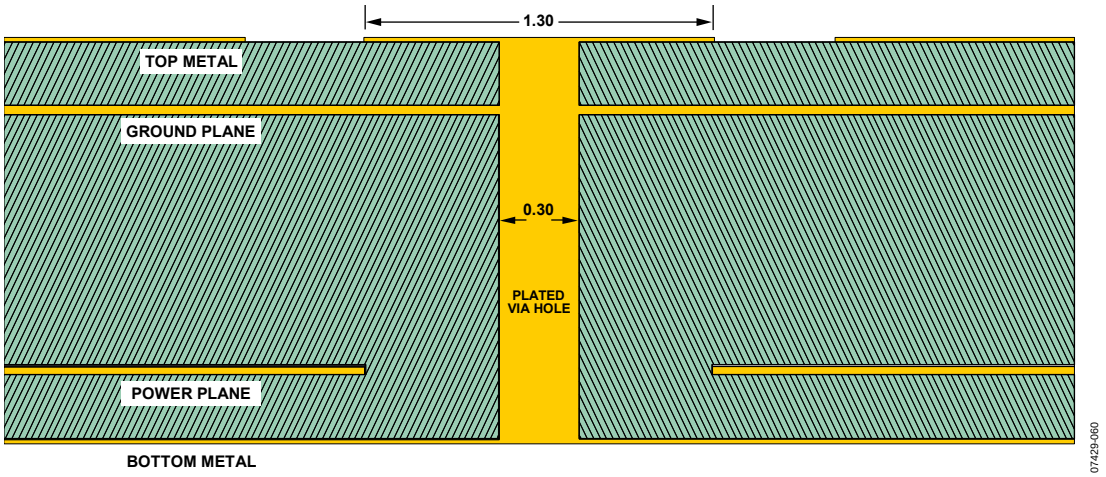


*Figure 53. Cross-Section of 4-Layer PCB Showing Thermal Via Connection to Buried Ground Plane (Dimensions in Millimeters)*

# HIGH PERFORMANCE ADC DRIVING

The ADA4939-1/ADA4939-2 are ideally suited for broadband ac-coupled and differential-to-differential applications on a single supply.

The circuit in Figure 54 shows a front-end connection for an ADA4939-1 driving an AD9445, 14-bit, 105 MSPS ADC, with ac coupling on the ADA4939-1 input and output. (The AD9445 achieves its optimum performance when driven differentially.) The ADA4939-1 eliminates the need for a transformer to drive the ADC and perform a single-ended-to-differential conversion and buffering of the driving signal.

The ADA4939-1 is configured with a single 5 V supply and gain of 2 for a single-ended input to differential output. The 60.4 Ω termination resistor, in parallel with the single-ended input impedance of approximately 300 Ω, provides a 50 Ω termination for the source. The additional 27.4 Ω (227.4 Ω total) at the inverting input balances the parallel impedance of the 50 Ω source and the termination resistor driving the noninverting input.

In this example, the signal generator has a 1 V p-p symmetric, ground-referenced bipolar output when terminated in 50 Ω.

The $V_{OCM}$ pin of the ADA4939-1 is bypassed for noise reduction and left floating such that the internal divider sets the output common-mode voltage nominally at midsupply. Because the inputs are ac-coupled, no dc common-mode current flows in the feedback loops, and a nominal dc level of midsupply is present at the amplifier input terminals. Besides placing the amplifier inputs at their optimum levels, the ac coupling technique lightens the load on the amplifier and dissipates less power than applications with dc-coupled inputs. With an output common-mode voltage of nominally 2.5 V, each ADA4939-1 output swings between 2.0 V and 3.0 V, providing a gain of 2 and a 2 V p-p differential signal to the ADC input.

The output of the amplifier is ac-coupled to the ADC through a second-order, low-pass filter with a cutoff frequency of 100 MHz. This reduces the noise bandwidth of the amplifier and isolates the driver outputs from the ADC inputs.

The AD9445 is configured for a 2 V p-p full-scale input by connecting the SENSE pin to AGND, as shown in Figure 54.

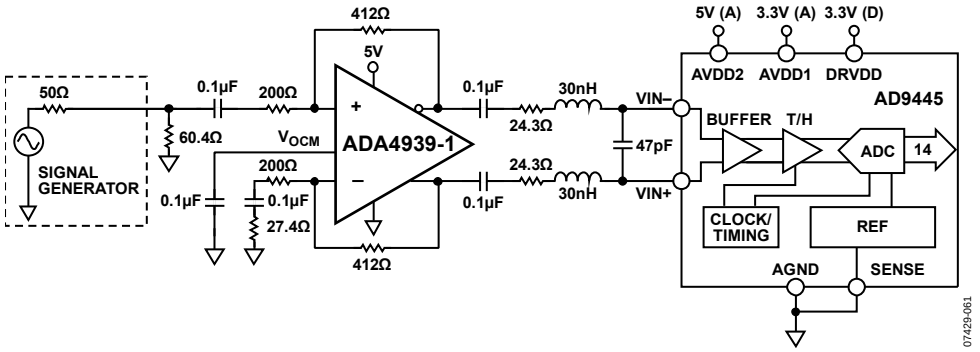


*Figure 54. ADA4939-1 Driving an AD9445 ADC with AC-Coupled Input and Output*

# OUTLINE DIMENSIONS

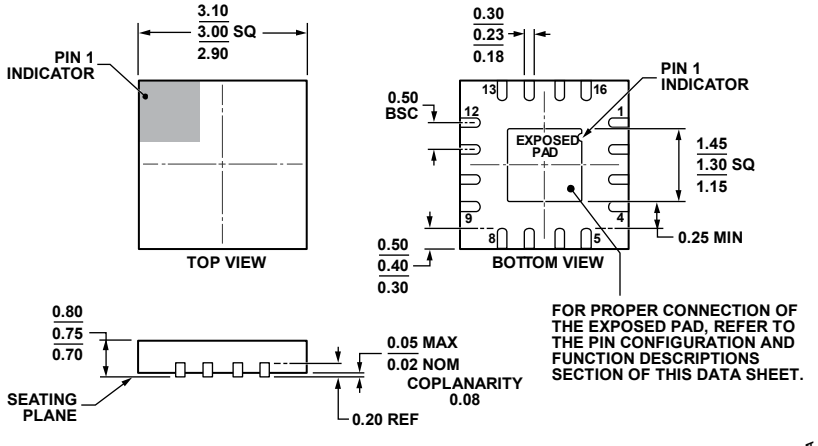


*Figure 55. 16-Lead Lead Frame Chip Scale Package [LFCSP]*
*3 mm × 3 mm Body and 0.75 mm Package Height*
*(CP-16-21)*
*Dimensions shown in millimeters*

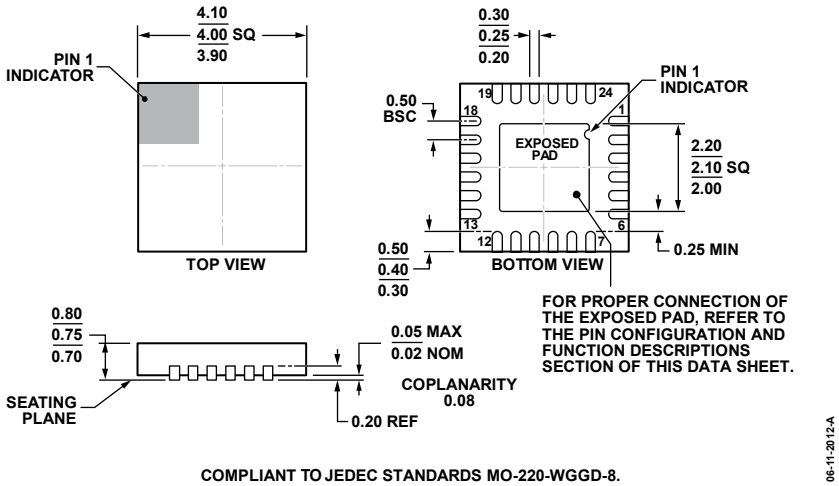


*Figure 56. 24-Lead Lead Frame Chip Scale Package [LFCSP]*
*4 mm × 4 mm Body and 0.75 mm Package Height*
*(CP-24-10)*
*Dimensions shown in millimeters*

## ORDERING GUIDE

| Model[1] | Temperature Range | Package Description | Package Option | Ordering Quantity | Branding |
|---|---|---|---|---|---|
| ADA4939-1YCPZ-R2 | −40°C to +105°C | 16-Lead LFCSP | CP-16-21 | 250 | H1E |
| ADA4939-1YCPZ-RL | −40°C to +105°C | 16-Lead LFCSP | CP-16-21 | 5,000 | H1E |
| ADA4939-1YCPZ-R7 | −40°C to +105°C | 16-Lead LFCSP | CP-16-21 | 1,500 | H1E |
| ADA4939-2YCPZ-R2 | −40°C to +105°C | 24-Lead LFCSP | CP-24-10 | 250 | |
| ADA4939-2YCPZ-RL | −40°C to +105°C | 24-Lead LFCSP | CP-24-10 | 5,000 | |
| ADA4939-2YCPZ-R7 | −40°C to +105°C | 24-Lead LFCSP | CP-24-10 | 1,500 | |

[1] Z = RoHS Compliant Part.