TABLE OF CONTENTS

REVISION HISTORY

7/09—Rev. A to Rev. B

Added BGA Package ... Universal
Changes to Features and General Description Sections ... 1
Changes to Product Highlights Section ... 3
Changes to Full-Channel (TGC) Characteristics Parameter, Table 1 ... 4
Changes to Gain Control Interface Parameter and to CW Doppler Mode Parameter, Table 1 ... 6
Change to Wake-Up Time (Standby), GAIN+ = 0.8 V Parameter ... 9
Changes to Figure 2 and Figure 3 ... 10
Changes to Table 4 ... 11
Addded Figure 5; Renumbered Sequentially ... 12
Changes to Table 6 ... 13
Changes to Figure 34 and Figure 35 ... 20
Changes to Ultrasound Section ... 21
Changes to Low Noise Amplifier (LNA) Section ... 22
Changes to Active Impedance Matching Section and Figure 40 ... 23
Changes to LNA Noise Section ... 24
Changes to Input Overload Protection Section and Figure 44 ... 25
Changes to Figure 48 ... 28
Changes to Figure 49 and Figure 50 ... 29
Changes to Clock Input Considerations Section and to Figure 56 to Figure 59 ... 31
Changes to Digital Outputs and Timing Section ... 33
Changes to CSB Pin Section ... 36
Changes to Reading the Memory Map Table Section ... 40
Updated Outline Dimensions ... 44
Changes to Ordering Guide ... 45

4/09—Revision A: Initial Version

The AD9273 requires a LVPECL-/CMOS-/LVDS-compatible sample rate clock for full performance operation. No external reference or driver components are required for many applications.

The ADC automatically multiplies the sample rate clock for the appropriate LVDS serial data rate. A data clock (DCO±) for capturing data on the output and a frame clock (FCO±) trigger for signaling a new output byte are provided.

Powering down individual channels is supported to increase battery life for portable applications. There is also a standby mode option that allows quick power-up for power cycling. In CW Doppler operation, the VGA, AAF, and ADC are powered down. The power of the time gain control (TGC) path scales with selectable speed grades.

The ADC contains several features designed to maximize flexibility and minimize system cost, such as a programmable clock, data alignment, and programmable digital test pattern generation. The digital test patterns include built-in fixed patterns, built-in pseudorandom patterns, and custom user-defined test patterns entered via the serial port interface.

Fabricated in an advanced CMOS process, the AD9273 is available in a 16 mm × 16 mm, RoHS compliant, 100-lead TQFP or a 144-ball BGA. It is specified over the industrial temperature range of −40°C to +85°C.

PRODUCT HIGHLIGHTS

1. Small Footprint. Eight channels are contained in a small, space-saving package. A full TGC path, ADC, and crosspoint switch contained within a 100-lead, 16 mm × 16 mm TQFP or a 144-ball BGA.
2. Low Power of 109 mW per Channel at 40 MSPS.
3. Integrated Crosspoint Switch. This switch allows numerous multichannel configuration options to enable the CW Doppler mode.
4. Ease of Use. A data clock output (DCO±) operates up to 300 MHz and supports double data rate (DDR) operation.
5. User Flexibility. Serial port interface (SPI) control offers a wide range of flexible features to meet specific system requirements.
6. Integrated Second-Order Antialiasing Filter. This filter is placed between the VGA and the ADC and is programmable from 8 MHz to 18 MHz.

SPECIFICATIONS

AC SPECIFICATIONS

AVDD1 = 1.8 V, AVDD2 = 3.0 V, DRVDD = 1.8 V, 1.0 V internal ADC reference, f_{IN} = 5 MHz, R_S = 50 Ω, LNA gain = 21.3 dB, LNA bias =mid-high (default), PGA gain = 24 dB, GAIN− = 0.8 V, AAF LPF cutoff = f_{SAMPLE}/3 (default), HPF = LPF cutoff/20.7 (default), full temperature, ANSI-644 LVDS mode, unless otherwise noted.

Table 1.

		AD9273-25			AD9273-40			AD9273-50			
Parameter[1]	**Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
LNA CHARACTERISTICS											
Gain	Single-ended input to differential output		15.6/17.9/21.3			15.6/17.9/21.3			15.6/17.9/21.3		dB
	Single-ended input to single-ended output		9.6/11.9/15.3			9.6/11.9/15.3			9.6/11.9/15.3		dB
Input Voltage Range	LNA gain = 15.6 dB/ 17.9 dB/ 21.3 dB, LNA output limited to 4.4 V p-p differential output		733/550/367			733/550/367			733/550/367		mV p-p SE[2]
Input Common Mode			0.9			0.9			0.9		V
Input Resistance	R_{FB} = 250 Ω		50			50			50		Ω
	R_{FB} = 500 Ω		100			100			100		Ω
	R_{FB} = ∞		15			15			15		kΩ
Input Capacitance	LI-x		22			22			22		pF
−3 dB Bandwidth			70			70			70		MHz
Input-Referred Noise Voltage	LNA gain = 15.6 dB/ 17.9 dB/ 21.3 dB, R_S = 0 Ω, R_{FB} = ∞		1.6/1.42/1.26			1.6/1.42/1.26			1.6/1.42/1.26		nV/√Hz
Input Noise Current	R_{FB} = ∞		1			1			1		pA/√Hz
1 dB Input Compression Point	LNA gain = 15.6 dB/ 17.9 dB/ 21.3 dB, GAIN+ = 0 V		1.0/0.8/0.5			1.0/0.8/0.5			1.0/0.8/0.5		mV p-p
Noise Figure	LNA gain = 15.6 dB/ 17.9 dB/ 21.3 dB										
Active Termination Matched	R_S = 50 Ω, R_{FB} = 200 Ω/ 250 Ω/350 Ω		5.8/5.1/4.3			5.8/5.1/4.3			5.8/5.1/4.3		dB
Unterminated	R_{FB} = ∞		6.3/5.3/4.4			6.3/5.3/4.4			6.3/5.3/4.4		dB
FULL-CHANNEL (TGC) CHARACTERISTICS											
AAF Low-Pass Filter Cutoff	In range, −3 dB, programmable		8 to 18			8 to 18			8 to 18		MHz
	Out of range,[3] −3 dB, programmable, >>AAF bandwidth tolerance		5 to 8, 18 to 35			5 to 8, 18 to 35			5 to 8, 18 to 35		MHz

Parameter[1]	Conditions	AD9273-25 Min	AD9273-25 Typ	AD9273-25 Max	AD9273-40 Min	AD9273-40 Typ	AD9273-40 Max	AD9273-50 Min	AD9273-50 Typ	AD9273-50 Max	Unit
AAF Bandwidth Tolerance	In range		±10			±10			±10		%
Group Delay Variation	f = 1 MHz to 18 MHz, GAIN+ = 0 V to 1.6 V		±2			±2			±2		ns
Input-Referred Noise Voltage	LNA gain = 15.6 dB/ 17.9 dB/ 21.3 dB, R_{FB} = ∞		1.94/1.64/1.38			1.94/1.64/1.38			1.94/1.64/1.38		nV/√Hz
Noise Figure	LNA gain = 15.6 dB/ 17.9 dB/ 21.3 dB										
Active Termination Matched	R_S = 50 Ω, R_{FB} = 200 Ω/ 250 Ω/350 Ω		10.3/8.7/6.8			10.3/8.6/6.7			10.3/8.6/6.7		dB
Unterminated	R_{FB} = ∞		7.1/6.0/4.8			7.1/5.9/4.8			7.1/5.9/4.8		dB
Correlated Noise Ratio	No signal, correlated/ uncorrelated		−30			−30			−30		dB
Output Offset		−35		+35	−35		+35	−35		+35	LSB
Signal-to-Noise Ratio (SNR)	f_{IN} = 5 MHz at −10 dBFS, GAIN+ = 0 V		65.5			64			63.5		dBFS
	f_{IN} = 5 MHz at −1 dBFS, GAIN+ = 1.6 V		58.5			57			56.5		dBFS
Harmonic Distortion											
Second Harmonic	f_{IN} = 5 MHz at −10 dBFS, GAIN+ = 0 V		−55			−52			−52		dBc
	f_{IN} = 5 MHz at −1 dBFS, GAIN+ = 1.6 V		−67			−62			−58		dBc
Third Harmonic	f_{IN} = 5 MHz at −10 dBFS, GAIN+ = 0 V		−56			−50			−47		dBc
	f_{IN} = 5 MHz at −1 dBFS, GAIN+ = 1.6 V		−61			−56			−55		dBc
Two-Tone IMD3 (2 × F1 − F2) Distortion	f_{IN1} = 5.0 MHz at −1 dBFS, f_{IN2} = 5.01 MHz at −21 dBFS, GAIN+ = 1.6 V, LNA gain = 21.3 dB		−75			−75			−75		dBc
Channel-to-Channel Crosstalk	f_{IN1} = 5.0 MHz at −1 dBFS		−70			−70			−70		dB
	Overrange condition[4]		−65			−65			−65		dB
Channel-to-Channel Delay Variation	Full TGC path, f_{IN} = 5 MHz, GAIN+ = 0 V to 1.6 V		0.3			0.3			0.3		Degrees
PGA GAIN	Differential input to differential output		21/24/27/30			21/24/27/30			21/24/27/30		dB

Parameter[1]	Conditions	AD9273-25 Min	AD9273-25 Typ	AD9273-25 Max	AD9273-40 Min	AD9273-40 Typ	AD9273-40 Max	AD9273-50 Min	AD9273-50 Typ	AD9273-50 Max	Unit
GAIN ACCURACY	25°C										
Gain Law Conformance Error	0 V < GAIN+ < 0.16 V		1.5			1.5			1.5		dB
	0.16 V < GAIN+ < 1.44 V	−1.6		+1.6	−1.6		+1.6	−1.7		+1.7	dB
	1.44 V < GAIN+ < 1.6 V		−2.5			−2.5			−2.5		dB
Linear Gain Error	GAIN+ = 0.8 V, normalized for ideal AAF loss	−1.6		+1.6	−1.6		+1.6	−1.7		+1.7	dB
Channel-to-Channel Matching	0.16 V < GAIN+ < 1.44 V		0.1			0.1			0.1		dB
GAIN CONTROL INTERFACE											
Normal Operating Range		0		1.6	0		1.6	0		1.6	V
Gain Range	GAIN+ = 0 V to 1.6 V		42			42			42		dB
Scale Factor			28			28			28		dB/V
Response Time	42 dB change		750			750			750		ns
Gain+ Impedance	Single ended		10			10			10		MΩ
Gain− Impedance	Single ended		70			70			70		kΩ
CW DOPPLER MODE											
Transconductance	Differential, LNA gain = 15.6 dB/ 17.9 dB/ 21.3 dB		5.4/7.3/10.9			5.4/7.3/10.9			5.4/7.3/10.9		mA/V
Output Level Range	Differential, CW Doppler output pins	1.5		3.6	1.5		3.6	1.5		3.6	V
Input-Referred Noise Voltage	LNA gain = 15.6 dB/ 17.9 dB/ 21.3 dB, R_S = 0 Ω, R_{FB} = ∞, R_L = 675 Ω		2.6/2.1/1.6			2.6/2.1/1.6			2.6/2.1/1.6		nV/√Hz
Input-Referred Dynamic Range	LNA gain = 15.6 dB/ 17.9 dB/ 21.3 dB, R_S = 0 Ω, R_{FB} = ∞		160/159/158			160/159/158			160/159/158		dBFS/√Hz
Two-Tone IMD3 (2 × F1 − F2) Distortion	f_{IN1} = 5.0 MHz at −1 dBFS (FS at LNA input), f_{IN2} = 5.01 MHz at −21 dBFS (FS at LNA input), LNA gain = 21.3 dB		−70			−70			−70		dBc
Output DC Bias	Single ended, per channel		2.4			2.4			2.4		mA
Maximum Output Swing	Single ended, per channel		±2			±2			±2		mA p-p
POWER SUPPLY											
AVDD1		1.7	1.8	1.9	1.7	1.8	1.9	1.7	1.8	1.9	V
AVDD2		2.7	3.0	3.6	2.7	3.0	3.6	2.7	3.0	3.6	V
DRVDD		1.7	1.8	1.9	1.7	1.8	1.9	1.7	1.8	1.9	V
I_{AVDD1}	Full-channel mode		158			186			223		mA
	CW Doppler mode with four channels enabled		32			32			32		mA

Parameter[1]	Conditions	AD9273-25			AD9273-40			AD9273-50			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{AVDD2}	Full-channel mode		150			150			150		mA
	CW Doppler mode with four channels enabled		70			70			70		mA
I_{DRVDD}			47			49			50		mA
Total Power Dissipation	Includes output drivers, full-channel mode, no signal		819	940		873	996		943	1072	mW
	CW Doppler mode with four channels enabled		275			275			275		mW
Power-Down Dissipation				5			5			5	mW
Standby Power Dissipation				148			158			170	mW
Power Supply Rejection Ratio (PSRR)			1.6			1.6			1.6		mV/V
ADC RESOLUTION			12			12			12		Bits
ADC REFERENCE											
Output Voltage Error	VREF = 1 V			±20			±20			±20	mV
Load Regulation	At 1.0 mA, VREF = 1 V		2			2			2		mV
Input Resistance			6			6			6		kΩ

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for a complete set of definitions and how these tests were completed.
[2] SE = single ended.
[3] AAF settings < 5 MHz are out of range and are not supported.
[4] The overrange condition is specified as being 6 dB more than the full-scale input range.

DIGITAL SPECIFICATIONS

AVDD1 = 1.8 V, AVDD2 = 3.0 V, DRVDD = 1.8 V, 1.0 V internal ADC reference, f_{IN} = 5 MHz, full temperature, unless otherwise noted.

Table 2.

Parameter[1]	Temperature	Min	Typ	Max	Unit
CLOCK INPUTS (CLK+, CLK–)					
Logic Compliance			CMOS/LVDS/LVPECL		
Differential Input Voltage[2]	Full	250			mV p-p
Input Common-Mode Voltage	Full		1.2		V
Input Resistance (Differential)	25°C		20		kΩ
Input Capacitance	25°C		1.5		pF
LOGIC INPUTS (PDWN, STBY, SCLK)					
Logic 1 Voltage	Full	1.2		3.6	V
Logic 0 Voltage	Full			0.3	V
Input Resistance	25°C		30		kΩ
Input Capacitance	25°C		0.5		pF
LOGIC INPUT (CSB)					
Logic 1 Voltage	Full	1.2		3.6	V
Logic 0 Voltage	Full			0.3	V
Input Resistance	25°C		70		kΩ
Input Capacitance	25°C		0.5		pF
LOGIC INPUT (SDIO)					
Logic 1 Voltage	Full	1.2		DRVDD + 0.3	V
Logic 0 Voltage	Full	0		0.3	V
Input Resistance	25°C		30		kΩ
Input Capacitance	25°C		2		pF
LOGIC OUTPUT (SDIO)[3]					
Logic 1 Voltage (I_{OH} = 800 µA)	Full		1.79		V
Logic 0 Voltage (I_{OL} = 50 µA)	Full			0.05	V
DIGITAL OUTPUTS (DOUTx+, DOUTx–) IN ANSI-644 MODE[1]					
Logic Compliance			LVDS		
Differential Output Voltage (V_{OD})	Full	247		454	mV
Output Offset Voltage (V_{OS})	Full	1.125		1.375	V
Output Coding (Default)			Offset binary		
DIGITAL OUTPUTS (DOUTx+, DOUTx–) WITH LOW POWER, REDUCED-SIGNAL OPTION[1]					
Logic Compliance			LVDS		
Differential Output Voltage (V_{OD})	Full	150		250	mV
Output Offset Voltage (V_{OS})	Full	1.10		1.30	V
Output Coding (Default)			Offset binary		

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for a complete set of definitions and how these tests were completed.
[2] Specified for LVDS and LVPECL only.
[3] Specified for 13 SDIO pins sharing the same connection.

SWITCHING SPECIFICATIONS

AVDD1 = 1.8 V, AVDD2 = 3.0 V, DRVDD = 1.8 V, 1.0 V internal ADC reference, f_{IN} = 5 MHz, full temperature, unless otherwise noted.

Table 3.

Parameter[1]	Temp	Min	Typ	Max	Unit
CLOCK[2]					
Clock Rate	Full	10		50	MSPS
Clock Pulse Width High (t_{EH})	Full		10		ns
Clock Pulse Width Low (t_{EL})	Full		10		ns
OUTPUT PARAMETERS[2, 3]					
Propagation Delay (t_{PD})	Full	(t_{SAMPLE}/2) + 1.5	(t_{SAMPLE}/2) + 2.3	(t_{SAMPLE}/2) + 3.1	ns
Rise Time (t_R) (20% to 80%)	Full		300		ps
Fall Time (t_F) (20% to 80%)	Full		300		ps
FCO± Propagation Delay (t_{FCO})	Full	(t_{SAMPLE}/2) + 1.5	(t_{SAMPLE}/2) + 2.3	(t_{SAMPLE}/2) + 3.1	ns
DCO± Propagation Delay (t_{CPD})[4]	Full		t_{FCO} + (t_{SAMPLE}/24)		ns
DCO± to Data Delay (t_{DATA})[4]	Full	(t_{SAMPLE}/24) − 300	(t_{SAMPLE}/24)	(t_{SAMPLE}/24) + 300	ps
DCO± to FCO± Delay (t_{FRAME})[4]	Full	(t_{SAMPLE}/24) − 300	(t_{SAMPLE}/24)	(t_{SAMPLE}/24) + 300	ps
Data-to-Data Skew ($t_{DATA-MAX}$ − $t_{DATA-MIN}$)	Full		±100	±350	ps
Wake-Up Time (Standby), GAIN+ = 0.8 V	25°C		<2		µs
Wake-Up Time (Power-Down)	25°C		1		ms
Pipeline Latency	Full		8		Clock cycles
APERTURE					
Aperture Uncertainty (Jitter)	25°C		<1		ps rms

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for a complete set of definitions and how these tests were completed.
[2] Can be adjusted via the SPI.
[3] Measurements were made using a part soldered to FR-4 material.
[4] t_{SAMPLE}/24 is based on the number of bits divided by 2 because the delays are based on half duty cycles.

ADC TIMING DIAGRAMS

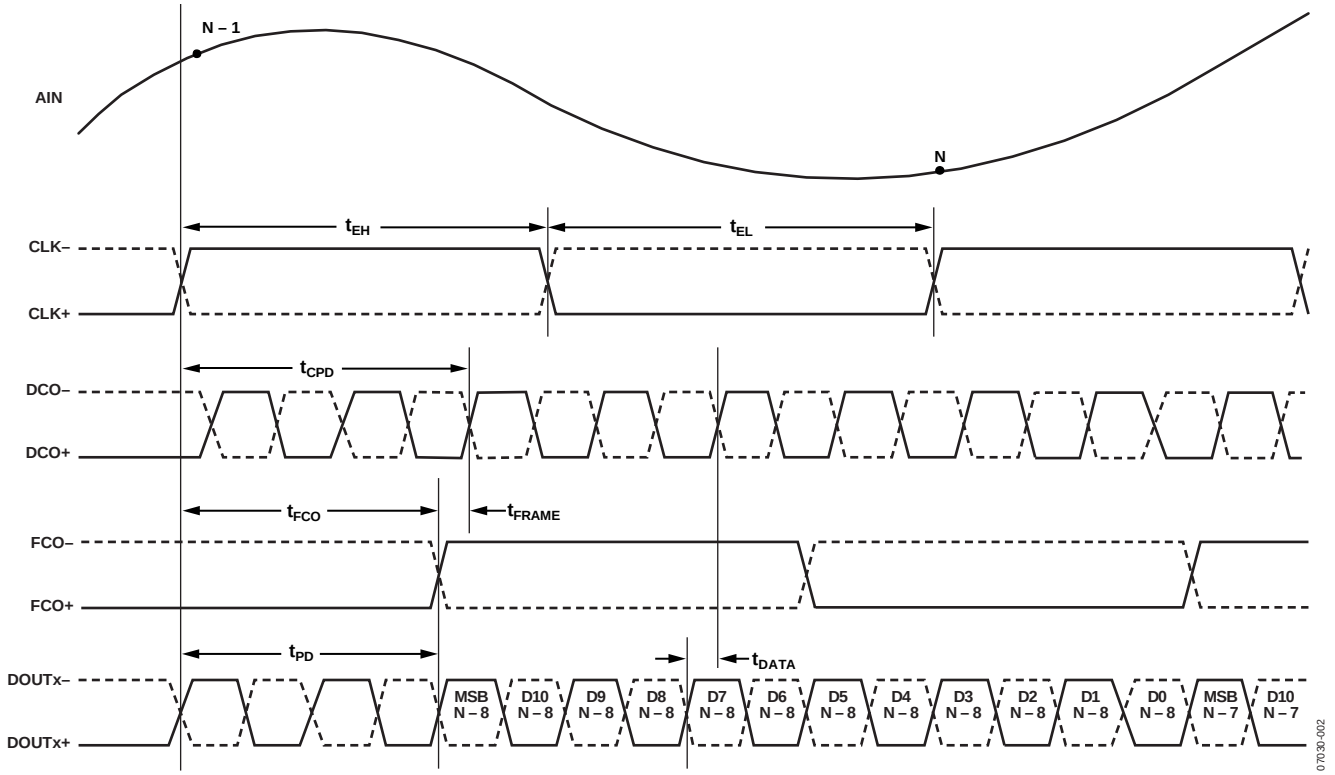


Figure 2. 12-Bit Data Serial Stream (Default)

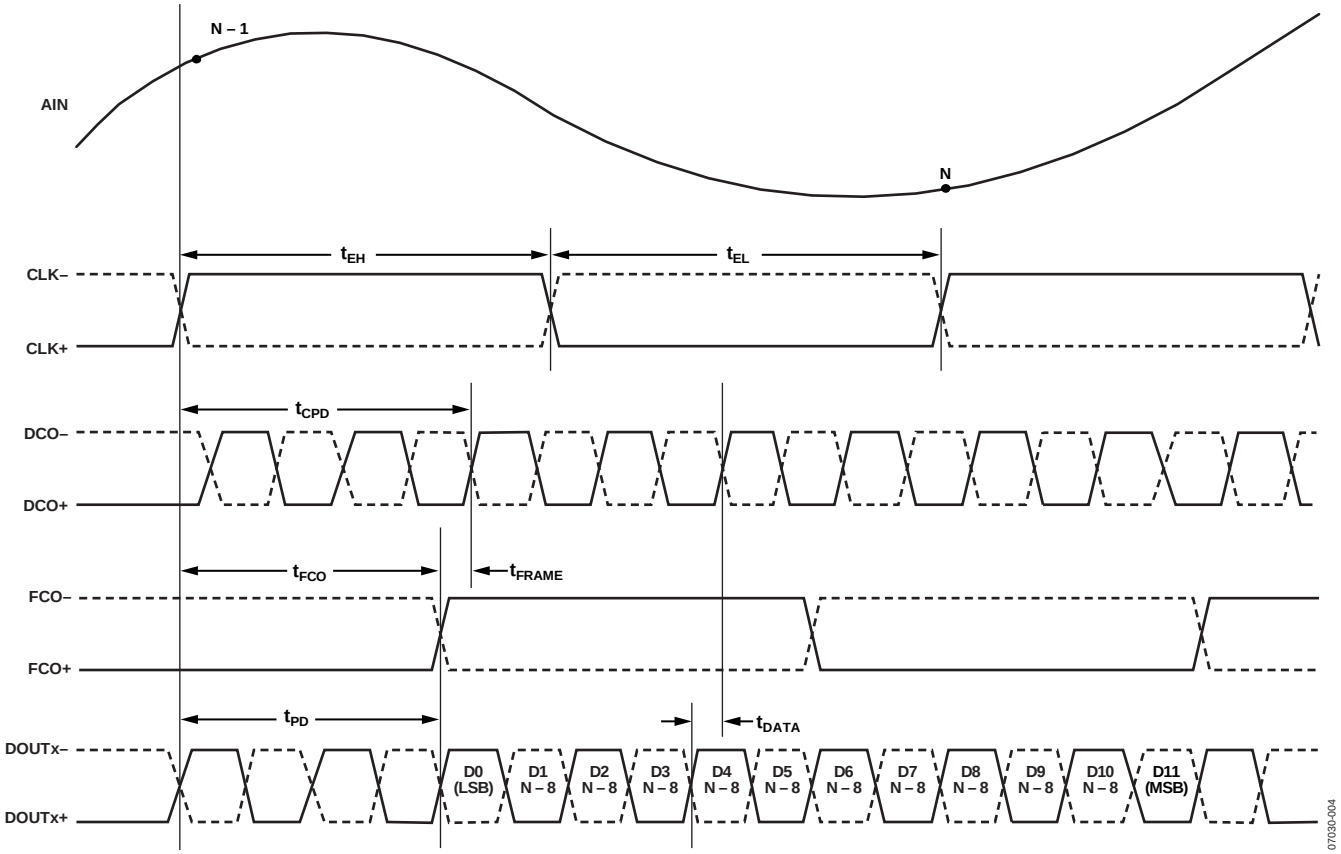


Figure 3. 12-Bit Data Serial Stream, LSB First

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	With Respect To	Rating
Electrical		
AVDD1	GND	−0.3 V to +2.0 V
AVDD2	GND	−0.3 V to +3.9 V
DRVDD	GND	−0.3 V to +2.0 V
GND	GND	−0.3 V to +0.3 V
AVDD2	AVDD1	−2.0 V to +3.9 V
AVDD2	DRVDD	−2.0 V to +3.9 V
AVDD1	DRVDD	−2.0 V to +2.0 V
Digital Outputs (DOUTx+, DOUTx−, DCO+, DCO−, FCO+, FCO−)	GND	−0.3 V to +2.0 V
CLK+, CLK−, GAIN+, GAIN−	GND	−0.3 V to +3.9 V
LI-x, LO-x, LOSW-x	LG-x	−0.3 V to +2.0 V
CWDx−, CWDx+	GND	−0.3 V to +3.9 V
PDWN, STBY, SCLK, CSB	GND	−0.3 V to +3.9 V
RBIAS, VREF, SDIO	GND	−0.3 V to +2.0 V
Environmental		
Operating Temperature Range (Ambient)		−40°C to +85°C
Storage Temperature Range (Ambient)		−65°C to +150°C
Maximum Junction Temperature		150°C
Lead Temperature (Soldering, 10 sec)		300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL IMPEDANCE

Table 5.

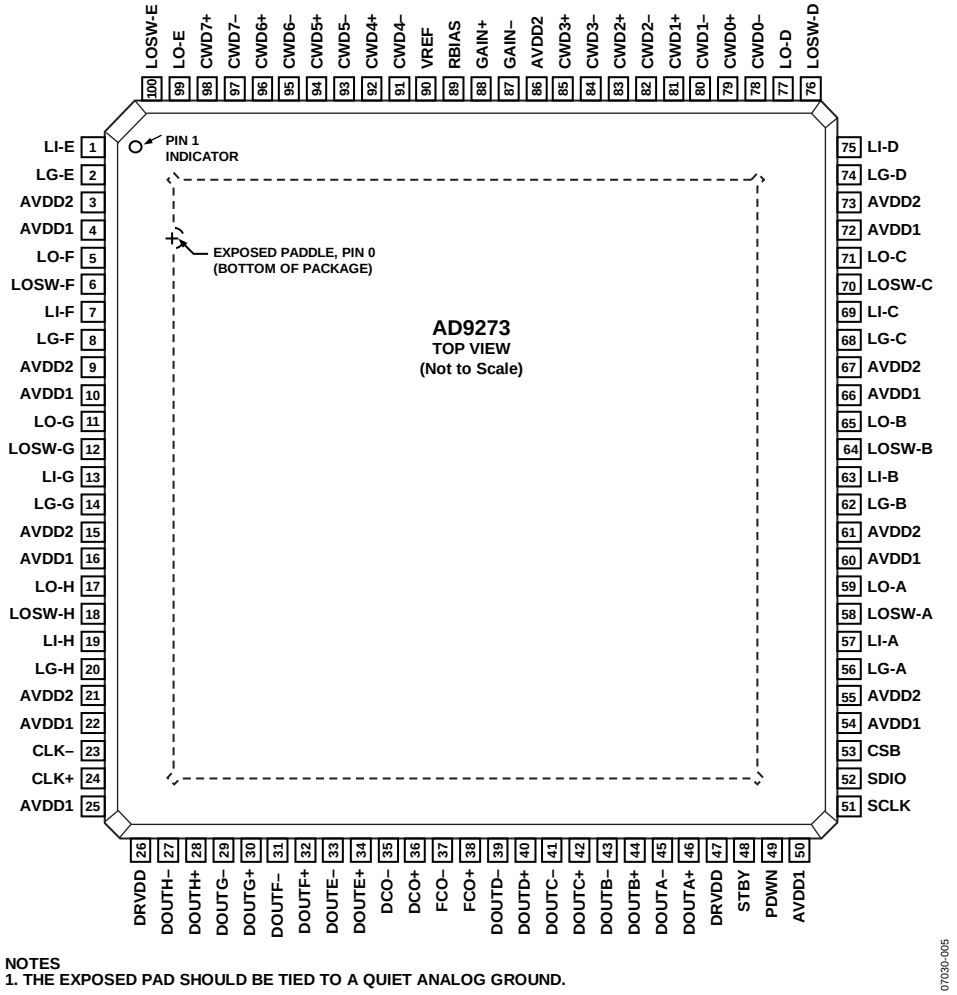
Airflow Velocity (m/sec)	θ_{JA}[1]	θ_{JB}	θ_{JC}	Unit
0.0	20.3	N/A	N/A	°C/W
1.0	14.4	7.6	4.7	°C/W
2.5	12.9	N/A	N/A	°C/W

[1] θ_{JA} is for a 4-layer PCB with a solid ground plane (simulated). The exposed pad is soldered to the PCB.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. THE EXPOSED PAD SHOULD BE TIED TO A QUIET ANALOG GROUND.

Figure 4. TQFP Pin Configuration

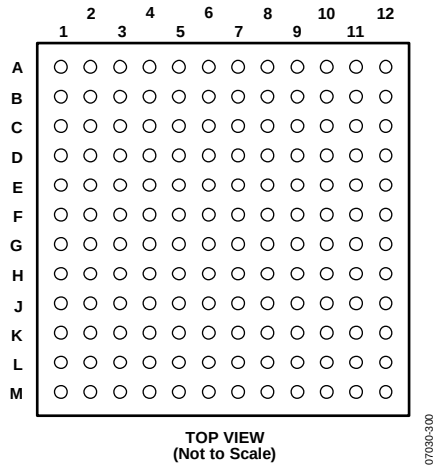


Figure 5. BGA Pin Configuration

Table 6. Pin Function Descriptions

Pin No.			
TQFP	**BGA**	**Name**	**Description**
0	N/A	GND	Ground (the exposed paddle should be tied to a quiet analog ground)
N/A	B5, B6, B8, C5, C6, C7, C8, D5, D6, D7, D8, E1, E5, E6, E7, E8, E12, F2, F4, F6, F7, F9, F11, G1, G3, G5, G6, G7, G8, G10, G12, H2, H3, H4, H5, H6, H7, H8, H9, H10, H11, J2, K1, K2, M1, M12	GND	Ground
4, 10, 16, 22, 25, 50, 54, 60, 66, 72	F1, F3, F5, F8, F10, F12, G2, G4, G9, G11	AVDD1	1.8 V Analog Supply
3, 9, 15, 21, 55, 61, 67, 73, 86	B7, E2, E3, E4, E9, E10, E11	AVDD2	3.0 V Analog Supply
26, 47	L1, L12	DRVDD	1.8 V Digital Output Driver Supply
1	A1	LI-E	LNA Analog Input for Channel E
2	B1	LG-E	LNA Ground for Channel E
5	C2	LO-F	LNA Analog Inverted Output for Channel F
6	D2	LOSW-F	LNA Analog Switched Output for Channel F
7	A2	LI-F	LNA Analog Input for Channel F
8	B2	LG-F	LNA Ground for Channel F
11	C3	LO-G	LNA Analog Inverted Output for Channel G
12	D3	LOSW-G	LNA Analog Switched Output for Channel G
13	A3	LI-G	LNA Analog Input for Channel G
14	B3	LG-G	LNA Ground for Channel G
17	C4	LO-H	LNA Analog Inverted Output for Channel H
18	D4	LOSW-H	LNA Analog Switched Output for Channel H
19	A4	LI-H	LNA Analog Input for Channel H
20	B4	LG-H	LNA Ground for Channel H
23	H1	CLK–	Clock Input Complement
24	J1	CLK+	Clock Input True
27	M2	DOUTH–	ADC H Digital Output Complement
28	L2	DOUTH+	ADC H Digital Output True
29	M3	DOUTG–	ADC G Digital Output Complement
30	L3	DOUTG+	ADC G Digital Output True
31	M4	DOUTF–	ADC F Digital Output Complement
32	L4	DOUTF+	ADC F Digital Output True
33	M5	DOUTE–	ADC E Digital Output Complement
34	L5	DOUTE+	ADC E Digital Output True
35	M6	DCO–	Digital Clock Output Complement
36	L6	DCO+	Digital Clock Output True
37	M7	FCO–	Frame Clock Digital Output Complement
38	L7	FCO+	Frame Clock Digital Output True
39	M8	DOUTD–	ADC D Digital Output Complement
40	L8	DOUTD+	ADC D Digital Output True
41	M9	DOUTC–	ADC C Digital Output Complement
42	L9	DOUTC+	ADC C Digital Output True
43	M10	DOUTB–	ADC B Digital Output Complement
44	L10	DOUTB+	ADC B Digital Output True

Pin No.			
TQFP	BGA	Name	Description
45	M11	DOUTA−	ADC A Digital Output Complement
46	L11	DOUTA+	ADC A Digital Output True
48	K11	STBY	Standby Power-Down
49	J11	PDWN	Full Power-Down
51	K12	SCLK	Serial Clock
52	J12	SDIO	Serial Data Input/Output
53	H12	CSB	Chip Select Bar
56	B9	LG-A	LNA Ground for Channel A
57	A9	LI-A	LNA Analog Input for Channel A
58	D9	LOSW-A	LNA Analog Switched Output for Channel A
59	C9	LO-A	LNA Analog Inverted Output for Channel A
62	B10	LG-B	LNA Ground for Channel B
63	A10	LI-B	LNA Analog Input for Channel B
64	D10	LOSW-B	LNA Analog Switched Output for Channel B
65	C10	LO-B	LNA Analog Inverted Output for Channel B
68	B11	LG-C	LNA Ground for Channel C
69	A11	LI-C	LNA Analog Input for Channel C
70	D11	LOSW-C	LNA Analog Switched Output for Channel C
71	C11	LO-C	LNA Analog Inverted Output for Channel C
74	B12	LG-D	LNA Ground for Channel D
75	A12	LI-D	LNA Analog Input for Channel D
76	D12	LOSW-D	LNA Analog Switched Output for Channel D
77	C12	LO-D	LNA Analog Inverted Output for Channel D
78	K10	CWD0−	CW Doppler Output Complement for Channel 0
79	J10	CWD0+	CW Doppler Output True for Channel 0
80	K9	CWD1−	CW Doppler Output Complement for Channel 1
81	J9	CWD1+	CW Doppler Output True for Channel 1
82	K8	CWD2−	CW Doppler Output Complement for Channel 2
83	J8	CWD2+	CW Doppler Output True for Channel 2
84	K7	CWD3−	CW Doppler Output Complement for Channel 3
85	J7	CWD3+	CW Doppler Output True for Channel 3
87	A8	GAIN−	Gain Control Voltage Input Complement
88	A7	GAIN+	Gain Control Voltage Input True
89	A6	RBIAS	External Resistor to Set the Internal ADC Core Bias Current
90	A5	VREF	Voltage Reference Input/Output
91	K6	CWD4−	CW Doppler Output Complement for Channel 4
92	J6	CWD4+	CW Doppler Output True for Channel 4
93	K5	CWD5−	CW Doppler Output Complement for Channel 5
94	J5	CWD5+	CW Doppler Output True for Channel 5
95	K4	CWD6−	CW Doppler Output Complement for Channel 6
96	J4	CWD6+	CW Doppler Output True for Channel 6
97	K3	CWD7−	CW Doppler Output Complement for Channel 7
98	J3	CWD7+	CW Doppler Output True for Channel 7
99	C1	LO-E	LNA Analog Inverted Output for Channel E
100	D1	LOSW-E	LNA Analog Switched Output for Channel E

TYPICAL PERFORMANCE CHARACTERISTICS

f_{SAMPLE} = 40 MSPS, f_{IN} = 5 MHz, R_S = 50 Ω, LNA gain = 21.3 dB, LNA bias = mid-high, PGA gain = 24 dB, AAF LPF cutoff = $f_{SAMPLE}/3$, HPF = LPF cutoff/20.7 (default), GAIN− = 0.8 V

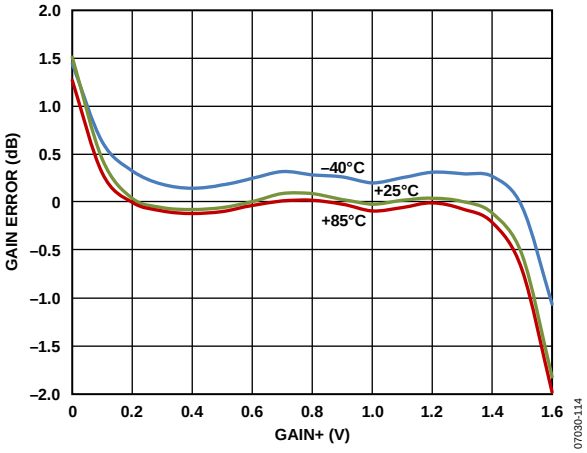


Figure 6. Gain Error vs. GAIN+ at Three Temperatures

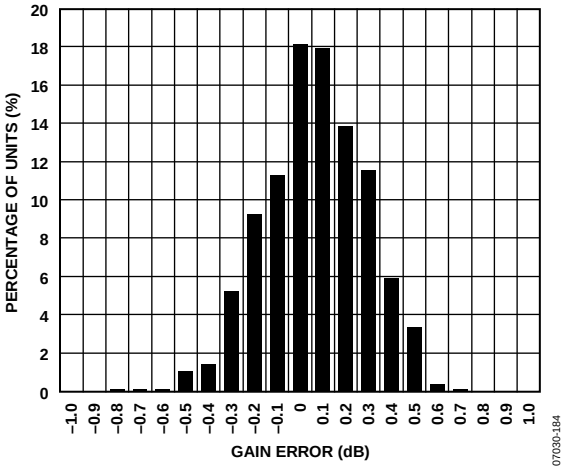


Figure 7. Gain Error Histogram, GAIN+ = 0.16 V

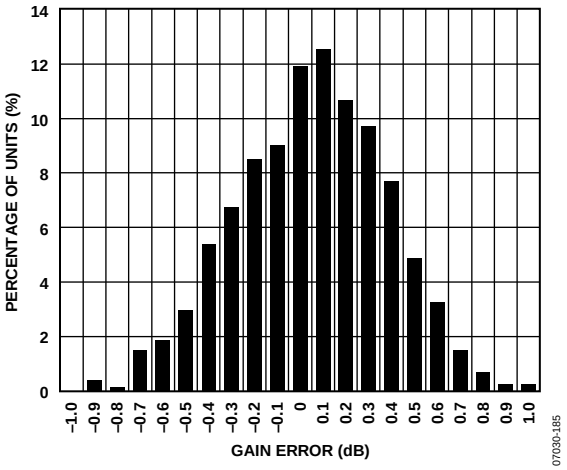


Figure 8. Gain Error Histogram, GAIN+ = 0.8 V

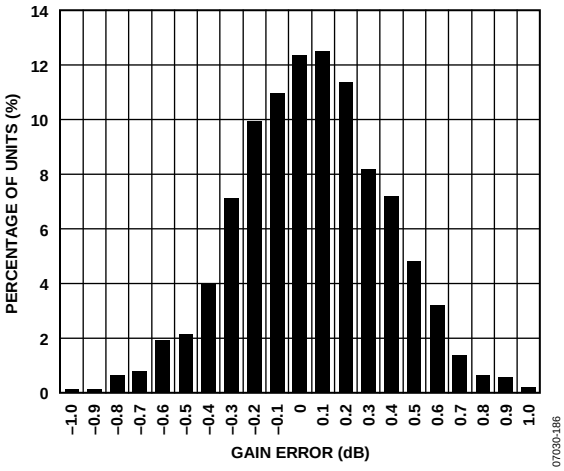


Figure 9. Gain Error Histogram, GAIN+ = 1.44 V

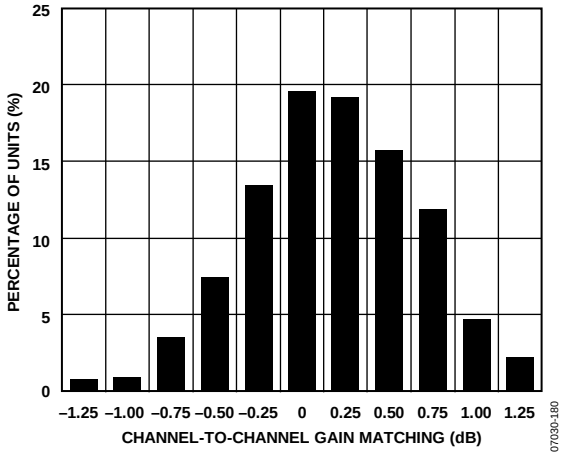


Figure 10. Gain Match Histogram, GAIN+ = 0.3 V

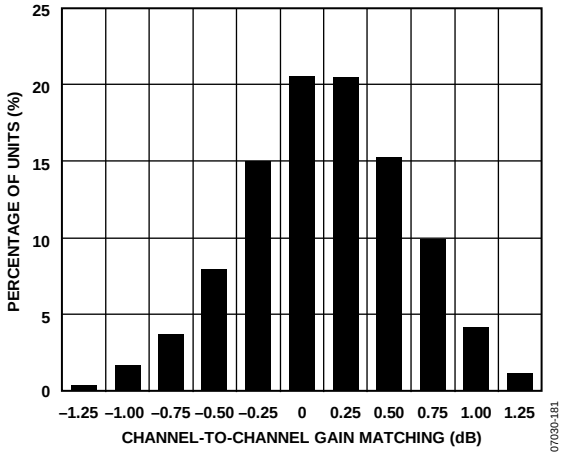


Figure 11. Gain Match Histogram, GAIN+ = 1.3 V

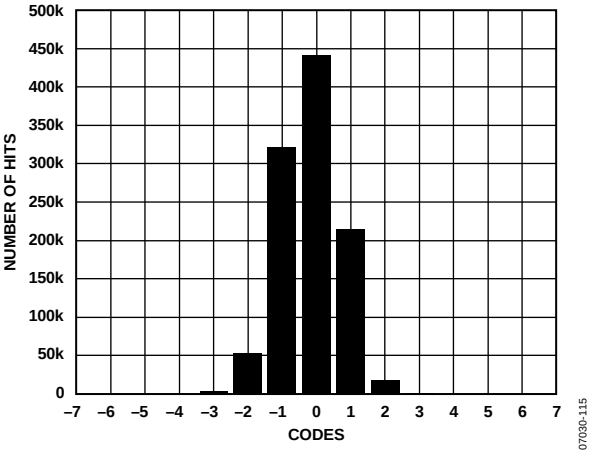


Figure 12. Output-Referred Noise Histogram, GAIN+ = 0.0 V

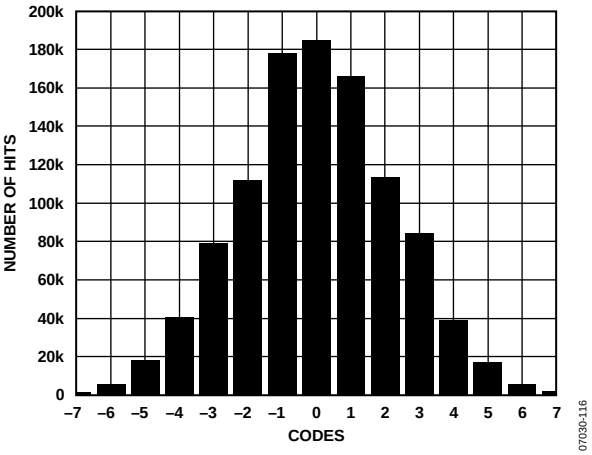


Figure 13. Output-Referred Noise Histogram, GAIN+ = 1.6 V

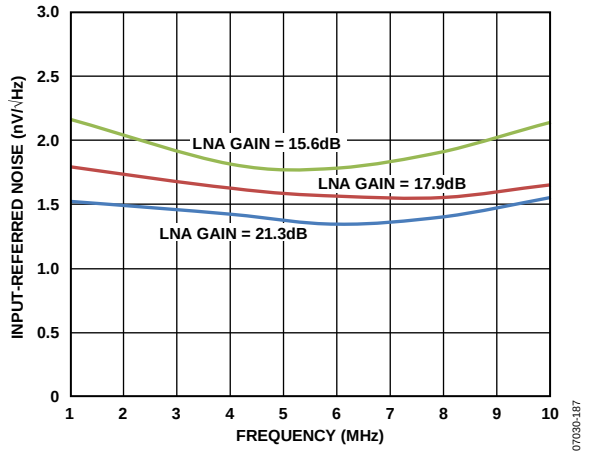


Figure 14. Short-Circuit, Input-Referred Noise vs. Frequency, PGA Gain = 30 dB, GAIN+ = 1.6 V

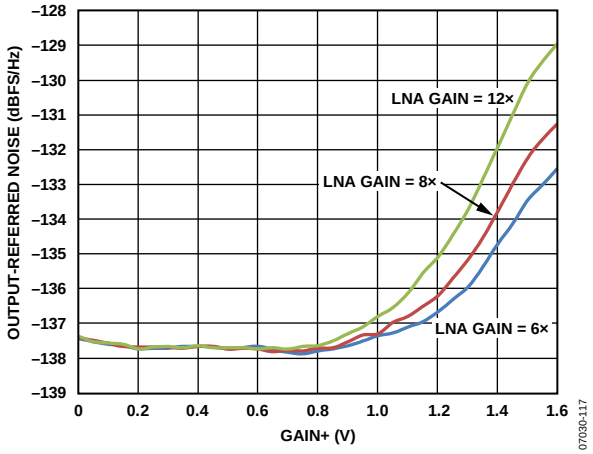


Figure 15. Short-Circuit, Output-Referred Noise vs. GAIN+

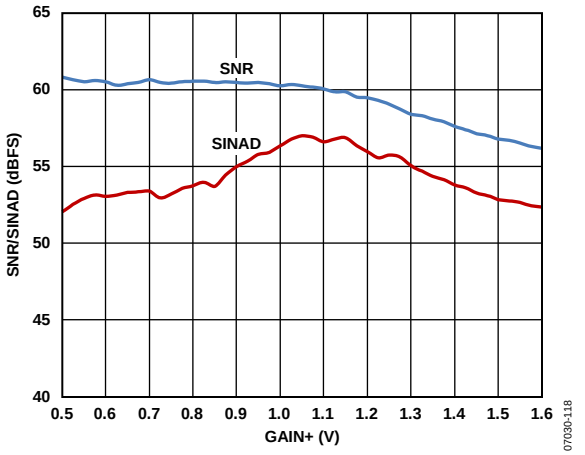


Figure 16. SNR/SINAD vs. GAIN+, AIN = −1.0 dBFS

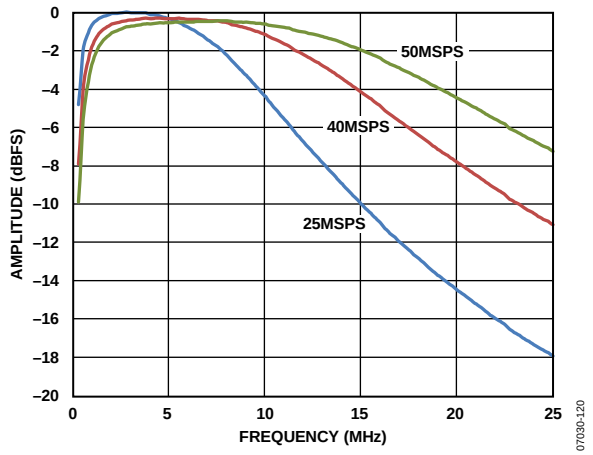


Figure 17. Antialiasing Filter (AAF) Pass-Band Response, LPF Cutoff = 1 × (1/3) × f_{SAMPLE}

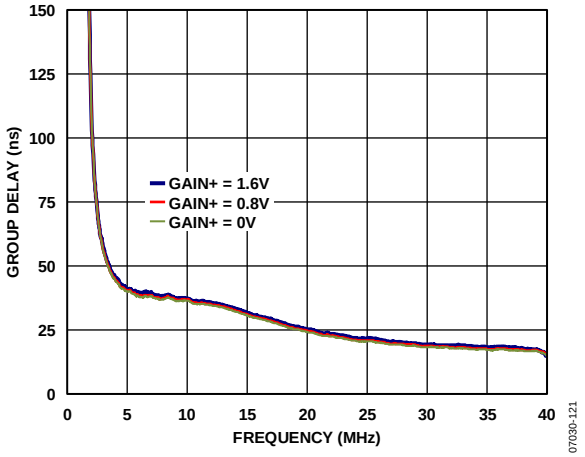


Figure 18. Antialiasing Filter (AAF) Group Delay Response

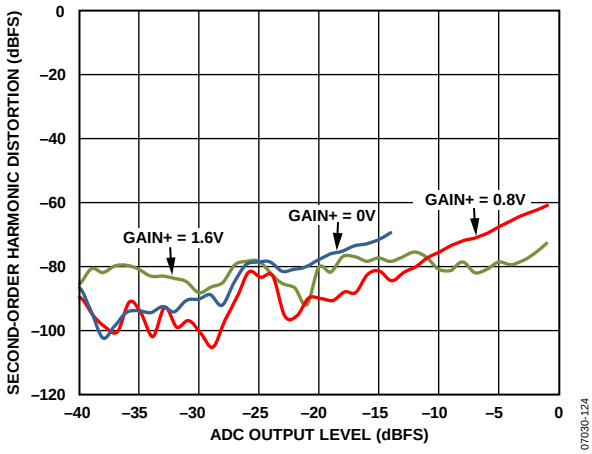


Figure 21. Second-Order Harmonic Distortion vs. ADC Output Level

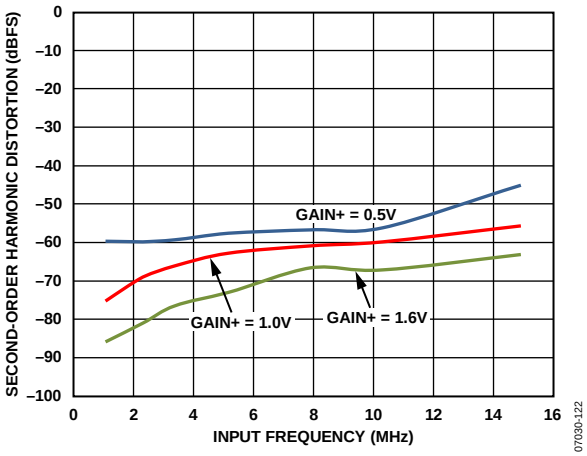


Figure 19. Second-Order Harmonic Distortion vs. Input Frequency, AIN = −1.0 dBFS

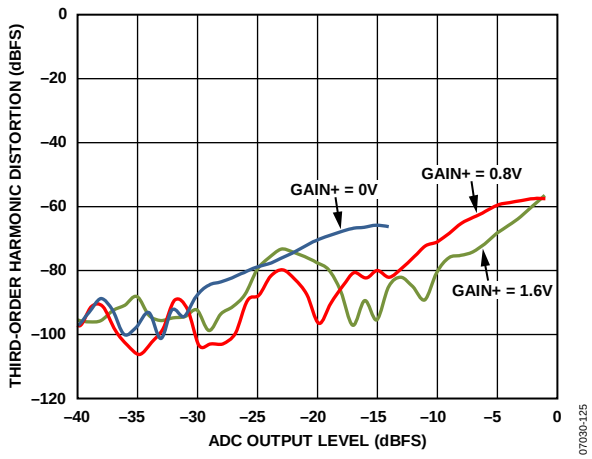


Figure 22. Third-Order Harmonic Distortion vs. ADC Output Level

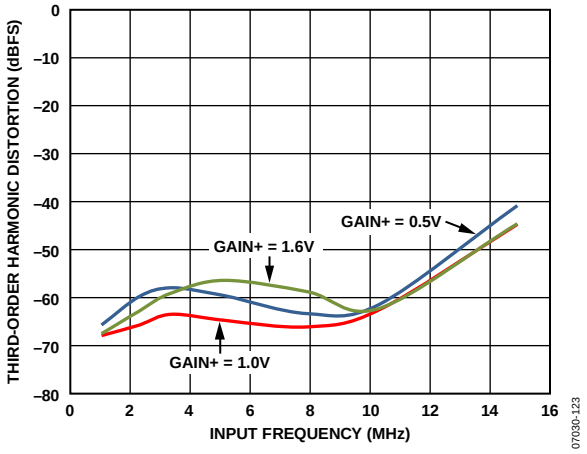


Figure 20. Third-Order Harmonic Distortion vs. Input Frequency, AIN = −1.0 dBFS

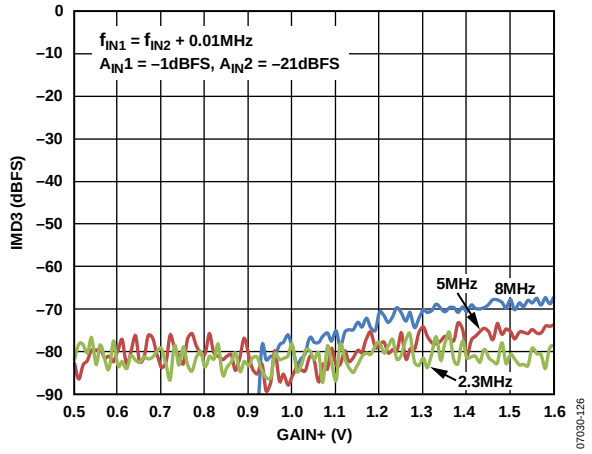


Figure 23. IMD3 vs. GAIN+

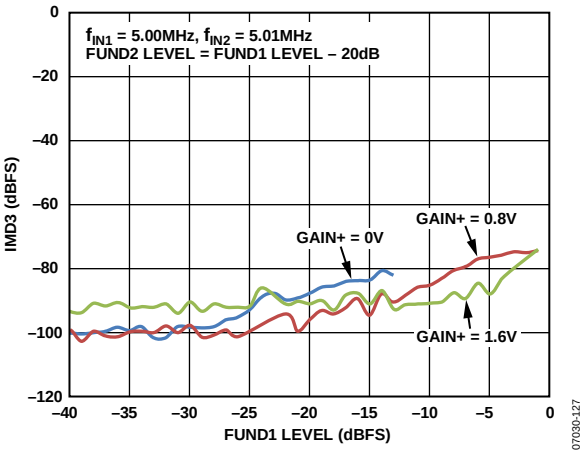


Figure 24. IMD3 vs. Fundamental 1 Amplitude (FUND1) Level

EQUIVALENT CIRCUITS

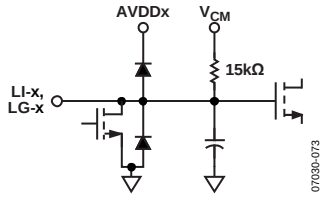


Figure 25. Equivalent LNA Input Circuit

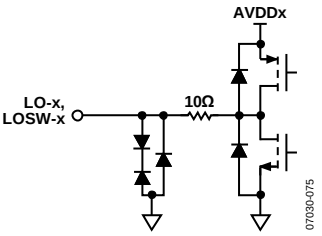


Figure 26. Equivalent LNA Output Circuit

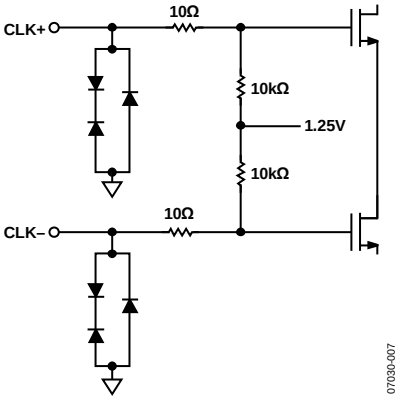


Figure 27. Equivalent Clock Input Circuit

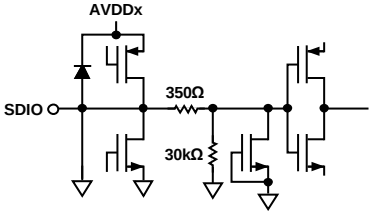


Figure 28. Equivalent SDIO Input Circuit

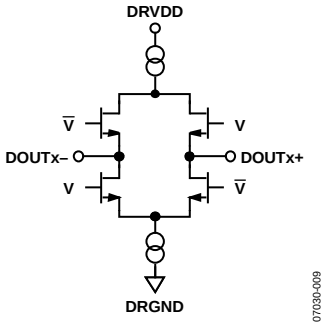


Figure 29. Equivalent Digital Output Circuit

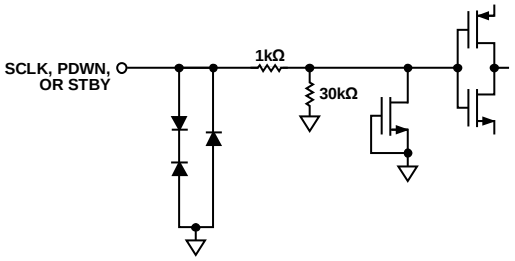


Figure 30. Equivalent SCLK, PDWN, or STBY Input Circuit

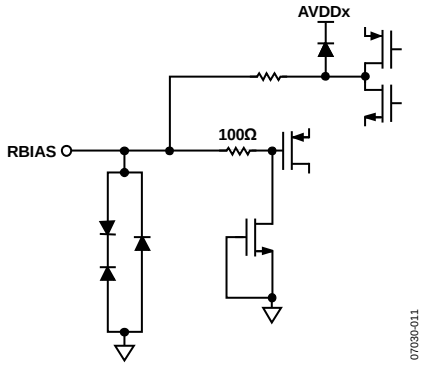


Figure 31. Equivalent RBIAS Circuit

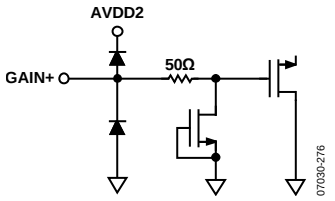


Figure 34. Equivalent GAIN+ Input Circuit

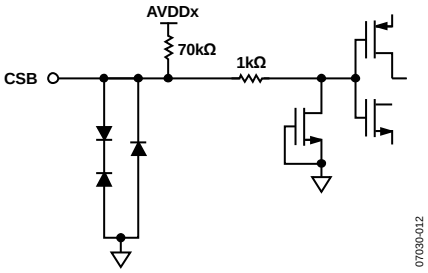


Figure 32. Equivalent CSB Input Circuit

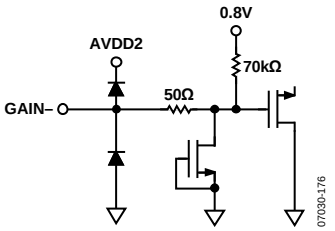


Figure 35. Equivalent GAIN– Input Circuit

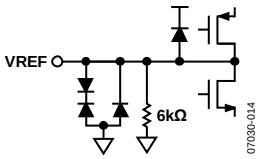


Figure 33. Equivalent VREF Circuit

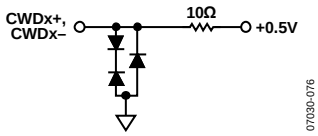


Figure 36. Equivalent CWDx± Output Circuit

THEORY OF OPERATION

ULTRASOUND

The primary application for the AD9273 is medical ultrasound. Figure 37 shows a simplified block diagram of an ultrasound system. A critical function of an ultrasound system is the time gain control (TGC) compensation for physiological signal attenuation. Because the attenuation of ultrasound signals is exponential with respect to distance (time), a linear-in-dB VGA is the optimal solution.

Key requirements in an ultrasound signal chain are very low noise, active input termination, fast overload recovery, low power, and differential drive to an ADC. Because ultrasound machines use beam-forming techniques requiring a large binary-weighted number of channels (for example, 32 to 512 channels), using the lowest power at the lowest possible noise is of chief importance.

Most modern machines use digital beam forming. In this technique, the signal is converted to digital format immediately following the TGC amplifier, and then beam forming is accomplished digitally.

The ADC resolution of 12 bits with up to 50 MSPS sampling satisfies the requirements of both general-purpose and high-end systems.

Power conservation and low cost are two of the most important factors in low-end and portable ultrasound machines, and the AD9273 is designed to meet these criteria.

For additional information regarding ultrasound systems, refer to "How Ultrasound System Considerations Influence Front-End Component Choice," *Analog Dialogue*, Volume 36, Number 3, May–July 2002, and "The AD9271—A Revolutionary Solution for Portable Ultrasound," *Analog Dialogue*, Volume 41, Number 3, July 2007.

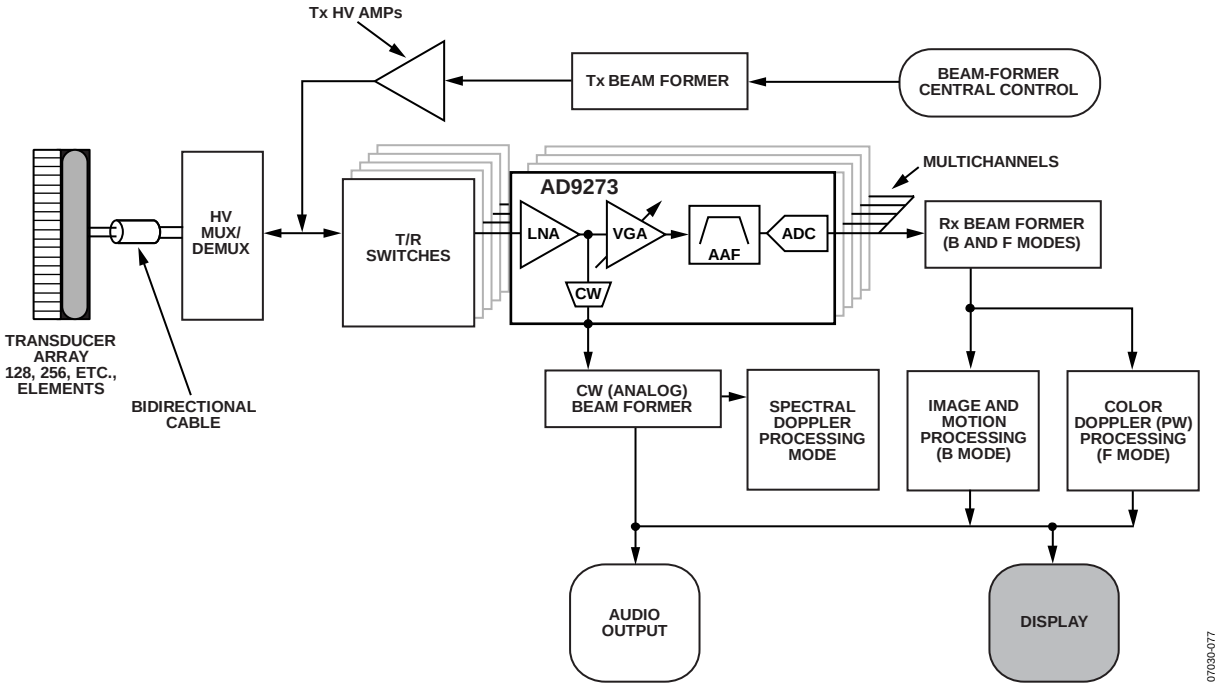


Figure 37. Simplified Ultrasound System Block Diagram

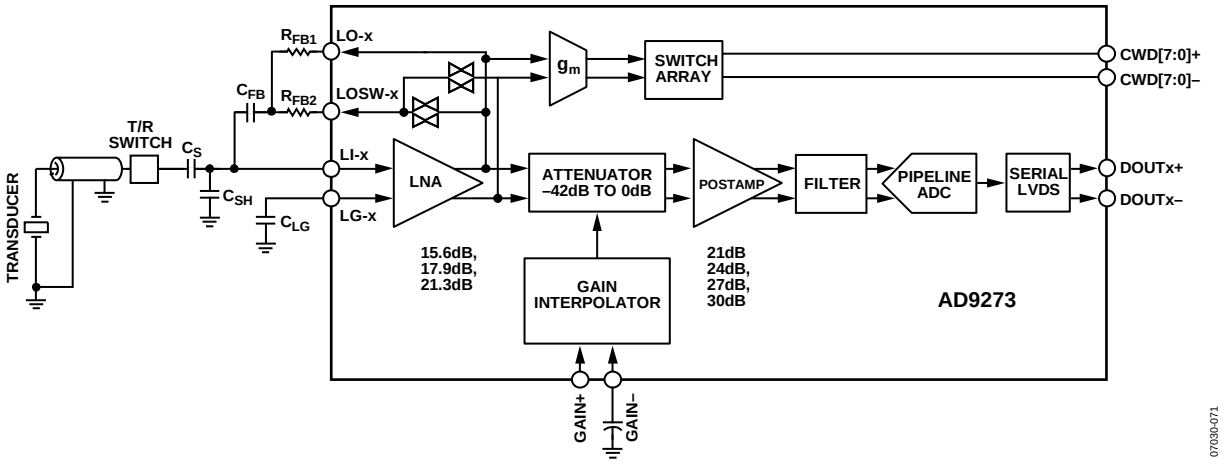


Figure 38. Simplified Block Diagram of a Single Channel

CHANNEL OVERVIEW

Each channel contains both a TGC signal path and a CW Doppler signal path. Common to both signal paths, the LNA provides user-adjustable input impedance termination. The CW Doppler path includes a transconductance amplifier and a crosspoint switch. The TGC path includes a differential X-AMP® VGA, an antialiasing filter, and an ADC. Figure 38 shows a simplified block diagram with external components.

The signal path is fully differential throughout to maximize signal swing and reduce even-order distortion; however, the LNA is designed to be driven from a single-ended signal source.

Low Noise Amplifier (LNA)

Good noise performance relies on a proprietary ultralow noise LNA at the beginning of the signal chain, which minimizes the noise contribution in the following VGA. Active impedance control optimizes noise performance for applications that benefit from input impedance matching.

A simplified schematic of the LNA is shown in Figure 39. LI-x is capacitively coupled to the source. An on-chip bias generator establishes dc input bias voltages of around 0.9 V and centers the output common-mode levels at 1.5 V (AVDD2 divided by 2). A capacitor, C_{LG}, of the same value as the input coupling capacitor, C_S, is connected from the LG-x pin to ground.

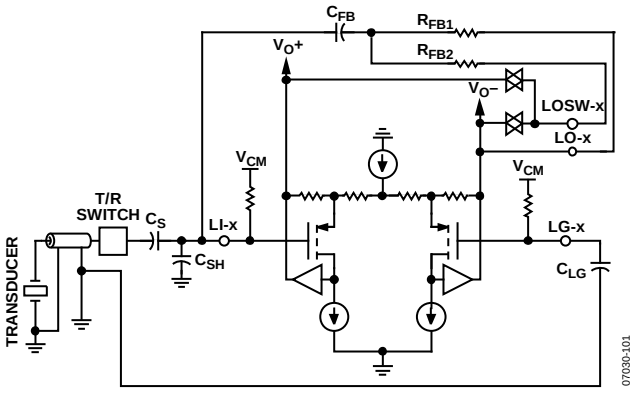


Figure 39. Simplified LNA Schematic

The LNA supports differential output voltages as high as 4.4 V p-p with positive and negative excursions of ±1.1 V from a common-mode voltage of 1.5 V. The LNA differential gain sets the maximum input signal before saturation. One of three gains is set through the SPI. The corresponding full-scale input for the gain settings of 6, 8, and 12 is 733 mV p-p, 550 mV p-p, and 367 mV p-p, respectively. Overload protection ensures quick recovery time from large input voltages. Because the inputs are capacitively coupled to a bias voltage near midsupply, very large inputs can be handled without interacting with the ESD protection.

Low value feedback resistors and the current-driving capability of the output stage allow the LNA to achieve a low input-referred noise voltage of 1.26 nV/√Hz at a gain of 21.3 dB. This is achieved with a current consumption of only 10 mA per channel (30 mW). On-chip resistor matching results in precise single-ended gains, which are critical for accurate impedance control. The use of a fully differential topology and negative feedback minimizes distortion. Low second-order harmonic distortion is particularly important in second-order harmonic ultrasound imaging applications. Differential signaling enables smaller swings at each output, further reducing third-order distortion.

Recommendation

It is highly recommended that the LG-x pins form a Kelvin type connection to the input or probe connection ground. Simply connecting the LG pin to ground near the device may allow differences in potential to be amplified through the LNA. This generally shows up as a dc offset voltage that can vary from channel to channel and part to part, depending on the application and layout of the PCB (see Figure 38).

Active Impedance Matching

The LNA consists of a single-ended voltage gain amplifier with differential outputs and the negative output available externally. For example, with a fixed gain of 8× (17.9 dB), an active input termination is synthesized by connecting a feedback resistor between the negative output pin, LO-x, and the positive input pin, LI-x. This well-known technique is used for interfacing multiple probe impedances to a single system. The input resistance is shown in Equation 1.

$$R_{IN} = \frac{R_{FB}}{(1 + A/2)} \quad (1)$$

where $A/2$ is the single-ended gain or the gain from the LI-x inputs to the LO-x outputs, and R_{FB} is the resulting impedance of the R_{FB1} and R_{FB2} combination (see Figure 39).

Because the amplifier has a gain of 8× from its input to its differential output, it is important to note that the gain A/2 is the gain from Pin LI-x to Pin LO-x, and it is 6 dB less than the gain of the amplifier, or 12.1 dB (4×). The input resistance is reduced by an internal bias resistor of 15 kΩ in parallel with the source resistance connected to Pin LI-x while Pin LG-x is ac grounded. Equation 2 can be used to calculate the needed R_{FB} for a desired R_{IN}, even for higher values of R_{IN}.

$$R_{IN} = \frac{R_{FB}}{(1+3)} \,||\, 15\ \text{k}\Omega \quad (2)$$

For example, to set R_{IN} to 200 Ω, the value of R_{FB} must be 1000 Ω. If the simplified equation (Equation 2) is used to calculate R_{IN}, the value is 188 Ω, resulting in a gain error less than 0.6 dB. Some factors, such as the presence of a dynamic source resistance, might influence the absolute gain accuracy more significantly. At higher frequencies, the input capacitance of the LNA needs to be considered. The user must determine the level of matching accuracy and adjust R_{FB} accordingly.

The bandwidth (BW) of the LNA is greater than 100 MHz. Ultimately, the BW of the LNA limits the accuracy of the synthesized R_{IN}. For $R_{IN} = R_S$ up to about 200 Ω, the best match is between 100 kHz and 10 MHz, where the lower frequency limit is determined by the size of the ac-coupling capacitors, and the upper limit is determined by the LNA BW. Furthermore, the input capacitance and R_S limit the BW at higher frequencies. Figure 40 shows R_{IN} vs. frequency for various values of R_{FB}.

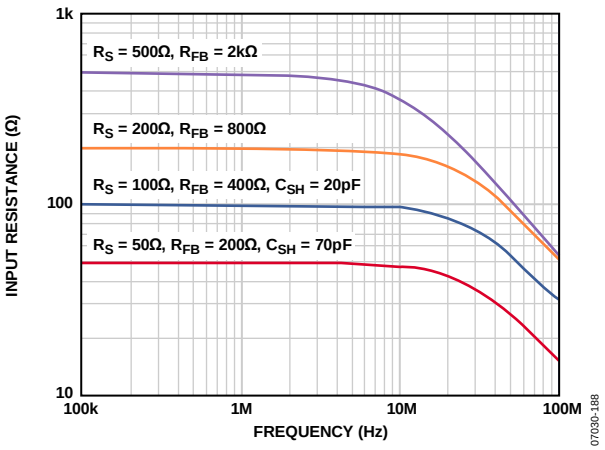


Figure 40. R_{IN} vs. Frequency for Various Values of R_{FB} (Effects of R_S and C_{SH} Are Also Shown)

Note that at the lowest value (50 Ω), R_{IN} peaks at frequencies greater than 10 MHz. This is due to the BW roll-off of the LNA, as mentioned previously.

However, as can be seen for larger R_{IN} values, parasitic capacitance starts rolling off the signal BW before the LNA can produce peaking. C_{SH} further degrades the match; therefore, C_{SH} should not be used for values of R_{IN} that are greater than 100 Ω. Table 7 lists the recommended values for R_{FB} and C_{SH} in terms of R_{IN}.

C_{FB} is needed in series with R_{FB} because the dc levels at Pin LO-x and Pin LI-x are unequal.

Table 7. Active Termination External Component Values

LNA Gain (dB)	R_{IN} (Ω)	R_{FB} (Ω)	Minimum C_{SH} (pF)	BW (MHz)
15.6	50	200	90	57
17.9	50	250	70	69
21.3	50	350	50	88
15.6	100	400	30	57
17.9	100	500	20	69
21.3	100	700	10	88
15.6	200	800	N/A	72
17.9	200	1000	N/A	72
21.3	200	1400	N/A	72

LNA Noise

The short-circuit noise voltage (input-referred noise) is an important limit on system performance. The short-circuit input-referred noise voltage for the LNA is 1.4 nV/√Hz at a gain of 21.3 dB, including the VGA noise at a VGA postamp gain of 27 dB. These measurements, which were taken without a feedback resistor, provide the basis for calculating the input noise and noise figure (NF) performance of the configurations shown in Figure 41.

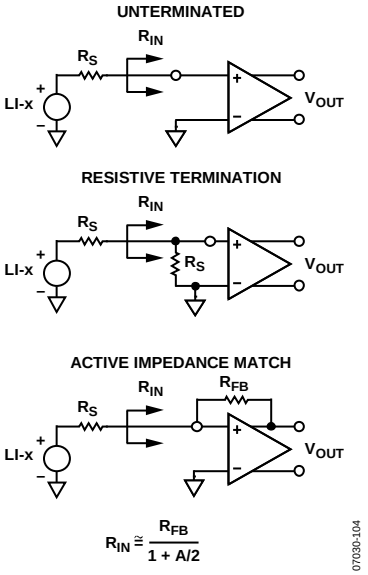


Figure 41. Input Configurations

Figure 42 and Figure 43 are simulations of noise figure vs. source resistance (R_S) results using these configurations and an input-referred noise voltage of 6 nV/√Hz for the VGA. Unterminated ($R_{FB} = \infty$) operation exhibits the lowest equivalent input noise and noise figure. Figure 43 shows the noise figure vs. R_S rising at low R_S—where the LNA voltage noise is large compared with the source noise—and at high R_S due to the noise contribution from R_{FB}. The lowest NF is achieved when R_S matches R_{IN}.

The main purpose of input impedance matching is to improve the transient response of the system. With resistive termination, the input noise increases due to the thermal noise of the matching resistor and the increased contribution of the LNA's input voltage noise generator. With active impedance matching, however, the contributions of both are smaller (by a factor of 1/(1 + LNA Gain)) than they would be for resistive termination.

Figure 42 shows the relative noise figure performance. In this graph, the input impedance was swept with R_S to preserve the match at each point. The noise figures for a source impedance of 50 Ω are 7.3 dB, 4.2 dB, and 2.8 dB for the resistive termination, active termination, and unterminated configurations, respectively. The noise figures for 200 Ω are 4.5 dB, 1.7 dB, and 1.0 dB, respectively.

Figure 43 shows the noise figure as it relates to R_S for various values of R_{IN}, which is helpful for design purposes.

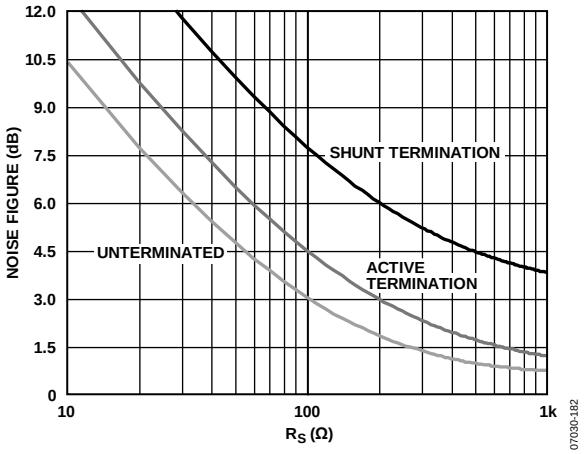


Figure 42. Noise Figure vs. R_S for Shunt Termination, Active Termination Matched, and Unterminated Inputs, V_{GAIN} = 0.8 V

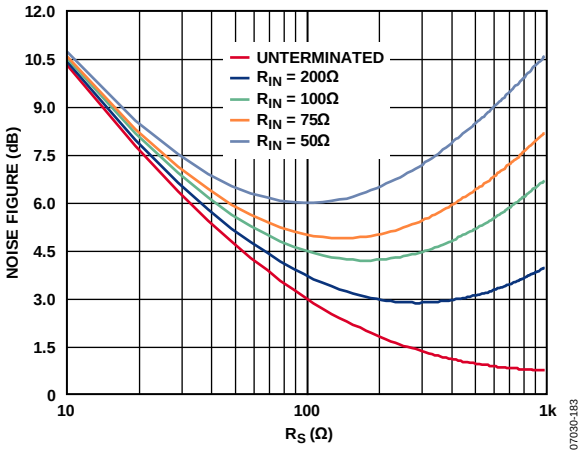


Figure 43. Noise Figure vs. R_S for Various Fixed Values of R_{IN}, Active Termination Matched Inputs, V_{GAIN} = 0.8 V

INPUT OVERDRIVE

Excellent overload behavior is of primary importance in ultrasound. Both the LNA and VGA have built-in overdrive protection and quickly recover after an overload event.

Input Overload Protection

As with any amplifier, voltage clamping prior to the inputs is highly recommended if the application is subject to high transient voltages.

In Figure 44, a simplified ultrasound transducer interface is shown. A common transducer element serves the dual functions of transmitting and receiving ultrasound energy. During the transmitting phase, high voltage pulses are applied to the ceramic elements. A typical transmit/receive (T/R) switch can consist of four high voltage diodes in a bridge configuration. Although the diodes ideally block transmit pulses from the sensitive receiver input, diode characteristics are not ideal, and the resulting leakage transients imposed on the LI-x inputs can be problematic.

Because ultrasound is a pulse system and time-of-flight is used to determine depth, quick recovery from input overloads is essential. Overload can occur in the preamp and the VGA. Immediately following a transmit pulse, the typical VGA gains are low, and the LNA is subject to overload from T/R switch leakage. With increasing gain, the VGA can become overloaded due to strong echoes that occur near field echoes and acoustically dense materials, such as bone.

Figure 44 illustrates an external overload protection scheme. A pair of back-to-back signal diodes is installed prior to installing the ac-coupling capacitors. Keep in mind that all diodes shown in this example are prone to exhibiting some amount of shot noise. Many types of diodes are available for achieving the desired noise performance. The configuration shown in Figure 44 tends to add 2 nV/√Hz of input-referred noise. Decreasing the 5 kΩ resistor and increasing the 2 kΩ resistor may improve noise contribution, depending on the application. With the diodes shown in Figure 44, clamping levels of ±0.5 V or less significantly enhance the overload performance of the system.

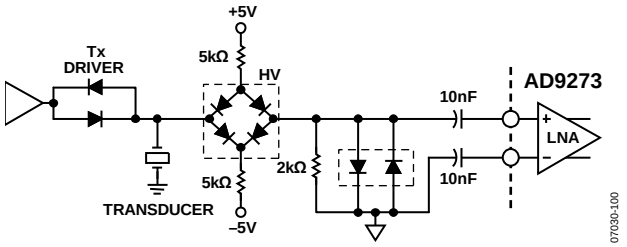


Figure 44. Input Overload Protection

CW DOPPLER OPERATION

Modern ultrasound machines used for medical applications employ a 2^N binary array of receivers for beam forming, with typical array sizes of 16 or 32 receiver channels phase-shifted and summed together to extract coherent information. When used in multiples, the desired signals from each channel can be summed to yield a larger signal (increased by a factor N, where N is the number of channels), and the noise is increased by the square root of the number of channels. This technique enhances the signal-to-noise performance of the machine. The critical elements in a beam-former design are the means to align the incoming signals in the time domain and the means to sum the individual signals into a composite whole.

Beam forming, as applied to medical ultrasound, is defined as the phase alignment and summation of signals that are generated from a common source but received at different times by a multielement ultrasound transducer. Beam forming has two functions: it imparts directivity to the transducer, enhancing its gain, and it defines a focal point within the body from which the location of the returning echo is derived.

The AD9273 includes the front-end components needed to implement analog beam forming for CW Doppler operation. These components allow CW channels with similar phases to be coherently combined before phase alignment and down mixing, thus reducing the number of delay lines or adjustable phase shifters/down mixers (AD8333 or AD8339) required. Next, if delay lines are used, the phase alignment is performed, and then the channels are coherently summed and down converted by a dynamic range I/Q demodulator. Alternatively, if phase shifters/down mixers, such as the AD8333 and AD8339, are used, phase alignment and downconversion are done before coherently summing all channels into I/Q signals. In either case, the resultant I and Q signals are filtered and sampled by two high resolution ADCs, and the sampled signals are processed to extract the relevant Doppler information.

Alternately, the LNA of the AD9273 can directly drive the AD8333 or AD8339 without the crosspoint switch. The LO-x pins present the inverting LNA output, and the LOSW-x pins can be configured via Register 0x2C (see Table 17) to connect to the noninverting output to provide a differential output of the LNA. The LNA output full-scale voltage of the AD9273 is 4.4 V p-p, and the input full-scale voltage is 2.7 V p-p. If no attenuation is provided between the LNA output and the demodulator, the LNA input full-scale voltage must be limited.

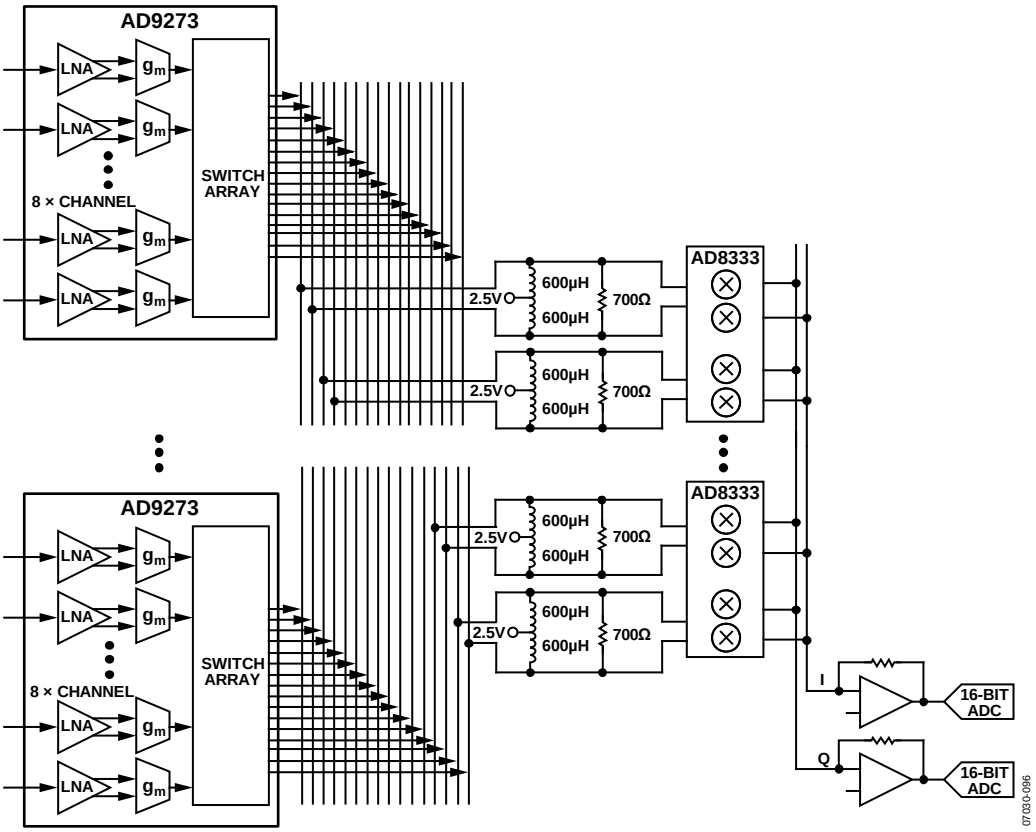


Figure 45. Typical Connection Interface with the AD8333 or AD8339 using the CWDx± Outputs

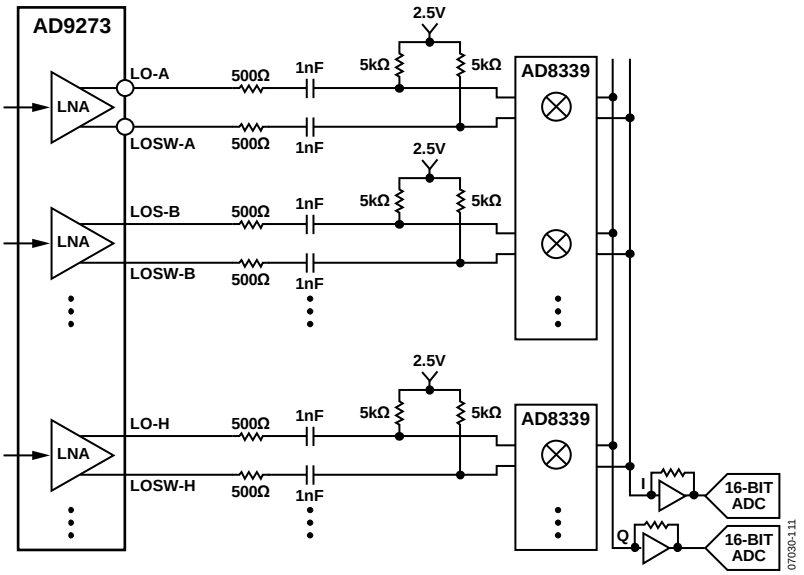


Figure 46. Typical Connection Interface with the AD8333 or AD8339 using the LO-x and LOSW-x Outputs

Crosspoint Switch

Each LNA is followed by a transconductance amp for voltage-to-current conversion. Currents can be routed to one of eight pairs of differential outputs or to 16 single-ended outputs for summing. Each CWD output pin sinks 2.4 mA dc current, and the signal has a full-scale current of ±2 mA for each channel selected by the crosspoint switch. For example, if four channels are summed on one CWD output, the output sinks 9.6 mA dc and has a full-scale current output of ±8 mA.

The maximum number of channels combined must be considered when setting the load impedance for current-to-voltage conversion to ensure that the full-scale swing and common-mode voltage are within the operating limits of the AD9273. When interfacing to the AD8339, a common-mode voltage of 2.5 V and a full-scale swing of 2.8 V p-p are desired. This can be accomplished by connecting an inductor between each CWD output and a 2.5 V supply, and then connecting either a single-ended or differential load resistance to the CWDx± outputs. The value of resistance should be calculated based on the maximum number of channels that can be combined.

CWDx± outputs are required under full-scale swing to be greater than 1.5 V and less than AVDD2 (3.0 V supply).

TGC OPERATION

The TGC signal path is fully differential throughout to maximize signal swing and reduce even-order distortion; however, the LNAs are designed to be driven from a single-ended signal source. Gain values are referenced from the single-ended LNA input to the differential ADC input. A simple exercise in understanding the maximum and minimum gain requirements is shown in Figure 47.

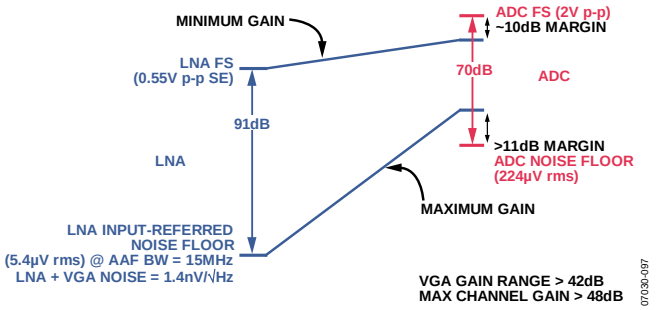


Figure 47. Gain Requirements of TGC Operation for a 12-Bit, 40 MSPS ADC

The maximum gain required is determined by

(*ADC Noise Floor*/*VGA Input Noise Floor*) + *Margin* =
20 log(224/5.4) + 11 dB = 43 dB

The minimum gain required is determined by

(*ADC Input FS*/*VGA Input FS*) + *Margin* =
20 log(2/0.55) − 10 dB = 3 dB

Therefore, 42 dB of gain range for a 12-bit, 40 MSPS ADC with 15 MHz of bandwidth should suffice in achieving the dynamic range required for most of today's ultrasound systems.

The system gain is distributed as listed in Table 8.

Table 8. Channel Gain Distribution

Section	Nominal Gain (dB)
LNA	15.6/17.9/21.3
Attenuator	−42 to 0
VGA Amp	21/24/27/30
Filter	0
ADC	0

The linear-in-dB gain (law conformance) range of the TGC path is 42 dB. The slope of the gain control interface is 28 dB/V, and the gain control range is −0.8 V to +0.8 V. Equation 3 is the expression for the differential voltage V_{GAIN}, and Equation 4 is the expression for the channel gain.

$$V_{GAIN}(V) = GAIN(+) - GAIN(-) \quad (3)$$

$$Gain\ (\text{dB}) = 28\frac{\text{dB}}{\text{V}} V_{GAIN} + ICPT \quad (4)$$

where *ICPT* is the intercept point of the TGC gain.

In its default condition, the LNA has a gain of 21.3 dB (12×) and the VGA postamp gain is 24 dB if the voltage on the GAIN+ pin is 0 V and the voltage on the GAIN− pin is 0.8 V (42 dB attenuation). This gives rise to a total gain (or ICPT) of 3.6 dB through the TGC path if the LNA input is unmatched, or of −2.4 dB if the LNA is matched to 50 Ω (R_{FB} = 350 Ω). If the voltage on the GAIN+ pin is 1.6 V and the voltage on the GAIN− pin is 0.8 V (0 dB attenuation), however, the VGA gain is 24 dB. This results in a total gain of 45 dB through the TGC path if the LNA input is unmatched, or in a total gain of 39 dB if the LNA input is matched.

Each LNA output is dc-coupled to a VGA input. The VGA consists of an attenuator with a range of −42 dB to 0 dB followed by an amplifier with 21 dB, 24 dB, 27 dB, or 30 dB of gain. The X-AMP gain-interpolation technique results in low gain error and uniform bandwidth, and differential signal paths minimize distortion.

Table 9. Sensitivity and Dynamic Range of Trade-Offs[1, 2, 3]

LNA				Channel			
Gain				Typical Output Dynamic Range			
(V/V)	(dB)	Full-Scale Input (V p-p)	Input-Referred Noise Voltage (nV/√Hz)	VGA Postamp Gain (dB)	GAIN+ = 0 V[4]	GAIN+ = 1.6 V[5]	Input-Referred Noise[6] @ GAIN+ = 1.6 V (nV/√Hz)
6	15.6	0.733	1.6	21	65.9	62.3	1.98
				24	64.1	59.7	1.91
				27	61.8	57.0	1.87
				30	59.2	54.1	1.85
8	17.9	0.550	1.42	21	65.9	61.6	1.66
				24	64.1	58.9	1.61
				27	61.8	56.2	1.58
				30	59.2	53.3	1.57
12	21.3	0.367	1.26	21	65.9	60.1	1.35
				24	64.1	57.3	1.32
				27	61.8	54.4	1.31
				30	59.2	51.5	1.30

[1] LNA: output full scale = 4.4 V p-p differential.
[2] Filter: loss ~ 1 dB, NBW = 13.3 MHz, GAIN– = 0.8 V.
[3] ADC: 40 MSPS, 70 dB SNR, 2 V p-p full-scale input.
[4] Output dynamic range at minimum VGA gain (VGA dominated).
[5] Output dynamic range at maximum VGA gain (LNA dominated).
[6] Channel noise at maximum VGA gain.

Table 9 demonstrates the sensitivity and dynamic range of trade-offs that can be achieved relative to various LNA and VGA gain settings.

For example, when the VGA is set for the minimum gain voltage, the TGC path is dominated by VGA noise and achieves the maximum output SNR. However, as the postamp gain options are increased, the input-referred noise is reduced and the SNR is degraded.

If the VGA is set for the maximum gain voltage, the TGC path is dominated by LNA noise and achieves the lowest input-referred noise, but with degraded output SNR. The higher the TGC (LNA + VGC) gain, the lower the output SNR. As the postamp gain is increased, the input-referred noise is reduced.

At low gains, the VGA should limit the system noise performance (SNR); at high gains, the noise is defined by the source and the LNA. The maximum voltage swing is bound by the full-scale peak-to-peak ADC input voltage (2 V p-p).

Both the LNA and VGA have full-scale limitations within each section of the TGC path. These limitations are dependent on the gain setting of each function block and on the voltage applied to the GAIN+ and GAIN– pins. The LNA has three limitations, or full-scale settings, that can be applied through the SPI. Similarly, the VGA has four postamp gain settings that can be applied through the SPI. The voltage applied to the GAIN± pins determines which amplifier (the LNA or VGA) saturates first. The maximum signal input level that can be applied as a function of voltage on the GAIN± pins for the selectable gain options of the SPI is shown in Figure 48 to Figure 50.

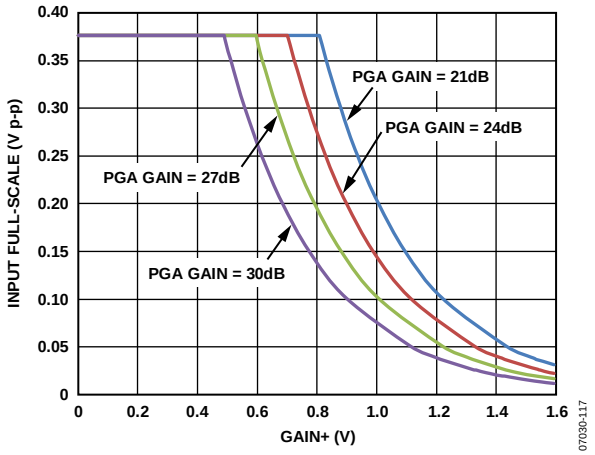


Figure 48. LNA with 15.6 dB Gain Setting/VGA Full-Scale Limitations

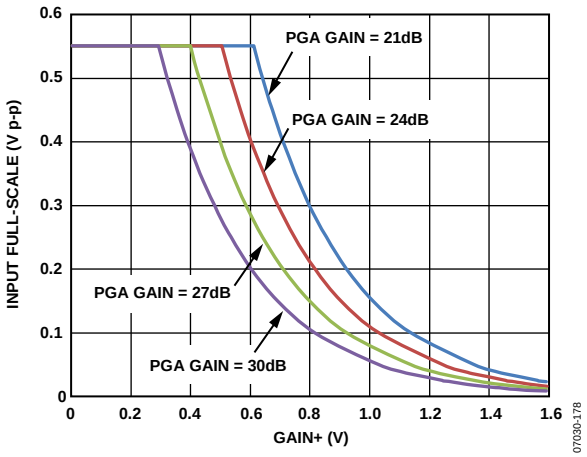


Figure 49. LNA with 17.9 dB Gain Setting/VGA Full-Scale Limitations

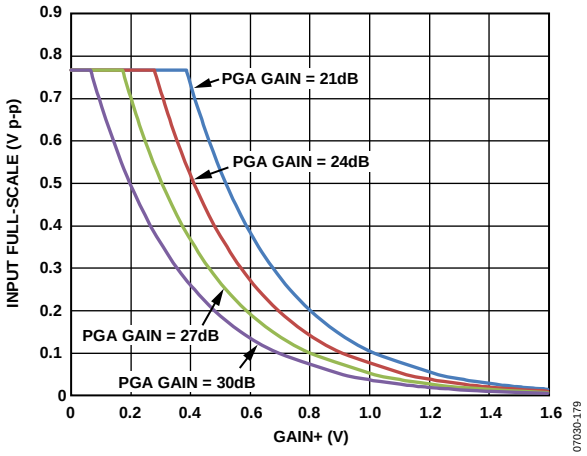


Figure 50. LNA with 21.3 dB Gain Setting/VGA Full-Scale Limitations

Variable Gain Amplifier

The differential X-AMP VGA provides precise input attenuation and interpolation. It has a low input-referred noise of 6 nV/√Hz and excellent gain linearity. A simplified block diagram is shown in Figure 51.

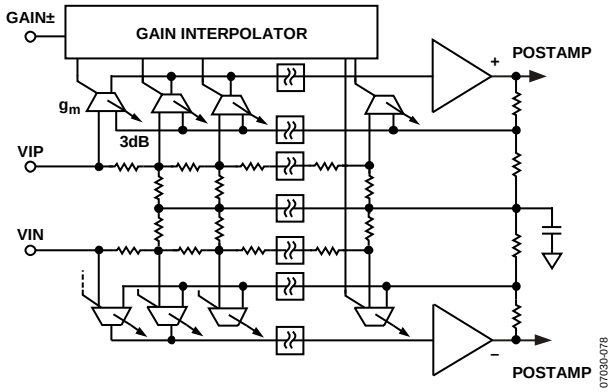


Figure 51. Simplified VGA Schematic

The input of the VGA is a 14-stage differential resistor ladder with 3.5 dB per tap. The resulting total gain range is 42 dB, which allows for range loss at the endpoints. The effective input resistance per side is 180 Ω nominally for a total differential resistance of 360 Ω. The ladder is driven by a fully differential input signal from the LNA. LNA outputs are dc-coupled to avoid external decoupling capacitors. The common-mode voltage of the attenuator and the VGA is controlled by an amplifier that uses the same midsupply voltage derived in the LNA, permitting dc coupling of the LNA to the VGA without introducing large offsets due to common-mode differences. However, any offset from the LNA becomes amplified as the gain increases, producing an exponentially increasing VGA output offset.

The input stages of the X-AMP are distributed along the ladder, and a biasing interpolator, controlled by the gain interface, determines the input tap point. With overlapping bias currents, signals from successive taps merge to provide a smooth attenuation range from −42 dB to 0 dB. This circuit technique results in linear-in-dB gain law conformance and low distortion levels—only deviating ±0.5 dB or less from the ideal. The gain slope is monotonic with respect to the control voltage and is stable with variations in process, temperature, and supply.

The X-AMP inputs are part of a programmable gain feedback amplifier that completes the VGA. Its bandwidth is approximately 100 MHz. The input stage is designed to reduce feedthrough to the output and to ensure excellent frequency response uniformity across the gain setting.

Gain Control

The gain control interface, GAIN±, is a differential input. V_{GAIN} varies the gain of all VGAs through the interpolator by selecting the appropriate input stages connected to the input attenuator. For GAIN− at 0.8 V, the nominal GAIN+ range for 28 dB/V is 0 V to 1.6 V, with the best gain linearity from about 0.16 V to 1.44 V, where the error is typically less than ±0.5 dB. For GAIN+ voltages greater than 1.44 V and less than 0.16 V, the error increases. The value of GAIN+ can exceed the supply voltage by 1 V without gain foldover.

Gain control response time is less than 750 ns to settle within 10% of the final value for a change from minimum to maximum gain.

There are two ways in which the GAIN+ and GAIN− pins can be interfaced. With the single-ended method, a Kelvin type of connection to ground can be used as shown in Figure 52. For driving multiple devices, it is preferable to use the differential method shown in Figure 53. In either method, the GAIN+ and GAIN− pins should be dc-coupled and driven to accommodate a 1.6 V full-scale input.

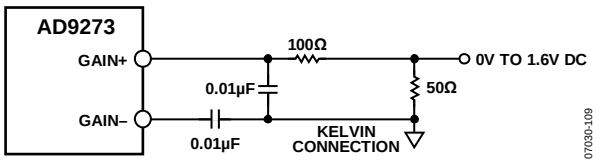


Figure 52. Single-Ended GAIN± Pins Configuration

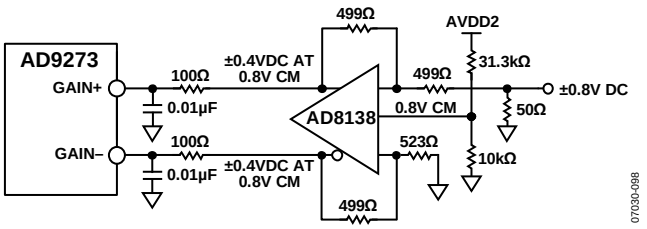


Figure 53. Differential GAIN± Pins Configuration

VGA Noise

In a typical application, a VGA compresses a wide dynamic range input signal to within the input span of an ADC. The input-referred noise of the LNA limits the minimum resolvable input signal, whereas the output-referred noise, which depends primarily on the VGA, limits the maximum instantaneous dynamic range that can be processed at any one particular gain control voltage. This latter limit is set in accordance with the total noise floor of the ADC.

Output-referred noise as a function of GAIN+ is shown in Figure 15 for the short-circuit input conditions. The input noise voltage is simply equal to the output noise divided by the measured gain at each point in the control range.

The output-referred noise is a flat 90 nV/√Hz (postamp gain = 24 dB) over most of the gain range because it is dominated by the fixed output-referred noise of the VGA. At the high end of the gain control range, the noise of the LNA and of the source prevail. The input-referred noise reaches its minimum value near the maximum gain control voltage, where the input-referred contribution of the VGA is miniscule.

At lower gains, the input-referred noise, and therefore the noise figure, increases as the gain decreases. The instantaneous dynamic range of the system is not lost, however, because the input capacity increases as the input-referred noise increases. The contribution of the ADC noise floor has the same dependence. The important relationship is the magnitude of the VGA output noise floor relative to that of the ADC.

Gain control noise is a concern in very low noise applications. Thermal noise in the gain control interface can modulate the channel gain. The resultant noise is proportional to the output signal level and is usually evident only when a large signal is present. The gain interface includes an on-chip noise filter, which significantly reduces this effect at frequencies greater than 5 MHz. Care should be taken to minimize noise impinging at the GAIN± inputs. An external RC filter can be used to remove V_{GAIN} source noise. The filter bandwidth should be sufficient to accommodate the desired control bandwidth.

Antialiasing Filter

The filter that the signal reaches prior to the ADC is used to reject dc signals and to band limit the signal for antialiasing. Figure 54 shows the architecture of the filter.

The antialaising filter is a combination of a single-pole high-pass filter and a second-order low-pass filter. The high-pass filter can be configured at a ratio of the low-pass filter cutoff. This is selectable through the SPI.

The filter uses on-chip tuning to trim the capacitors and in turn set the desired cutoff frequency and reduce variations. The default −3 dB low-pass filter cutoff is 1/3 or 1/4.5 the ADC sample clock rate. The cutoff can be scaled to 0.7, 0.8, 0.9, 1, 1.1, 1.2, or 1.3 times this frequency through the SPI. The cutoff tolerance is maintained from 8 MHz to 18 MHz.

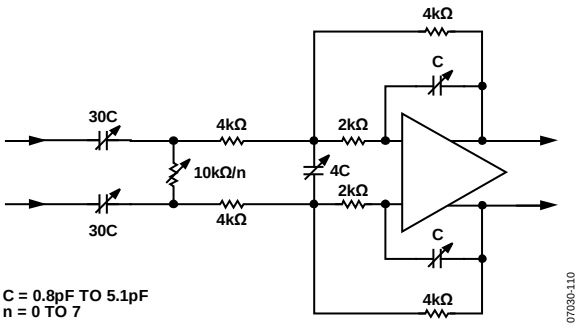


Figure 54. Simplified Filter Schematic

Tuning is normally off to avoid changing the capacitor settings during critical times. The tuning circuit is enabled and disabled through the SPI. Initializing the tuning of the filter must be performed after initial power-up and after reprogramming the filter cutoff scaling or ADC sample rate. Occasional retuning during an idle time is recommended to compensate for temperature drift.

There is a total of eight SPI-programmable settings that allow the user to vary the high-pass filter cutoff frequency as a function of the low-pass cutoff frequency. Two examples are shown in Table 10: one is for an 8 MHz low-pass cutoff frequency, and the other is for an 18 MHz low-pass cutoff frequency. In both cases, as the ratio decreases, the amount of rejection on the low-end frequencies increases. Therefore, making the entire AAF frequency pass band narrow can reduce low frequency noise or maximize dynamic range for harmonic processing.

Table 10. SPI-Selectable High-Pass Filter Cutoff Options

		High-Pass Cutoff	
SPI Setting	Ratio[1]	Low-Pass Cutoff = 8 MHz	Low-Pass Cutoff = 18 MHz
0	20.65	387 kHz	872 kHz
1	11.45	698 kHz	1.571 MHz
2	7.92	1.010 MHz	2.273 MHz
3	6.04	1.323 MHz	2.978 MHz
4	4.88	1.638 MHz	3.685 MHz
5	4.10	1.953 MHz	4.394 MHz
6	3.52	2.270 MHz	5.107 MHz
7	3.09	2.587 MHz	5.822 MHz

[1] Ratio = low-pass filter cutoff frequency/high-pass filter cutoff frequency.

ADC

The AD9273 uses a pipelined ADC architecture. The quantized output from each stage is combined into a 12-bit result in the digital correction logic. The pipelined architecture permits the first stage to operate on a new input sample and the remaining stages to operate on preceding samples. Sampling occurs on the rising edge of the clock.

The output staging block aligns the data, corrects errors, and passes the data to the output buffers. The data is then serialized and aligned to the frame and output clocks.

CLOCK INPUT CONSIDERATIONS

For optimum performance, the AD9273 sample clock inputs (CLK+ and CLK–) should be clocked with a differential signal. This signal is typically ac-coupled into the CLK+ and CLK– pins via a transformer or using capacitors. These pins are biased internally and require no additional bias.

Figure 55 shows the preferred method for clocking the AD9273. A low jitter clock source, such as the Valpey Fisher oscillator VFAC3-BHL-50MHz, is converted from single ended to differential using an RF transformer. The back-to-back Schottky diodes across the secondary transformer limit clock excursions into the AD9273 to approximately 0.8 V p-p differential. This helps prevent the large voltage swings of the clock from feeding through to other portions of the AD9273, and it preserves the fast rise and fall times of the signal, which are critical to low jitter performance.

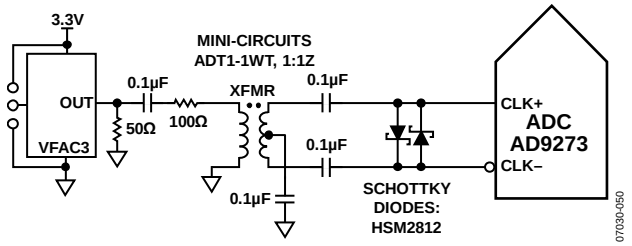
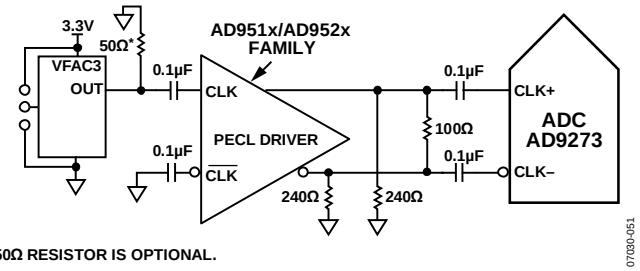


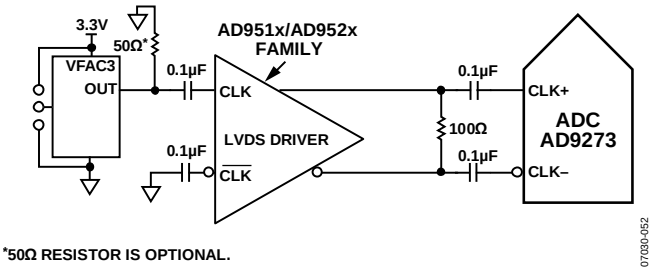
Figure 55. Transformer-Coupled Differential Clock

If a low jitter clock is available, another option is to ac-couple a differential PECL signal to the sample clock input pins as shown in Figure 56. The AD951x/AD952x family of clock drivers offers excellent jitter performance.



*50Ω RESISTOR IS OPTIONAL.

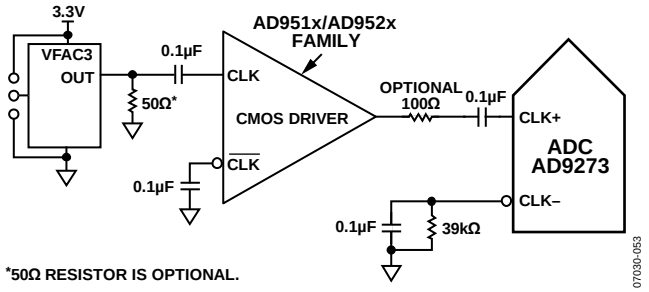
Figure 56. Differential PECL Sample Clock



*50Ω RESISTOR IS OPTIONAL.

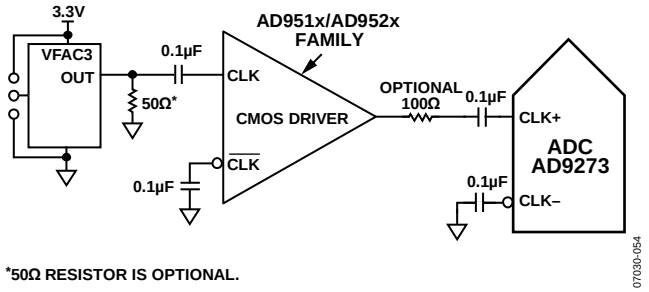
Figure 57. Differential LVDS Sample Clock

In some applications, it is acceptable to drive the sample clock inputs with a single-ended CMOS signal. In such applications, CLK+ should be driven directly from a CMOS gate, and the CLK– pin should be bypassed to ground with a 0.1 µF capacitor in parallel with a 39 kΩ resistor (see Figure 58). Although the CLK+ input circuit supply is AVDDx (1.8 V), this input is designed to withstand input voltages of up to 3.3 V, making the selection of the drive logic voltage very flexible.



*50Ω RESISTOR IS OPTIONAL.

Figure 58. Single-Ended 1.8 V CMOS Sample Clock



*50Ω RESISTOR IS OPTIONAL.

Figure 59. Single-Ended 3.3 V CMOS Sample Clock

Clock Duty Cycle Considerations

Typical high speed ADCs use both clock edges to generate a variety of internal timing signals. As a result, these ADCs may be sensitive to the clock duty cycle. Commonly, a 5% tolerance is required on the clock duty cycle to maintain dynamic performance characteristics. The AD9273 contains a duty cycle stabilizer (DCS) that retimes the nonsampling edge, providing an internal clock signal with a nominal 50% duty cycle. This allows a wide range of clock input duty cycles without affecting the performance of the AD9273. When the DCS is on, noise and distortion performance are nearly flat for a wide range of duty cycles. However, some applications may require the DCS function to be off. If so, keep in mind that the dynamic range performance can be affected when operated in this mode. See Table 17 for more details on using this feature.

The duty cycle stabilizer uses a delay-locked loop (DLL) to create the nonsampling edge. As a result, any changes to the sampling frequency require approximately eight clock cycles to allow the DLL to acquire and lock to the new rate.

Clock Jitter Considerations

High speed, high resolution ADCs are sensitive to the quality of the clock input. The degradation in SNR at a given input frequency (f_A) due only to aperture jitter (t_J) can be calculated by

$$SNR\ Degradation = 20 \times \log 10[1/2 \times \pi \times f_A \times t_J]$$

In this equation, the rms aperture jitter represents the root mean square of all jitter sources, including the clock input, analog input signal, and ADC aperture jitter. IF undersampling applications are particularly sensitive to jitter (see Figure 60).

The clock input should be treated as an analog signal in cases where aperture jitter may affect the dynamic range of the AD9273. Power supplies for clock drivers should be separated from the ADC output driver supplies to avoid modulating the clock signal with digital noise. Low jitter, crystal-controlled oscillators make the best clock sources, such as the Valpey Fisher VFAC3 series. If the clock is generated from another type of source (by gating, dividing, or other methods), it should be retimed by the original clock during the last step.

Refer to the AN-501 Application Note and the AN-756 Application Note for more in-depth information about how jitter performance relates to ADCs (visit www.analog.com).

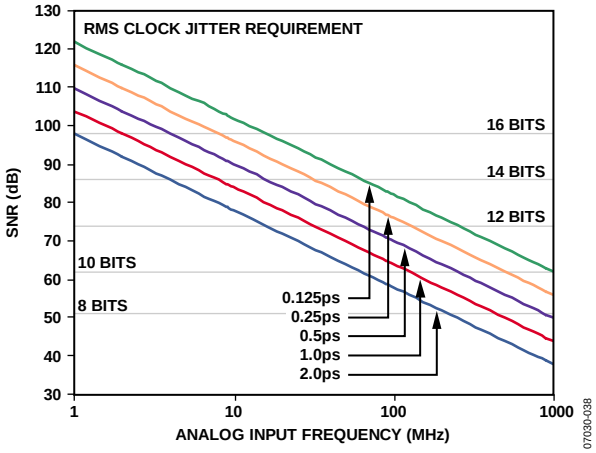


Figure 60. Ideal SNR vs. Analog Input Frequency and Jitter

Power Dissipation and Power-Down Mode

As shown in Figure 62, the power dissipated by the AD9273 is proportional to its sample rate. The digital power dissipation does not vary much because it is determined primarily by the DRVDD supply and bias current of the LVDS output drivers.

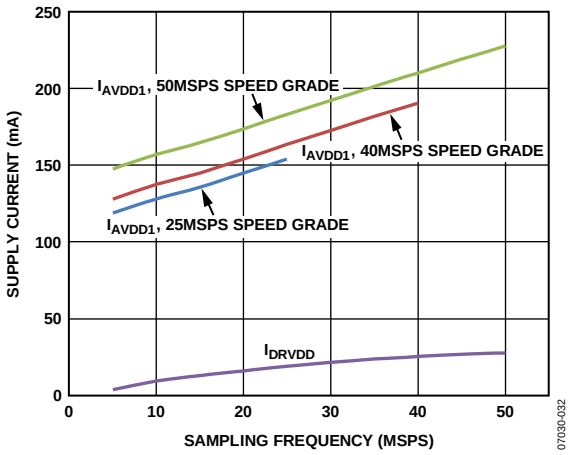


Figure 61. Supply Current vs. f_{SAMPLE} for f_{IN} = 5 MHz

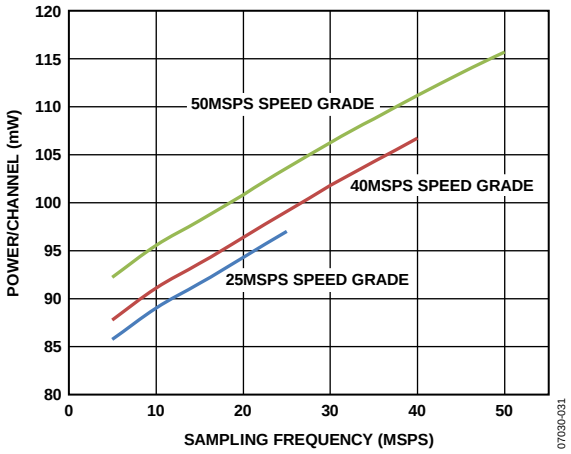


Figure 62. Power per Channel vs. f_{SAMPLE} for f_{IN} = 5 MHz

The AD9273 features scalable LNA bias currents (see Register 0x12 in Table 17). The default LNA bias current settings are high. Figure 63 shows the typical reduction of AVDD2 current with each bias setting. It is also recommended to adjust the LNA offset using Register 0x10 (see Table 17) when the LNA bias setting is low.

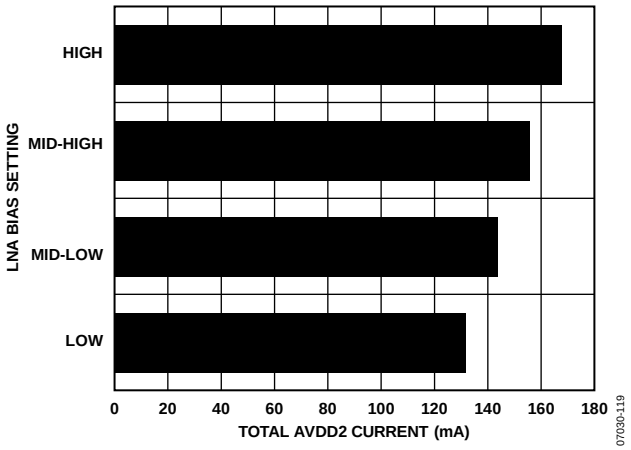


Figure 63. AVDD2 Current at Different LNA Bias Settings, AD9273-40

By asserting the PDWN pin high, the AD9273 is placed into power-down mode. In this state, the device typically dissipates 2 mW. During power-down, the LVDS output drivers are placed into a high impedance state. The AD9273 returns to normal operating mode when the PDWN pin is pulled low. This pin is both 1.8 V and 3.3 V tolerant.

By asserting the STBY pin high, the AD9273 is placed into a standby mode. In this state, the device typically dissipates 140 mW. During standby, the entire part is powered down except the internal references. The LVDS output drivers are placed into a high impedance state. This mode is well suited for applications that require power savings because it allows the device to be powered down when not in use and then quickly powered up. The time to power this device back up is also greatly reduced. The AD9273 returns to normal operating mode when the STBY pin is pulled low. This pin is both 1.8 V and 3.3 V tolerant.

In power-down mode, low power dissipation is achieved by shutting down the reference, reference buffer, PLL, and biasing networks. The decoupling capacitors on VREF are discharged when entering power-down mode and must be recharged when returning to normal operation. As a result, the wake-up time is related to the time spent in the power-down mode: shorter cycles result in proportionally shorter wake-up times. To restore the device to full operation, approximately 0.5 ms is required when using the recommended 1 µF and 0.1 µF decoupling capacitors on the VREF pin and a 0.01 µF capacitor on the GAIN± pins. Most of this time is dependent on the gain decoupling: higher value decoupling capacitors on the GAIN± pins result in longer wake-up times.

There are a number of other power-down options available when using the SPI port interface. The user can individually power down each channel or put the entire device into standby mode. This allows the user to keep the internal PLL powered up when fast wake-up times are required. The wake-up time is slightly dependent on gain. To achieve a 1 µs wake-up time when the device is in standby mode, 0.8 V must be applied to the GAIN± pins. See Table 17 for more details on using these features.

Digital Outputs and Timing

The AD9273 differential outputs conform to the ANSI-644 LVDS standard by default at power-up. This can be changed to a low power, reduced-signal option similar to the IEEE 1596.3 standard by using the SDIO pin or via the SPI. This LVDS standard can further reduce the overall power dissipation of the device by approximately 36 mW. See the SDIO Pin section or Table 17 for more information.

The LVDS driver current is derived on chip and sets the output current at each output equal to a nominal 3.5 mA. A 100 Ω differential termination resistor placed at the LVDS receiver inputs results in a nominal 350 mV swing at the receiver.

The AD9273 LVDS outputs facilitate interfacing with LVDS receivers in custom ASICs and FPGAs that have LVDS capability for superior switching performance in noisy environments. Single point-to-point net topologies are recommended with a 100 Ω termination resistor placed as close to the receiver as possible. No far-end receiver termination and poor differential trace routing may result in timing errors. It is recommended that the trace length be no longer than 24 inches and that the differential output traces be kept close together and at equal lengths. An example of the FCO, DCO, and data stream with proper trace length and position can be found in Figure 64.

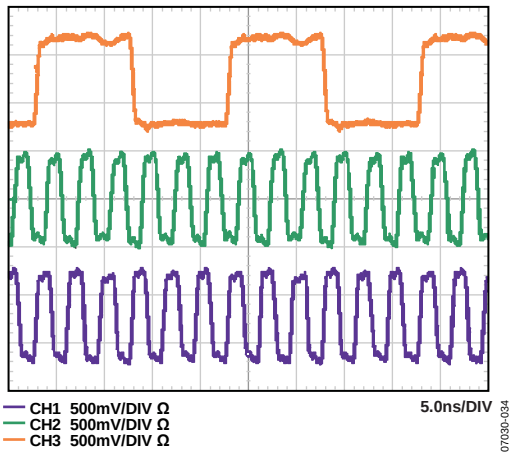


Figure 64. LVDS Output Timing Example in ANSI-644 Mode (Default)

An example of the LVDS output using the ANSI-644 standard (default) data eye and a time interval error (TIE) jitter histogram with trace lengths of less than 24 inches on regular FR-4 material is shown in Figure 65. Figure 66 shows an example of the trace lengths exceeding 24 inches on regular FR-4 material. Notice that the TIE jitter histogram reflects the decrease of the data eye opening as the edge deviates from the ideal position; therefore, the user must determine if the waveforms meet the timing budget of the design when the trace lengths exceed 24 inches.

Additional SPI options allow the user to further increase the internal termination and therefore increase the current of all eight outputs in order to drive longer trace lengths (see Figure 67). Even though this produces sharper rise and fall times on the data edges, is less prone to bit errors, and improves frequency distribution (see Figure 67), the power dissipation of the DRVDD supply increases when this option is used.

In cases that require increased driver strength to the DCO± and FCO± outputs because of load mismatch, Register 0x15 allows the user to double the drive strength. To do this, set Bit 0 in Register 0x15. Note that this feature cannot be used with Bit 4 and Bit 5 in Register 0x15 because these bits take precedence over this feature. See Table 17 for more details.

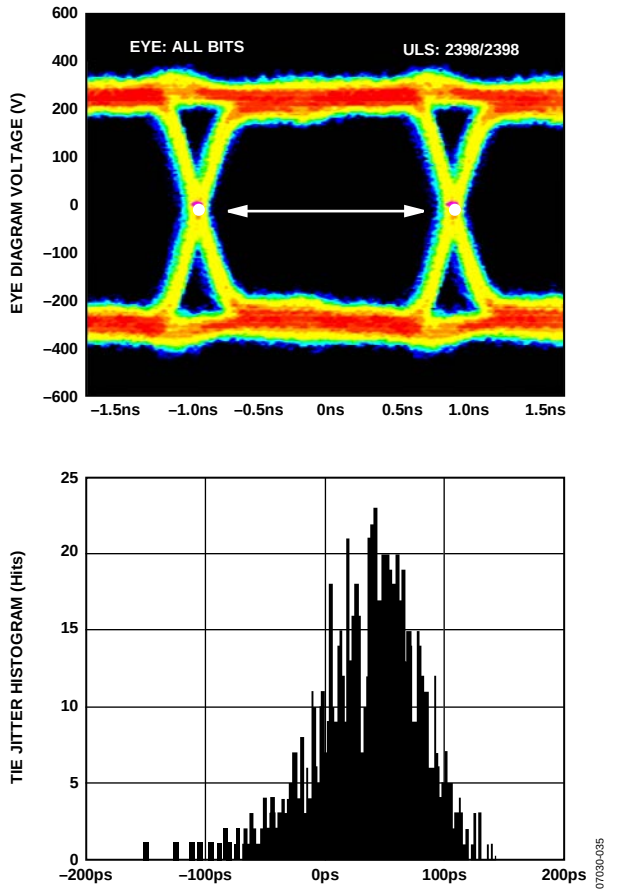


Figure 65. Data Eye for LVDS Outputs in ANSI-644 Mode with Trace Lengths of Less than 24 Inches on Standard FR-4

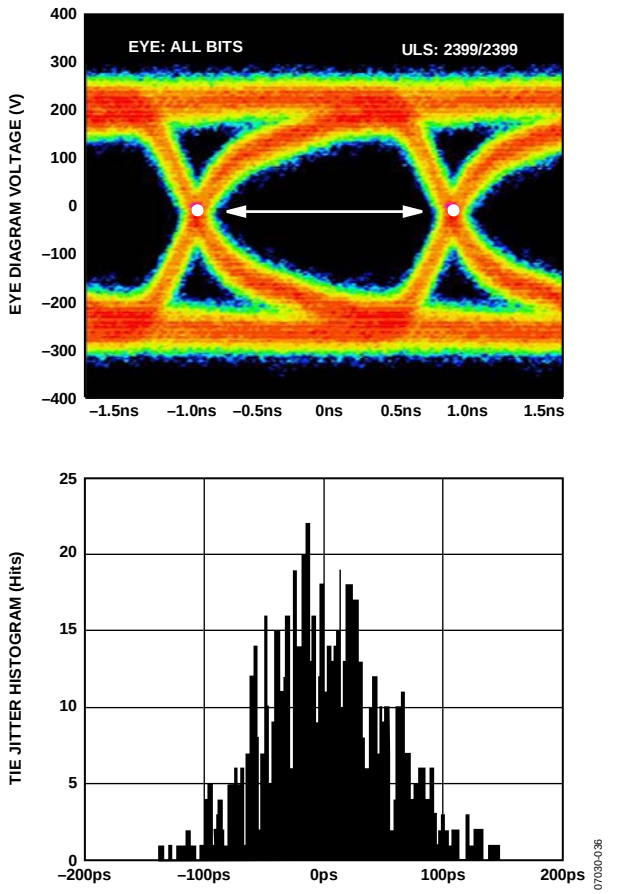


Figure 66. Data Eye for LVDS Outputs in ANSI-644 Mode with Trace Lengths of Greater than 24 Inches on Standard FR-4

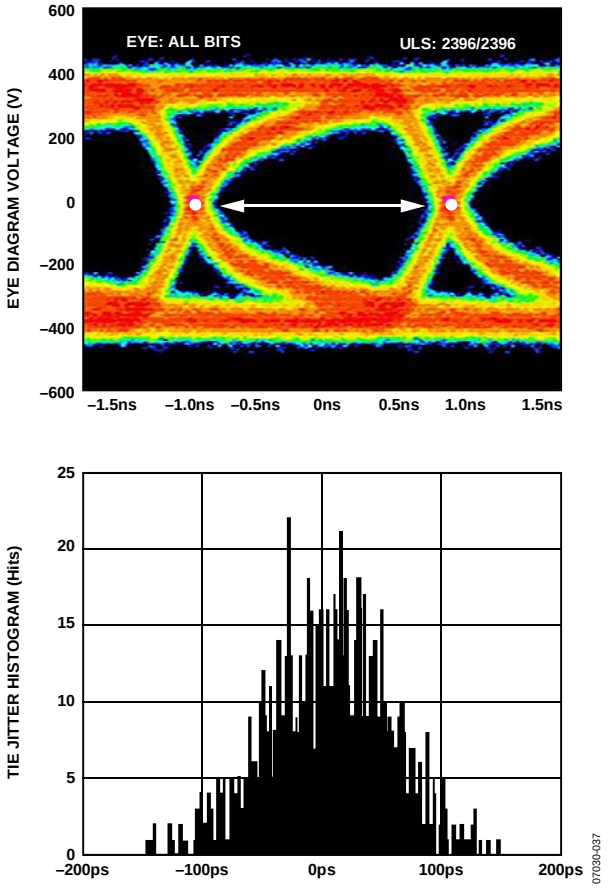


Figure 67. Data Eye for LVDS Outputs in ANSI-644 Mode with 100 Ω Termination Resistor and Trace Lengths of Greater than 24 Inches on Standard FR-4

The format of the output data is offset binary by default. An example of the output coding format can be found in Table 11. To change the output data format to twos complement, see the Memory Map section.

Table 11. Digital Output Coding

Code	(VIN+) – (VIN–), Input Span = 2 V p-p (V)	Digital Output Offset Binary (D11 ... D0)
4095	+1.00	1111 1111 1111
2048	0.00	1000 0000 0000
2047	–0.000488	0111 1111 1111
0	–1.00	0000 0000 0000

Data from each ADC is serialized and provided on a separate channel. The data rate for each serial stream is equal to 12 bits times the sample clock rate, with a maximum of 600 Mbps (12 bits × 50 MSPS = 600 Mbps). The lowest typical conversion rate is 10 MSPS, but the PLL can be set up for encode rates as low as 5 MSPS via the SPI if lower sample rates are required for a specific application. See Table 17 for details on enabling this feature.

Two output clocks are provided to assist in capturing data from the AD9273. DCO± is used to clock the output data and is equal to six times the sampling clock rate. Data is clocked out of the AD9273 and must be captured on the rising and falling edges of the DCO± that supports double data rate (DDR) capturing. The frame clock output (FCO±) is used to signal the start of a new output byte and is equal to the sampling clock rate. See the timing diagram shown in Figure 2 for more information.

Table 12. Flexible Output Test Modes

Output Test Mode Bit Sequence	Pattern Name	Digital Output Word 1	Digital Output Word 2	Subject to Data Format Select
0000	Off (default)	N/A	N/A	N/A
0001	Midscale short	1000 0000 0000	1000 0000 0000	Yes
0010	+Full-scale short	1111 1111 1111	1111 1111 1111	Yes
0011	–Full-scale short	0000 0000 0000	0000 0000 0000	Yes
0100	Checkerboard output	1010 1010 1010	0101 0101 0101	No
0101	PN sequence long	N/A	N/A	Yes
0110	PN sequence short	N/A	N/A	Yes
0111	One-/zero-word toggle	1111 1111 1111	0000 0000 0000	No
1000	User input	Register 0x19 and Register 0x1A	Register 0x1B and Register 0x1C	No
1001	1-/0-bit toggle	1010 1010 1010	N/A	No
1010	1× sync	0000 0011 1111	N/A	No
1011	One bit high	1000 0000 0000	N/A	No
1100	Mixed bit frequency	1010 0011 0011	N/A	No

When using the serial port interface (SPI), the DCO± phase can be adjusted in 60° increments relative to the data edge. This enables the user to refine system timing margins if required. The default DCO± timing, as shown in Figure 2, is 90° relative to the output data edge.

An 8-, 10-, and 14-bit serial stream can also be initiated from the SPI. This allows the user to implement different serial streams and to test the device's compatibility with lower and higher resolution systems. When changing the resolution to an 8- or 10-bit serial stream, the data stream is shortened. When using the 14-bit option, the data stream stuffs two 0s at the end of the normal 14-bit serial data.

When the SPI is used, all of the data outputs can also be inverted from their nominal state. This is not to be confused with inverting the serial stream to an LSB-first mode. In default mode, as shown in Figure 2, the MSB is represented first in the data output serial stream. However, this can be inverted so that the LSB is represented first in the data output serial stream (see Figure 3).

There are 12 digital output test pattern options available that can be initiated through the SPI. This is a useful feature when validating receiver capture and timing. Refer to Table 12 for the output bit sequencing options available. Some test patterns have two serial sequential words and can be alternated in various ways, depending on the test pattern chosen. Note that some patterns may not adhere to the data format select option. In addition, customer user patterns can be assigned in the 0x19, 0x1A, 0x1B, and 0x1C register addresses. All test mode options except PN sequence short and PN sequence long can support 8- to 14-bit word lengths in order to verify data capture to the receiver.

The PN sequence short pattern produces a pseudorandom bit sequence that repeats itself every $2^9 - 1$ bits, or 511 bits. A description of the PN sequence and how it is generated can be found in Section 5.1 of the ITU-T 0.150 (05/96) standard. The only difference is that the starting value is a specific value instead of all 1s (see Table 13 for the initial values).

The PN sequence long pattern produces a pseudorandom bit sequence that repeats itself every $2^{23} - 1$ bits, or 8,388,607 bits. A description of the PN sequence and how it is generated can be found in Section 5.6 of the ITU-T 0.150 (05/96) standard. The only differences are that the starting value is a specific value instead of all 1s and the AD9273 inverts the bit stream with relation to the ITU standard (see Table 13 for the initial values).

Table 13. PN Sequence

Sequence	Initial Value	First Three Output Samples (MSB First)
PN Sequence Short	0x0DF	0xDF9, 0x353, 0x301
PN Sequence Long	0x29B80A	0x591, 0xFD7, 0x0A3

Consult the Memory Map section for information on how to change these additional digital output timing features through the SPI.

SDIO Pin

This pin is required to operate the SPI. It has an internal 30 kΩ pull-down resistor that pulls this pin low and is only 1.8 V tolerant. If applications require that this pin be driven from a 3.3 V logic level, insert a 1 kΩ resistor in series with this pin to limit the current.

SCLK Pin

This pin is required to operate the SPI port interface. It has an internal 30 kΩ pull-down resistor that pulls this pin low and is both 1.8 V and 3.3 V tolerant.

CSB Pin

This pin is required to operate the SPI port interface. It has an internal 70 kΩ pull-up resistor that pulls this pin high and is both 1.8 V and 3.3 V tolerant.

RBIAS Pin

To set the internal core bias current of the ADC, place a resistor nominally equal to 10.0 kΩ to ground at the RBIAS pin. Using other than the recommended 10.0 kΩ resistor for RBIAS degrades the performance of the device. Therefore, it is imperative that at least a 1% tolerance on this resistor be used to achieve consistent performance.

Voltage Reference

A stable and accurate 0.5 V voltage reference is built into the AD9273. This is gained up internally by a factor of 2, setting VREF to 1.0 V, which results in a full-scale differential input span of 2.0 V p-p for the ADC. VREF is set internally by default, but the VREF pin can be driven externally with a 1.0 V reference to achieve more accuracy. However, this device does not support ADC full-scale ranges below 2.0 V p-p.

When applying the decoupling capacitors to the VREF pin, use ceramic low-ESR capacitors. These capacitors should be close to the reference pin and on the same layer of the PCB as the AD9273. The VREF pin should have both a 0.1 µF capacitor and a 1 µF capacitor connected in parallel to the analog ground. These capacitor values are recommended for the ADC to properly settle and acquire the next valid sample.

The reference settings can be selected using the SPI. The settings allow two options: using the internal reference or using an external reference. The internal reference option is the default setting and has a resulting differential span of 2 V p-p.

Table 14. SPI-Selectable Reference Settings

SPI-Selected Mode	Resulting VREF (V)	Resulting Differential Span (V p-p)
External Reference	N/A	2 × external reference
Internal Reference (Default)	1.0	2.0

Power and Ground Recommendations

When connecting power to the AD9273, it is recommended that two separate 1.8 V supplies be used: one for analog (AVDD) and one for digital (DRVDD). If only one 1.8 V supply is available, it should be routed to the AVDD1 first and then tapped off and isolated with a ferrite bead or a filter choke preceded by decoupling capacitors for the DRVDD. The user should employ several decoupling capacitors on all supplies to cover both high and low frequencies. These should be located close to the point of entry at the PC board level and close to the parts with minimal trace lengths.

A single PC board ground plane should be sufficient when using the AD9273. With proper decoupling and smart partitioning of the PC board's analog, digital, and clock sections, optimum performance can be achieved easily.

Exposed Paddle Thermal Heat Slug Recommendations

It is required that the exposed paddle on the underside of the device be connected to a quiet analog ground to achieve the best electrical and thermal performance of the AD9273. An exposed continuous copper plane on the PCB should mate to the AD9273 exposed paddle, Pin 0. The copper plane should have several vias to achieve the lowest possible resistive thermal path for heat dissipation to flow through the bottom of the PCB. These vias should be filled or plugged with nonconductive epoxy.

To maximize the coverage and adhesion between the device and PCB, partition the continuous copper pad by overlaying a silkscreen or solder mask to divide this into several uniform sections. This ensures several tie points between the two during the reflow process. Using one continuous plane with no partitions only guarantees one tie point between the AD9273 and PCB. See Figure 68 for a PCB layout example. For more detailed information on packaging and for more PCB layout examples, see the AN-772 Application Note.

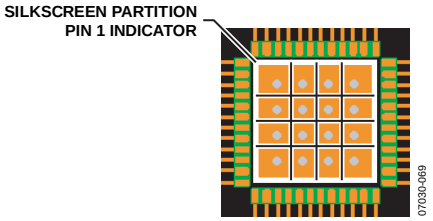


Figure 68. Typical PCB Layout

SERIAL PORT INTERFACE (SPI)

The AD9273 serial port interface allows the user to configure the signal chain for specific functions or operations through a structured register space provided inside the chip. This offers the user added flexibility and customization depending on the application. Addresses are accessed via the serial port and can be written to or read from via the port. Memory is organized into bytes that can be further divided down into fields, as documented in the Memory Map section. Detailed operational information can be found in the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*.

There are three pins that define the serial port interface (SPI): the SCLK, SDIO, and CSB pins. The SCLK (serial clock) is used to synchronize the read and write data presented to the device. The SDIO (serial data input/output) is a dual-purpose pin that allows data to be sent to and read from the device's internal memory map registers. The CSB (chip select bar) is an active low control that enables or disables the read and write cycles (see Table 15).

Table 15. Serial Port Pins

Pin	Function
SCLK	Serial clock. The serial shift clock input. SCLK is used to synchronize serial interface reads and writes.
SDIO	Serial data input/output. A dual-purpose pin. The typical role for this pin is as an input or output, depending on the instruction sent and the relative position in the timing frame.
CSB	Chip select bar (active low). This control gates the read and write cycles.

The falling edge of the CSB in conjunction with the rising edge of the SCLK determines the start of the framing sequence. During an instruction phase, a 16-bit instruction is transmitted, followed by one or more data bytes, which is determined by Bit Field W0 and Bit Field W1. An example of the serial timing and its definitions can be found in Figure 70 and Table 16.

During normal operation, CSB is used to signal to the device that SPI commands are to be received and processed. When CSB is brought low, the device processes SCLK and SDIO to process instructions. Normally, CSB remains low until the communication cycle is complete. However, if connected to a slow device, CSB can be brought high between bytes, allowing older microcontrollers enough time to transfer data into shift registers. CSB can be stalled when transferring one, two, or three bytes of data. When W0 and W1 are set to 11, the device enters streaming mode and continues to process data, either reading or writing, until CSB is taken high to end the communication cycle. This allows complete memory transfers without having to provide additional instructtions. Regardless of the mode, if CSB is taken high in the middle of any byte transfer, the SPI state machine is reset and the device waits for a new instruction.

In addition to the operation modes, the SPI port can be configured to operate in different manners. For applications that do not require a control port, the CSB line can be tied and held high. This places the remainder of the SPI pins in their secondary mode, as defined in the SDIO Pin and SCLK Pin sections. CSB can also be tied low to enable 2-wire mode. When CSB is tied low, SCLK and SDIO are the only pins required for communication. Although the device is synchronized during power-up, caution must be exercised when using this mode to ensure that the serial port remains synchronized with the CSB line. When operating in 2-wire mode, it is recommended to use a 1-, 2-, or 3-byte transfer exclusively. Without an active CSB line, streaming mode can be entered but not exited.

In addition to word length, the instruction phase determines if the serial frame is a read or write operation, allowing the serial port to be used to both program the chip and read the contents of the on-chip memory. If the instruction is a readback operation, performing a readback causes the serial data input/output (SDIO) pin to change direction from an input to an output at the appropriate point in the serial frame.

Data can be sent in MSB- or LSB-first mode. MSB-first mode is the default at power-up and can be changed by adjusting the configuration register. For more information about this and other features, see the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*.

HARDWARE INTERFACE

The pins described in Table 15 constitute the physical interface between the user's programming device and the serial port of the AD9273. The SCLK and CSB pins function as inputs when using the SPI interface. The SDIO pin is bidirectional, functioning as an input during write phases and as an output during readback.

In cases where multiple SDIO pins share a common connection, care should be taken to ensure that proper V_{OH} levels are met. Figure 69 shows the number of SDIO pins that can be connected together, assuming the same load as the AD9273, as well as the resulting V_{OH} level.

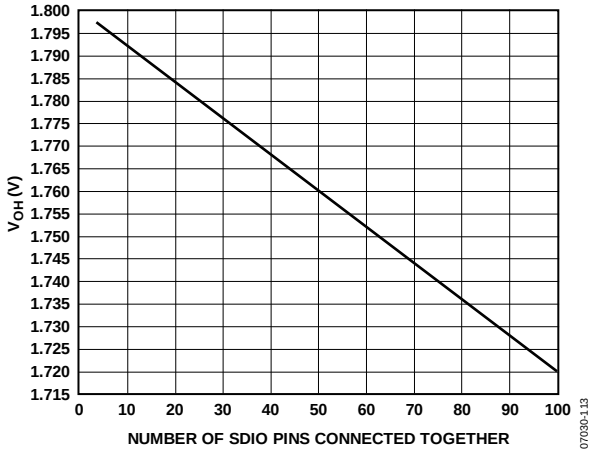


Figure 69. SDIO Pin Loading

This interface is flexible enough to be controlled by either serial PROMS or PIC mirocontrollers. This provides the user with an alternative method, other than a full SPI controller, for programming the device (see the AN-812 Application Note).

If the user chooses not to use the SPI interface, these pins serve a dual function and are associated with secondary functions when the CSB is strapped to AVDD during device power-up. See the SDIO Pin and SCLK Pin sections for details on which pin-strappable functions are supported on the SPI pins.

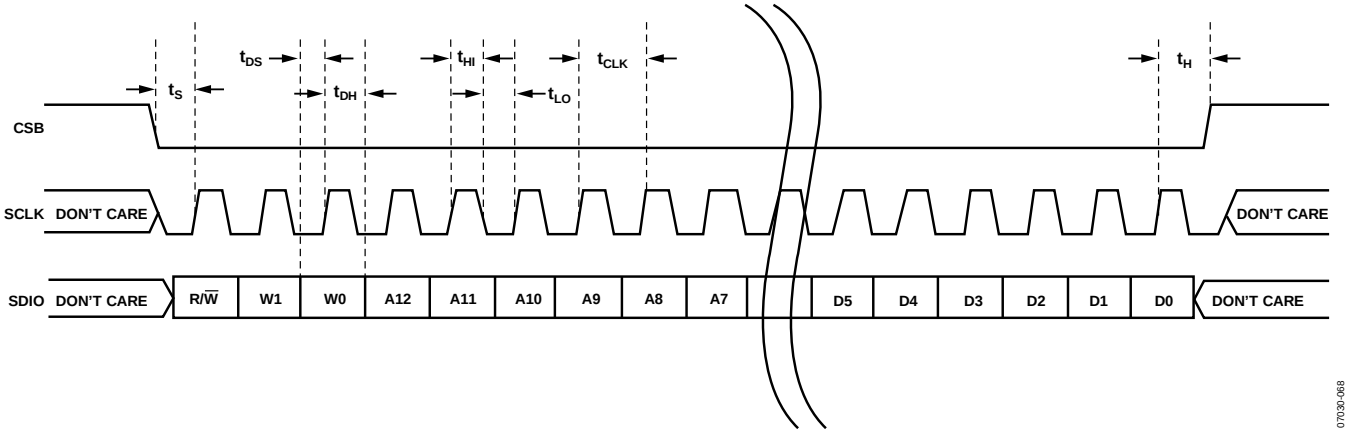


Figure 70. Serial Timing Details

Table 16. Serial Timing Definitions

Parameter	Minimum Timing (ns)	Description
t_{DS}	5	Setup time between the data and the rising edge of SCLK
t_{DH}	2	Hold time between the data and the rising edge of SCLK
t_{CLK}	40	Period of the clock
t_S	5	Setup time between CSB and SCLK
t_H	2	Hold time between CSB and SCLK
t_{HI}	16	Minimum period that SCLK should be in a logic high state
t_{LO}	16	Minimum period that SCLK should be in a logic low state
t_{EN_SDIO}	10	Minimum time for the SDIO pin to switch from an input to an output relative to the SCLK falling edge (not shown in Figure 70)
t_{DIS_SDIO}	10	Minimum time for the SDIO pin to switch from an output to an input relative to the SCLK rising edge (not shown in Figure 70)

MEMORY MAP

READING THE MEMORY MAP TABLE

Each row in the memory map table has eight address locations. The memory map is roughly divided into three sections: the chip configuration register map (Address 0x00 to Address 0x02), the device index and transfer register map (Address 0x04 to Address 0xFF), and the ADC functions register map (Address 0x08 to Address 0x2D).

The leftmost column of the memory map indicates the register address number, and the default value is shown in the second rightmost column. The Bit 7 (MSB) column is the start of the default hexadecimal value given. For example, Address 0x09, the clock register, has a default value of 0x01, meaning that Bit 7 = 0, Bit 6 = 0, Bit 5 = 0, Bit 4 = 0, Bit 3 = 0, Bit 2 = 0, Bit 1 = 0, and Bit 0 = 1, or 0000 0001 in binary. This setting is the default for the duty cycle stabilizer in the on condition. By writing a 0 to Bit 0 of this address followed by an 0x01 to the SW transfer bit in Register 0xFF, the duty cycle stabilizer turns off. It is important to follow each writing sequence with a write to the SW transfer bit to update the SPI registers.

Caution

All registers except Register 0x00, Register 0x02, Register 0x04, Register 0x05, and Register 0xFF are buffered with a master slave latch and require writing to the transfer bit. For more information on this and other functions, consult the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*.

RESERVED LOCATIONS

Undefined memory locations should not be written to except when writing the default values suggested in this data sheet. Addresses that have values marked as 0 should be considered reserved and have a 0 written into their registers during power-up.

DEFAULT VALUES

After a reset, critical registers are automatically loaded with default values. These values are indicated in Table 17, where an X refers to an undefined feature.

LOGIC LEVELS

An explanation of various registers follows: "bit is set" is synonymous with "bit is set to Logic 1" or "writing Logic 1 for the bit." Similarly, "clear a bit" is synonymous with "bit is set to Logic 0" or "writing Logic 0 for the bit."

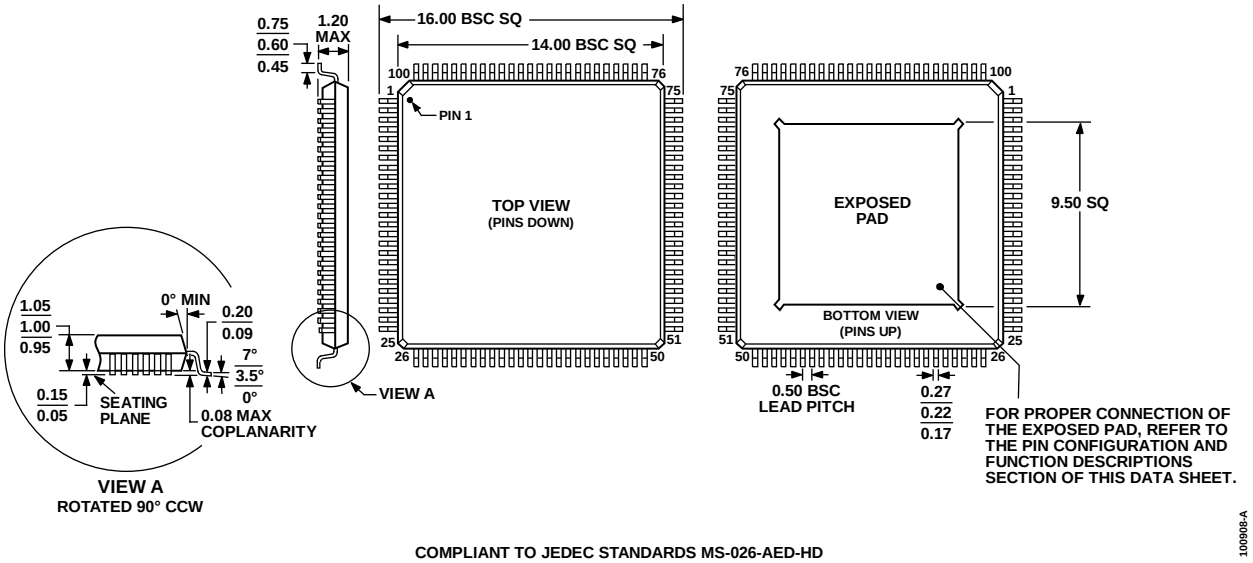
Table 17. AD9273 Memory Map Register

Addr. (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value	Default Notes/ Comments
Chip Configuration Registers											
00	CHIP_PORT_CONFIG	0	LSB first 1 = on 0 = off (default)	Soft reset 1 = on 0 = off (default)	1	1	Soft reset 1 = on 0 = off (default)	LSB first 1 = on 0 = off (default)	0	0x18	The nibbles should be mirrored so that LSB- or MSB-first mode is set correctly regardless of shift mode.
01	CHIP_ID	Chip ID Bits[7:0] (AD9273 = 0x2F, default)								Read only	Default is unique chip ID, different for each device. This is a read-only register.
02	CHIP_GRADE	X	X	Child ID[5:4] (identify device variants of Chip ID) 00 = 40 MSPS (default) 01 = 25 MSPS 10 = 50 MSPS		X	X	X	X	0x00	Child ID used to differentiate graded devices.
Device Index and Transfer Registers											
04	DEVICE_INDEX_2	X	X	X	X	Data Channel H 1 = on (default) 0 = off	Data Channel G 1 = on (default) 0 = off	Data Channel F 1 = on (default) 0 = off	Data Channel E 1 = on (default) 0 = off	0x0F	Bits are set to determine which on-chip device receives the next write command.
05	DEVICE_INDEX_1	X	X	Clock Channel DCO± 1 = on 0 = off (default)	Clock Channel FCO± 1 = on 0 = off (default)	Data Channel D 1 = on (default) 0 = off	Data Channel C 1 = on (default) 0 = off	Data Channel B 1 = on (default) 0 = off	Data Channel A 1 = on (default) 0 = off	0x0F	Bits are set to determine which on-chip device receives the next write command.
FF	DEVICE_UPDATE	X	X	X	X	X	X	X	SW transfer 1 = on 0 = off (default)	0x00	Synchronously transfers data from the master shift register to the slave.
ADC Functions Registers											
08	Modes	X	X	X	X	0	Internal power-down mode 000 = chip run (default) 001 = full power-down 010 = standby 011 = reset 100 = CW mode (TGC PDWN)			0x00	Determines various generic modes of chip operation (global).
09	Clock	X	X	X	X	X	X	X	Duty cycle stabilizer 1 = on (default) 0 = off	0x01	Turns the internal duty cycle stabilizer on and off (global).
0D	TEST_IO	User test mode 00 = off (default) 01 = on, single alternate 10 = on, single once 11 = on, alternate once		Reset PN long gen 1 = on 0 = off (default)	Reset PN short gen 1 = on 0 = off (default)	Output test mode—see Table 12 0000 = off (default) 0001 = midscale short 0010 = +FS short 0011 = –FS short 0100 = checkerboard output 0101 = PN sequence long 0110 = PN sequence short 0111 = one-/zero-word toggle 1000 = user input 1001 = 1-/0-bit toggle 1010 = 1× sync 1011 = one bit high 1100 = mixed bit frequency (format determined by the OUTPUT_MODE register)				0x00	When this register is set, the test data is placed on the output pins in place of normal data. (Local, expect for PN sequence.)

Addr. (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value	Default Notes/ Comments
0F	FLEX_CHANNEL_ INPUT	Filter cutoff frequency control 0000 = 1.3 × 1/3 × f_{SAMPLE} 0001 = 1.2 × 1/3 × f_{SAMPLE} 0010 = 1.1 × 1/3 × f_{SAMPLE} 0011 = 1.0 × 1/3 × f_{SAMPLE} (default) 0100 = 0.9 × 1/3 × f_{SAMPLE} 0101 = 0.8 × 1/3 × f_{SAMPLE} 0110 = 0.7 × 1/3 × f_{SAMPLE} 1000 = 1.3 × 1/4.5 × f_{SAMPLE} 1001 = 1.2 × 1/4.5 × f_{SAMPLE} 1010 = 1.1 × 1/4.5 × f_{SAMPLE} 1011 = 1.0 × 1/4.5 × f_{SAMPLE} 1100 = 0.9 × 1/4.5 × f_{SAMPLE} 1101 = 0.8 × 1/4.5 × f_{SAMPLE} 1110 = 0.7 × 1/4.5 × f_{SAMPLE}				X	X	X	X	0x30	Antialiasing filter cutoff (global).
10	FLEX_OFFSET	X	X	6-bit LNA offset adjustment 10 0000 = LNA bias high, mid-high, mid-low (default) 10 0001 = LNA bias low						0x20	LNA force offset correction (local).
11	FLEX_GAIN	X	X	X	X	PGA gain 00 = 21 dB 01 = 24 dB (default) 10 = 27 dB 11 = 30 dB		LNA gain 00 = 15.6 dB 01 = 17.9 dB 10 = 21.3 dB (default)		0x06	LNA and PGA gain adjustment (global).
12	BIAS_CURRENT	X	X	X	X	1	X	LNA bias 00 = high 01 = mid-high (default) 10 = mid-low 11 = low		0x08	LNA bias current adjustment (global).
14	OUTPUT_MODE	X	0 = LVDS ANSI-644 (default) 1 = LVDS low power, (IEEE 1596.3 similar)	X	X	X	Output invert 1 = on 0 = off (default)	00 = offset binary (default) 01 = twos complement		0x00	Configures the outputs and the format of the data (Bits[7:3] and Bits[1:0] are global; Bit 2 is local).
15	OUTPUT_ADJUST	X	X	Output driver termination 00 = none (default) 01 = 200 Ω 10 = 100 Ω 11 = 100 Ω		X	X	X	DCO± and FCO± 2× drive strength 1 = on 0 = off (default)	0x00	Determines LVDS or other output properties. Primarily functions to set the LVDS span and common-mode levels in place of an external resistor (Bits[7:1] are global; Bit 0 is local).
16	OUTPUT_PHASE	X	X	X	X	0011 = output clock phase adjust (0000 through 1010) 0000 = 0° relative to data edge 0001 = 60° relative to data edge 0010 = 120° relative to data edge 0011 = 180° relative to data edge (default) 0100 = 240° relative to data edge 0101 = 300° relative to data edge 0110 = 360° relative to data edge 0111 = 420° relative to data edge 1000 = 480° relative to data edge 1001 = 540° relative to data edge 1010 = 600° relative to data edge 1011 to 1111 = 660° relative to data edge				0x03	On devices that utilize global clock divide, determines which phase of the divider output is used to supply the output clock. Internal latching is unaffected.
18	FLEX_VREF	X	0 = internal reference 1 = external reference	X	X	X	X	X	X	0x00	Select internal reference (recommended default) or external reference (global).

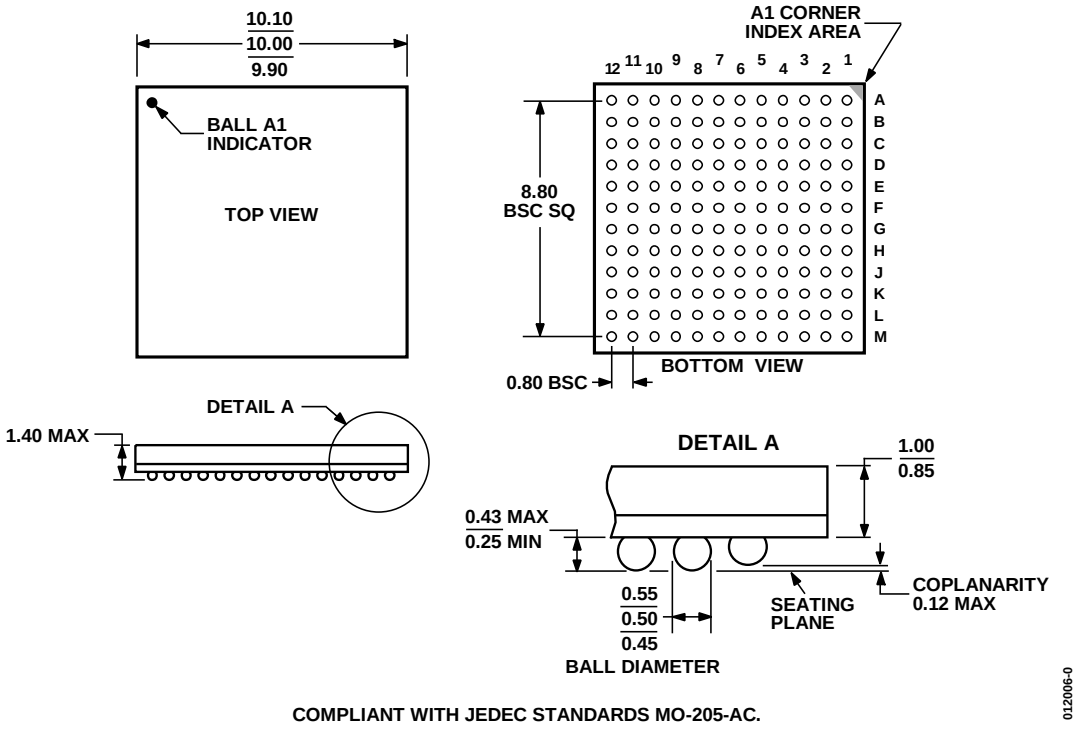
Addr. (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value	Default Notes/ Comments
19	USER_PATT1_LSB	B7	B6	B5	B4	B3	B2	B1	B0	0x00	User-defined pattern, 1 LSB (global).
1A	USER_PATT1_MSB	B15	B14	B13	B12	B11	B10	B9	B8	0x00	User-defined pattern, 1 MSB (global).
1B	USER_PATT2_LSB	B7	B6	B5	B4	B3	B2	B1	B0	0x00	User-defined pattern, 2 LSB (global).
1C	USER_PATT2_MSB	B15	B14	B13	B12	B11	B10	B9	B8	0x00	User-defined pattern, 2 MSB (global).
21	SERIAL_CONTROL	LSB first 1 = on 0 = off (default)	X	X	X	<10 MSPS, low encode rate mode 1 = on 0 = off (default)	000 = 12 bits (default, normal bit stream) 001 = 8 bits 010 = 10 bits 011 = 12 bits 100 = 14 bits			0x00	Serial stream control. Default causes MSB first and the native bit stream (global).
22	SERIAL_CH_STAT	X	X	X	X	X	X	Channel output reset 1 = on 0 = off (default)	Channel power-down 1 = on 0 = off (default)	0x00	Used to power down individual sections of a converter (local).
2B	FLEX_FILTER	X	Enable automatic low-pass tuning 1 = on (self-clearing)	X	X	High-pass filter cutoff 0000 = f_{LP}/20.7 0001 = f_{LP} /11.5 0010 = f_{LP} /7.9 0011 = f_{LP} /6.0 0100 = f_{LP} /4.9 0101 = f_{LP} /4.1 0110 = f_{LP} /3.5 0111 = f_{LP} /3.1				0x00	Filter cutoff (global). (f_{LP} = low-pass filter cutoff frequency.)
2C	ANALOG_INPUT	X	X	X	X	X	X	LOSW-x connect 00 = high-Z 01 = (–)LNA output 10 = (+)LNA output 11 = high-Z		0x00	LNA active termination/input impedance (global).
2D	CROSS_POINT_ SWITCH	X	X	Crosspoint switch enable 10 0000 = CWD0± (differential) 10 0001 = CWD1± (differential) 10 0010 = CWD2± (differential) 10 0011 = CWD3± (differential) 10 0100 = CWD4± (differential) 10 0101 = CWD5± (differential) 10 0110 = CWD6± (differential) 10 0111 = CWD7± (differential) 11 0000 = CWD0+ (single ended) 11 0001 = CWD1+ (single ended) 11 0010 = CWD2+ (single ended) 11 0011 = CWD3+ (single ended) 11 0100 = CWD4+ (single ended) 11 0101 = CWD5+ (single ended) 11 0110 = CWD6+ (single ended) 11 0111 = CWD7+ (single ended) 11 1000 = CWD0– (single ended) 11 1001 = CWD1– (single ended) 11 1010 = CWD2– (single ended) 11 1011 = CWD3– (single ended) 11 1100 = CWD4– (single ended) 11 1101 = CWD5– (single ended) 11 1110 = CWD6– (single ended) 11 1111 = CWD7– (single ended) 0x xxxx = power down CW channel (default)								0x00	Crosspoint switch enable (local).

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-026-AED-HD

Figure 71. 100-Lead Thin Quad Flat Package, Exposed Pad [TQFP_EP]
(SV-100-3)
Dimensions shown in millimeters



COMPLIANT WITH JEDEC STANDARDS MO-205-AC.

Figure 72. 144-Ball Chip Scale Package, Ball Grid Array [CSP_BGA]
(BC-144-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD9273BSVZ-50[1]	−40°C to +85°C	100-Lead Thin Quad Flat Package, Exposed Pad [TQFP_EP]	SV-100-3
AD9273BSVZRL-50[1]	−40°C to +85°C	100-Lead Thin Quad Flat Package, Exposed Pad [TQFP_EP] Tape and Reel	SV-100-3
AD9273BSVZ-40[1]	−40°C to +85°C	100-Lead Thin Quad Flat Package, Exposed Pad [TQFP_EP]	SV-100-3
AD9273BSVZRL-40[1]	−40°C to +85°C	100-Lead Thin Quad Flat Package, Exposed Pad [TQFP_EP] Tape and Reel	SV-100-3
AD9273BSVZ-25[1]	−40°C to +85°C	100-Lead Thin Quad Flat Package, Exposed Pad [TQFP_EP]	SV-100-3
AD9273BSVZRL-25[1]	−40°C to +85°C	100-Lead Thin Quad Flat Package, Exposed Pad [TQFP_EP] Tape and Reel	SV-100-3
AD9273BBCZ-25[1]	−40°C to +85°C	144-Ball Chip Scale Package, Ball Grid Array [CSP_BGA]	BC-144-1
AD9273BBCZ-40[1]	−40°C to +85°C	144-Ball Chip Scale Package, Ball Grid Array [CSP_BGA]	BC-144-1
AD9273BBCZ-50[1]	−40°C to +85°C	144-Ball Chip Scale Package, Ball Grid Array [CSP_BGA]	BC-144-1
AD9273-50EBZ[1]		Evaluation Board, 100-Lead Thin Quad Flat Package, Exposed Pad [TQFP_EP]	

[1] Z = RoHS Compliant Part.

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