TABLE OF CONTENTS

REVISION HISTORY

8/07—Rev. A to Rev. B

Updated Format ..... Universal
Changes to Applications 1
Changes to General Description 1
Changes to Specifications 3
Changes to the Absolute Maximum Ratings Section 5
Changes to the Applications Information Section 9
Deleted Spice Model Section 11
Updated Outline Dimensions 12
Changes to Ordering Guide 13

6/99—Rev. 0 to Rev. A

SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

V_{+ANA} = V_{+DIG} = 5.0 V, V_{-ANA} = 0 V, T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			2.3	7	mV
		−40°C ≤ T_A ≤ +125°C[1]			8	mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			4		µV/°C
Input Bias Current	I_B	V_{CM} = 0 V			±4	µA
		−40°C ≤ T_A ≤ +125°C[1]			±9	µA
Input Offset Current	I_{OS}	V_{CM} = 0 V			±3	µA
Input Common-Mode Voltage Range	V_{CM}		0		2.75	V
Common-Mode Rejection Ratio	CMRR	0 V ≤ V_{CM} ≤ 3.0 V	65	85		dB
Large Signal Voltage Gain	A_{VO}	R_L = 10 kΩ		3000		V/V
Input Capacitance	C_{IN}			3.0		pF
DIGITAL OUTPUTS						
Logic 1 Voltage	V_{OH}	I_{OH} = −3.2 mA, ΔV_{IN} > 250 mV	2.4	3.5		V
Logic 0 Voltage	V_{OL}	I_{OL} = 3.2 mA, V_{IN} > 250 mV		0.3	0.4	V
DYNAMIC PERFORMANCE[2]						
Propagation Delay	t_P	200 mV step with 100 mV overdrive		6.75	9.8	ns
		−40°C ≤ T_A ≤ +125°C[1]			13	ns
		100 mV step with 5 mV overdrive		8		ns
Differential Propagation Delay (Rising Propagation Delay vs. Falling Propagation Delay)	Δt_P	100 mV step with 20 mV overdrive		0.5	2.0	ns
Rise Time		20% to 80%		3.8		ns
Fall Time		20% to 80%		1.5		ns
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	4.5 V ≤ V_{+ANA} and V_{+DIG} ≤ 5.5 V		80		dB
Analog Supply Current	I_{+ANA}			10.5	14.0	mA
		−40°C ≤ T_A ≤ +85°C[1]			15.6	mA
		−40°C ≤ T_A ≤ +125°C[1]			17	mA
Digital Supply Current	I_{DIG}	V_O = 0 V, R_L = ∞		6.0	7.0	mA
		−40°C ≤ T_A ≤ +125°C[1]			8.0	mA
Analog Supply Current	I_{-ANA}			−7.0	+14.0	mA
		−40°C ≤ T_A ≤ +85°C[1]			15.6	mA
		−40°C ≤ T_A ≤ +125°C[1]			17	mA

[1] Full electrical specifications to −55°C, but these package types are guaranteed for operation from −40°C to +125°C only. Package reliability below −40°C is not guaranteed.
[2] Guaranteed by design.

V_{+ANA} = V_{+DIG} = 5.0 V, V_{-ANA} = −5 V, T_A = 25°C, unless otherwise noted.

Table 2.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			2.3	7	mV
		−40°C ≤ T_A ≤ +125°C[1]			10	mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			4		µV/°C
Input Bias Current	I_B	V_{CM} = 0 V			±4	µA
		−40°C ≤ T_A ≤ +125°C[1]			±9	µA
Input Offset Current	I_{OS}	V_{CM} = 0 V			±3	µA
Input Common-Mode Voltage Range	V_{CM}		−4.9		+3.5	V
Common-Mode Rejection Ratio	CMRR	0 V ≤ V_{CM} ≤ 3.0 V	65	85		dB
Large Signal Voltage Gain	A_{VO}	R_L = 10 kΩ		3000		V/V
Input Capacitance	C_{IN}			3.0		pF
DIGITAL OUTPUTS						
Logic 1 Voltage	V_{OH}	I_{OH} = −3.2 mA, ΔV_{IN} > +250 mV	2.6	3.6		V
Logic 0 Voltage	V_{OL}	I_{OL} = 3.2 mA, ΔV_{IN} > 250 mV		0.2	0.3	V
DYNAMIC PERFORMANCE[2]						
Propagation Delay	t_P	200 mV step with 100 mV overdrive		6.75	9.8	ns
		−40°C ≤ T_A ≤ +85°C[1]		8	13	ns
		100 mV step with 5 mV overdrive		8		ns
Differential Propagation Delay (Rising Propagation Delay vs. Falling Propagation Delay)	Δt_P	100 mV step with 20 mV overdrive		0.5	2.0	ns
Rise Time		20% to 80%		3		ns
Fall Time		20% to 80%		3		ns
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	4.5 V ≤ V_{+ANA} and V_{+DIG} ≤ 5.5 V	50	70		dB
Analog Supply Current	I_{+ANA}			10.8	14.0	mA
		−40°C ≤ T_A ≤ +85°C[1]			15.6	mA
		−40°C ≤ T_A ≤ +125°C[1]			17	mA
Digital Supply Current	I_{DIG}	V_O = 0 V, R_L = ∞		3.6	4.4	mA
		−40°C ≤ T_A ≤ +125°C[1]			5.6	mA
Analog Supply Current	I_{-ANA}			−8.2	+14.0	mA
		−40°C ≤ T_A ≤ +85°C[1]			15.6	mA
		−40°C ≤ T_A ≤ +125°C[1]			17	mA

[1] Full electrical specifications to −55°C, but these package types are guaranteed for operation from −40°C to +125°C only. Package reliability below −40°C is not guaranteed.
[2] Guaranteed by design.

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Total Analog Supply Voltage	14 V
Digital Supply Voltage	17 V
Analog Positive Supply to Digital Positive Supply	−600 mV
Input Voltage[1]	±7 V
Differential Input Voltage	±8 V
Output Short-Circuit Duration to GND	Indefinite
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−55°C to +125°C
Junction Temperature Range	−65°C to +150°C
Lead Temperature Range (Soldering, 10 sec)	300°C

[1] The analog input voltage is equal to ±7 V or the analog supply voltage, whichever is less.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages (SOIC and TSSOP). θ_{JA} is specified for device in socket for PDIP.

Table 4. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
16-Lead PDIP (N)	90	47	°C/W
16-Lead Narrow Body SOIC (R)	113	37	°C/W
16-Lead TSSOP (RU)	180	37	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

$V_{+ANA} = V_{+DIG} = 5$ V, $V_{-ANA} = 0$ V, $T_A = 25°C$, unless otherwise noted.

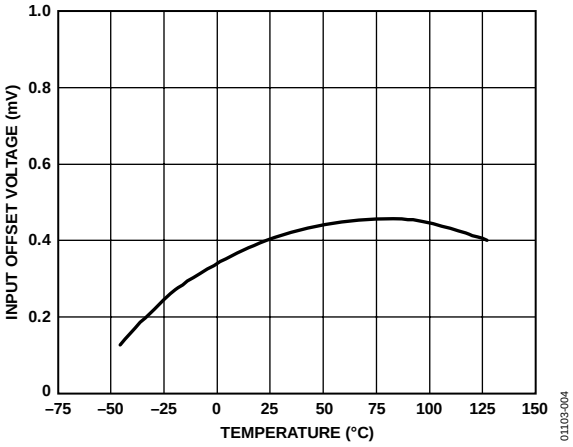


Figure 4. Input Offset Voltage vs. Temperature

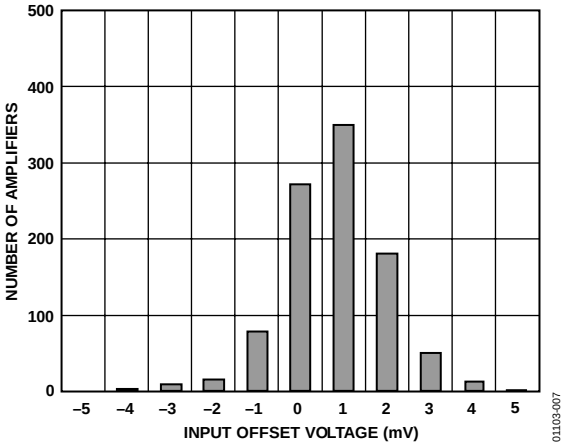


Figure 7. Input Offset Voltage Distribution

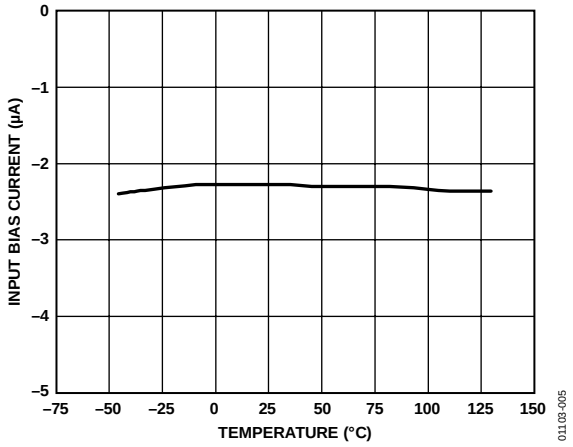


Figure 5. Input Bias Current vs. Temperature

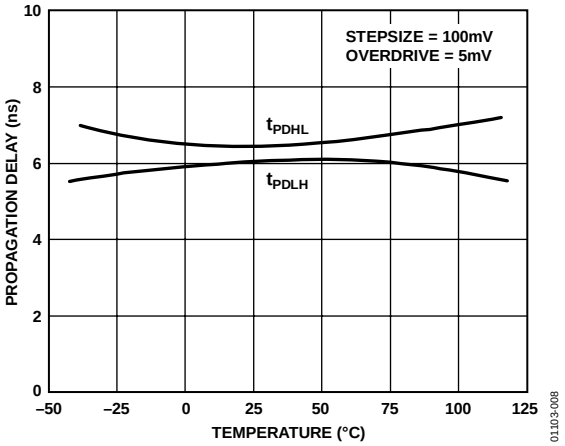


Figure 8. Propagation Delay, t_{PDHL}/t_{PDLH} vs. Temperature

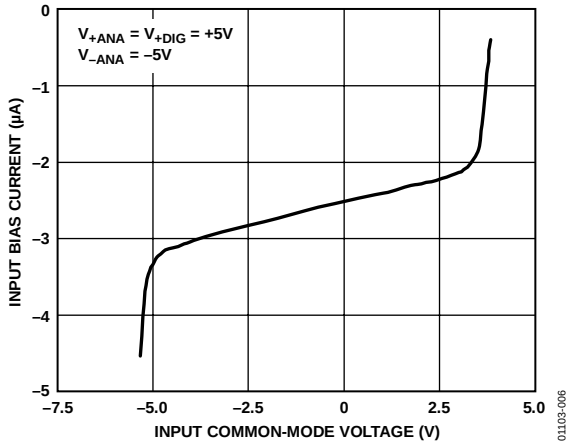


Figure 6. Input Bias Current vs. Input Common-Mode Voltage

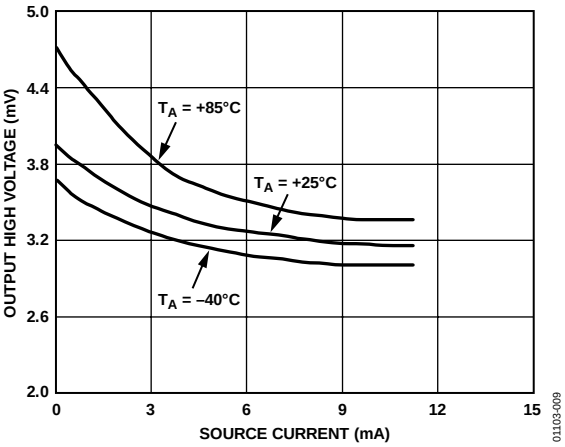


Figure 9. Output High Voltage, V_{OH} vs. Source Current

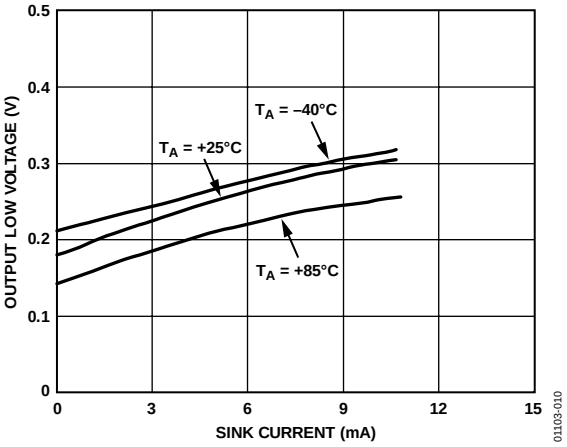


Figure 10. Output Low Voltage, V_{OL} vs. Sink Current

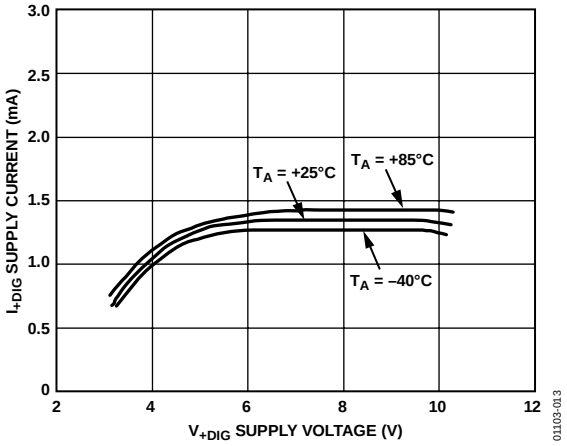


Figure 13. I_{+DIG} Supply Current/Comparator vs. V_{+DIG} Supply Voltage

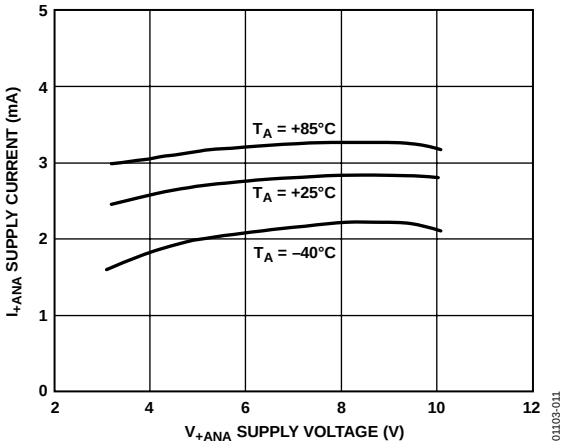


Figure 11. I_{+ANA} Supply Current/Comparator vs. V_{+ANA} Supply Voltage

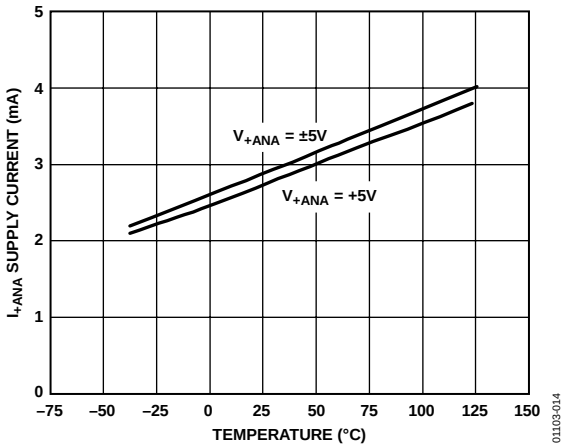


Figure 14. I_{+ANA} Supply Current/Comparator vs. Temperature

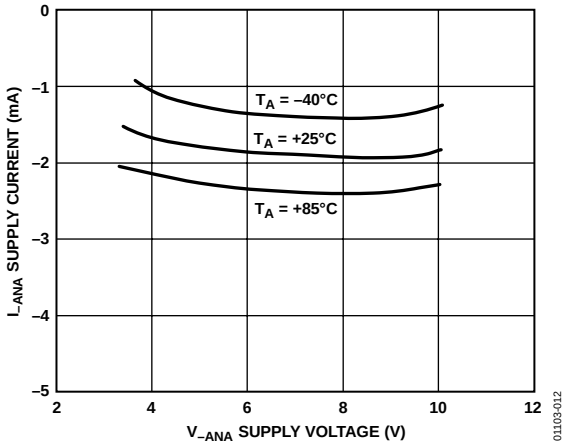


Figure 12. $I_{–ANA}$ Supply Current/Comparator vs. $V_{–ANA}$ Supply Voltage

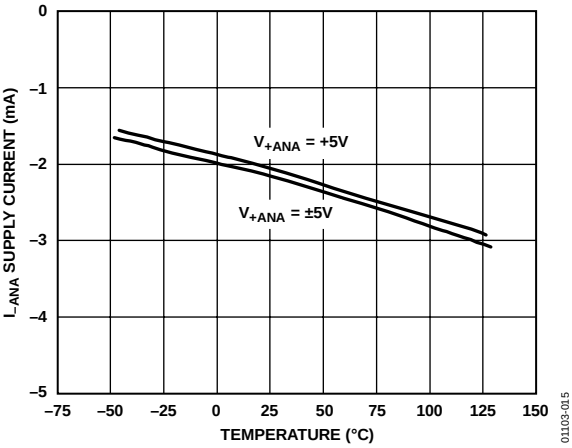


Figure 15. $I_{–ANA}$ Supply Current/Comparator vs. Temperature

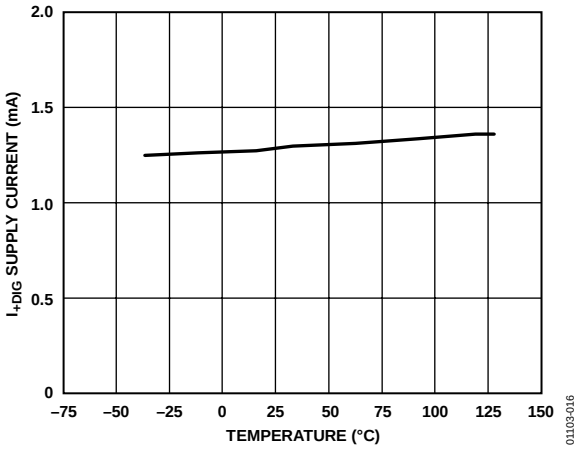


Figure 16. I_{+DIG} Supply Current/Comparator vs. Temperature

APPLICATIONS INFORMATION

OPTIMIZING HIGH SPEED PERFORMANCE

As with any high speed comparator or amplifier, proper design and layout techniques should be used to ensure optimal performance from the AD8564. The performance limits of high speed circuitry can easily be a result of stray capacitance, improper ground impedance, or other layout issues.

Minimizing resistance from the source to the input is an important consideration in maximizing the high speed operation of the AD8564. Source resistance, in combination with equivalent input capacitance, may cause a lagged response at the input, thus delaying the output. The input capacitance of the AD8564, in combination with stray capacitance from an input pin to ground, may result in several picofarads of equivalent capacitance. A combination of 3 kΩ source resistance and 5 pF of input capacitance yields a time constant of 15 ns, which is slower than the 5 ns capability of the AD8564. Source impedances should be less than 1 kΩ for the best performance.

It is also important to provide bypass capacitors for the power supply in a high speed application. A 1 μF electrolytic bypass capacitor should be placed within 0.5 inches of each power supply pin to ground. These capacitors reduce any potential voltage ripples from the power supply. In addition, a 10 nF ceramic capacitor should be placed as close as possible to the power supply pins to ground. These capacitors act as a charge reservoir for the device during high frequency switching.

A ground plane is recommended for proper high speed performance. This can be created by using a continuous conductive plane over the surface of the circuit board, only allowing breaks in the plane for necessary current paths. The ground plane provides a low inductance ground, eliminating any potential differences at different ground points throughout the circuit board caused from ground bounce. A proper ground plane also minimizes the effects of stray capacitance on the circuit board.

OUTPUT LOADING CONSIDERATIONS

The AD8564 output can deliver up to 40 mA of output current without any significant increase in propagation delay. The output of the device should not be connected to more than 20 TTL input logic gates or drive a load resistance less than 100 Ω.

To ensure the best performance from the AD8564, it is important to minimize capacitive loading of the output of the device. Capacitive loads greater than 50 pF cause ringing on the output waveform and reduce the operating bandwidth of the comparator. Propagation delay also increases with capacitive loads above 100 pF.

INPUT STAGE AND BIAS CURRENTS

The AD8564 uses a PNP differential input stage that enables the input common-mode range to extend all the way from the negative supply rail to within 2.2 V of the positive supply rail. The input common-mode voltage can be found as the average of the voltage at the two inputs of the device. To ensure the fastest response time, care should be taken to not allow the input common-mode voltage to exceed this voltage.

The input bias current for the AD8564 is 4 μA. As with any PNP differential input stage, this bias current goes to 0 on an input that is high and doubles on an input that is low. Care should be taken in choosing resistor values to be connected to the inputs because large resistors could cause significant voltage drops due to the input bias current.

The input capacitance for the AD8564 is typically 3 pF. This can be measured by inserting a large source resistance to the input and measuring the change in propagation delay.

USING HYSTERESIS

Hysteresis can easily be added to a comparator through the addition of positive feedback. Adding hysteresis to a comparator offers an advantage in noisy environments where it is not desirable for the output to toggle between states when the input signal is near the switching threshold. Figure 17 shows a method for configuring the AD8564 with hysteresis.

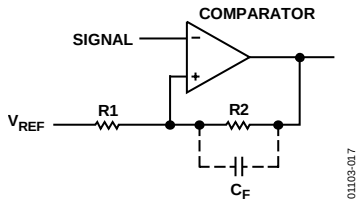


Figure 17. Configuring the AD8564 with Hysteresis

The input signal is connected directly to the inverting input of the comparator. The output is fed back to the noninverting input through R2 and R1. The ratio of R1 to R1 + R2 and the output swing establishes the width of the hysteresis window, with V_{REF} setting the center of the window or the average switching voltage. The output switches high when the input voltage is greater than V_{HI} and does not switch low again until the input voltage is less than V_{LO}, as given in Equation 2.

$$V_{HI} = \left(V_{+} - 1 - V_{REF}\right)\frac{R1}{R1 + R2}V_{REF} \quad (1)$$

$$V_{LO} = V_{REF}\left(1 - \frac{R1}{R1 + R2}\right) \quad (2)$$

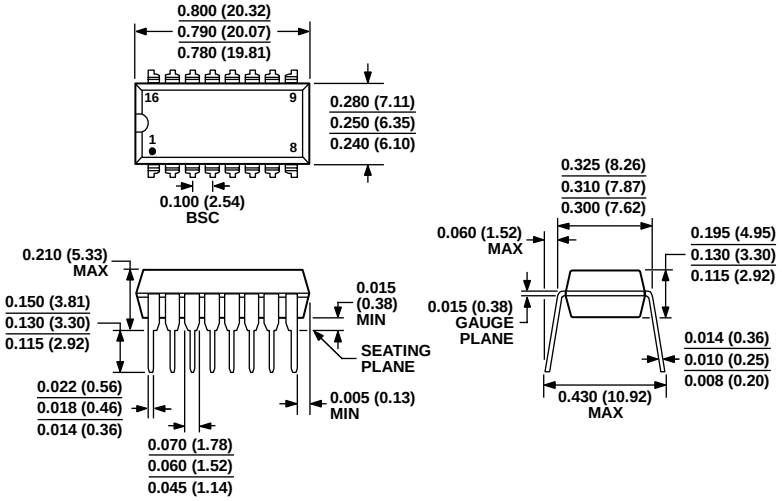
where V_+ is the positive supply voltage.

The C_F capacitor may also be added to introduce a pole into the feedback network. This has the effect of increasing the amount of hysteresis at high frequencies. This can be useful when comparing a relatively slow signal in a high frequency noise environment.

At frequencies greater than $f_P = \frac{1}{2\pi C_F R2}$, the hysteresis window approaches $V_{HI} = V_+ - 1$ V and $V_{LO} = 0$ V.

At frequencies less than f_P, the threshold voltages remain as it is in Equation 1.

OUTLINE DIMENSIONS

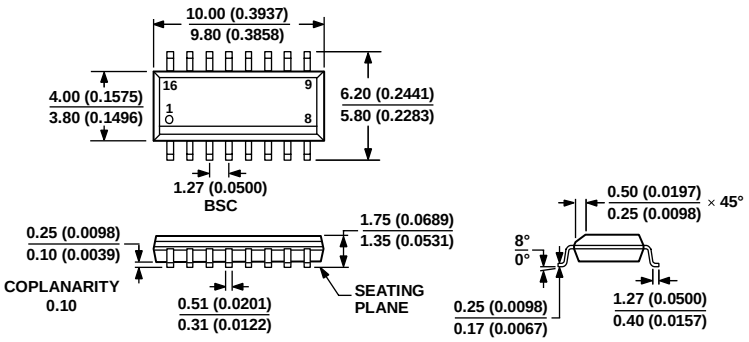


COMPLIANT TO JEDEC STANDARDS MS-001-AB

CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN. CORNER LEADS MAY BE CONFIGURED AS WHOLE OR HALF LEADS.

073106-B

Figure 18. 16-Lead Plastic Dual In-Line Package [PDIP]
(N-16)
Dimensions shown in inches and (millimeters)



COMPLIANT TO JEDEC STANDARDS MS-012-AC

CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

060606-A

Figure 19. 16-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-16)
Dimensions shown in millimeters and (inches)

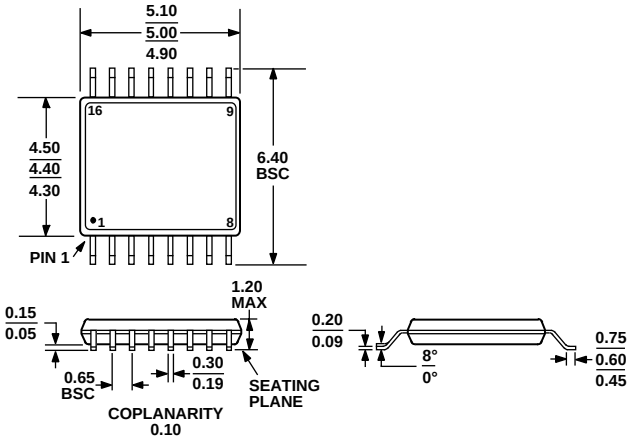


Figure 20. 16-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-16)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD8564AN	−40°C to +125°C	16-Lead Plastic Dual In-Line Package [PDIP]	N-16
AD8564ANZ[1]	−40°C to +125°C	16-Lead Plastic Dual In-Line Package [PDIP]	N-16
AD8564AR	−40°C to +125°C	16-Lead Standard Small Outline Package [SOIC_N]	R-16
AD8564AR-REEL	−40°C to +125°C	16-Lead Standard Small Outline Package [SOIC_N]	R-16
AD8564AR-REEL7	−40°C to +125°C	16-Lead Standard Small Outline Package [SOIC_N]	R-16
AD8564ARZ[1]	−40°C to +125°C	16-Lead Standard Small Outline Package [SOIC_N]	R-16
AD8564ARZ-REEL[1]	−40°C to +125°C	16-Lead Standard Small Outline Package [SOIC_N]	R-16
AD8564ARZ-REEL7[1]	−40°C to +125°C	16-Lead Standard Small Outline Package [SOIC_N]	R-16
AD8564ARU-REEL	−40°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
AD8564ARUZ-REEL[1]	−40°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16

[1] Z = RoHS Compliant Part.