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REVISION HISTORY

10/13—Rev. A to Rev. B

Changed ENBA, ENBB, A0 to A4, B0 to B4 Maximum Rating to +0.6 V; Table 3 ... 5
Updated Outline Dimensions ... 23
Changes to Ordering Guide ... 23

10/10—Rev. 0 to Rev. A

Changes to Figure 3 and Table 4 ... 6
Changes to Figure 36 ... 14
Added Exposed Pad Notation to Outline Dimensions ... 23

8/07—Revision 0: Initial Version

SPECIFICATIONS

V_S = 5 V, T = 25°C, R_S = R_L = 150 Ω at 140 MHz, 2 V p-p differential output, both channels enabled, unless otherwise noted.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	V_{OUT} < 2 V p-p (5.2 dBm)		700		MHz
Slew Rate			5		V/ns
INPUT STAGE	Pin IPA+ and Pin IPA−, Pin IPB+ and Pin IPB−				
Maximum Input Swing	For linear operation (A_V = −4 dB)		8.5		V p-p
Differential Input Resistance	Differential	120	150	165	Ω
Common-Mode Input Voltage			1.85		V
CMRR	Gain code = 00000		45.5		dB
GAIN					
Amplifier Transconductance	Gain code = 00000	0.060	0.067	0.074	S
Maximum Voltage Gain	Gain code = 00000		20		dB
Minimum Voltage Gain	Gain code ≥ 11000		−4		dB
Gain Step Size	From gain code = 00000 to 11000	0.93	0.98	1.02	dB
Gain Flatness	All gain codes, 20% fractional bandwidth for f_C < 200 MHz		0.18		dB
Gain Temperature Sensitivity	Gain code = 00000		8		mdB/°C
Gain Step Response	For V_{IN} = 100 mV p-p, gain code = 10100 to 00000		5		ns
OUTPUT STAGE	Pin OPA+ and Pin OPA−, Pin OPB+ and Pin OPB−				
Output Voltage Swing	At P1dB, gain code = 00000		13.1		V p-p
Output Impedance	Differential		16||0.8		kΩ||pF
Channel Isolation	Measured at differential output for differential input applied to alternate channel (referred to output)		73		dB
NOISE/HARMONIC PERFORMANCE					
46 MHz	Gain code = 00000				
Noise Figure			8.7		dB
Second Harmonic	V_{OUT} = 2 V p-p		−92		dBc
Third Harmonic	V_{OUT} = 2 V p-p		−94		dBc
Output IP3	2 MHz spacing, 3 dBm per tone		50		dBm
Output 1 dB Compression Point			21.3		dBm
70 MHz	Gain code = 00000				
Noise Figure			8.7		dB
Second Harmonic	V_{OUT} = 2 V p-p		−89		dBc
Third Harmonic	V_{OUT} = 2 V p-p		−95		dBc
Output IP3	2 MHz spacing, 3 dBm per tone		50		dBm
Output 1 dB Compression Point			21.4		dBm
140 MHz	Gain code = 00000				
Noise Figure			8.7		dB
Second Harmonic	V_{OUT} = 2 V p-p		−87		dBc
Third Harmonic	V_{OUT} = 2 V p-p		−97		dBc
Output IP3	2 MHz spacing, 3 dBm per tone		51		dBm
Output 1 dB Compression Point			21.6		dBm
200 MHz	Gain code = 00000				
Noise Figure			8.7		dB
Second Harmonic	V_{OUT} = 2 V p-p		−82		dBc
Third Harmonic	V_{OUT} = 2 V p-p		−91		dBc
Output IP3	2 MHz spacing, 3 dBm per tone		50		dBm
Output 1 dB Compression Point			20.9		dBm

Parameter	Conditions	Min	Typ	Max	Unit
POWER INTERFACE					
Supply Voltage		4.5	5.0	5.5	V
VCC and Output Quiescent Current with Both Channels Enabled	Thermal connection made to exposed paddle under device	245	250	255	mA
vs. Temperature	$-40°C \le T_A \le +85°C$			285	mA
Power-Down Current, Both Channels	ENBA and ENBB Low		5.4		mA
vs. Temperature	$-40°C \le T_A \le +85°C$			7	mA
POWER-UP/GAIN CONTROL	Pin A0 to Pin A4, Pin B0 to Pin B4, Pin ENBA, and Pin ENBB				
V_{IH}	Minimum voltage for a logic high	1.6			V
V_{IL}	Maximum voltage for a logic low			0.8	V
Logic Input Bias Current			900		nA

Table 2. Gain Code vs. Voltage Gain Look-Up Table

5-Bit Binary Gain Code	Voltage Gain (dB)
00000	+20
00001	+19
00010	+18
00011	+17
00100	+16
00101	+15
00110	+14
00111	+13
01000	+12
01001	+11
01010	+10
01011	+9
01100	+8

5-Bit Binary Gain Code	Voltage Gain (dB)
01101	+7
01110	+6
01111	+5
10000	+4
10001	+3
10010	+2
10011	+1
10100	0
10101	−1
10110	−2
10111	−3
11000	−4
>11000	−4

ABSOLUTE MAXIMUM RATINGS

Table 3.

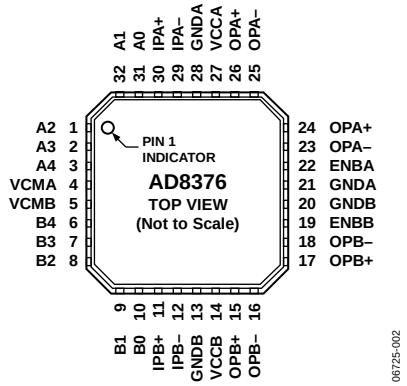
Parameter	Rating
Supply Voltage, V_{POS}	5.5 V
ENBA, ENBB, A0 to A4, B0 to B4	−0.6 V to (V_{POS} + 0.6 V)
Input Voltage, V_{IN+}, V_{IN-}	−0.15 V to +4.15 V
DC Common Mode	VCMA, VCMB ± 0.25 V
VCMA, VCMB	± 6 mA
Internal Power Dissipation	1.6 W
θ_{JA} (Exposed Paddle Soldered Down)	34.6°C/W
θ_{JC} (At Exposed Paddle)	3.6°C/W
Maximum Junction Temperature	140°C
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. THE EXPOSED PAD IS INTERNALLY CONNECTED TO GROUND. SOLDER TO A LOW IMPEDANCE GROUND PLANE.

Figure 3. 32-Lead LFCSP

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	A2	MSB – 2 for the Gain Control Interface for Channel A.
2	A3	MSB – 1 for the Gain Control Interface for Channel A.
3	A4	MSB for the 5-Bit Gain Control Interface for Channel A.
4	VCMA	Channel A Input Common-Mode Voltage. Typically bypassed to ground through capacitor.
5	VCMB	Channel B Input Common-Mode Voltage. Typically bypassed to ground through capacitor.
6	B4	MSB for the 5-Bit Gain Control Interface for Channel B.
7	B3	MSB – 1 for the Gain Control Interface for Channel B.
8	B2	MSB – 2 for the Gain Control Interface for Channel B.
9	B1	LSB + 1 for the Gain Control Interface for Channel B.
10	B0	LSB for the Gain Control Interface for Channel B.
11	IPB+	Channel B Positive Input.
12	IPB–	Channel B Negative Input.
13, 20	GNDB	Device Common (DC Ground) for Channel B.
14	VCCB	Positive Supply Pin for Channel B. Should be bypassed to ground using suitable bypass capacitor.
15, 17	OPB+	Positive Output Pins (Open Collector) for Channel B. Require dc bias of +5 V nominal.
16, 18	OPB–	Negative Output Pins (Open Collector) for Channel B. Require dc bias of +5 V nominal.
19	ENBB	Power Enable Pin for Channel B. Channel B is enabled with a logic high and disabled with a logic low.
21, 28	GNDA	Device Common (DC Ground) for Channel A.
22	ENBA	Power Enable Pin for Channel A. Channel A is enabled with a logic high and disabled with a logic low.
23, 25	OPA–	Negative Output Pins (Open Collector) for Channel A. Require dc bias of +5 V nominal.
24, 26	OPA+	Positive Output Pins (Open Collector) for Channel A. Require dc bias of +5 V nominal.
27	VCCA	Positive Supply Pins for Channel A. Should be bypassed to ground using suitable bypass capacitor.
29	IPA–	Channel A Negative Input.
30	IPA+	Channel A Positive Input.
31	A0	LSB for the Gain Control Interface for Channel A.
32	A1	LSB + 1 for the Gain Control Interface for Channel A.
	Exposed Pad	Internally connected to ground. Solder to a low impedance ground plane.

TYPICAL PERFORMANCE CHARACTERISTICS

V_S = 5 V, T_A = 25°C, R_S = R_L = 150 Ω, 2 V p-p output, maximum gain unless otherwise noted.

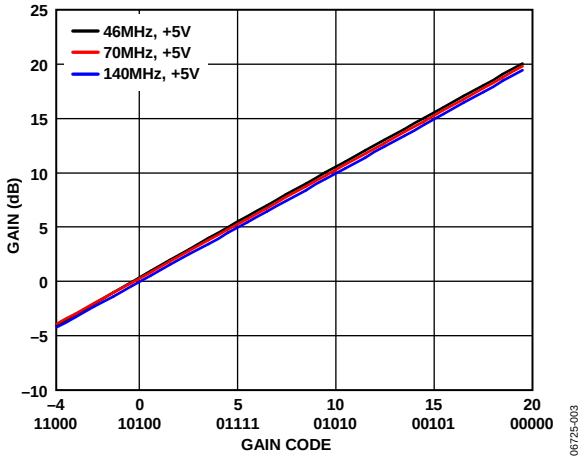


Figure 4. Gain vs. Gain Code at 46 MHz, 70 MHz, and 140 MHz

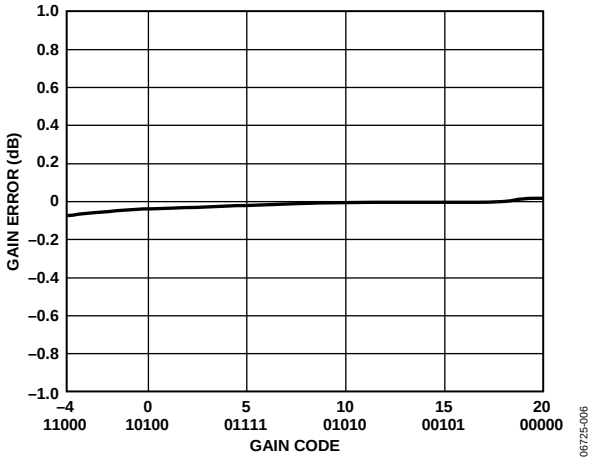


Figure 7. Gain Step Error, Frequency 140 MHz

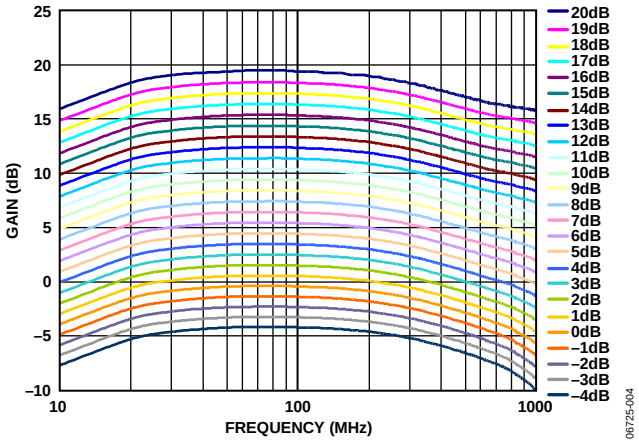


Figure 5. Gain vs. Frequency Response

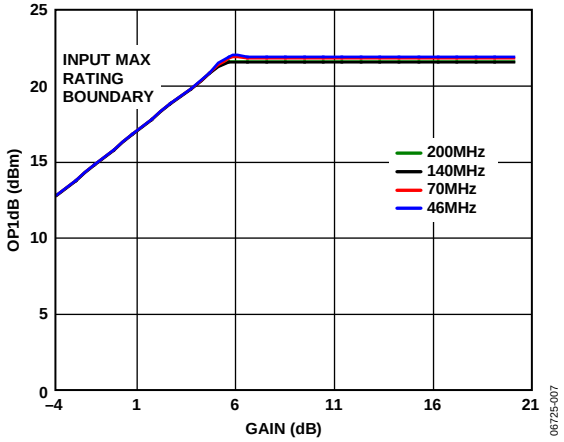


Figure 8. P1dB vs. Gain at 46 MHz, 70 MHz, 140 MHz, and 200 MHz

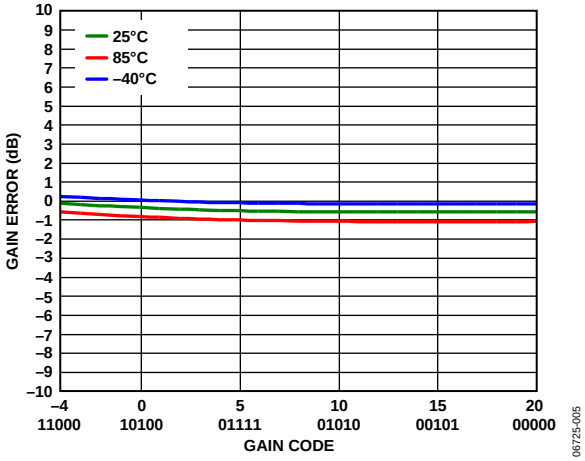


Figure 6. Gain Error over Temperature at 140 MHz

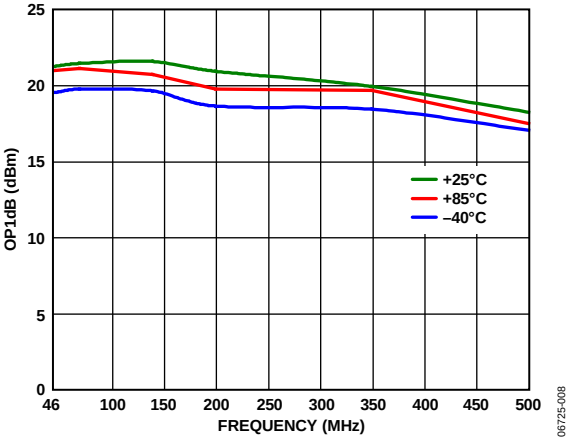


Figure 9. P1dB vs. Frequency at Maximum Gain, Three Temperatures

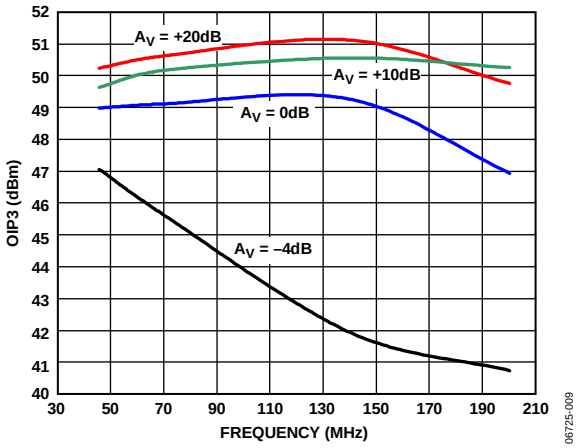


Figure 10. Output Third-Order Intercept at Four Gains, Output Level at 3 dBm/Tone

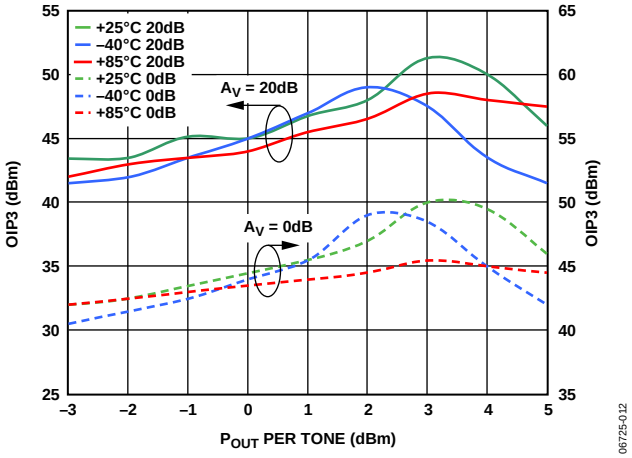


Figure 13. Output Third-Order Intercept vs. Power, Frequency 140 MHz, Three Temperatures

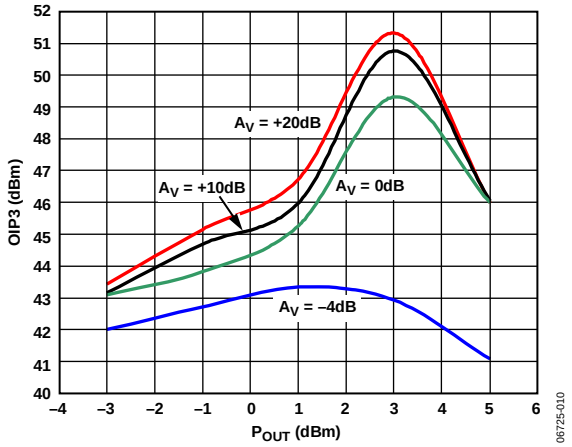


Figure 11. Output Third-Order Intercept vs. Power at Four Gains, Frequency 140 MHz

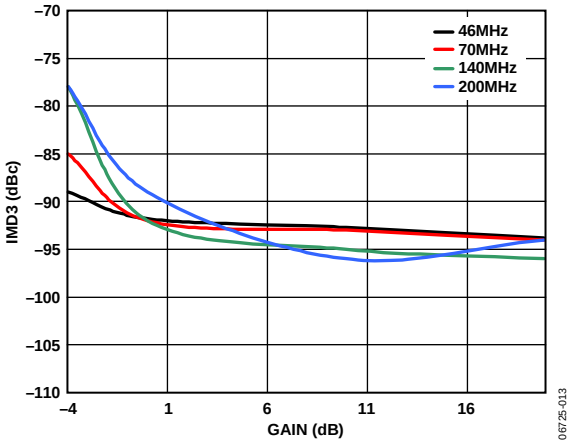


Figure 14. Two-Tone Output IMD vs. Gain at 46 MHz, 70 MHz, 140 MHz, and 200 MHz, Output Level at 3 dBm/Tone

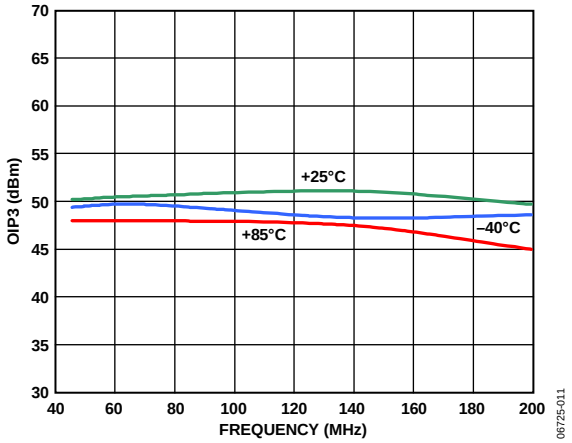


Figure 12. Output Third-Order Intercept vs. Frequency, Three Temperatures, Output Level at 3 dBm/Tone

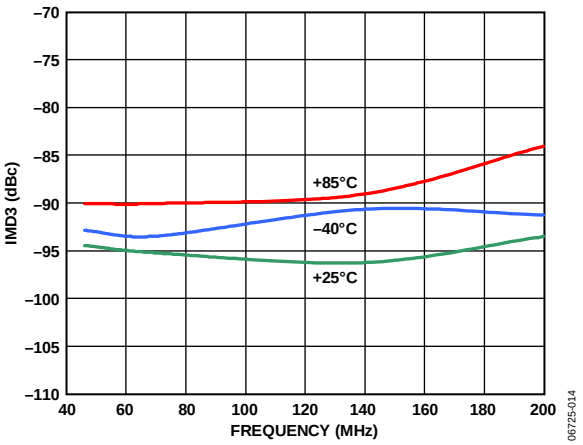


Figure 15. Two-Tone Output IMD vs. Frequency, Three Temperatures, Output Level at 3 dBm/Tone

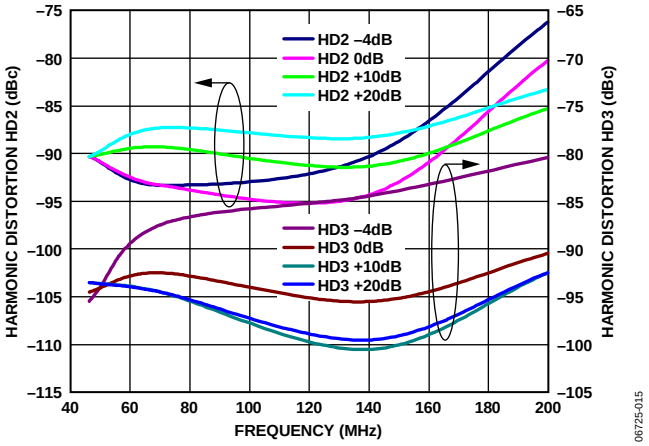


Figure 16. Harmonic Distortion vs. Frequency at Four Gain Codes, V_{OUT} = 2 V p-p

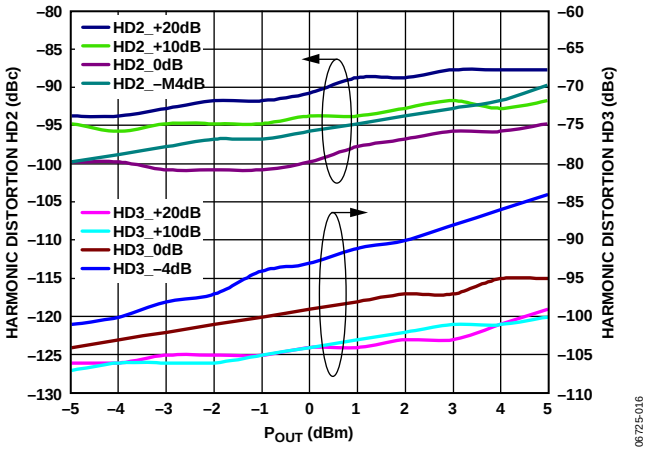


Figure 17. Harmonic Distortion vs. Power at Four Gain Codes, Frequency 140 MHz

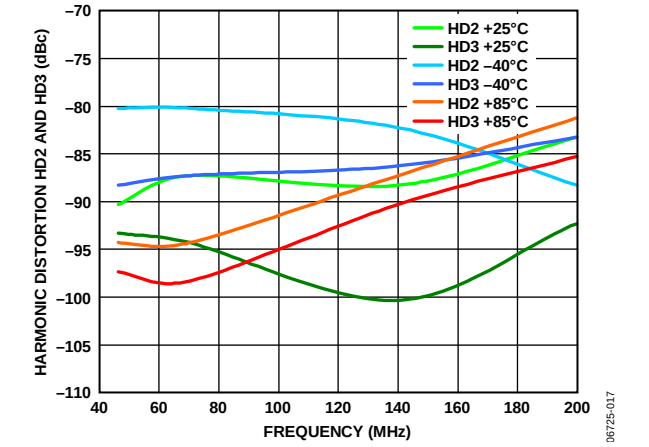


Figure 18. Harmonic Distortion vs. Frequency, Three Temperatures, V_{OUT} = 2 V p-p

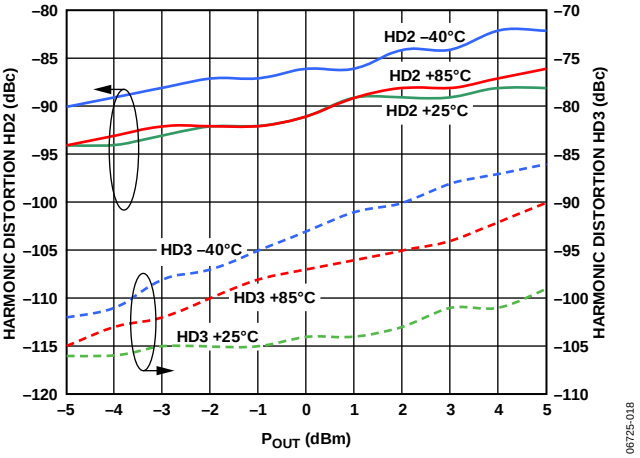


Figure 19. Harmonic Distortion vs. Power, Frequency 140 MHz, Three Temperatures

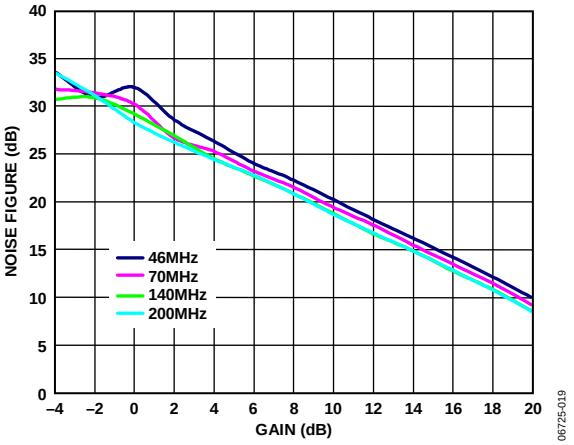


Figure 20. NF vs. Gain at 46 MHz, 70 MHz, 140 MHz, and 200 MHz

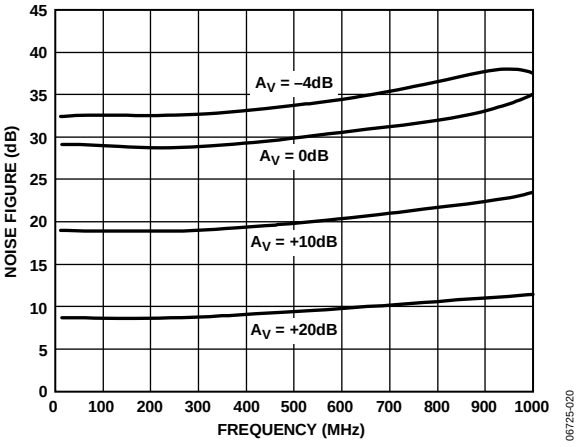


Figure 21. NF vs. Frequency

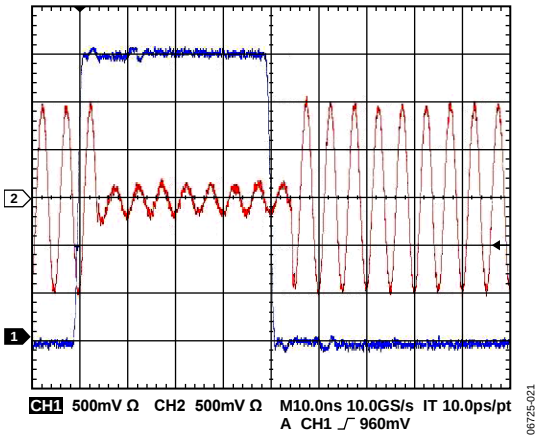


Figure 22. Gain Step Time Domain Response

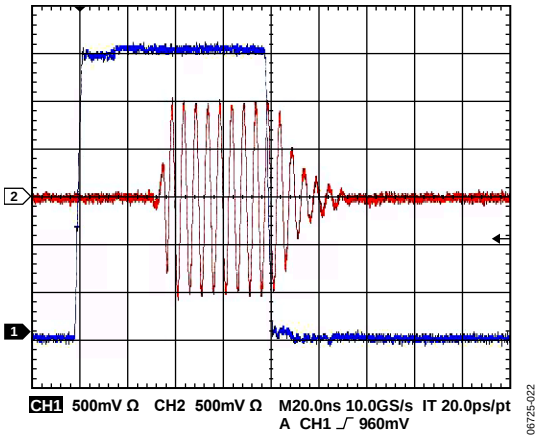


Figure 23. ENBL Time Domain Response

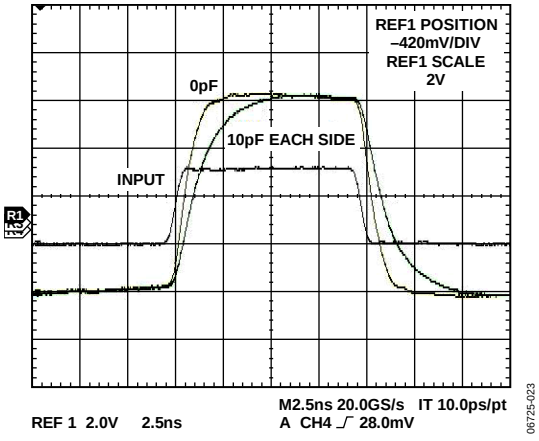


Figure 24. Pulse Response to Capacitive Loading, Gain −4 dB

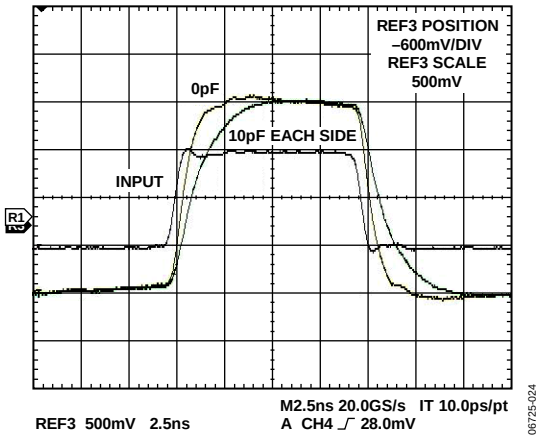


Figure 25. Pulse Response to Capacitive Loading, Gain 20 dB

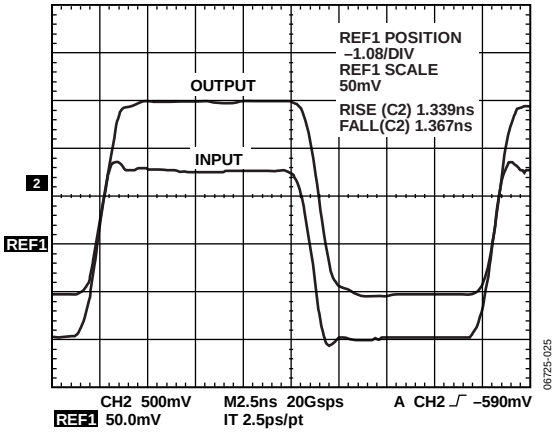


Figure 26. Large Signal Pulse Response

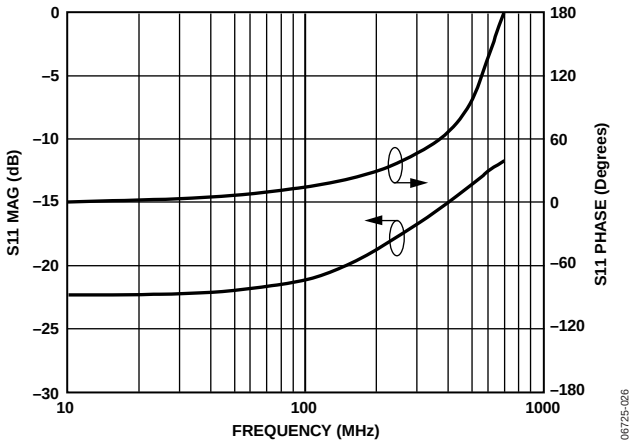


Figure 27. S11 vs. Frequency

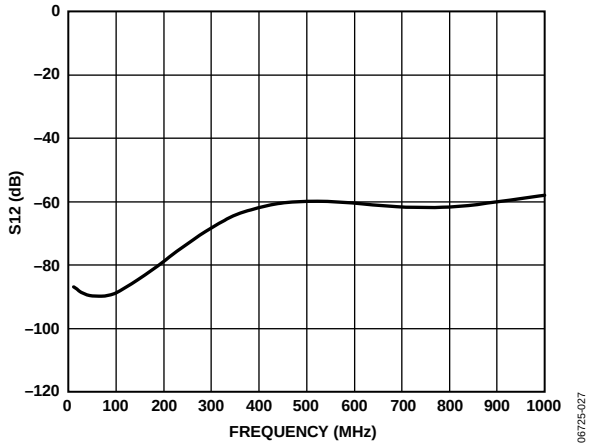


Figure 28. Reverse Isolation vs. Frequency

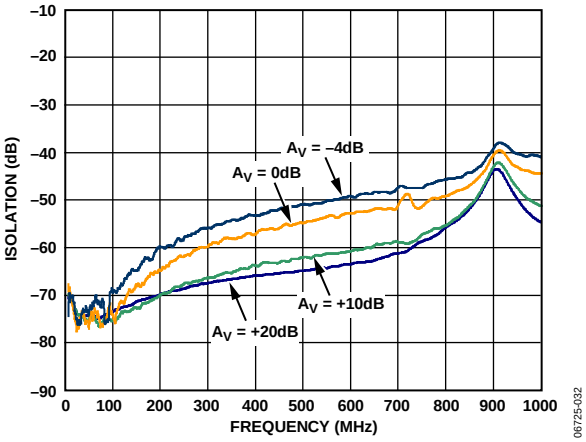


Figure 31. Channel Isolation (Output to Output) vs. Frequency

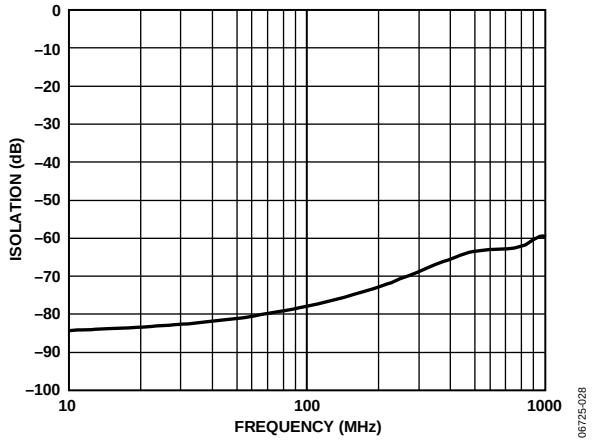


Figure 29. Off-State Isolation vs. Frequency

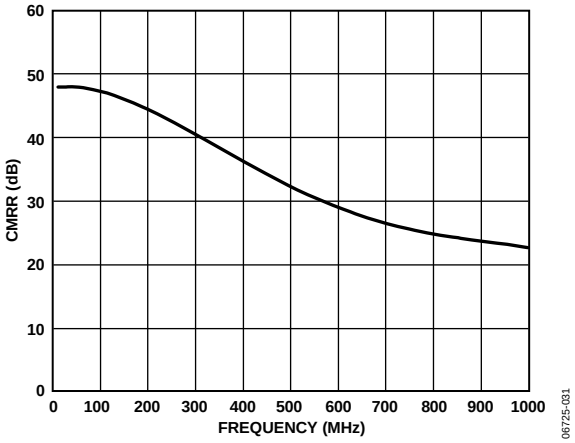


Figure 32. Common-Mode Rejection Ratio vs. Frequency

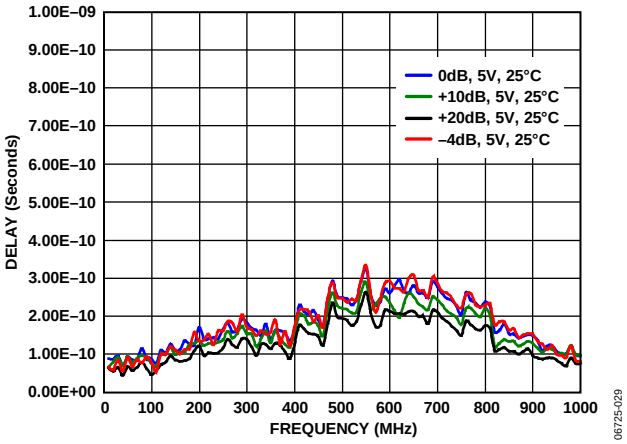


Figure 30. Group Delay vs. Frequency at Gain

CIRCUIT DESCRIPTION

BASIC STRUCTURE

The AD8376 is a dual differential variable gain amplifier with each amplifier consisting of a 150 Ω digitally controlled passive attenuator followed by a highly linear transconductance amplifier.

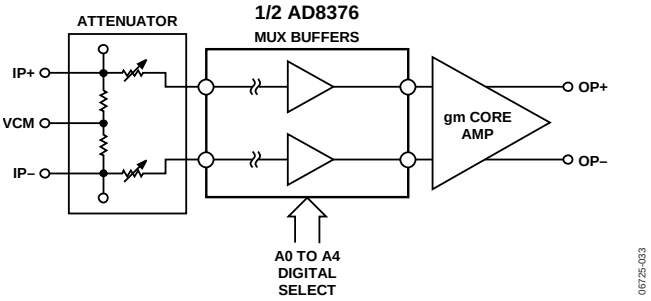


Figure 33. Simplified Schematic

Input System

The dc voltage level at the inputs of the AD8376 is set by an internal voltage reference circuit to about 2 V. This reference is accessible at VCMA and VCMB and can be used to source or sink 100 µA. For cases where a common-mode signal is applied to the inputs, such as in a single-ended application, an external capacitor between VCMA/VCMB and ground is required. The capacitor improves the linearity performance of the part in this mode. This capacitor should be sized to provide a reactance of 10 Ω or less at the lowest frequency of operation. If the applied common-mode signal is dc, its amplitude should be limited to 0.25 V from VCMA/VCMB (VCMA or VCMB ± 0.25 V). Each device can be powered down by pulling the ENBA or ENBB pin down to below 0.8 V. In the powered down mode, the total current reduces to 3 mA (typical). The dc level at the inputs and at VCMA/VCMB remains at about 2 V, regardless of the state of the ENBA of ENBB pin.

Output Amplifier

The gain is based on a 150 Ω differential load and varies as R_L is changed per the following equations:

$$Voltage\ Gain = 20 \times (\log(R_L/150) + 1)$$

and

$$Power\ Gain = 10 \times (\log(R_L/150) + 2)$$

The dependency of the gain on the load is due to the open-collector architecture of the output stage.

The dc current to the outputs of each amplifier is supplied through two external chokes. The inductance of the chokes and the resistance of the load determine the low frequency pole of the amplifier. The parasitic capacitance of the chokes adds to the output capacitance of the part. This total capacitance in parallel with the load resistance sets the high frequency pole of the device. Generally, the larger the inductance of the choke, the higher its parasitic capacitance. Therefore, the value and type of the choke should be chosen keeping this trade-off in mind.

For operation frequency of 15 MHz to 700 MHz driving a 150 Ω load, 1 µH chokes with SRF of 160 MHz or higher are recommended (such as 0805LS-102XJBB from Coilcraft).

The supply current of each amplifier consists of about 50 mA through the VCC pin and 80 mA through the two chokes combined. The latter increases with temperature at about 2.5 mA per 10°C.

Each amplifier has two output pins for each polarity, and they are oriented in an alternating fashion. When designing the board, care should be taken to minimize the parasitic capacitance due to the routing that connects the corresponding outputs together. A good practice is to avoid any ground or power plane under this routing region and under the chokes to minimize the parasitic capacitance.

Gain Control

Two independent 5-bit binary codes change each attenuator setting in 1 dB steps such that the gain of each amplifier changes from +20 dB (Code 0) to −4 dB (Code 24 and higher).

The noise figure of each amplifier is about 8 dB at maximum gain setting, and it increases as the gain is reduced. The increase in noise figure is equal to the reduction in gain. The linearity of the part measured at the output is first-order independent of the gain setting. From 0 dB to 20 dB gain, OIP3 is approximately 50 dBm into 150 Ω load at 140 MHz (3 dBm per tone). At gain settings below 0 dB, it drops to approximately 45 dBm.

APPLICATIONS

BASIC CONNECTIONS

Figure 36 shows the basic connections for operating the AD8376. A voltage between 4.5 V and 5.5 V should be applied to the supply pins. Each supply pin should be decoupled with at least one low inductance, surface-mount ceramic capacitor of 0.1 µF placed as close as possible to the device.

The outputs of the AD8376 are open collectors that need to be pulled up to the positive supply with 1 µH RF chokes. The differential outputs are biased to the positive supply and require ac-coupling capacitors, preferably 0.1 µF. Similarly, the input pins are at bias voltages of about 2 V above ground and should be ac-coupled as well. The ac-coupling capacitors and the RF chokes are the principle limitations for operation at low frequencies.

To enable each channel of the AD8376, the ENBA or ENBB pin must be pulled high. Taking ENBA or ENBB low puts the channels of the AD8376 in sleep mode, reducing current consumption to approximately 5 mA per channel at ambient.

SINGLE-ENDED-TO-DIFFERENTIAL CONVERSION

The AD8376 can be configured as a single-ended input to differential output driver, as shown in Figure 34. A 150 Ω resistor in parallel with the input impedance of input pin provides an impedance matching of 50 Ω. The voltage gain and the bandwidth of this configuration, using a 150 Ω load, remains the same as when using a differential input.

Using a single-ended input decreases the power gain by 3 dB and limits distortion cancellation. Consequently, the second-order distortion is degraded. The third-order distortion remains low to 200 MHz, as shown in Figure 35.

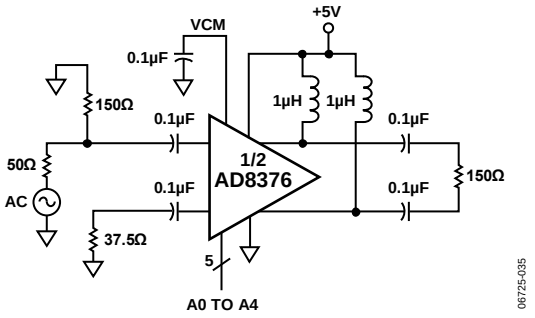


Figure 34. Single-Ended-to-Differential Conversion Featuring ½ of the AD8376

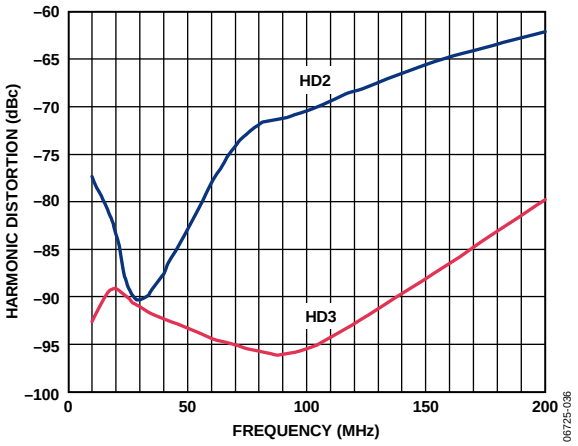


Figure 35. Harmonic Distortion vs. Frequency of Single-Ended-to-Differential Conversion

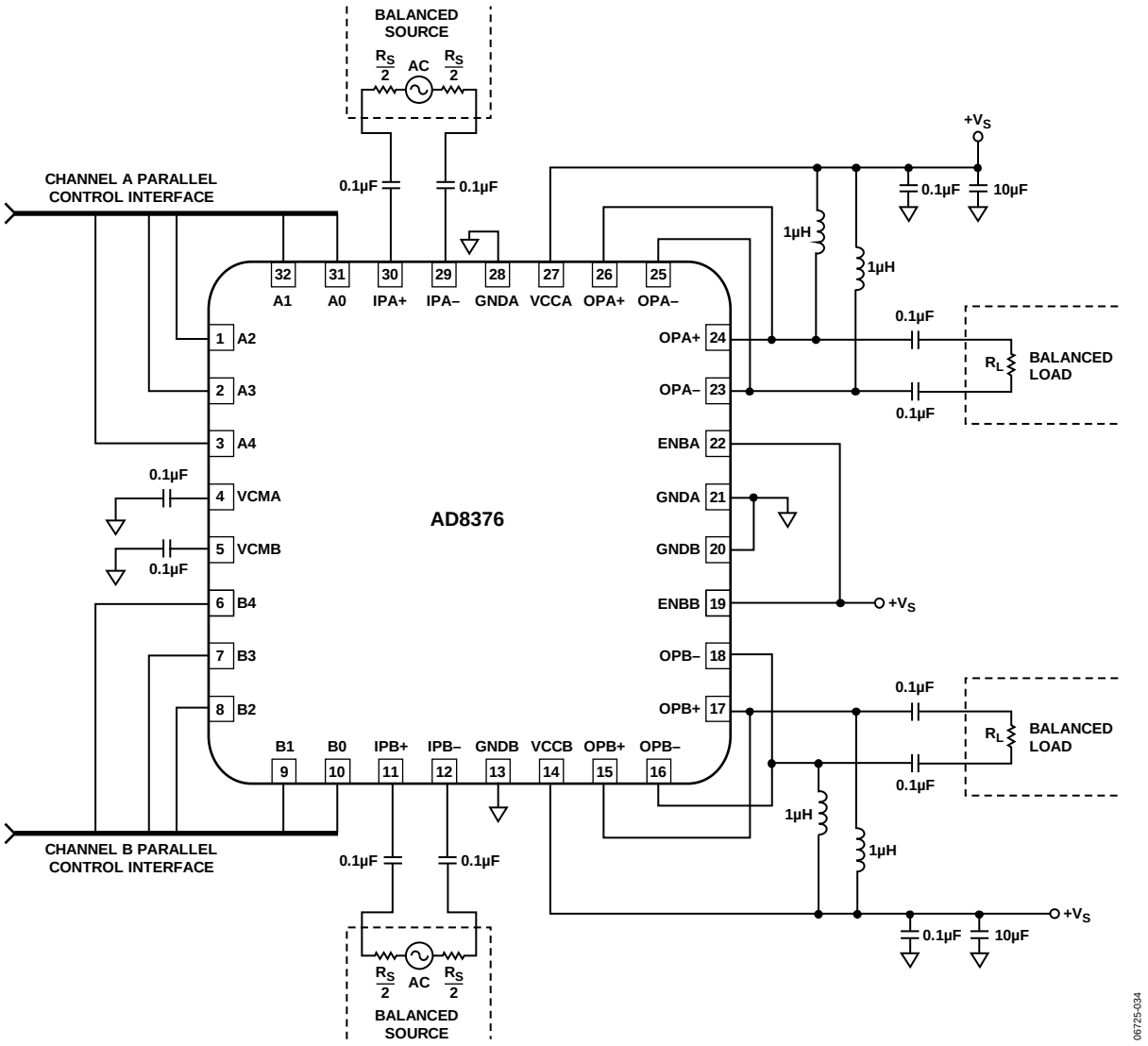


Figure 36. Basic Connections

BROADBAND OPERATION

The AD8376 uses an open-collector output structure that requires dc bias through an external bias network. Typically, choke inductors are used to provide bias to the open-collector outputs. Choke inductors work well at signal frequencies where the impedance of the choke is substantially larger than the target ac load impedance. In broadband applications, it may not be possible to find large enough choke inductors that offer enough reactance at the lowest frequency of interest while offering a high enough self resonant frequency (SRF) to support the maximum bandwidth available from the device. The circuit in Figure 37 can be used when frequency response below 10 MHz is desired. This circuit replaces the bias chokes with bias resistors. The bias resistor has the disadvantage of a greater IR drop, and requires a supply rail that is several volts above the local 5 V supply used to power the device. Additionally, it is necessary to account for the ac loading effect of the bias resistors when designing the output interface. Whereas the gain of the AD8376 is load dependent, R_L in parallel with R1 + R2 should equal the optimum 150 Ω target load impedance to provide the expected ac performance depicted in the data sheet. Additionally, to ensure good output balance and even-order distortion performance, it is essential that R1 = R2.

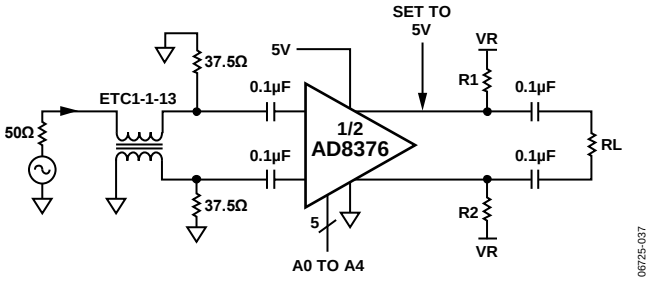


Figure 37. Single-Ended Broadband Operation with Resistive Pull-Ups

Using the formula for R1 (Equation 1), the values of R1 = R2 that provide a total presented load impedance of 150 Ω can be found. The required voltage applied to the bias resistors, VR, can be found by using the VR formula (Equation 2).

$$R1 = \frac{75 \times R_L}{R_L - 150} \quad (1)$$

and

$$VR = R1 \times 40 \times 10^{-3} + 5 \quad (2)$$

For example, in the extreme case where the load is assumed to be high impedance, $R_L = \infty$, the equation for R1 reduces to R1 = 75 Ω. Using the equation for VR, the applied voltage should be VR = 8 V. The measured single-tone low frequency harmonic distortion for a 2 V p-p output using 75 Ω resistive pull-ups is provided in Figure 38.

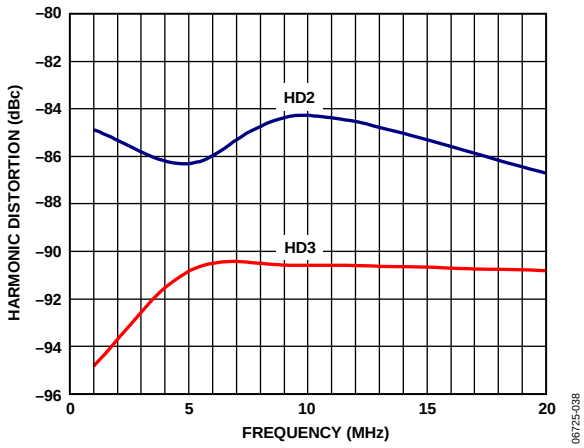


Figure 38. Harmonic Distortion vs. Frequency Using Resistive Pull-Ups

ADC INTERFACING

The AD8376 is a high output linearity variable gain amplifier that is optimized for ADC interfacing. The output IP3 and noise floor essentially remain constant vs. the 24 dB available gain range. This is a valuable feature in a variable gain receiver where it is desirable to maintain a constant instantaneous dynamic range as the receiver gain is modified. The output noise density is typically around 20 nV/√Hz, which is comparable to 14-/16-bit sensitivity limits. The two-tone IP3 performance of the AD8376 is typically around 50 dBm. This results in SFDR levels of better than 86 dB when driving the AD9445 up to 140 MHz.

There are several options available to the designer when using the AD8376. The open-collector output provides the capability of driving a variety of loads. Figure 39 shows a simplified wideband interface with the AD8376 driving a AD9445. The AD9445 is a 14-bit 125 MSPS analog-to-digital converter with a buffered wideband input, which presents a 2 kΩ||3 pF differential load impedance and requires a 2 V p-p differential input swing to reach full scale.

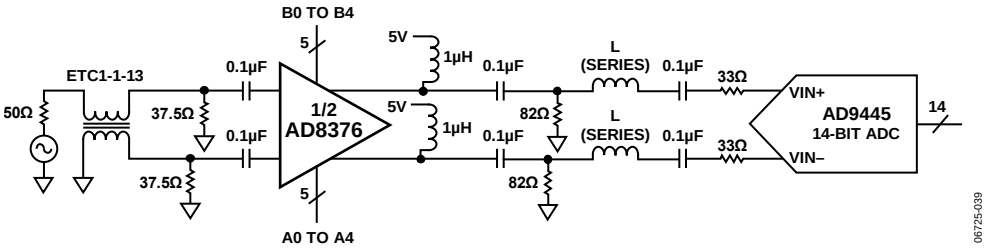


Figure 39. Wideband ADC Interfacing Example Featuring ½ of the AD8376 and the AD9445

For optimum performance, the AD8376 should be driven differentially using an input balun or impedance transformer. Figure 39 uses a wideband 1:1 transmission line balun followed by two 37.5 Ω resistors in parallel with the 150 Ω input impedance of the AD8376 to provide a 50 Ω differential terminated input impedance. This provides a wideband match to a 50 Ω source. The open-collector outputs of the AD8376 are biased through the two 1 µH inductors and are ac-coupled to the two 82 Ω load resistors. The 82 Ω load resistors in parallel with the series-terminated ADC impedance yields the target 150 Ω differential load impedance, which is recommended to provide the specified gain accuracy of the device. The load resistors are ac-coupled from the AD9445 to avoid common-mode dc loading. The 33 Ω series resistors help to improve the isolation between the AD8376 and any switching currents present at the analog-to-digital sample and hold input circuitry.

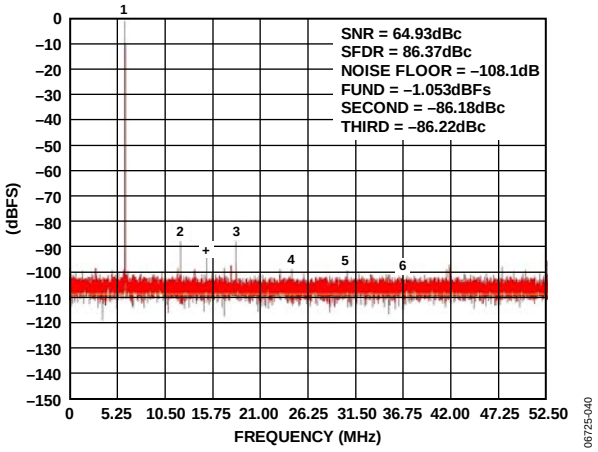


Figure 40. Measured Single-Tone Performance of the Circuit in Figure 39 for a 100 MHz Input Signal

The circuit depicted in Figure 39 provides variable gain, isolation, and source matching for the AD9445. Using this circuit with the AD8376 in a gain of 20 dB (maximum gain), an SFDR performance of 86 dBc is achieved at 100 MHz, as indicated in Figure 40.

The addition of the series inductors L (series) in Figure 39 extends the bandwidth of the system and provides response flatness. Using 100 nH inductors as L (series), the wideband system response of Figure 41 is obtained. The wideband frequency response is an advantage in broadband applications such as predistortion receiver designs and instrumentation applications. However, by designing for a wide analog input frequency range, the cascaded SNR performance is somewhat degraded due to high frequency noise aliasing into the wanted Nyquist zone.

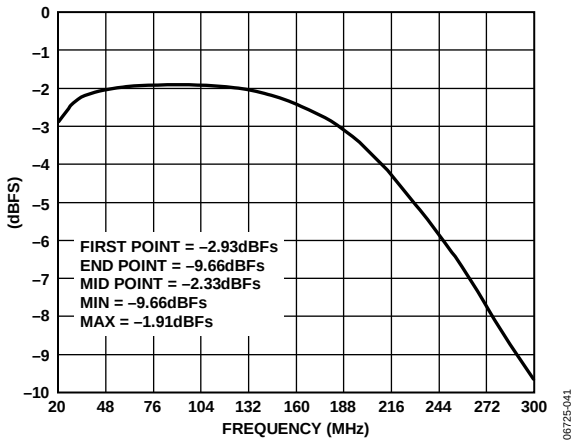


Figure 41. Measured Frequency Response of Wideband ADC Interface Depicted in Figure 39

An alternative narrow-band approach is presented in Figure 42. By designing a narrow band-pass antialiasing filter between the AD8376 and the target ADC, the output noise of the AD8376 outside of the intended Nyquist zone can be attenuated, helping to preserve the available SNR of the ADC. In general, the SNR improves several dB when including a reasonable order antialiasing filter. In this example, a low loss 1:3 input transformer is used to match the AD8376's 150 Ω balanced input to a 50 Ω unbalanced source, resulting in minimum insertion loss at the input.

Figure 42 is optimized for driving some of Analog Devices popular unbuffered ADCs, such as the AD9246, AD9640, and AD6655. Table 5 includes antialiasing filter component recommendations for popular IF sampling center frequencies. Inductor L5 works in parallel with the on-chip ADC input capacitance and a portion of the capacitance presented by C4 to form a resonant tank circuit. The resonant tank helps to ensure the ADC input looks like a real resistance at the target center frequency. Additionally, the L5 inductor shorts the ADC inputs at dc, which introduces a zero into the transfer function. In addition, the ac coupling capacitors and the bias chokes introduce additional zeros into the transfer function. The final overall frequency response takes on a band-pass characteristic, helping to reject noise outside of the intended Nyquist zone. Table 5 provides initial suggestions for prototyping purposes. Some empirical optimization may be needed to help compensate for actual PCB parasitics.

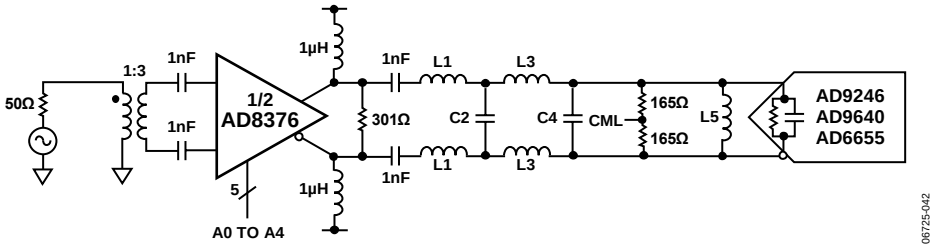


Figure 42. Narrow-Band IF Sampling Solution for Unbuffered ADC Applications

Table 5. Interface Filter Recommendations for Various IF Sampling Frequencies

Center Frequency	1 dB Bandwidth	L1	C2	L3	C4	L5
96 MHz	27 MHz	390 nH	5.6 pF	390 nH	25 pF	100 nH
140 MHz	30 MHz	330 nH	3.3 pF	330 nH	20 pF	56 nH
170 MHz	32 MHz	270 nH	2.7 pF	270 nH	20 pF	39 nH
211 MHz	32 MHz	220 nH	2.2 pF	220 nH	18 pF	27 nH

LAYOUT CONSIDERATIONS

Each amplifier has two output pins for each polarity, and they are oriented in an alternating fashion. When designing the board, care should be taken to minimize the parasitic capacitance due to the routing that connects the corresponding outputs together. A good practice is to avoid any ground or power plane under this routing region and under the chokes to minimize the parasitic capacitance.

CHARACTERIZATION TEST CIRCUITS

Differential-to-Differential Characterization

The S-parameter characterization for the AD8376 was performed using a dedicated differential input to differential output characterization board. Figure 45 shows the layout of the characterization board. The board was designed for optimum impedance matching into a 75 Ω system. Because both the input and output impedances of the AD8376 are 150 Ω differentially, 75 Ω impedance runs were used to match 75 Ω network analyzer port impedances. On-board 1 µH inductors were used for output biasing, and the output board traces were designed for minimum capacitance.

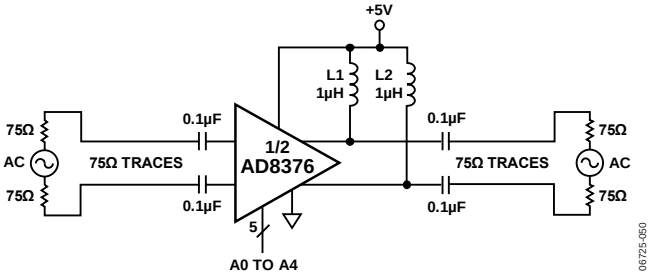


Figure 43. Test Circuit for S-Parameters on Dedicated 75 Ω Differential-to-Differential Board

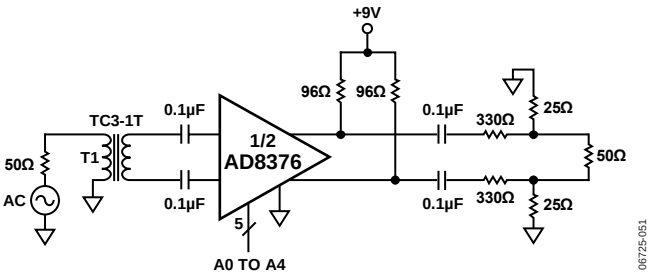


Figure 44. Test Circuit for Time Domain Measurements

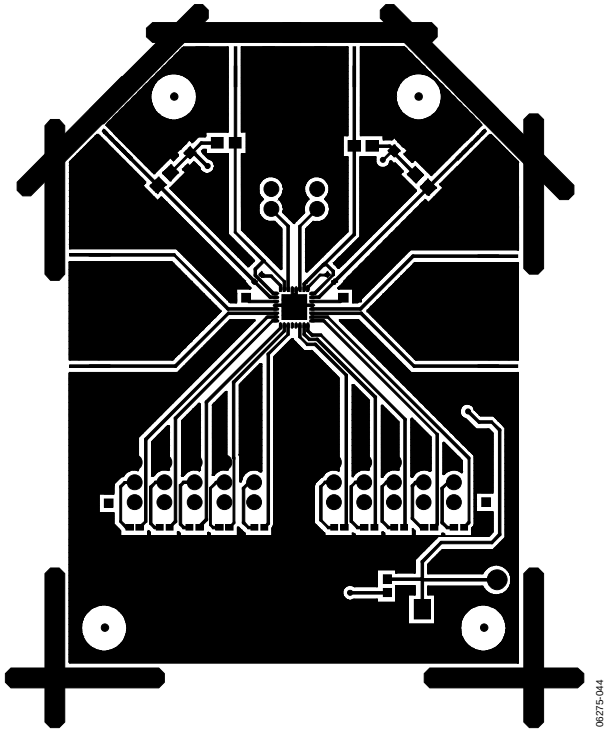


Figure 45. Differential-to-Differential Characterization Board Circuit Side Layout

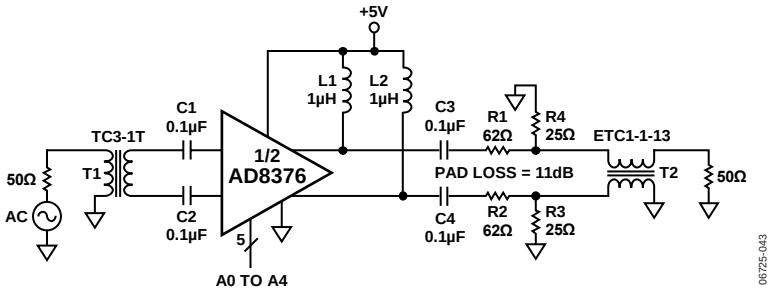


Figure 46. Test Circuit for Distortion, Gain, and Noise

EVALUATION BOARD

Figure 47 shows the schematic of the AD8376 evaluation board. The silkscreen and layout of the component and circuit sides are shown in Figure 48 through Figure 51. The board is powered by a single supply in the 4. 5 V to 5.5 V range. The power supply is decoupled by 10 µF and 0.1 µF capacitors at each power supply pin. Additional decoupling, in the form of a series resistor or inductor at the supply pins, can also be added. Table 6 details the various configuration options of the evaluation board.

The output pins of the AD8376 require supply biasing with 1 µH RF chokes. Both the input and output pins must be ac-coupled. These pins are converted to single-ended with a pair of baluns (Mini-Circuits® TC3-1T+ and M/A-COM ETC1-1-13). The baluns at the input, T1 and T2, are used to transform 50 Ω source impedances to the desired 150 Ω reference levels. The output baluns, T3 and T4, and the matching components are configured to provide 150 Ω to 50 Ω impedance transformations with insertion losses of about 11 dB.

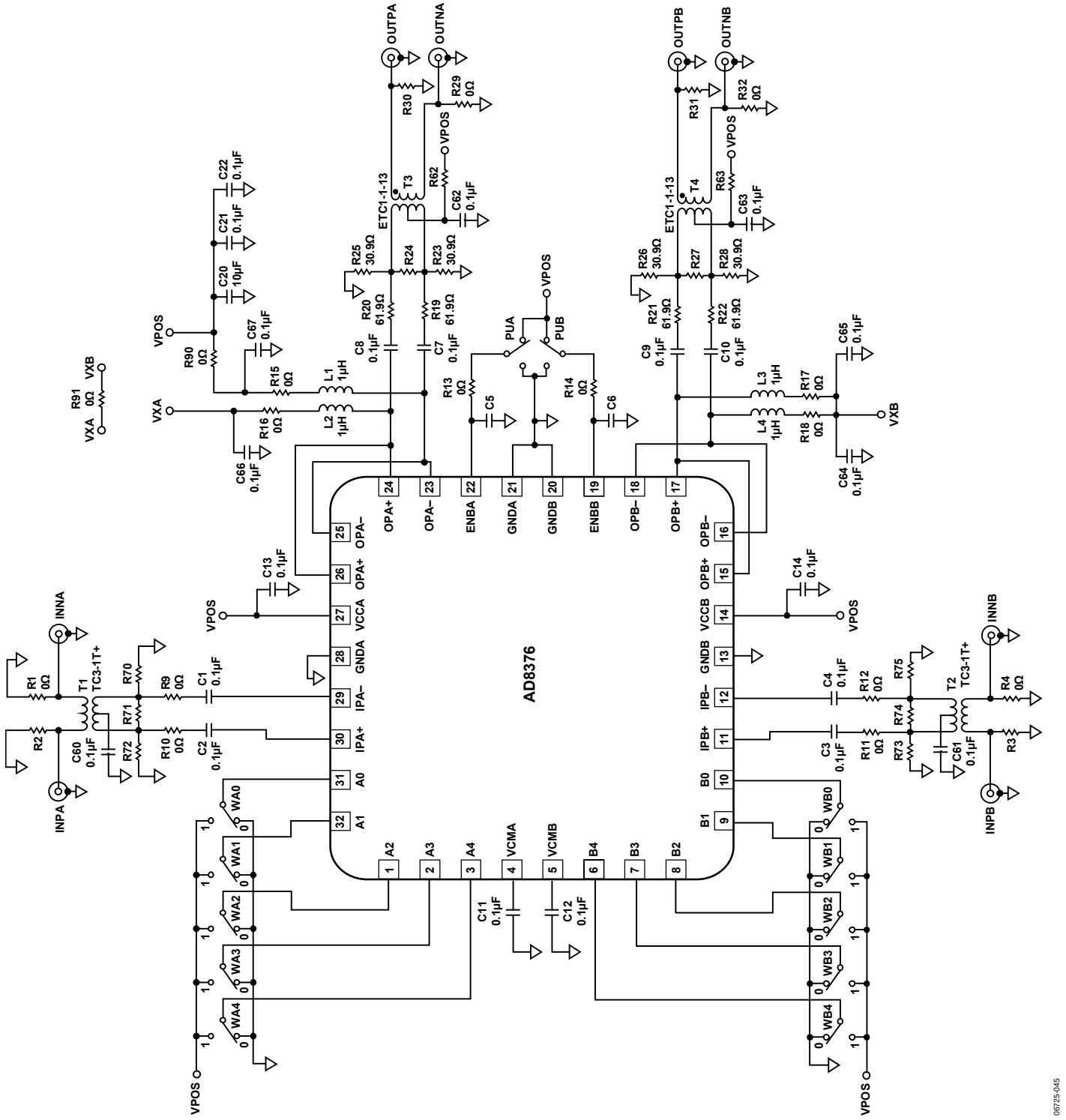


Figure 47. AD8376 Evaluation Board Schematic

Table 6. Evaluation Board Configuration Options

Components	Function	Default Conditions
C13, C14, C20 to C22, C64 to C67, R90, R91	Power Supply Decoupling. Nominal supply decoupling consists a 10 µF capacitor to ground followed by 0.1 µF capacitors to ground positioned as close to the device as possible.	C20 = 10 µF (size 3528) C13, C14 = 0.1 µF (size 0402) C21, C22, C64 to C67 = 0.1 µF (size 0603) R90, R91 = 0 Ω (size 0603)
T1, T2, C1 to C4, C61, C62, R1 to R4, R9 to R12, R70 to R75	Input Interface. T1 and T2 are 3:1 impedance ratio baluns to transform a 50 Ω single-ended input into a 150 Ω balanced differential signal. R1 and R4 ground one side of the differential drive interface for single-ended applications. R9 to R12 and R70 to R75 are provided for generic placement of matching components. C1 to C4 are dc blocks.	T1, T2 = TC3-1+ (Mini-Circuits) C1 to C4, C60, C61 = 0.1 µF (size 0402) R1, R4, R9 to R12 = 0 Ω (size 0402) R2, R3, R70 to R75 = open (size 0402)
T3, T4, C7 to C10, L1 to L4, R15 to R32, R62, R63, C62, C63	Output Interface. C7 to C10 are dc blocks. L1 to L4 provide dc biases for the outputs. R19 to R28 are provided for generic placement of matching components. The evaluation board is configured to provide a 150 Ω to 50 Ω impedance transformation with an insertion loss of about 11 dB. T3 and T4 are 1:1 impedance ratio baluns to transform the balanced differential signals to single-ended signals. R29 and R32 ground one side of the differential output interface for single-ended applications.	C7 to C10 = 0.1 µF (size 0402) L1 to L4 = 1 µH (size 0805) T3, T4 = ETC1-1-13 (M/A-COM) R19 to R22 = 61.9 Ω (size 0402) R23, R25, R26, R28 = 30.9 Ω (size 0402) R15 to R18 = 0 Ω (size 0603) R29, R32 = 0 Ω (size 0402) R24, R27, R30, R31, R62, R63 = open (size 0402) C62, C63 = 0.1 µF (size 0402)
PUA, PUB, R13, R14, C5, C6	Enable Interface. The AD8376 is enabled by applying a logic high voltage to the ENBA pin for Channel A or the ENBB pin for Channel B. Channel A is enabled when the PUA switch is set in the up position, connecting the ENBA pin to VPOS. Likewise, Channel B is enabled when the PUB switch is set in the up position, connecting the ENBB pin to VPOS. Both channels are disabled by setting the switches to the down position, connecting the ENBA and ENBB pins to GND.	PUA, PUB = installed R13, R14 = 0 Ω (size 0603) C5, C6 = open (size 0603)
WA0 to WA4, WB0 to WB4	Parallel Interface Control. Used to hardwire A0 through A4 and B0 through B4 to the desired gain. The bank of switches WA0 to WA4 set the binary gain code for Channel A. The bank of switches WB0 to WB4 set the binary gain code for Channel B. WA0 and WB0 represent the LSB for each of the respective channels.	WA0 to WA4, WB0 to WB4 = installed
C11, C12	Voltage Reference. Input common-mode voltage ac-coupled to ground by 0.1 µF capacitors, C11 and C12.	C11, C12 = 0.1 µF (size 0402)

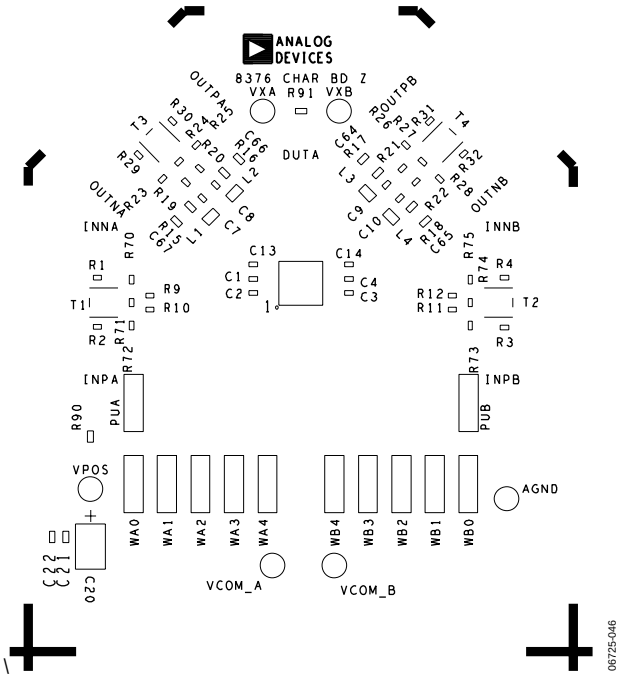


Figure 48. Component Side Silkscreen

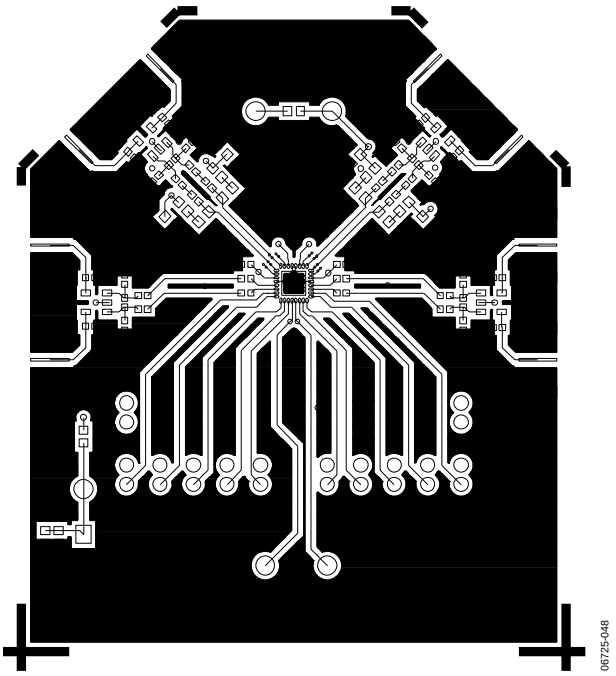


Figure 50. Component Side Layout

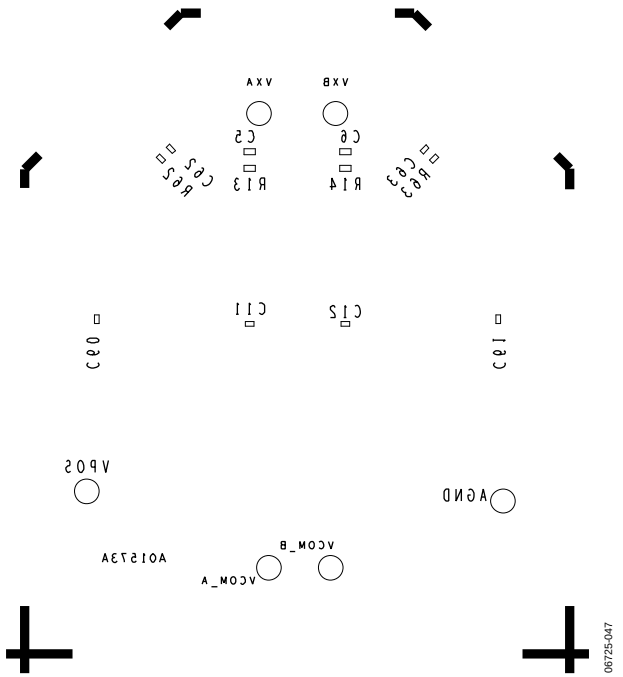


Figure 49. Circuit Side Silkscreen

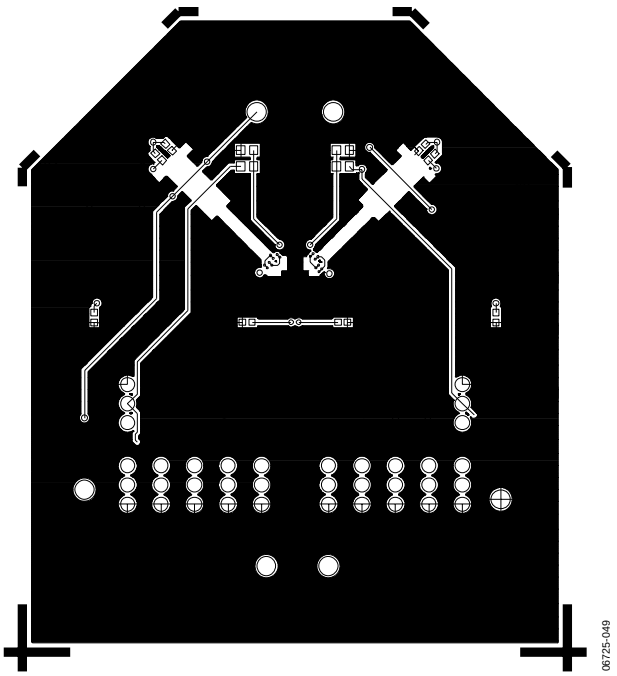


Figure 51. Circuit Side Layout

OUTLINE DIMENSIONS

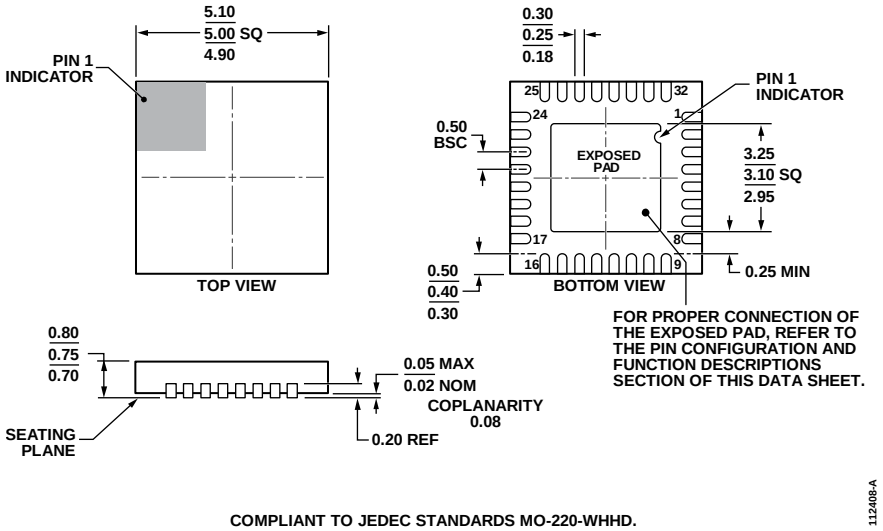


Figure 52. 32-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
5 mm × 5 mm Body, Very Very Thin Quad
(CP-32-7)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD8376ACPZ-WP	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package [LFCSP_WQ] , Waffle Pack	CP-32-7
AD8376ACPZ-R7	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package [LFCSP_WQ], 7″Tape and Reel	CP-32-7
AD8376-EVALZ		Evaluation Board	

[1] Z = RoHS Compliant Part.

NOTES