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- AN-1401: Instrumentation Amplifier Common-Mode Range: The Diamond Plot

Data Sheet

- AD8251: 10 MHz, 20 V/ μ s, G = 1, 2, 4, 8 *i*CMOS Programmable Gain Instrumentation Amplifier Data Sheet

Technical Books

- A Designer's Guide to Instrumentation Amplifiers, 3rd Edition, 2006

User Guides

- UG-925: Evaluating the AD8251 10 MHz, 20 V/ μ s, G = 1, 2, 4, 8 *ii*CMOS Programmable Gain Instrumentation Amplifier

Tools and Simulations

- AD8251 SPICE Macro Model

Reference Materials

Technical Articles

- Auto-Zero Amplifiers
- High-performance Adder Uses Instrumentation Amplifiers

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REVISION HISTORY

11/10—Rev. A to Rev. B

Changes to Voltage Offset, Offset RTI V_{OS} , Average TC	
Parameter in Table 2	3
Updated Outline Dimensions	23

5/08—Rev. 0 to Rev. A

Changes to Table 1	1
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Changes to Table 2	3
Changes to Table 3	6
Inserted Figure 17; Renumbered Sequentially	9
Inserted Figure 29	11
Changes to Timing for Latched Gain Mode Section	17

5/07—Revision 0: Initial Version

SPECIFICATIONS

$+V_S = 15\text{ V}$, $-V_S = -15\text{ V}$, $V_{REF} = 0\text{ V}$ @ $T_A = 25^\circ\text{C}$, $G = 1$, $R_L = 2\text{ k}\Omega$, unless otherwise noted.

Table 2.

Parameter	Conditions	Min	Typ	Max	Unit
COMMON-MODE REJECTION RATIO (CMRR)					
CMRR to 60 Hz with 1 k Ω Source Imbalance	$+IN = -IN = -10\text{ V to }+10\text{ V}$				
$G = 1$		80	98		dB
$G = 2$		86	104		dB
$G = 4$		92	110		dB
$G = 8$		98	110		dB
CMRR to 50 kHz	$+IN = -IN = -10\text{ V to }+10\text{ V}$				
$G = 1$		80			dB
$G = 2$		84			dB
$G = 4$		86			dB
$G = 8$		86			dB
NOISE					
Voltage Noise, 1 kHz, RTI					
$G = 1$				40	nV/ $\sqrt{\text{Hz}}$
$G = 2$				27	nV/ $\sqrt{\text{Hz}}$
$G = 4$				22	nV/ $\sqrt{\text{Hz}}$
$G = 8$				18	nV/ $\sqrt{\text{Hz}}$
0.1 Hz to 10 Hz, RTI					
$G = 1$				2.5	$\mu\text{V p-p}$
$G = 2$				2.5	$\mu\text{V p-p}$
$G = 4$				1.8	$\mu\text{V p-p}$
$G = 8$				1.2	$\mu\text{V p-p}$
Current Noise, 1 kHz			5		pA/ $\sqrt{\text{Hz}}$
Current Noise, 0.1 Hz to 10 Hz			60		pA p-p
VOLTAGE OFFSET					
Offset RTI V_{OS}	$G = 1, 2, 4, 8$		$\pm(70 + 200/G)$	$\pm(200 + 600/G)$	μV
Over Temperature	$T = -40^\circ\text{C to }+85^\circ\text{C}$		$\pm(90 + 300/G)$	$\pm(260 + 900/G)$	μV
Average TC	$T = -40^\circ\text{C to }+85^\circ\text{C}$		$\pm(0.6 + 1.5/G)$	$\pm(1.2 + 5/G)$	$\mu\text{V}/^\circ\text{C}$
Offset Referred to the Input vs. Supply (PSR)	$V_S = \pm 5\text{ V to } \pm 15\text{ V}$		$\pm(2 + 7/G)$	$\pm(6 + 20/G)$	$\mu\text{V/V}$
INPUT CURRENT					
Input Bias Current			5	30	nA
Over Temperature	$T = -40^\circ\text{C to }+85^\circ\text{C}$			40	nA
Average TC	$T = -40^\circ\text{C to }+85^\circ\text{C}$			400	pA/ $^\circ\text{C}$
Input Offset Current			5	30	nA
Over Temperature	$T = -40^\circ\text{C to }+85^\circ\text{C}$			30	nA
Average TC	$T = -40^\circ\text{C to }+85^\circ\text{C}$			160	pA/ $^\circ\text{C}$
DYNAMIC RESPONSE					
Small Signal -3 dB Bandwidth					
$G = 1$		10			MHz
$G = 2$		10			MHz
$G = 4$		8			MHz
$G = 8$		2.5			MHz
Settling Time 0.01%	$\Delta\text{OUT} = 10\text{ V step}$				
$G = 1$				615	ns
$G = 2$				460	ns
$G = 4$				460	ns
$G = 8$				625	ns

AD8251

Parameter	Conditions	Min	Typ	Max	Unit
Settling Time 0.001%	$\Delta\text{OUT} = 10\text{ V step}$				
G = 1				785	ns
G = 2				700	ns
G = 4				700	ns
G = 8				770	ns
Slew Rate					
G = 1		20			V/ μs
G = 2		30			V/ μs
G = 4		30			V/ μs
G = 8		30			V/ μs
Total Harmonic Distortion + Noise	f = 1 kHz, $R_L = 10\text{ k}\Omega$, $\pm 10\text{ V}$, G = 1, 10 Hz to 22 kHz band-pass filter		–110		dB
GAIN					
Gain Range	G = 1, 2, 4, 8	1		8	V/V
Gain Error	OUT = $\pm 10\text{ V}$				
G = 1				0.03	%
G = 2, 4, 8				0.04	%
Gain Nonlinearity	OUT = $-10\text{ V to }+10\text{ V}$				
G = 1	$R_L = 10\text{ k}\Omega$, 2 k Ω , 600 Ω			9	ppm
G = 2	$R_L = 10\text{ k}\Omega$, 2 k Ω , 600 Ω			12	ppm
G = 4	$R_L = 10\text{ k}\Omega$, 2 k Ω , 600 Ω			12	ppm
G = 8	$R_L = 10\text{ k}\Omega$, 2 k Ω , 600 Ω			15	ppm
Gain vs. Temperature	All gains		3	10	ppm/ $^{\circ}\text{C}$
INPUT					
Input Impedance					
Differential			5.3 0.5		G Ω pF
Common Mode			1.25 2		G Ω pF
Input Operating Voltage Range	$V_S = \pm 5\text{ V to } \pm 15\text{ V}$	$-V_S + 1.5$		$+V_S - 1.5$	V
Over Temperature	T = $-40^{\circ}\text{C to }+85^{\circ}\text{C}$	$-V_S + 1.6$		$+V_S - 1.7$	V
OUTPUT					
Output Swing		–13.5		+13.5	V
Over Temperature	T = $-40^{\circ}\text{C to }+85^{\circ}\text{C}$	–13.5		+13.5	V
Short-Circuit Current			37		mA
REFERENCE INPUT					
R_{IN}			20		k Ω
I_{IN}	+IN, –IN, REF = 0			1	μA
Voltage Range		$-V_S$		$+V_S$	V
Gain to Output			1 ± 0.0001		V/V
DIGITAL LOGIC					
Digital Ground Voltage, DGND	Referred to GND	$-V_S + 4.25$	0	$+V_S - 2.7$	V
Digital Input Voltage Low	Referred to GND	DGND		2.1	V
Digital Input Voltage High	Referred to GND	2.8		$+V_S$	V
Digital Input Current			1		μA
Gain Switching Time ¹				325	ns
t_{SU}	See Figure 3 timing diagram	20			ns
t_{HD}	See Figure 3 timing diagram	10			ns
$t_{\overline{WR-LOW}}$	See Figure 3 timing diagram	20			ns
$t_{\overline{WR-HIGH}}$	See Figure 3 timing diagram	40			ns

Parameter	Conditions	Min	Typ	Max	Unit
POWER SUPPLY					
Operating Range		±5		±15	V
Quiescent Current, +I _s			4.1	4.5	mA
Quiescent Current, -I _s			3.7	4.5	mA
Over Temperature	T = -40°C to +85°C			4.5	mA
TEMPERATURE RANGE					
Specified Performance		-40		+85	°C

¹ Add time for the output to slew and settle to calculate the total time for a gain change.

TIMING DIAGRAM

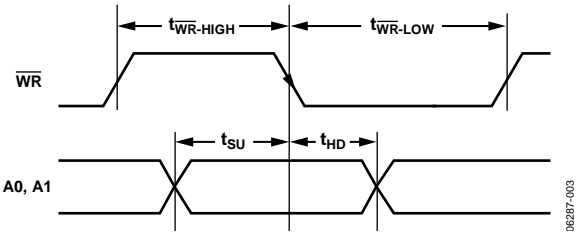


Figure 3. Timing Diagram for Latched Gain Mode (See the Timing for Latched Gain Mode Section)

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage	±17 V
Power Dissipation	See Figure 4
Output Short-Circuit Current	Indefinite ¹
Common-Mode Input Voltage	+V _S + 13 V to -V _S - 13 V
Differential Input Voltage	+V _S + 13 V, -V _S - 13 V ²
Digital Logic Inputs	±V _S
Storage Temperature Range	-65°C to +125°C
Operating Temperature Range ³	-40°C to +85°C
Lead Temperature (Soldering, 10 sec)	300°C
Junction Temperature	140°C
θ _{JA} (Four-Layer JEDEC Standard Board)	112°C/W
Package Glass Transition Temperature	140°C

¹ Assumes the load is referenced to midsupply.

² Current must be kept to less than 6 mA.

³ Temperature for specified performance is -40°C to +85°C. For performance to +125°C, see the Typical Performance Characteristics section.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

MAXIMUM POWER DISSIPATION

The maximum safe power dissipation in the AD8251 package is limited by the associated rise in junction temperature (T_J) on the die. The plastic encapsulating the die locally reaches the junction temperature. At approximately 140°C, which is the glass transition temperature, the plastic changes its properties. Even temporarily exceeding this temperature limit can change the stresses that the package exerts on the die, permanently shifting the parametric performance of the AD8251. Exceeding a junction temperature of 140°C for an extended period can result in changes in silicon devices, potentially causing failure.

The still air thermal properties of the package and PCB (θ_{JA}), the ambient temperature (T_A), and the total power dissipated in the package (P_D) determine the junction temperature of the die. The junction temperature is calculated as

$$T_J = T_A + (P_D \times \theta_{JA})$$

The power dissipated in the package (P_D) is the sum of the quiescent power dissipation and the power dissipated in the package due to the load drive for all outputs. The quiescent power is the voltage between the supply pins (V_S) times the quiescent current (I_S). Assuming the load (R_L) is referenced to midsupply, the total drive power is V_S/2 × I_{OUT}, some of which is dissipated in the package and some in the load (V_{OUT} × I_{OUT}).

The difference between the total drive power and the load power is the drive power dissipated in the package.

$$P_D = \text{Quiescent Power} + (\text{Total Drive Power} - \text{Load Power})$$

$$P_D = (V_S \times I_S) + \left(\frac{V_S}{2} \times \frac{V_{OUT}}{R_L} \right) - \frac{V_{OUT}^2}{R_L}$$

In single-supply operation with R_L referenced to -V_S, the worst case is V_{OUT} = V_S/2.

Airflow increases heat dissipation, effectively reducing θ_{JA}. In addition, more metal directly in contact with the package leads from metal traces, through holes, ground, and power planes reduces the θ_{JA}.

Figure 4 shows the maximum safe power dissipation in the package vs. the ambient temperature on a four-layer JEDEC standard board.

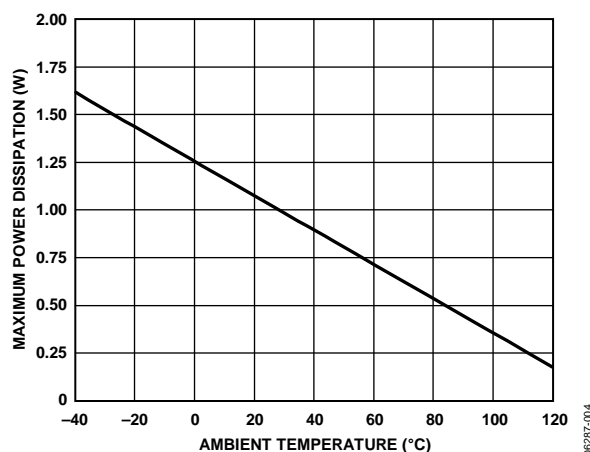


Figure 4. Maximum Power Dissipation vs. Ambient Temperature

ESD CAUTION



ESD (electrostatic discharge) sensitive device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

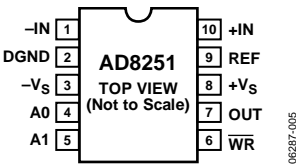


Figure 5. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	–IN	Inverting Input Terminal. True differential input.
2	DGND	Digital Ground.
3	–Vs	Negative Supply Terminal.
4	A0	Gain Setting Pin (LSB).
5	A1	Gain Setting Pin (MSB).
6	$\overline{\text{WR}}$	Write Enable.
7	OUT	Output Terminal.
8	+Vs	Positive Supply Terminal.
9	REF	Reference Voltage Terminal.
10	+IN	Noninverting Input Terminal. True differential input.

TYPICAL PERFORMANCE CHARACTERISTICS

$T_A = 25^\circ\text{C}$, $+V_S = +15\text{ V}$, $-V_S = -15\text{ V}$, $R_L = 10\text{ k}\Omega$, unless otherwise noted.

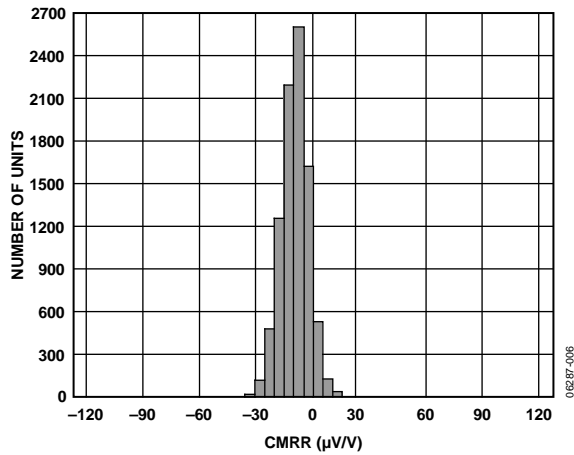


Figure 6. Typical Distribution of CMRR, $G = 1$

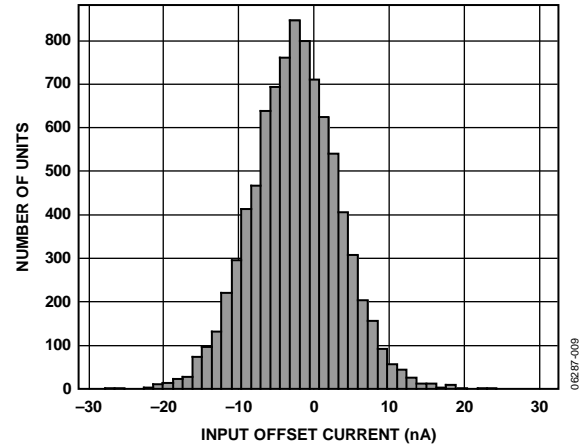


Figure 9. Typical Distribution of Input Offset Current

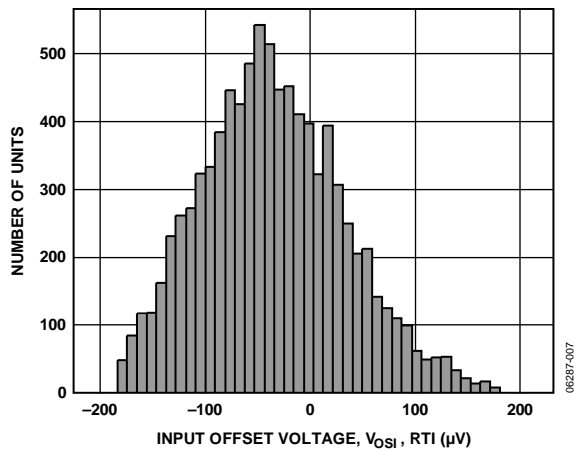


Figure 7. Typical Distribution of Offset Voltage, V_{OSI}

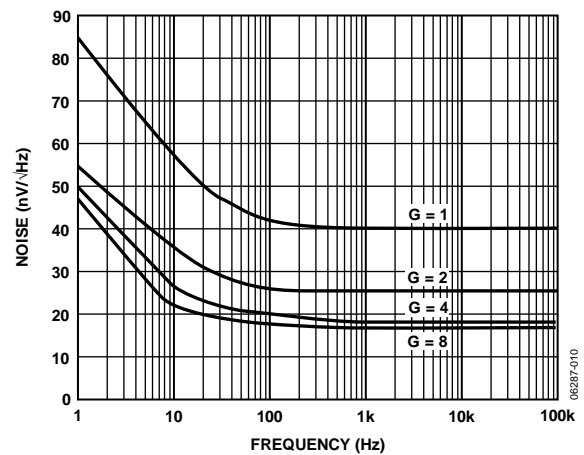


Figure 10. Voltage Spectral Density Noise vs. Frequency

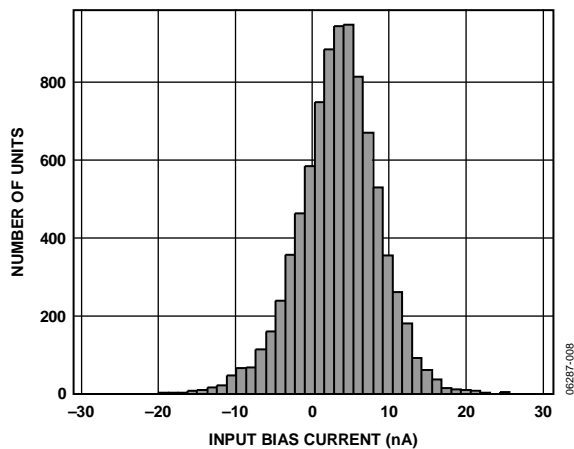


Figure 8. Typical Distribution of Input Bias Current

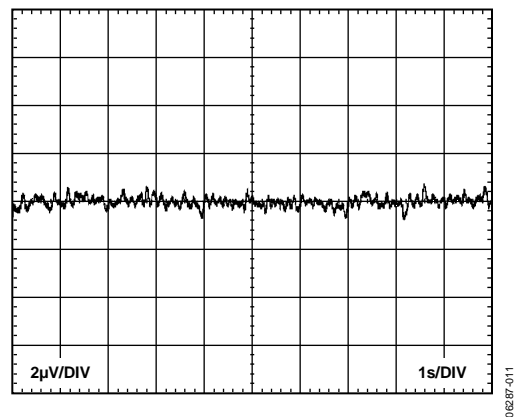


Figure 11. 0.1 Hz to 10 Hz RTI Voltage Noise, $G = 1$

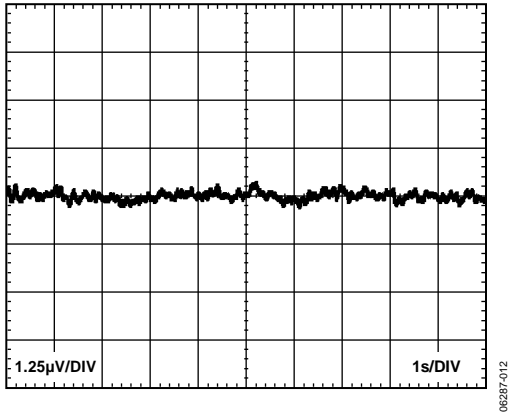


Figure 12. 0.1 Hz to 10 Hz RTI Voltage Noise, G = 8

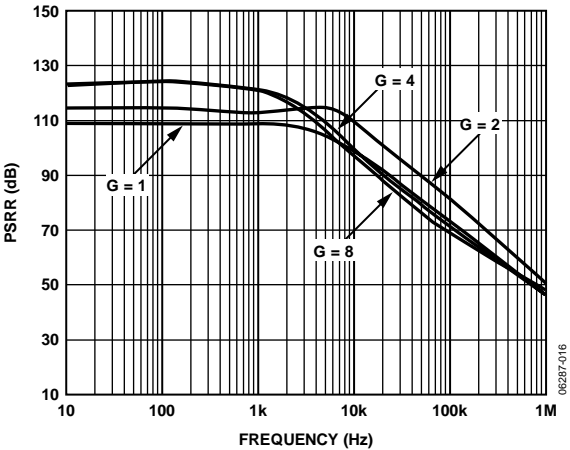


Figure 15. Positive PSRR vs. Frequency, RTI

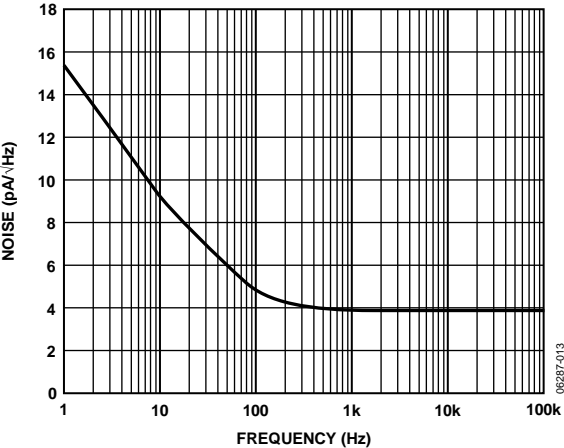


Figure 13. Current Noise Spectral Density vs. Frequency

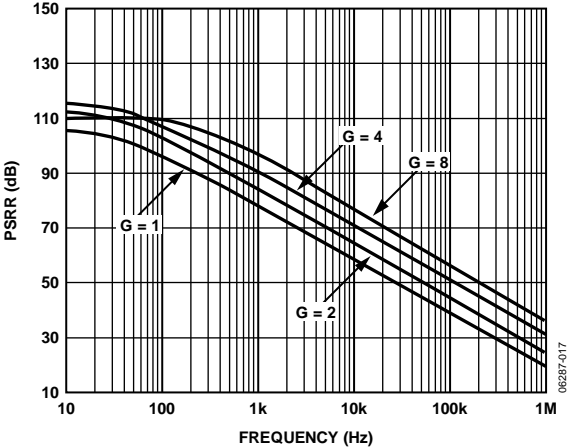


Figure 16. Negative PSRR vs. Frequency, RTI

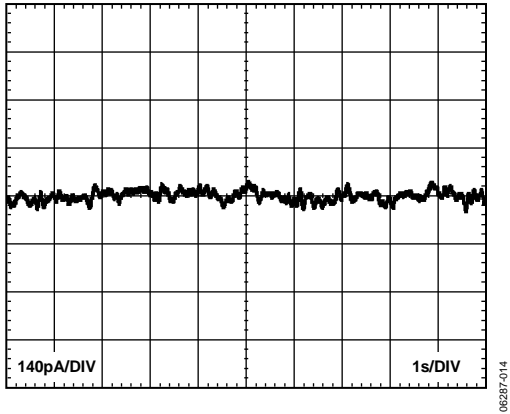


Figure 14. 0.1 Hz to 10 Hz Current Noise

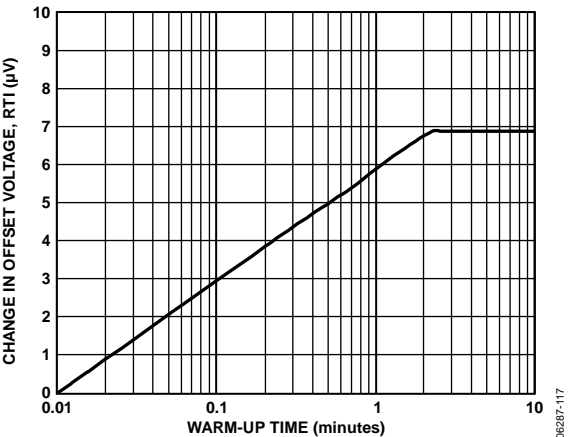


Figure 17. Change in Offset Voltage, RTI vs. Warmup Time

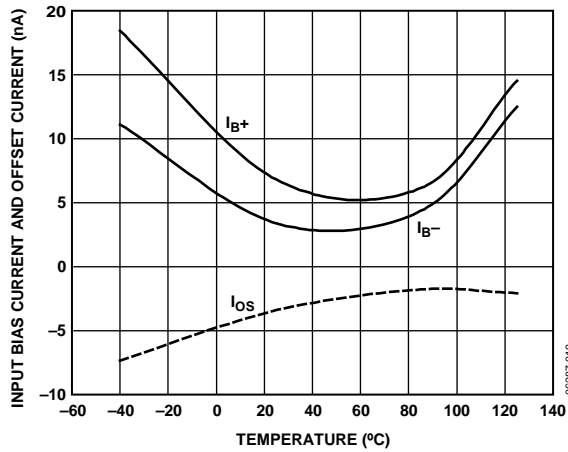


Figure 18. Input Bias Current and Offset Current vs. Temperature

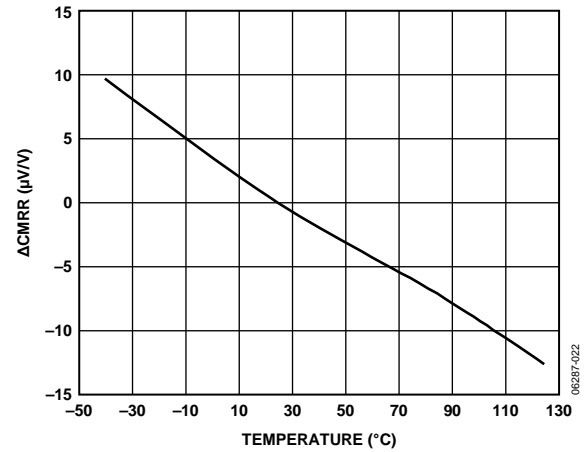


Figure 21. Δ CMRR vs. Temperature, $G = 1$

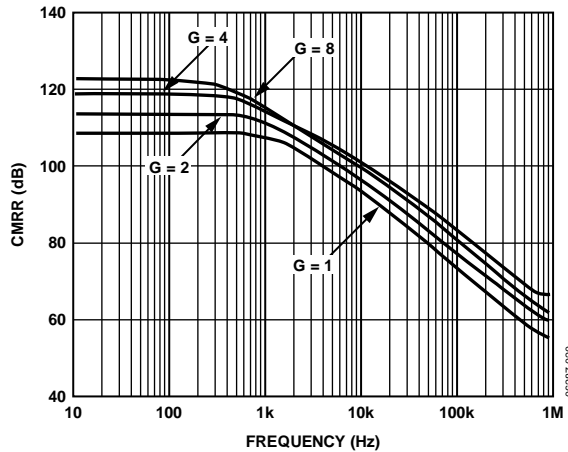


Figure 19. CMRR vs. Frequency

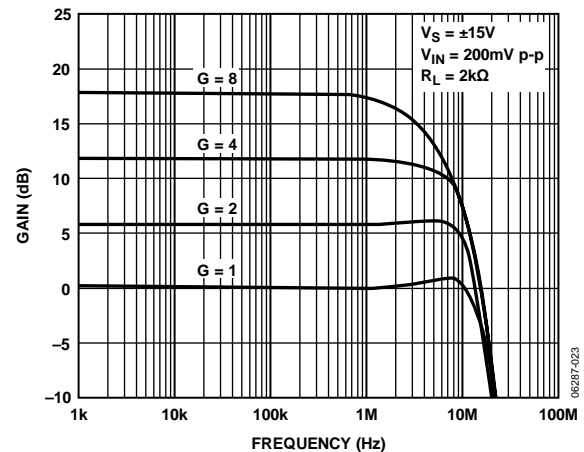


Figure 22. Gain vs. Frequency

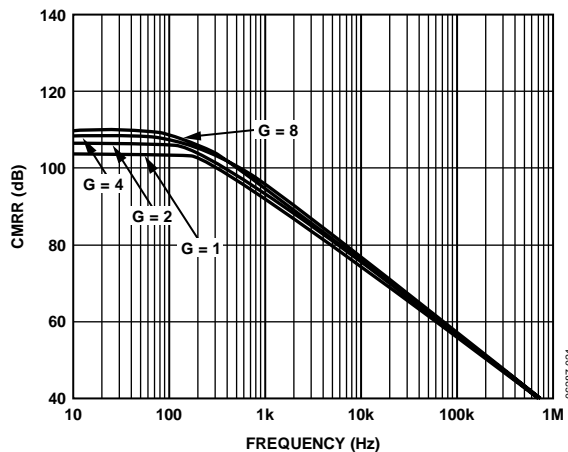


Figure 20. CMRR vs. Frequency, 1 k Ω Source Imbalance

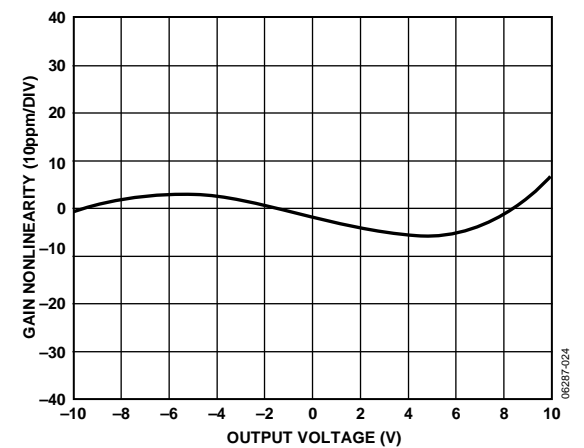


Figure 23. Gain Nonlinearity vs. Output Voltage, $G = 1$, $R_L = 10\text{ k}\Omega$, $2\text{ k}\Omega$, $600\text{ }\Omega$

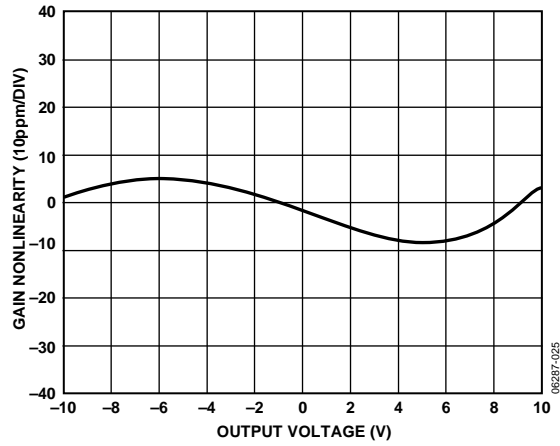


Figure 24. Gain Nonlinearity vs. Output Voltage, $G = 2$, $R_L = 10\text{ k}\Omega$, $2\text{ k}\Omega$, 600Ω

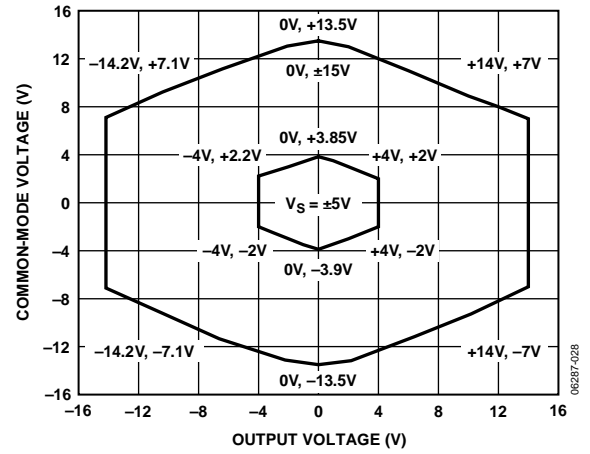


Figure 27. Input Common-Mode Voltage Range vs. Output Voltage, $G = 1$

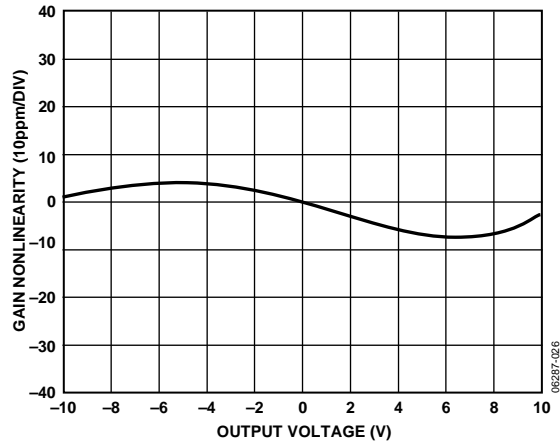


Figure 25. Gain Nonlinearity vs. Output Voltage, $G = 4$, $R_L = 10\text{ k}\Omega$, $2\text{ k}\Omega$, 600Ω

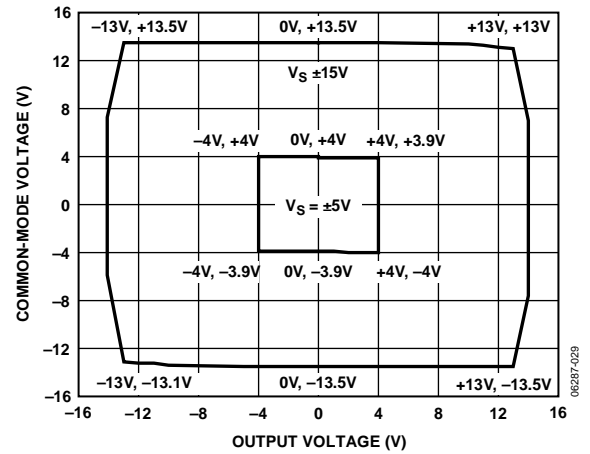


Figure 28. Input Common-Mode Voltage Range vs. Output Voltage, $G = 8$

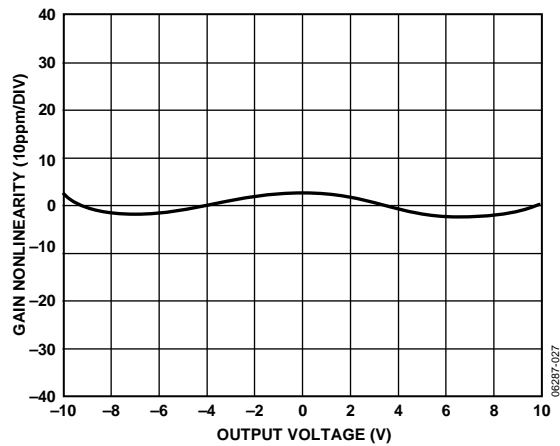


Figure 26. Gain Nonlinearity vs. Output Voltage, $G = 8$, $R_L = 10\text{ k}\Omega$, $2\text{ k}\Omega$, 600Ω

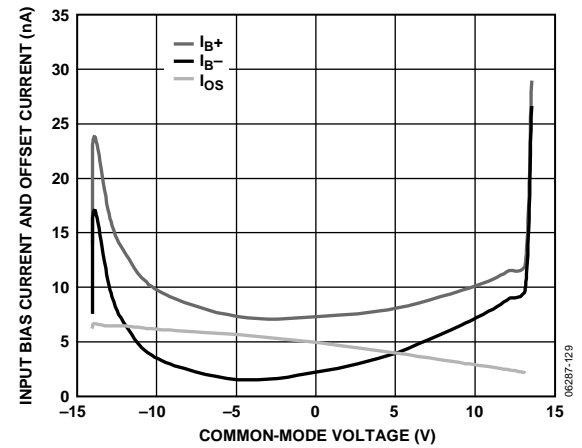


Figure 29. Input Bias Current and Offset Current vs. Common-Mode Voltage

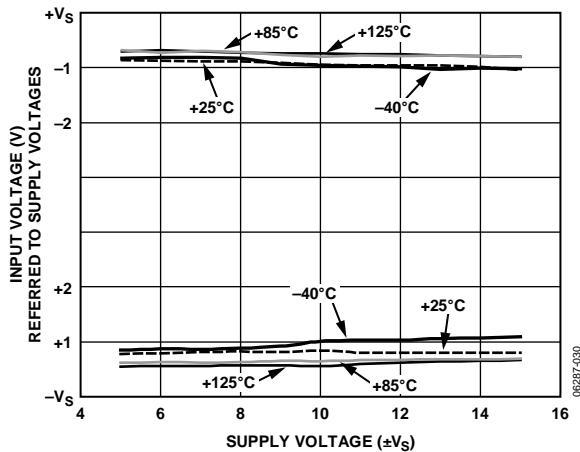


Figure 30. Input Voltage Limit vs. Supply Voltage, $G = 1$, $V_{REF} = 0$ V, $R_L = 10$ k Ω

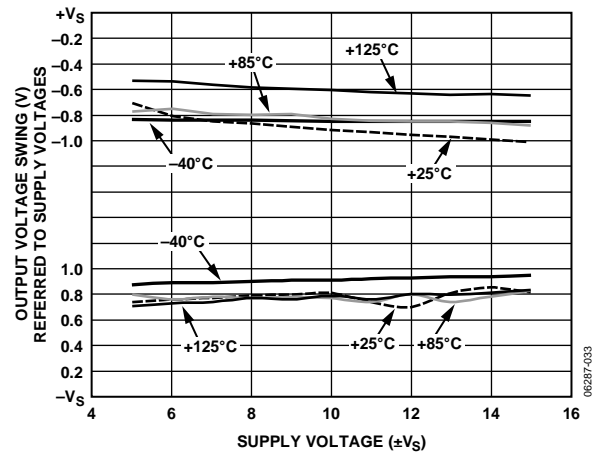


Figure 33. Output Voltage Swing vs. Supply Voltage, $G = 8$, $R_L = 10$ k Ω

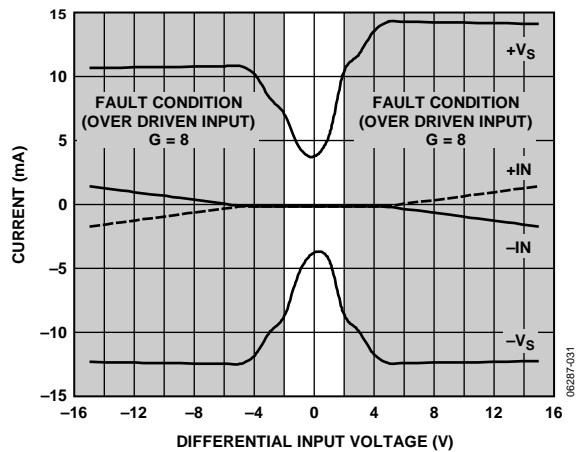


Figure 31. Fault Current Draw vs. Input Voltage, $G = 8$, $R_L = 10$ k Ω

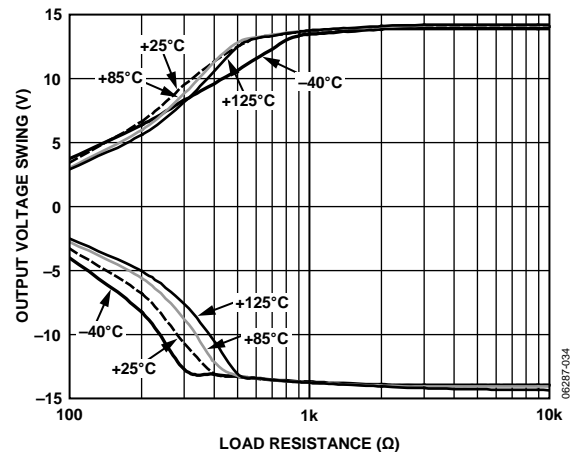


Figure 34. Output Voltage Swing vs. Load Resistance

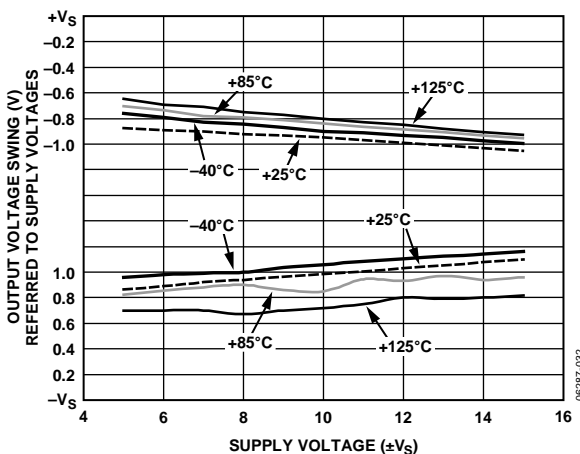


Figure 32. Output Voltage Swing vs. Supply Voltage, $G = 8$, $R_L = 2$ k Ω

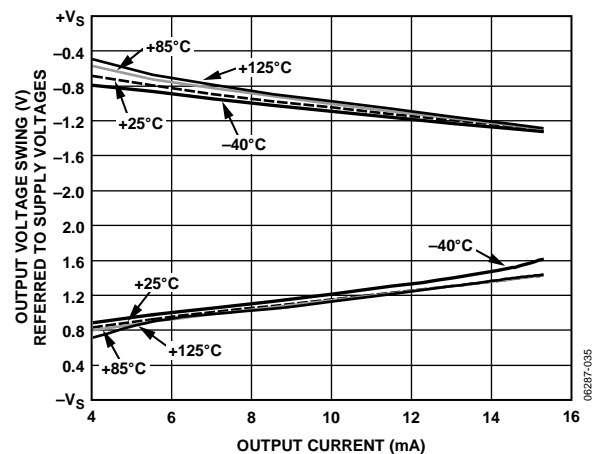


Figure 35. Output Voltage Swing vs. Output Current

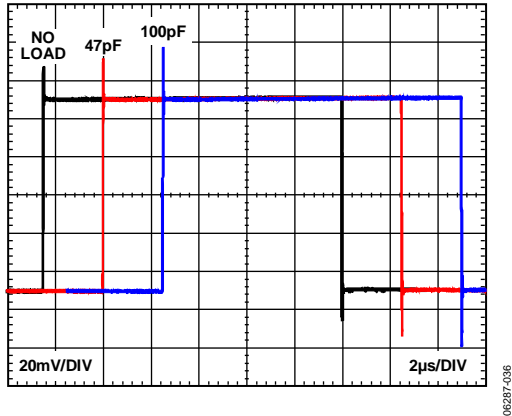


Figure 36. Small Signal Pulse Response for Various Capacitive Loads

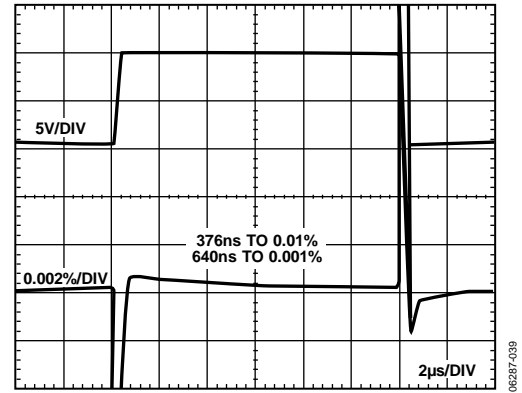


Figure 39. Large Signal Pulse Response and Settling Time,
 $G = 4$, $R_L = 10\text{ k}\Omega$

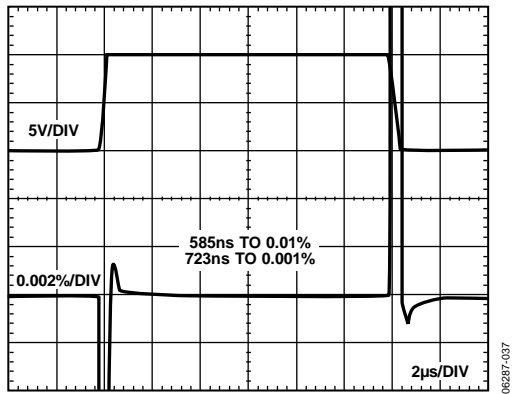


Figure 37. Large Signal Pulse Response and Settling Time,
 $G = 1$, $R_L = 10\text{ k}\Omega$

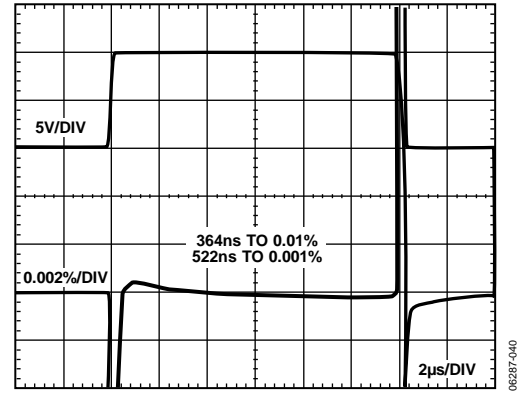


Figure 40. Large Signal Pulse Response and Settling Time,
 $G = 8$, $R_L = 10\text{ k}\Omega$

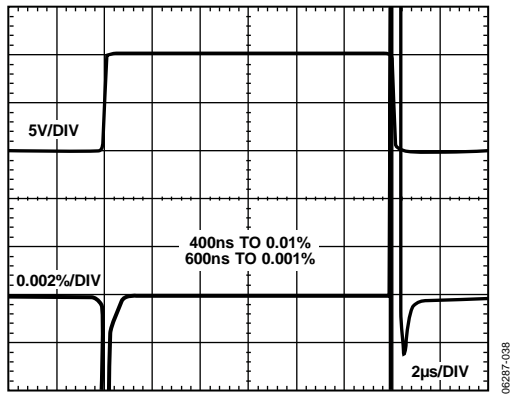


Figure 38. Large Signal Pulse Response and Settling Time,
 $G = 2$, $R_L = 10\text{ k}\Omega$

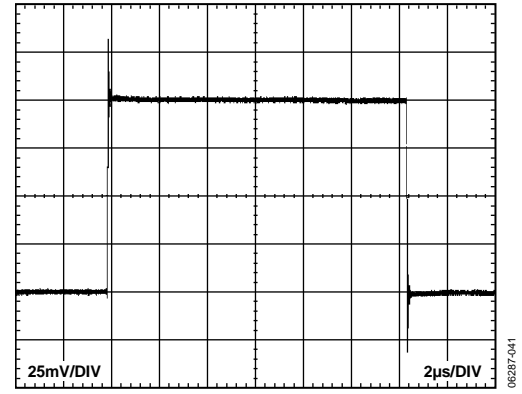


Figure 41. Small Signal Response,
 $G = 1$, $R_L = 2\text{ k}\Omega$, $C_L = 100\text{ pF}$

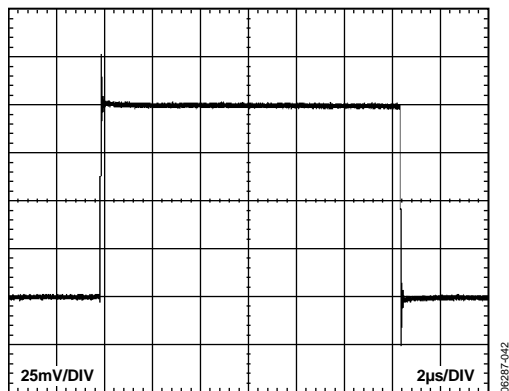


Figure 42. Small Signal Response,
 $G = 2$, $R_L = 2\text{ k}\Omega$, $C_L = 100\text{ pF}$

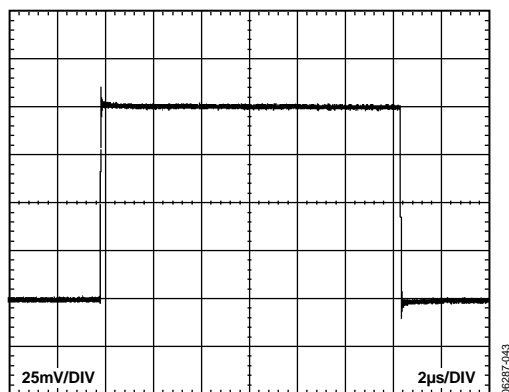


Figure 43. Small Signal Response,
 $G = 4$, $R_L = 2\text{ k}\Omega$, $C_L = 100\text{ pF}$

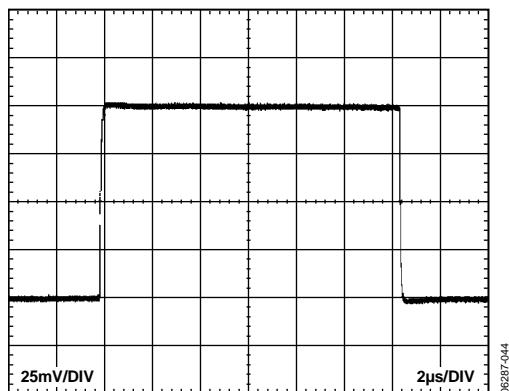


Figure 44. Small Signal Response,
 $G = 8$, $R_L = 2\text{ k}\Omega$, $C_L = 100\text{ pF}$

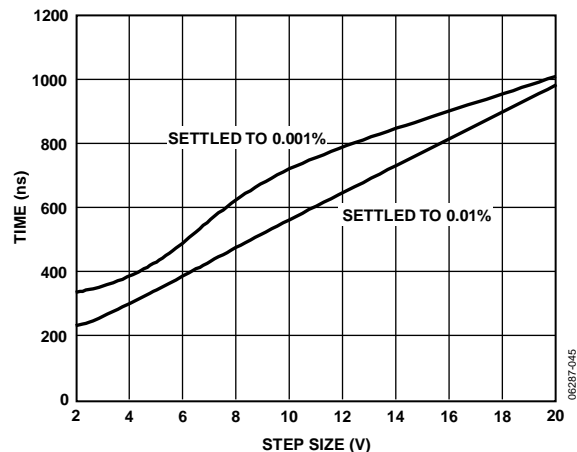


Figure 45. Settling Time vs. Step Size, $G = 1$, $R_L = 10\text{ k}\Omega$

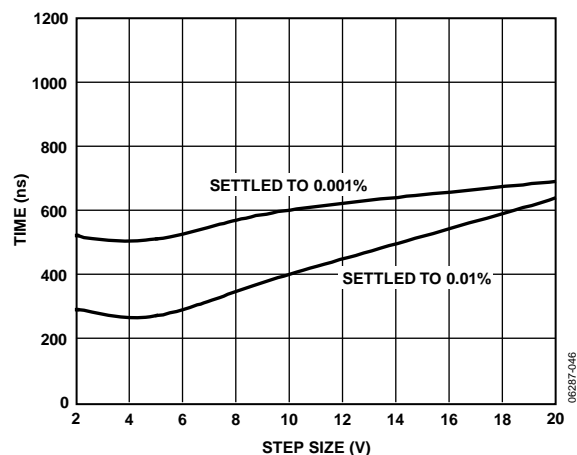


Figure 46. Settling Time vs. Step Size, $G = 2$, $R_L = 10\text{ k}\Omega$

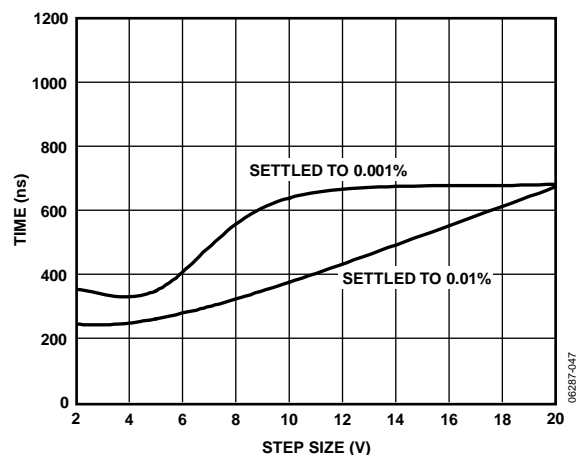


Figure 47. Settling Time vs. Step Size, $G = 4$, $R_L = 10\text{ k}\Omega$

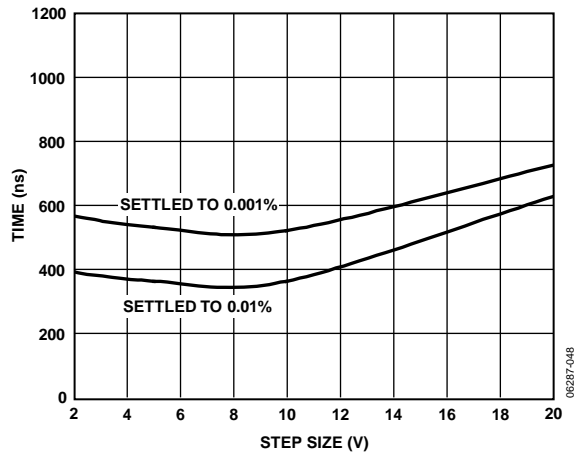


Figure 48. Settling Time vs. Step Size, $G = 8$, $R_L = 10\text{ k}\Omega$

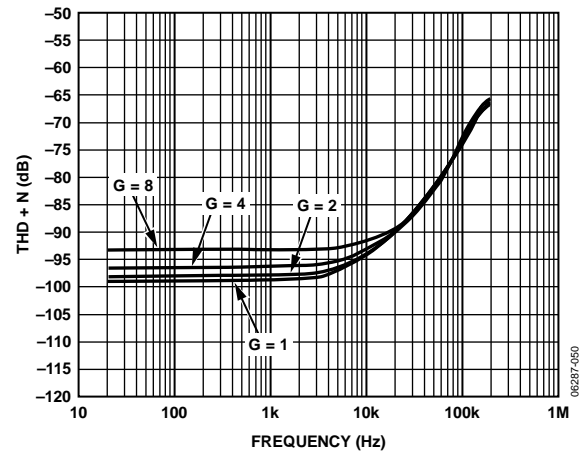


Figure 50. Total Harmonic Distortion + Noise vs. Frequency, 10 Hz to 500 kHz Band-Pass Filter, $R_L = 2\text{ k}\Omega$

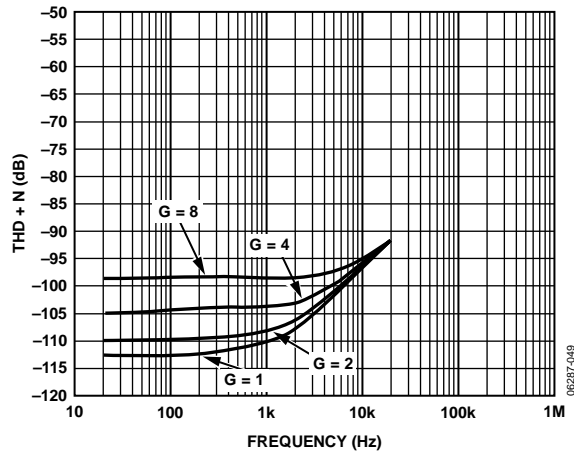


Figure 49. Total Harmonic Distortion + Noise vs. Frequency, 10 Hz to 22 kHz Band-Pass Filter, $R_L = 2\text{ k}\Omega$

THEORY OF OPERATION

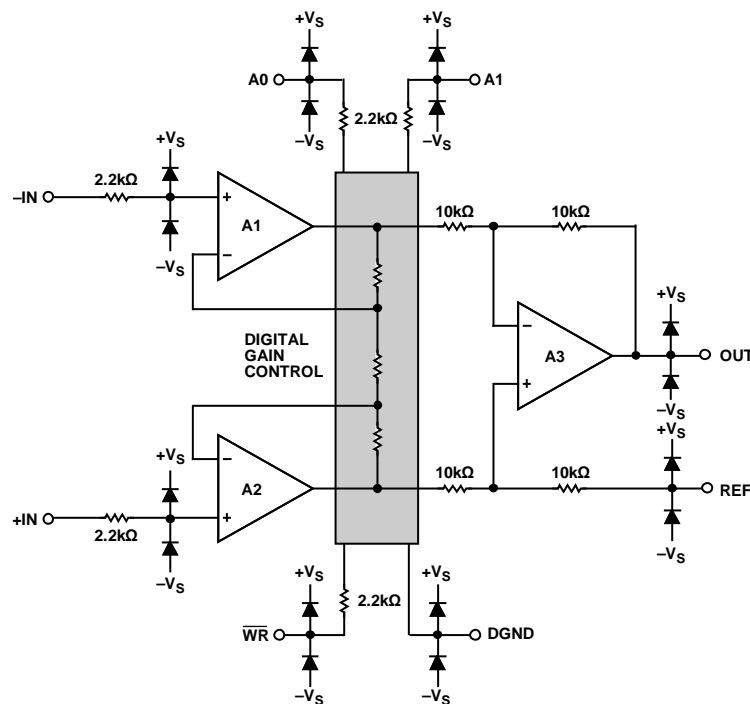


Figure 51. Simplified Schematic

The AD8251 is a monolithic instrumentation amplifier based on the classic 3-op-amp topology, as shown in Figure 51. It is fabricated on the Analog Devices, Inc., proprietary *iCMOS*® process that provides precision, linear performance, and a robust digital interface. A parallel interface allows users to digitally program gains of 1, 2, 4, and 8. Gain control is achieved by switching resistors in an internal, precision resistor array (as shown in Figure 51). Although the AD8251 has a voltage feedback topology, the gain bandwidth product increases for gains of 1, 2, and 4 because each gain has its own frequency compensation. This results in maximum bandwidth at higher gains.

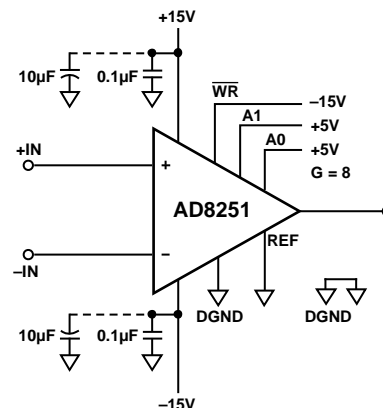
All internal amplifiers employ distortion cancellation circuitry and achieve high linearity and ultralow THD. Laser trimmed resistors allow for a maximum gain error of less than 0.03% for $G = 1$ and minimum CMRR of 98 dB for $G = 8$. A pinout optimized for high CMRR over frequency enables the AD8251 to offer a guaranteed minimum CMRR over frequency of 80 dB at 50 kHz ($G = 1$). The balanced input reduces the parasitics that, in the past, adversely affected CMRR performance.

GAIN SELECTION

Logic low and logic high voltage limits are listed in the Specifications section. Typically, logic low is 0 V and logic high is 5 V; both voltages are measured with respect to DGND. See Table 2 for the permissible voltage range of DGND. The gain of the AD8251 can be set using two methods.

Transparent Gain Mode

The easiest way to set the gain is to program it directly via a logic high or logic low voltage applied to A0 and A1. Figure 52 shows an example of this gain setting method, referred to throughout the data sheet as transparent gain mode. Tie \overline{WR} to the negative supply to engage transparent gain mode. In this mode, any change in voltage applied to A0 and A1 from logic low to logic high, or vice versa, immediately results in a gain change. Table 5 is the truth table for transparent gain mode, and Figure 52 shows the AD8251 configured in transparent gain mode.



NOTE:
1. IN TRANSPARENT GAIN MODE, \overline{WR} IS TIED TO $-V_S$. THE VOLTAGE LEVELS ON A0 AND A1 DETERMINE THE GAIN. IN THIS EXAMPLE, BOTH A0 AND A1 ARE SET TO LOGIC HIGH, RESULTING IN A GAIN OF 8.

Figure 52. Transparent Gain Mode, A0 and A1 = High, $G = 8$

Table 5. Truth Table Logic Levels for Transparent Gain Mode

WR	A1	A0	Gain
$-V_S$	Low	Low	1
$-V_S$	Low	High	2
$-V_S$	High	Low	4
$-V_S$	High	High	8

Latched Gain Mode

Some applications have multiple programmable devices such as multiplexers or other programmable gain instrumentation amplifiers on the same PCB. In such cases, devices can share a data bus. The gain of the AD8251 can be set using $\overline{\text{WR}}$ as a latch, allowing other devices to share A0 and A1. Figure 53 shows a schematic using this method, known as latched gain mode. The AD8251 is in this mode when $\overline{\text{WR}}$ is held at logic high or logic low, typically 5 V and 0 V, respectively. The voltages on A0 and A1 are read on the downward edge of the $\overline{\text{WR}}$ signal as it transitions from logic high to logic low. This latches in the logic levels on A0 and A1, resulting in a gain change. See the truth table in Table 6 for more information on these gain changes.

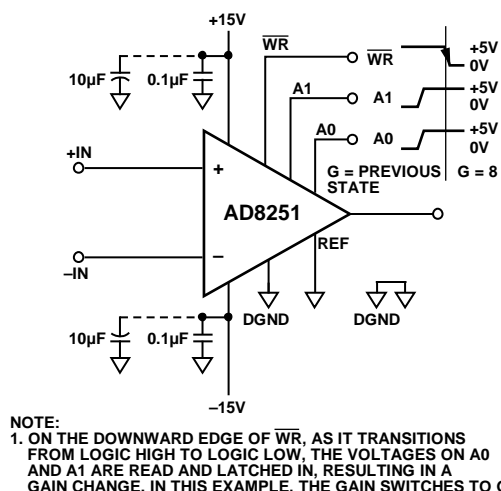
Figure 53. Latched Gain Mode, $G = 8$

Table 6. Truth Table Logic Levels for Latched Gain Mode

WR	A1	A0	Gain
High to low	Low	Low	Change to 1
High to low	Low	High	Change to 2
High to low	High	Low	Change to 4
High to low	High	High	Change to 8
Low to low	X ¹	X ¹	No change
Low to high	X ¹	X ¹	No change
High to high	X ¹	X ¹	No change

¹ X = don't care.

On power-up, the AD8251 defaults to a gain of 1 when in latched gain mode. In contrast, if the AD8251 is configured in transparent gain mode, it starts at the gain indicated by the voltage levels on A0 and A1 at power-up.

Timing for Latched Gain Mode

In latched gain mode, logic levels at A0 and A1 must be held for a minimum setup time, t_{SU} , before the downward edge of $\overline{\text{WR}}$ latches in the gain. Similarly, they must be held for a minimum hold time of t_{HD} after the downward edge of $\overline{\text{WR}}$ to ensure that the gain is latched in correctly. After t_{HD} , A0 and A1 can change logic levels, but the gain does not change (until the next downward edge of $\overline{\text{WR}}$). The minimum duration that $\overline{\text{WR}}$ can be held high is $t_{\text{WR-HIGH}}$, and the minimum duration that $\overline{\text{WR}}$ can be held low is $t_{\text{WR-LOW}}$. Digital timing specifications are listed in Table 2. The time required for a gain change is dominated by the settling time of the amplifier. A timing diagram is shown in Figure 54.

When sharing a data bus with other devices, logic levels applied to those devices can potentially feed through to the output of the AD8251. Feedthrough can be minimized by decreasing the edge rate of the logic signals. Furthermore, careful layout of the PCB also reduces coupling between the digital and analog portions of the board. Pull-up or pull-down resistors should be used to provide a well-defined voltage at the A0 and A1 pins.

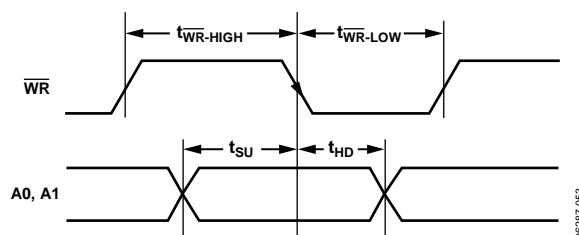


Figure 54. Timing Diagram for Latched Gain Mode

AD8251

POWER SUPPLY REGULATION AND BYPASSING

The AD8251 has high PSRR. However, for optimal performance, a stable dc voltage should be used to power the instrumentation amplifier. Noise on the supply pins can adversely affect performance. As in all linear circuits, bypass capacitors must be used to decouple the amplifier.

Place a 0.1 μF capacitor close to each supply pin. A 10 μF tantalum capacitor can be used farther away from the part (see Figure 55) and, in most cases, it can be shared by other precision integrated circuits.

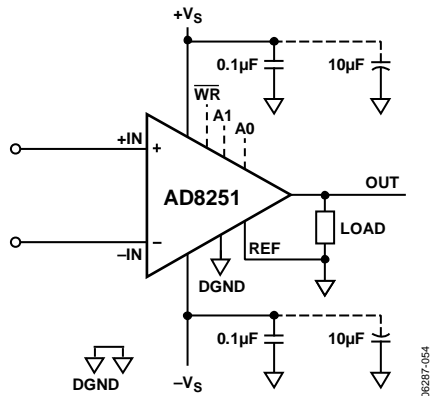


Figure 55. Supply Decoupling, REF, and Output Referred to Ground

INPUT BIAS CURRENT RETURN PATH

The AD8251 input bias current must have a return path to its local analog ground. When the source, such as a thermocouple, cannot provide a return current path, one should be created (see Figure 56).

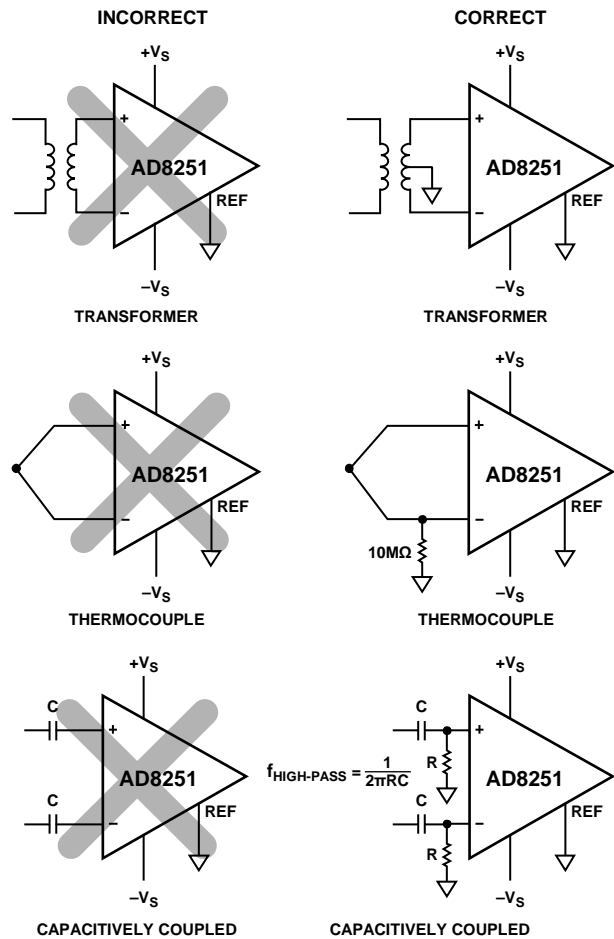


Figure 56. Creating an I_{BIAS} Return Path

INPUT PROTECTION

All terminals of the AD8251 are protected against ESD. Note that 2.2 k Ω series resistors precede the ESD diodes as shown in Figure 51. The resistors limit current into the diodes and allow for dc overload conditions 13 V above the positive supply and 13 V below the negative supply. An external resistor should be used in series with each input to limit current for voltages greater than 13 V beyond either supply rail. In either scenario, the AD8251 safely handles a continuous 6 mA current at room temperature. For applications where the AD8251 encounters extreme overload voltages, external series resistors and low leakage diode clamps, such as BAV199Ls, FJH1100s, or SP720s, should be used.

RF INTERFERENCE

RF rectification is often a problem when amplifiers are used in applications where there are strong RF signals. The disturbance can appear as a small dc offset voltage. High frequency signals can be filtered with a low-pass RC network placed at the input of the instrumentation amplifier, as shown in Figure 58. The filter limits the input signal bandwidth according to the following relationship:

$$FilterFreq_{DIFF} = \frac{1}{2\pi R(2C_D + C_C)}$$

$$FilterFreq_{CM} = \frac{1}{2\pi RC_C}$$

where $C_D \geq 10 C_C$.

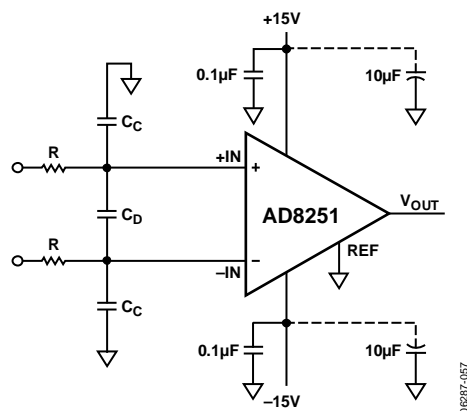


Figure 58. RFI Suppression

Values of R and C_C should be chosen to minimize RFI. A mismatch between the $R \times C_C$ at the positive input and the $R \times C_C$ at negative input degrades the CMRR of the AD8251. By using a value of C_D that is 10 times larger than the value of C_C , the effect of the mismatch is reduced and performance is improved.

DRIVING AN ADC

An instrumentation amplifier is often used in front of an ADC to provide CMRR. Usually, instrumentation amplifiers require a buffer to drive an ADC. However, the low output noise, low distortion, and low settle time of the AD8251 make it an excellent ADC driver.

In Figure 59, a 1 nF capacitor and a 49.9 Ω resistor create an antialiasing filter for the AD7612. The 1 nF capacitor stores and delivers the necessary charge to the switched capacitor input of the ADC. The 49.9 Ω series resistor reduces the burden of the 1 nF load from the amplifier and isolates it from the kickback current injected from the switched capacitor input of the AD7612. Selecting too small a resistor improves the correlation between the voltage at the output of the AD8251 and the voltage at the input of the AD7612 but may destabilize the AD8251. A trade-off must be made between selecting a resistor small enough to maintain accuracy and large enough to maintain stability.

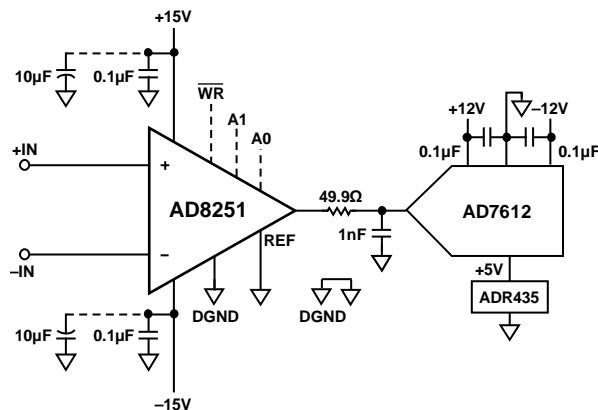


Figure 59. Driving an ADC

APPLICATIONS

DIFFERENTIAL OUTPUT

In certain applications, it is necessary to create a differential signal. High resolution ADCs often require a differential input. In other cases, transmission over a long distance can require differential signals for better immunity to interference.

Figure 61 shows how to configure the AD8251 to output a differential signal. An op amp, the [AD817](#), is used in an inverting topology to create a differential voltage. V_{REF} sets the output midpoint according to the equation shown in the figure. Errors from the op amp are common to both outputs and are thus common mode. Likewise, errors from using mismatched resistors cause a common-mode dc offset error. Such errors are rejected in differential signal processing by differential input ADCs or instrumentation amplifiers.

When using this circuit to drive a differential ADC, V_{REF} can be set using a resistor divider from the ADC reference to make the output ratiometric with the ADC.

SETTING GAINS WITH A MICROCONTROLLER

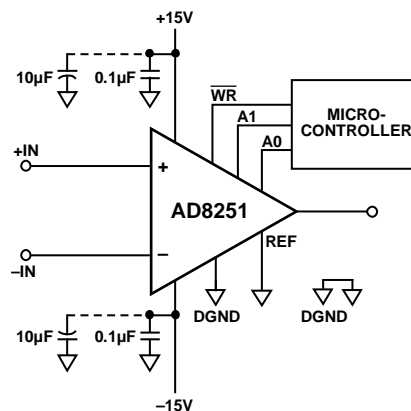


Figure 60. Programming Gain Using a Microcontroller

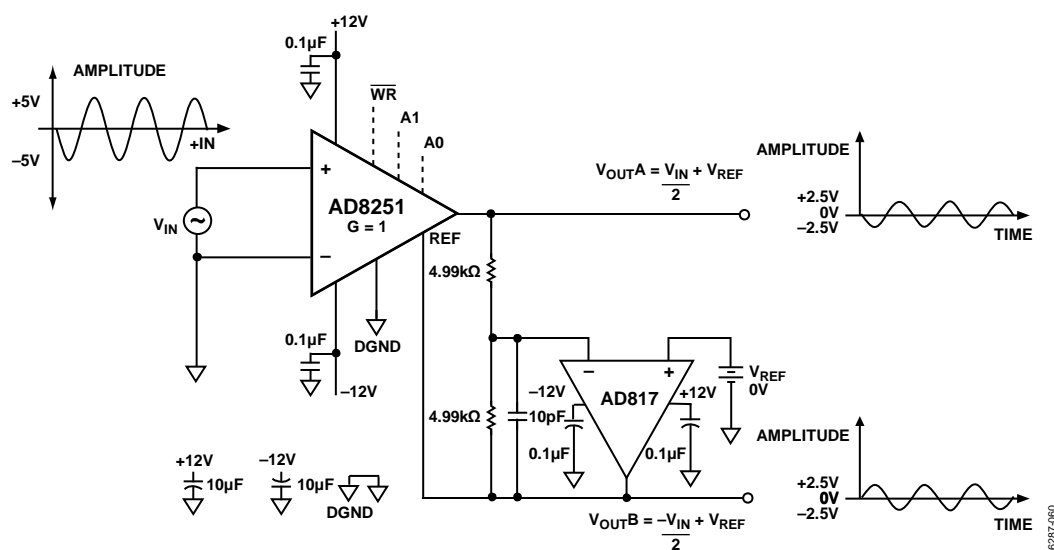


Figure 61. Differential Output with Level Shift

AD8251

DATA ACQUISITION

The AD8251 makes an excellent instrumentation amplifier for use in data acquisition systems. Its wide bandwidth, low distortion, low settling time, and low noise enable it to condition signals in front of a variety of 16-bit ADCs.

Figure 63 shows a schematic of the AD825x data acquisition demonstration board. The quick slew rate of the AD8251 allows it to condition rapidly changing signals from the multiplexed inputs. An FPGA controls the [AD7612](#), AD8251, and [ADG1209](#). In addition, mechanical switches and jumpers allow users to pin strap the gains when in transparent gain mode.

This system achieved -106 dB of THD at 1 kHz and a signal-to-noise ratio of 91 dB during testing, as shown in Figure 62.

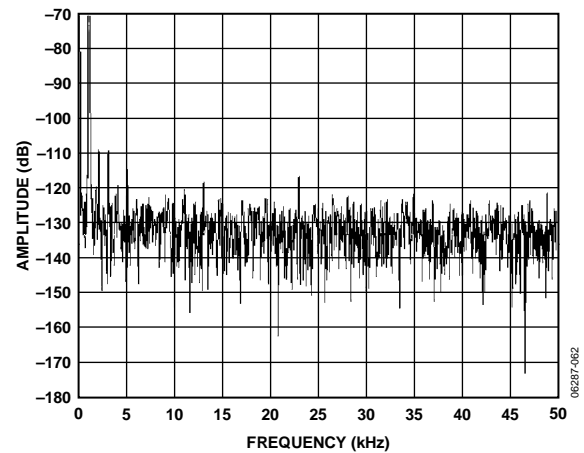


Figure 62. FFT of the AD825x DAQ Demo Board Using the AD8251 1 kHz Signal

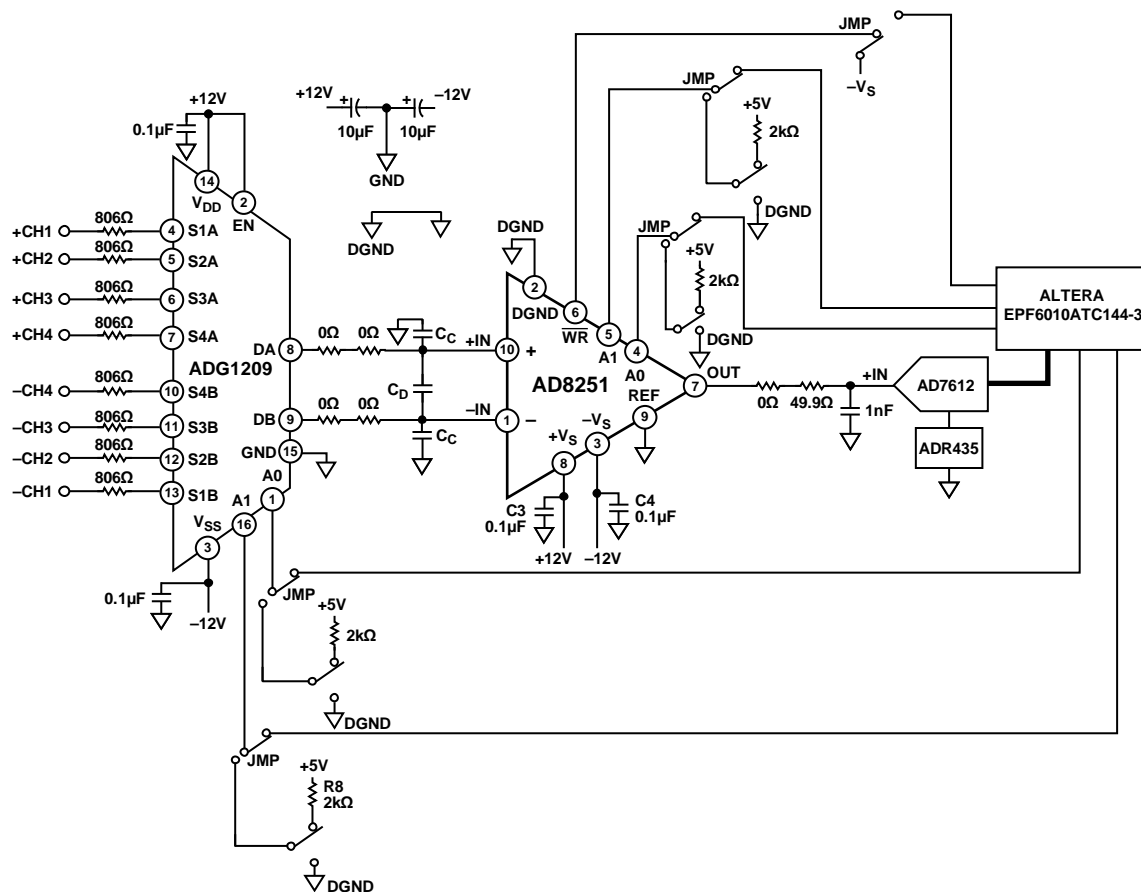
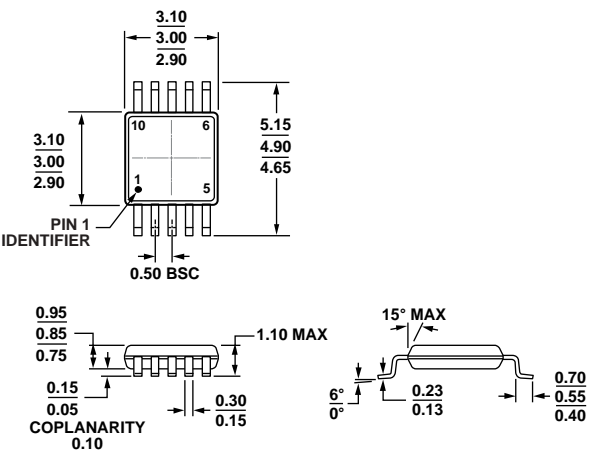


Figure 63. Schematic of ADG1209, AD8251, and AD7612 in the AD825x DAQ Demo Board

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-187-BA
Figure 64. 10-Lead Mini Small Outline Package [MSOP]
(RM-10)
Dimensions shown in millimeters

ORDERING GUIDE

Model ¹	Temperature Range	Package Description	Package Option	Branding
AD8251ARMZ	−40°C to +85°C	10-Lead Mini Small Outline Package [MSOP]	RM-10	HOT
AD8251ARMZ-RL	−40°C to +85°C	10-Lead Mini Small Outline Package [MSOP]	RM-10	HOT
AD8251ARMZ-R7	−40°C to +85°C	10-Lead Mini Small Outline Package [MSOP]	RM-10	HOT
AD8251-EVALZ		Evaluation Board		

¹ Z = RoHS Compliant Part.

AD8251

NOTES