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REVISION HISTORY

5/2020—Rev. C to Rev. D

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Add Figure 82; Renumbered Sequentially 30
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Changes to Core Signal Chain Section, Capacitive PGA Section, and Internal Reference and Reference Buffers Section 36
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6/2018—Rev. B to Rev. C

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8/2017—Rev. A to Rev. B

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9/2016—Rev. 0 to Rev. A

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2/2016—Revision 0: Initial Version

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FUNCTIONAL BLOCK DIAGRAM

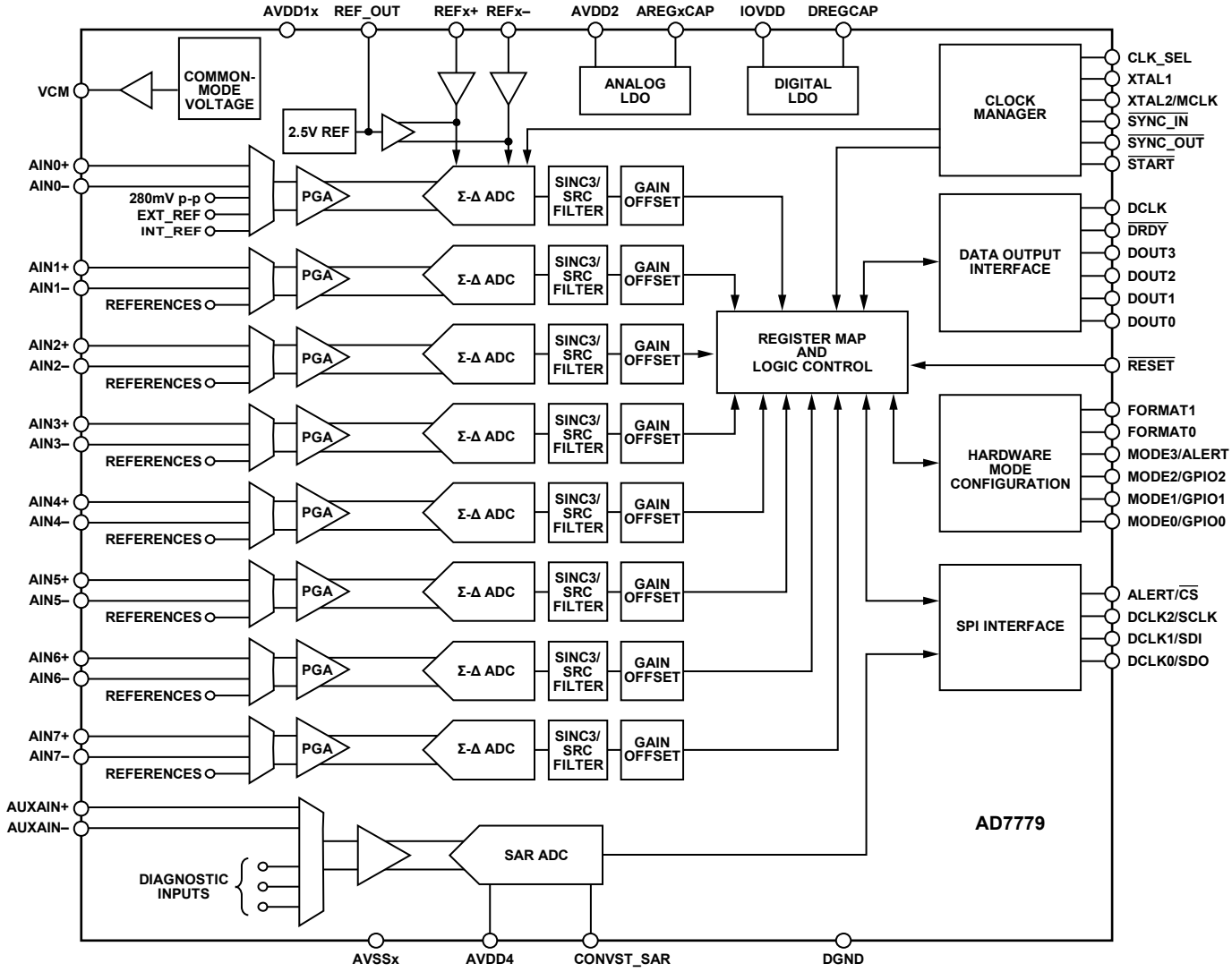

Figure 1.

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SPECIFICATIONS

AVDD1x = +1.65 V, AVSSx[1] = −1.65 V (dual supply operation), AVDD1x = 3.3 V, AVSSx = AGND (single-supply operation), AVDD2x − AVSSx = 2.2 V to 3.6 V; IOVDD = 1.8 V to 3.6 V; DGND = 0 V, REFx+/REFx− = 2.5 V AVSSx (internal/external), master clock (MCLK) = 8192 kHz for high resolution mode and 4096 kHz for low power mode, ODR = 16 kSPS for high resolution mode and 4 kSPS for low power mode; all specifications at T_{MIN} to T_{MAX}, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Σ-Δ ADC CHANNELS					
Speed and Performance					
Resolution		24			Bits
ODR	High resolution (HR) mode			16	kSPS
	Low power (LP) mode			8	kSPS
No Missing Codes		24			Bits
Gain Settings			1, 2, 4, or 8		
Bandwidth	Small signal, high resolution mode			2	MHz
	Small signal, low power mode			512	kHz
	Large signal, high resolution mode			5	kHz
	Large signal, low power mode			1.5	kHz
AC Accuracy					
Dynamic Range	Shorted inputs, PGA_{GAIN} = 1				
16 kSPS	High resolution mode		108		dB
4 kSPS	High resolution mode		116		dB
	Low power mode		106		dB
1 kSPS	Low power mode		116		dB
THD	−0.5 dBFS, HR mode		−109		dB
	−0.5 dBFS, LP mode		−105		dB
SINAD	f_{IN} = 60 Hz		106		dB
SFDR	HR mode, 16 kSPS, PGA_{GAIN} = 1		132		dB
Intermodulation Distortion (IMD)	f_A = 50 Hz, f_B = 51 Hz, HR mode		−125		dB
	f_A = 50 Hz, f_B = 51 Hz, LP mode		−105		dB
DC Power Supply Rejection	AVDD1x = 3.3 V		−90		dB
DC Common-Mode Rejection Ratio		80			dB
Crosstalk			−120		dB
DC ACCURACY					
INL	Endpoint method, PGA_{GAIN} = 1		±7		ppm of FSR
	Other PGA gains		±3		ppm of FSR
Offset Error			±40	±125	µV
Offset Error Drift			±0.5		µV/°C
Offset Error Drift vs. Time			−2		µV/ 1000 hrs
Offset Matching			25		µV
Gain Error			±0.1		% FS
Gain Drift vs. Temperature	PGA_{GAIN} = 1		±0.75		ppm/°C
Gain Matching			±0.1		%

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Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
ANALOG INPUTS					
Differential Input Voltage Range	V_{REF} = (REFx+ − REFx−)			$\pm V_{REF}/PGA_{GAIN}$	V
Single-Ended Input Voltage Range				0 to V_{REF}/PGA_{GAIN}	V
AINx± Common-Mode Input Range		AVSSx + 0.10	(AVDD1x + AVSSx)/2	AVDD1x − 0.10	V
Absolute AINx± Voltage Limits		AVSSx + 0.10		AVDD1x − 0.10	V
DC Input Current					
Differential	HR, MCLK = 8192 kHz		±1.5		nA
	Low power mode, MCLK = 4096 kHz		±0.6		nA
Single-Ended	HR, MCLK = 8192 kHz		±4		nA
	Low power mode, MCLK = 4096 kHz		±1.5		nA
Input Current Drift			50		pA/°C
AC Input Capacitance			8		pF
REFERENCE					
Internal					
Initial Accuracy	REF_OUT, T_A = 25°C	2.5 − 0.2%	2.5	2.5 + 0.2%	V
Temperature Coefficient			±10	±38	ppm/°C
Reference Load Current, I_L		−10		+10	mA
DC Power Supply Rejection	Line regulation		95		dB
Load Regulation, $\Delta V_{OUT}/\Delta I_L$			100		µV/mA
Voltage Noise	$e_{N\ p-p}$, 0.1 Hz to 10 Hz		6.8		µV rms
Voltage Noise Density	e_N, 1 kHz, 2.5 V reference		273.5		nV/√Hz
Turn On Settling Time	100 nF		1.5		ms
External					
Input Voltage	V_{REF} = (REFx+ − REFx−)	1	2.5	AVDD1x	V
Buffer Headroom		AVSSx + 0.1		AVDD1x − 0.1	
REFx− Input Voltage			AVSSx	AVDD1x − REFx+	V
Average REFx± Input Current	Current per channel				
	Reference buffer disabled, high resolution mode		18		µA/V
	Reference buffer precharge mode (pre-Q), high resolution mode		600		nA/V
	Reference buffer disabled, low power mode		4.5		µA/V
	Reference buffer pre-Q, low power mode		100		nA/V
	Reference buffer enabled, high resolution mode		10		nA/V
	Reference buffer enabled, low power mode		5		nA/V
TEMPERATURE RANGE					
Specified Performance	T_{MIN} to T_{MAX}	−40		+105	°C
Functional[2]	T_{MIN} to T_{MAX}	−40		+125	°C
TEMPERATURE SENSOR					
Accuracy			±2		°C

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Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DIGITAL FILTER RESPONSE (SINC3)					
Group Delay			See the SRC Group Delay section		
Settling Time			See the Settling Time section		
Pass Band	−0.1 dB		See the SRC Bandwidth section		
	−3 dB		See the SRC Bandwidth section		
Decimation Rate	High resolution mode	128		4095.99	
	Low power mode	64		4095.99	
CLOCK SOURCE					
Frequency	High resolution mode	0.655		8.192	MHz
	Low power mode	1.3		4.096	MHz
Duty Cycle		45:55	50:50	55:45	%
SAR ADC CHANNEL					
Speed and Performance					
Resolution			12		Bits
Analog Input Range		AVSS4 + 0.1		AVDD4 − 0.1	V
Analog Input Common-Mode Range		AVSS4 + 0.1	(AVDD4 + AVSS4)/2	AVDD4 − 0.1	V
Analog Input Dynamic Current	256 kSPS, 0 dBFS		±100		nA
Throughput				256	kSPS
DC Accuracy	Differential mode				
INL			1.5		LSB
DNL	No missing codes (12-bit)	−0.99		+1	LSB
Offset			1		LSB
Gain			12		LSB
AC Performance					
SNR	1 kHz		66		dB
THD	1 kHz		−81		dB
VCM PIN					
Output			(AVDD1x + AVSSx)/2		V
Load Current, I_L			1		mA
Load Regulation, $\Delta V_{OUT}/\Delta I_L$			12		mV/mA
Short-Circuit Current			5		mA
LOGIC INPUTS					
Input High Voltage, V_{IH}		0.7 × IOVDD			V
Input Low Voltage, V_{IL}				0.4	V
Hysteresis			0.1		V
Input Currents		−10		+10	µA
LOGIC OUTPUTS[3]					
Output High Voltage, V_{OH}	IOVDD ≥ 3 V, I_{SOURCE} = 1 mA	0.8 × IOVDD			V
	2.3 ≤ IOVDD < 3 V, I_{SOURCE} = 500 µA	0.8 × IOVDD			V
	IOVDD < 2.3 V, I_{SOURCE} = 200 µA	0.8 × IOVDD			V
Output Low Voltage, V_{OL}	IOVDD ≥ 3 V, I_{SINK} = 2 mA			0.4	V
	2.3 ≤ IOVDD < 3 V, I_{SINK} = 1 mA			0.4	V
	IOVDD < 2.3 V, I_{SINK} = 100 µA			0.4	V

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Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Leakage Current	Floating state	−10		+10	µA
Output Capacitance	Floating state		10		pF
Σ-Δ ADC Data Output Coding			Twos complement		
SAR ADC Data Output Coding			Binary		
POWER SUPPLIES	All Σ-Δ channels enabled				
AVDD1x – AVSSx		3.0		3.6	V
I_{AVDD1x}[4, 5]	Reference buffer pre-Q, VCM enabled, internal reference enabled				
	High resolution mode		17	22.7	mA
	Low power mode		4.5	6.1	mA
	Reference buffer enabled, VCM enabled, internal reference enabled				
	High resolution mode		19	25.5	mA
	Low power mode		5	6.8	mA
	Reference buffer disabled, VCM disabled, internal reference disabled				
	High resolution mode		13	17.8	mA
	Low power mode		3.5	4.8	mA
AVDD2x – AVSSx		2.2		3.6	V
I_{AVDD2x}	High resolution mode		9	9.45	mA
	Low power mode		3.5	3.7	mA
AVDD4 – AVSSx		AVDD1x – 0.3		AVDD1x	V
I_{AVDD4}	SAR enabled		1.7	2	mA
	SAR disabled		1	10	µA
AVSSx – DGND		−1.8		0	V
IOVDD – DGND		1.8		3.6	V
I_{IOVDD}	High resolution mode		8	10.7	mA
	Low power mode		3	4.4	mA
Power Dissipation[6]	Internal buffers bypassed, internal reference disabled, internal oscillator disabled, SAR disabled				
High Resolution Mode	16 kSPS		86	133	mW
Low Power Mode	4 kSPS		27	44	mW
Power-Down	All ADCs disabled		530		µW

[1] AVSSx is used to refer to the following pins: AVSS1A, AVSS1B, AVSS2B, and AVSS2A. This term is used throughout the data sheet.
[2] At temperatures higher than 105°C, the device can be operated normally, though slight degradation on the maximum/minimum specifications is expected because these specifications are only guaranteed up to 105°C. See the Typical Performance Characteristics section for plots showing the typical performance of the device at high temperatures.
[3] The SDO pin and the DOUTx pin are configured in the default mode of strength.
[4] AVDD1x = 3.3 V, AVSSx = GND = ground, IOVDD = 1.8 V, CMOS clock.
[5] Disabling either the VCM pin or the internal reference results in a 40 µA typical current consumption reduction.
[6] Power dissipation is calculated using the maximum supply voltage, 3.6 V.

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DOUTx TIMING CHARACTERISTISTICS

AVDD1x/AVSSx = ±1.65 V, 3.3 V/AGND, AVDD2 − AVSSx = 2.2 V to 3.6 V; IOVDD = 1.8 V to 3.6 V; DGND = 0 V, REFx+/REFx− = 2.5 V (internal/external), MCLK = 8192 kHz; all specifications at T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

Parameter	Description[1]	Test Conditions/Comments	Min	Typ	Max	Unit
t_1	MCLK frequency	50:50	0.655		8.192	MHz
t_2	MCLK low time		60			ns
t_3	MCLK high time		60			ns
t_4	DCLKx high time	MCLK/2	121			ns
t_5	DCLKx low time	MCLK/2	121			ns
t_6	MCLK falling edge to DCLK rising edge				45	ns
t_7	MCLK falling edge to DCLK falling edge				45	ns
t_8	DCLKx rising edge to $\overline{\text{DRDY}}$ rising edge		2			ns
t_9	DCLKx rising edge to $\overline{\text{DRDY}}$ falling edge		1			ns
t_{10}	DOUTx setup time		20			ns
t_{11}	DOUTx hold time		20			ns

[1] All input signals are specified with $t_R = t_F$ = 1 ns/V (10% to 90% of IOVDD) and timed from a voltage level of $(V_{IL} + V_{IH})/2$.

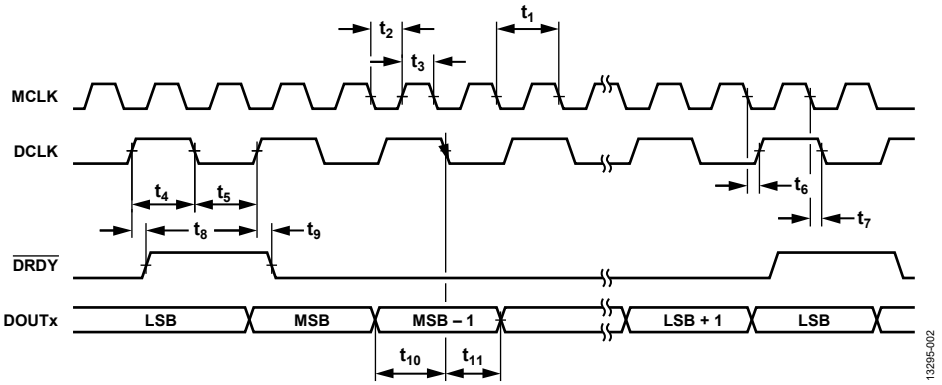

Figure 2. Data Interface Timing Diagram

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SPI TIMING CHARACTERISTICS

AVDD1x/AVSSx = ±1.65 V, 3.3 V/AGND, AVDD2 − AVSSx = 2.2 V to 3.6 V; IOVDD = 1.8 V to 3.6 V; DGND = 0 V, REFx+/REFx− = 2.5 V (internal/external), MCLK = 8192 kHz; all specifications at T_{MIN} to T_{MAX}, unless otherwise noted.

Table 3.

Parameter	Description[1]	Test Conditions/Comments	Min	Typ	Max	Unit
t_{12}	SCLK period	50:50			30	MHz
t_{13}	SCLK low time		7			ns
t_{14}	SCLK high time		7			ns
t_{15}	SCLK rising edge to $\overline{CS}$ falling edge		10			ns
t_{16}	$\overline{CS}$ falling edge to SCLK rising edge		10			ns
t_{17}	SCLK rising edge to $\overline{CS}$ rising edge		10			ns
t_{18}	$\overline{CS}$ rising edge to SCLK rising edge		10			ns
t_{19}	Minimum $\overline{CS}$ high time		10			ns
t_{20}	SDI setup time		5			ns
t_{21}	SDI hold time		5			ns
t_{22A}	$\overline{CS}$ falling edge to SDO enable (SPI = Mode 0)		30			ns
t_{22B}	SCLK falling edge to SDO enable (SPI = Mode 3)		49			ns
t_{23}	SDO setup time		10			ns
t_{24}	SDO hold time		10			ns
t_{25}	$\overline{CS}$ rising edge to SDO disable		30			ns

[1] All input signals are specified with $t_R = t_F$ = 1 ns/V (10% to 90% of IOVDD) and timed from a voltage level of $(V_{IL} + V_{IH})/2$.

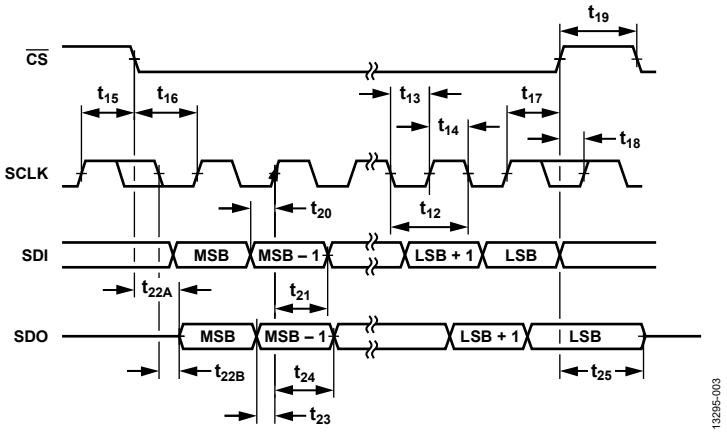

Figure 3. SPI Control Interface Timing Diagram

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SYNCHRONIZATION PINS AND RESET TIMING CHARACTERISTICS

AVDD1x/AVSSx = ±1.65 V, 3.3 V/AGND, AVDD2 − AVSSx = 2.2 V to 3.6 V; IOVDD = 1.8 V to 3.6 V; DGND = 0 V, REFx+/REFx− = 2.5 V (internal/external), MCLK = 8192 kHz; all specifications at T_{MIN} to T_{MAX}, unless otherwise noted.

Table 4.

Parameter	Description[1]	Test Conditions/Comments	Min	Typ	Max	Unit
t_{26}	$\overline{\text{START}}$ setup time		10			ns
t_{27}	$\overline{\text{START}}$ hold time		MCLK			ns
t_{28}	MCLK falling edge to $\overline{\text{SYNC_OUT}}$ falling edge		MCLK			ns
t_{29}	$\overline{\text{SYNC_IN}}$ setup time		10			ns
t_{30}	$\overline{\text{SYNC_IN}}$ hold time		MCLK			ns
$t_{INIT_\overline{SYNC_IN}}$	$\overline{\text{SYNC_IN}}$ rising edge to first $\overline{\text{DRDY}}$	16 kSPS, HR mode	145			µs
$t_{INIT_\overline{RESET}}$	$\overline{\text{RESET}}$ rising edge to first $\overline{\text{DRDY}}$	16 kSPS, HR mode	225			µs
t_{31}	$\overline{\text{RESET}}$ hold time		2 × MCLK			ns
t_{POWER_UP}	Start time	t_{POWER_UP} is not shown in Figure 4		2		ms

[1] All input signals are specified with $t_R = t_F$ = 1 ns/V (10% to 90% of IOVDD) and timed from a voltage level of $(V_{IL} + V_{IH})/2$.

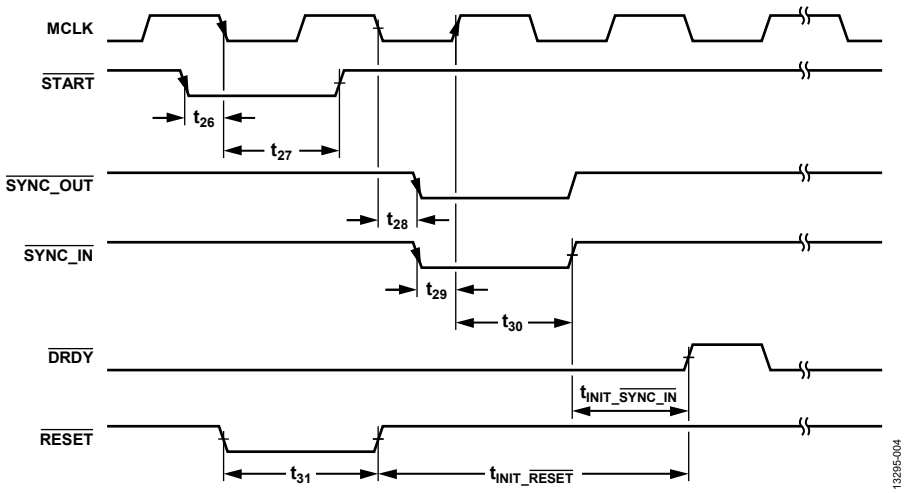

Figure 4. Synchronization Pins and Reset Control Interface Timing Diagram

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SAR ADC TIMING CHARACTERISTICS

AVDD1x/AVSSx = ±1.65 V, 3.3 V/AGND, AVDD2 − AVSSx = 2.2 V to 3.6 V; IOVDD = 1.8 V to 3.6 V; DGND = 0 V, REFx+/REFx− = 2.5 V (internal/external), MCLK = 8192 kHz; all specifications at T_{MIN} to T_{MAX}, unless otherwise noted.

Table 5.

Parameter	Description[1]	Min	Typ	Max	Unit
t_{32}	Conversion time	1		3.4	µs
t_{33}	Acquisition time[2]	500			ns
t_{34}	Delay time	50			ns
t_{35}	Throughput data			256	kSPS

[1] All input signals are specified with $t_R = t_F$ = 1 ns/V (10% to 90% of IOVDD) and timed from a voltage level of $(V_{IL} + V_{IH})/2$.
[2] Direct mode enabled. If deglitch mode is enabled, add 1.5/MCLK.

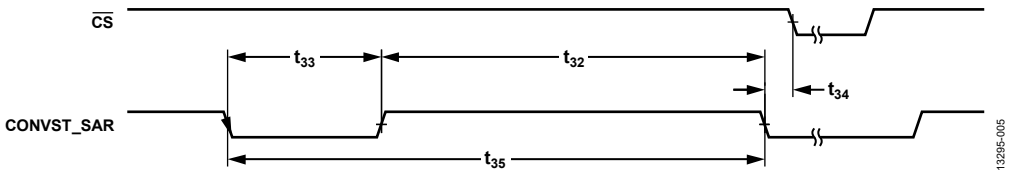

Figure 5. SAR ADC Timing Diagram

GPIO SRC UPDATE TIMING CHARACTERISTICS

AVDD1x/AVSSx = ±1.65 V, 3.3 V/AGND, AVDD2 − AVSSx = 2.2 V to 3.6 V; IOVDD = 1.8 V to 3.6 V; DGND = 0 V, REFx+/REFx− = 2.5 V (internal/external), MCLK = 8192 kHz; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 6.

Parameter	Description[1]	Min	Typ	Max	Unit
t_{36}	GPIO2 setup time	10			ns
t_{37}	GPIO2 hold time—high resolution mode	MCLK			ns
t_{37}	GPIO2 hold time—low power mode	2 × MCLK			
t_{38}	MCLK rising edge to GPIO1 rising edge time	20			ns
t_{39}	GPIO0 hold time	MCLK			ns
t_{40}	GPIO0 setup time	5			ns

[1] All input signals are specified with $t_R = t_F$ = 1 ns/V (10% to 90% of IOVDD) and timed from a voltage level of $(V_{IL} + V_{IH})/2$.

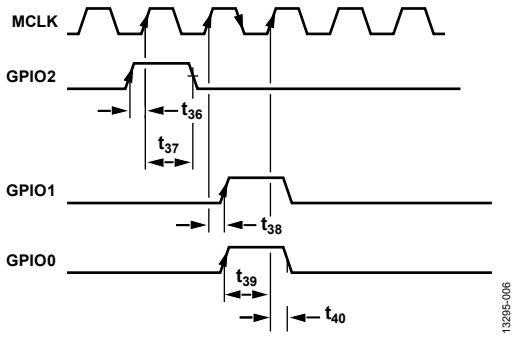

Figure 6. GPIOs for SRC Update Timing Diagram

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ABSOLUTE MAXIMUM RATINGS

Table 7.

Parameter	Rating
Any Supply Pin to AVSSx	−0.3 V to +3.96 V
AVSSx to DGND	−1.98 V to +0.3 V
AREGxCAP to AVSSx	−0.3 V to +1.98 V
DREGCAP to DGND	−0.3 V to +1.98 V
IOVDD to DGND	−0.3 V to +3.96 V
IOVDD to AVSSx	−0.3 V to +5.94 V
AVDD4 to AVSSx	AVDD1x − 0.3 V to 3.96 V
Analog Input Voltage	AVSSx − 0.3 V to AVDD1x + 0.3 V or 3.96 V (whichever is less)
REFx± Input Voltage	AVSSx − 0.3 V to AVDD1x + 0.3 V or 3.96 V (whichever is less)
AUXAIN±	AVSSx − 0.3 V to AVDD4 + 0.3 V or 3.96 V (whichever is less)
Digital Input Voltage to DGND	DGND − 0.3 V to IOVDD + 0.3 V or 3.96 V (whichever is less)
Digital Output Voltage to DGND	DGND − 0.3 V to IOVDD + 0.3 V or 3.96 V (whichever is less)
XTAL1 to DGND	DGND − 0.3 V to DREGCAP + 0.3 V or 1.98 V (whichever is less)
AINx±, AUXAIN±, and Digital Input Current	±10 mA
Temperature	
Operating Range	−40°C to +125°C
Junction, T_J Maximum	150°C
Storage Range	−65°C to +150°C
Reflow Soldering	260°C
Electrostatic Discharge (ESD)	2 kV
Field Induced Charged Device Model (FICDM)	500 V

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Close attention to PCB thermal design is required.

Table 8. Thermal Resistance

Package Type[1]	θ_{JA}	θ_{JB}	Ψ_{JT}	Ψ_{JB}	Unit
64-Lead LFCSP					
No Thermal Vias[1]	30.43	N/A[2]	0.13	6.59	°C/W
49 Thermal Vias[1]	22.62	3.17	0.09	3.19	°C/W

[1] Thermal impedance simulated values are based on a JEDEC 2S2P thermal test board. See JEDEC JESD51.
[2] N/A means not applicable.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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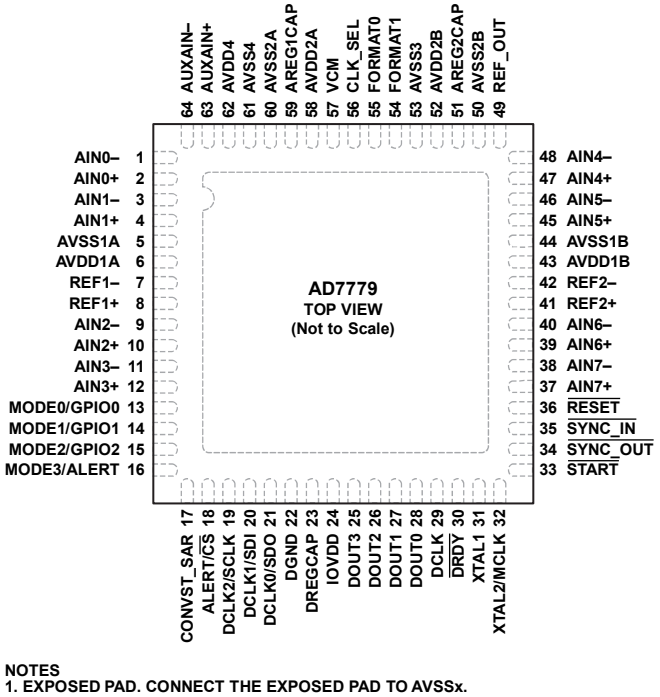
PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. EXPOSED PAD. CONNECT THE EXPOSED PAD TO AVSSx.

Figure 7. Pin Configuration

Table 9. Pin Function Descriptions

Pin No.	Mnemonic	Type	Direction	Description
1	AIN0–	Analog input	Input	Analog Input Channel 0, Negative.
2	AIN0+	Analog input	Input	Analog Input Channel 0, Positive.
3	AIN1–	Analog input	Input	Analog Input Channel 1, Negative.
4	AIN1+	Analog input	Input	Analog Input Channel 1, Positive.
5	AVSS1A	Supply	Supply	Negative Front-End Analog Supply for Channel 0 to Channel 3, Typical at –1.65 V (Dual Supply) and AGND (Single Supply). Connect all the AVSSx pins to the same potential.
6	AVDD1A	Supply	Supply	Positive Front-End Analog Supply for Channel 0 to Channel 3, Typical at AVSSx + 3.3 V. Connect this pin to AVDD1B.
7	REF1–	Reference	Input	Negative Reference Input 1 for Channel 0 to Channel 3, Typical at AVSSx. Connect all the REFx– pins to the same potential.
8	REF1+	Reference	Input	Positive Reference Input 1 for Channel 0 to Channel 3, Typical at REF1– + 2.5 V.
9	AIN2–	Analog input	Input	Analog Input Channel 2, Negative.
10	AIN2+	Analog input	Input	Analog Input Channel 2, Positive.
11	AIN3–	Analog input	Input	Analog Input Channel 3, Negative.
12	AIN3+	Analog input	Input	Analog Input Channel 3, Positive.
13	MODE0/GPIO0	Digital I/O	I/O	Mode 0 Input Pin in Pin Control Mode (MODE0). See Table 18 for more details. Configurable General-Purpose Input/Output 0 in SPI Control Mode (GPIO0). If not in use, connect this pin to DGND or IOVDD.
14	MODE1/GPIO1	Digital I/O	I/O	Mode 1 Input Pin in Pin Control Mode (MODE1). See Table 18 for more details. Configurable General-Purpose Input/Output 1 in SPI Control Mode (GPIO1). If not in use, connect this pin to DGND or IOVDD.
15	MODE2/GPIO2	Digital I/O	I/O	Mode 2 Input Pin in Pin Control Mode (MODE2). See Table 18 for more details. Configurable General-Purpose Input/Output 2 in SPI Control Mode (GPIO2). If not in use, connect this pin to DGND or IOVDD.
16	MODE3/ALERT	Digital I/O	I/O	Mode 3 Input Pin in Pin Control Mode (MODE3). See Table 18 for more details. Alert Output Pin in SPI Control Mode (ALERT).

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Pin No.	Mnemonic	Type	Direction	Description
17	CONVST_SAR	Digital input	Input	Σ-Δ Output Interface Selection Pin in Pin Control Mode. See Table 17 for more details. This pin also functions as the start for the SAR conversion in SPI control mode.
18	ALERT/$\overline{CS}$	Digital input	Input	Alert Output Pin in Pin Control Mode (ALERT). Chip Select Pin in SPI Control Mode ($\overline{CS}$).
19	DCLK2/SCLK	Digital input	Input	DCLK Frequency Selection Pin 2 in Pin Control Mode (DCLK2). See Table 19 for more details. SPI Clock in SPI Control Mode (SCLK).
20	DCLK1/SDI	Digital input	Input	DCLK Frequency Selection Pin 1 in Pin Control Mode (DCLK1). See Table 19 for more details. SPI Data Input in SPI Control Mode (SDI). Connect this pin to DGND if the device is configured in pin control mode with the SPI as the data output interface.
21	DCLK0/SDO	Digital output	Output	DCLK Frequency Selection Pin 0 in Pin Control Mode (DCLK0). See Table 19 for more details. SPI Data Output in SPI Control Mode (SDO).
22	DGND	Supply	Supply	Digital Ground.
23	DREGCAP	Supply	Output	Digital LDO Output. Decouple this pin to DGND with a 1 µF capacitor.
24	IOVDD	Supply	Supply	Digital Levels Input/Output and Digital LDO (DLDO) Supply from 1.8 V to 3.6 V. IOVDD must not be lower than DREGCAP.
25	DOUT3	Digital output	I/O	Data Output Pin 3. If the device is configured in daisy-chain mode, this pin acts as an input pin. See the Daisy-Chain Mode section for more details.
26	DOUT2	Digital output	I/O	Data Output Pin 2. If the device is configured in daisy-chain mode, this pin acts as an input pin. See the Daisy-Chain Mode section for more details.
27	DOUT1	Digital output	Output	Data Output Pin 1.
28	DOUT0	Digital output	Output	Data Output Pin 0.
29	$\overline{DCLK}$	Digital output	Output	Data Output Clock.
30	$\overline{DRDY}$	Digital output	Output	Data Output Ready Pin.
31	XTAL1	Clock	Input	Crystal 1 Input Connection. If CMOS is used as a clock source, tie this pin to DGND. See Table 16 for more details.
32	XTAL2/MCLK	Clock	Input	Crystal 2 Input Connection (XTAL2). See Table 16 for more details. CMOS Clock (MCLK). See Table 16 for more details.
33	$\overline{START}$	Digital input	Input	Synchronization Pulse. This pin is used to synchronize internally an external $\overline{START}$ asynchronous pulse with MCLK. The synchronize signal is shift out by the $\overline{SYNC_OUT}$ pin. If not in use, tie this pin to IOVDD. See the Phase Adjustment section and the Digital Reset and Synchronization Pins section for more details.
34	$\overline{SYNC_OUT}$	Digital output	Input	Synchronization Signal. This pin generates a synchronous pulse generated and driven by hardware (via the $\overline{START}$ pin) or by software ($\overline{GENERAL_USER_CONFIG_2}$, Bit 0). If this pin is in use, it must be wired to the $\overline{SYNC_IN}$ pin. See the Phase Adjustment and the Digital Reset and Synchronization Pins section for more details.
35	$\overline{SYNC_IN}$	Digital input	Input	Reset for the Internal Digital Block and Synchronize for Multiple Devices. See the Digital Reset and Synchronization Pins section for more details.
36	$\overline{RESET}$	Digital input	Input	Asynchronous Reset Pin. This pin resets all registers to their default value. It is recommended to generate a pulse on this pin after the device is powered up because a slow slew rate in the supplies may generate an incorrect initialization in the digital block.
37	AIN7+	Analog input	Input	Analog Input Channel 7, Positive.
38	AIN7−	Analog input	Input	Analog Input Channel 7, Negative.
39	AIN6+	Analog input	Input	Analog Input Channel 6, Positive.
40	AIN6−	Analog input	Input	Analog Input Channel 6, Negative.
41	REF2+	Reference	Input	Positive Reference Input 2 for Channel 4 to Channel 7, Typical at REF2− + 2.5 V.
42	REF2−	Reference	Input	Negative Reference Input 2 for Channel 4 to Channel 7, Typical at AVSSx. Connect all the REFx− pins to the same potential.

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Pin No.	Mnemonic	Type	Direction	Description
43	AVDD1B	Supply	Supply	Positive Front-End Analog Supply for Channel 4 to Channel 7. Connect this pin to AVDD1A.
44	AVSS1B	Supply	Supply	Negative Front-End Analog Supply for Channel 4 to Channel 7, Typical at −1.65 V (Dual Supply) or AGND (Single Supply). Connect all the AVSSx pins together.
45	AIN5+	Analog input	Input	Analog Input Channel 5, Positive.
46	AIN5−	Analog input	Input	Analog Input Channel 5, Negative.
47	AIN4+	Analog input	Input	Analog Input Channel 4, Positive.
48	AIN4−	Analog input	Input	Analog Input Channel 4, Negative.
49	REF_OUT	Reference	Output	2.5 V Reference Output. Connect a 100 nF capacitor on this pin if using the internal reference.
50	AVSS2B	Supply	Supply	Negative Analog Supply. Connect all the AVSSx pins together.
51	AREG2CAP	Supply	Output	Analog LDO Output 2. Decouple this pin to AVSS2B with a 1 µF capacitor.
52	AVDD2B	Supply	Supply	Positive Analog Supply. Connect this pin to AVDD2A.
53	AVSS3	Supply	Supply	Negative Analog Ground. Connect all the AVSSx pins together.
54	FORMAT1	Digital input	Input	Output Data Frame 1. See Table 17 for more details.
55	FORMAT0	Digital input	Input	Output Data Frame 0. See Table 17 for more details.
56	CLK_SEL	Digital input	Input	Select Clock Source. See Table 16 for more details.
57	VCM	Analog output	Output	Common-Mode Voltage Output, Typical at (AVDD1 + AVSSx)/2.
58	AVDD2A	Supply	Input	Analog Supply from 2.2 V to 3.6 V. AVSS2x must not be lower than AREGxCAP. Connect this pin to AVDD2B.
59	AREG1CAP	Supply	Output	Analog LDO Output 1. Decouple this pin to AVSS with a 1 µF capacitor.
60	AVSS2A	Supply	Input	Negative Analog supply. Connect all the AVSSx pins together.
61	AVSS4	Supply	Supply	Negative SAR Analog Supply and Reference. Connect all AVSSx pins together.
62	AVDD4	Supply	Supply	Positive SAR Analog Supply and Reference Source.
63	AUXAIN+	Analog input	Input	Positive SAR Analog Input Channel.
64	AUXAIN−	Analog input	Input	Negative SAR Analog Input Channel.
	EPAD	Supply	Input	Exposed Pad. Connect the exposed pad to AVSSx.

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TYPICAL PERFORMANCE CHARACTERISTICS

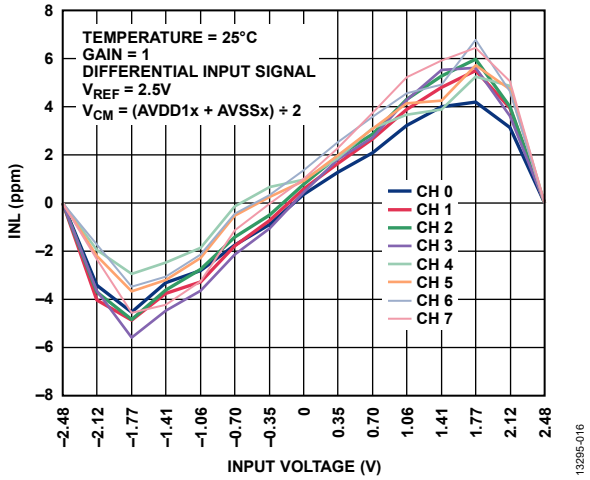

Figure 8. INL vs. Input Voltage and Channel at 8 kSPS, High Resolution Mode

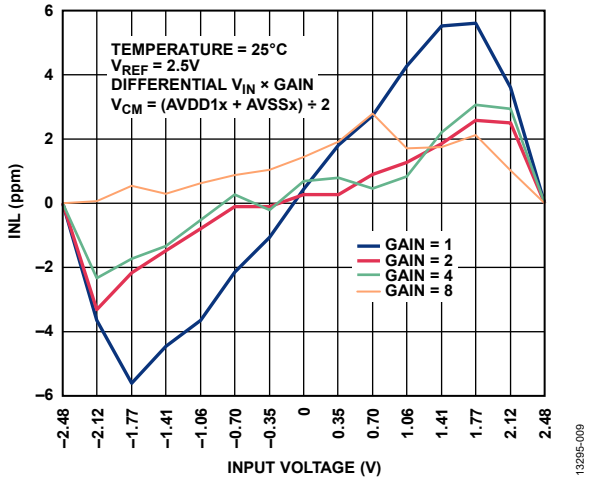

Figure 9. INL vs. Input Voltage and PGA Gain at 8 kSPS, High Resolution Mode

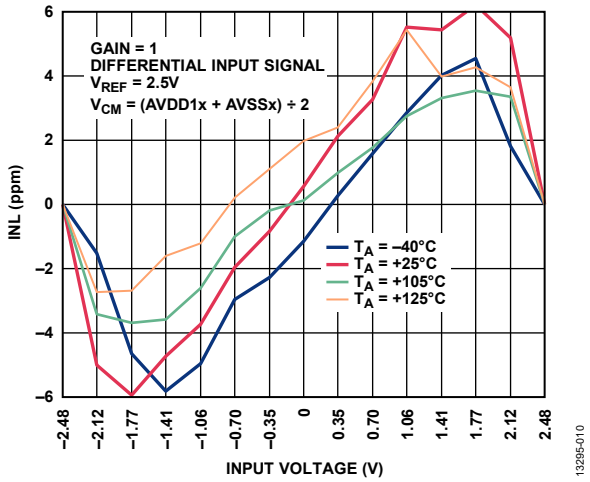

Figure 10. INL vs. Input Voltage and Temperature at 8 kSPS, High Resolution Mode

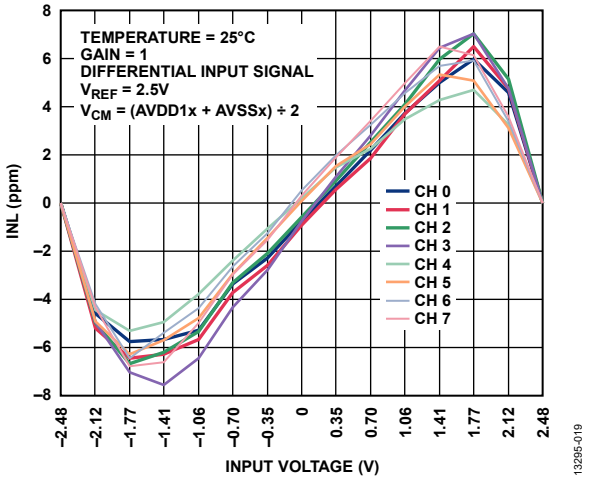

Figure 11. INL vs. Input Voltage and Channel at 2 kSPS, Low Power Mode

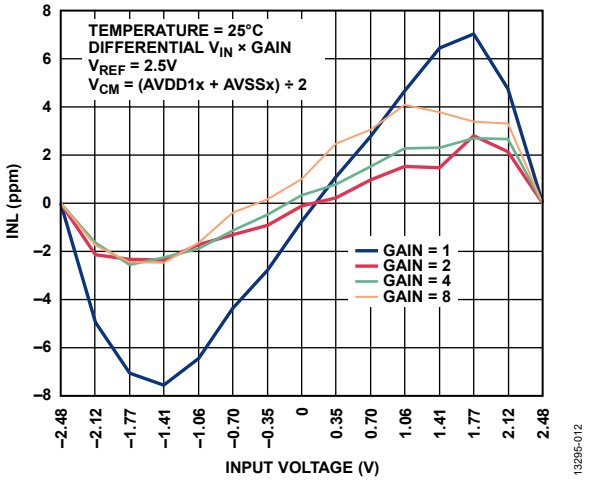

Figure 12. INL vs. Input Voltage and PGA Gain at 2 kSPS, Low Power Mode

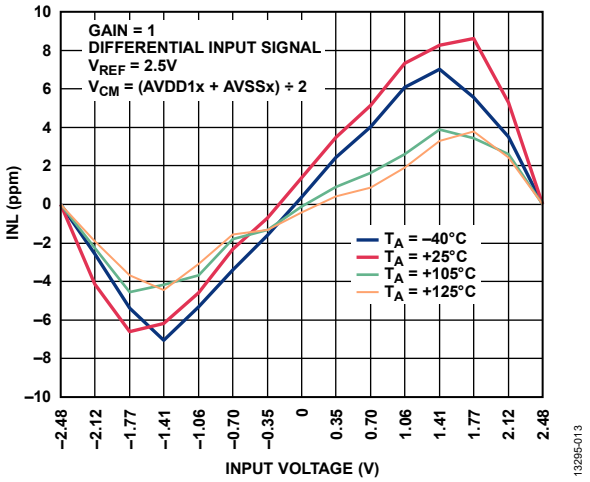

Figure 13. INL vs. Input Voltage and Temperature at 2 kSPS, Low Power Mode

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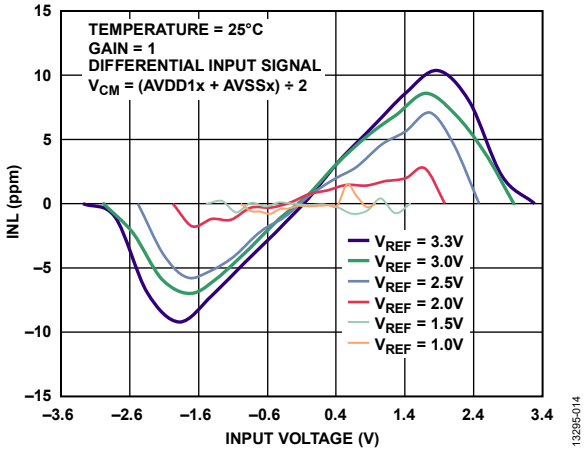

Figure 14. INL vs. Input Voltage and Reference Voltage (V_{REF}) at 8 kSPS, High Resolution Mode

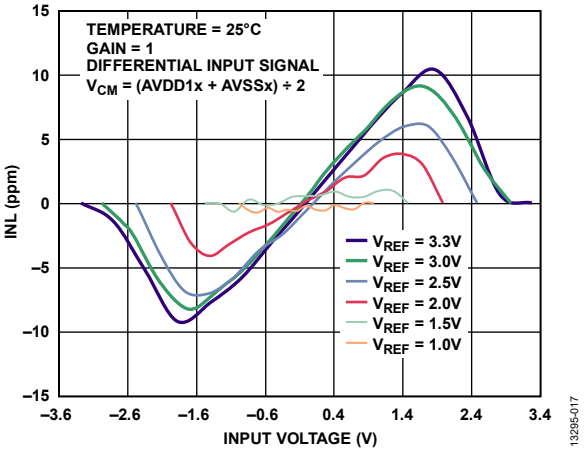

Figure 17. INL vs. Input Voltage and Reference Voltage (V_{REF}) at 2 kSPS, Low Power Mode

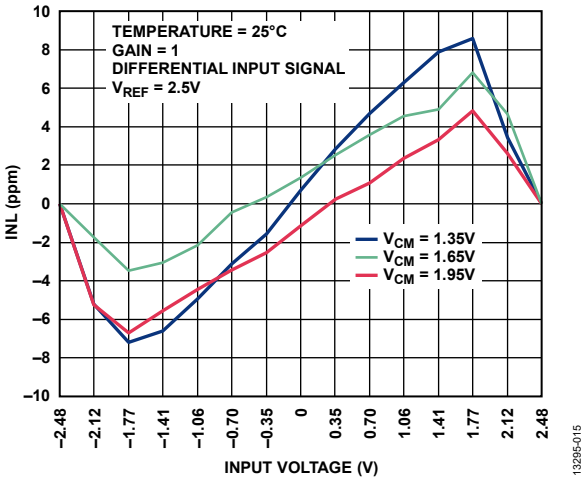

Figure 15. INL vs. Input Voltage and V_{CM} at 8 kSPS, High Resolution Mode

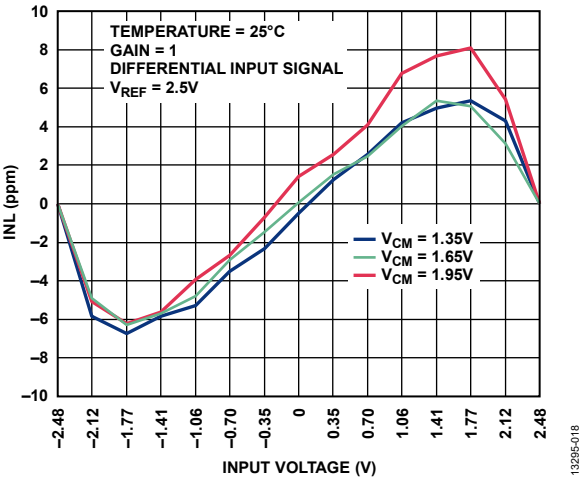

Figure 18. INL vs. Input Voltage and V_{CM} at 2 kSPS, Low Power Mode

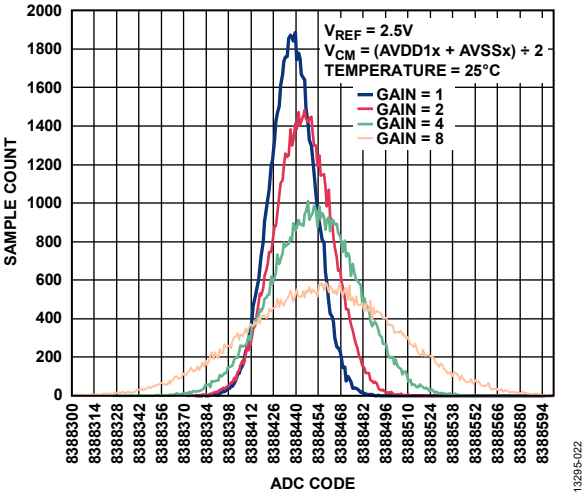

Figure 16. Noise Histogram at 8 kSPS, High Resolution Mode

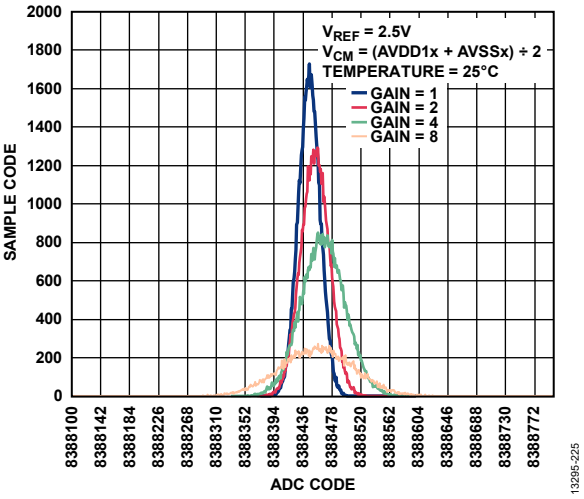

Figure 19. Noise Histogram at 2 kSPS, Low Power Mode

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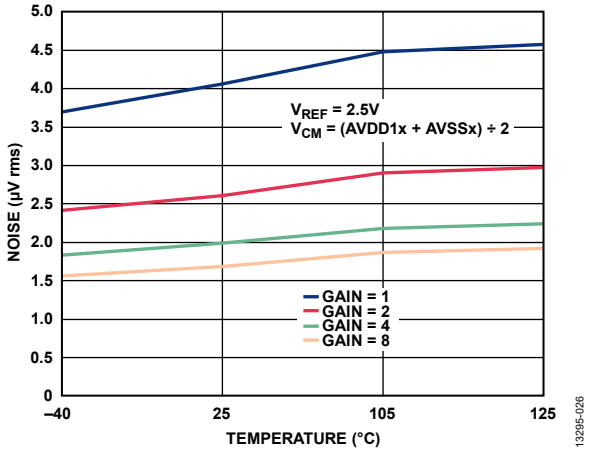

Figure 20. Noise vs. Temperature at 8 kSPS, High Resolution Mode

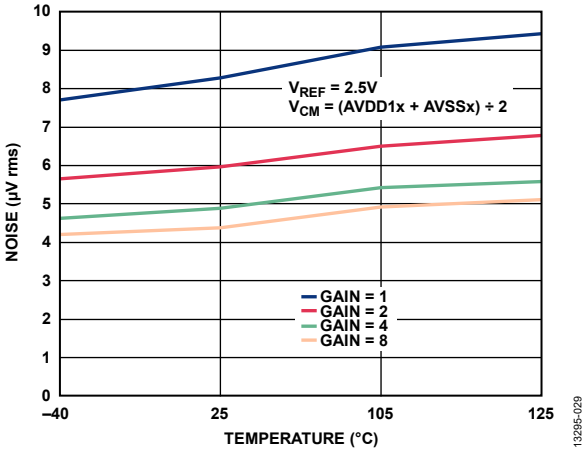

Figure 23. Noise vs. Temperature at 2 kSPS, Low Power Mode

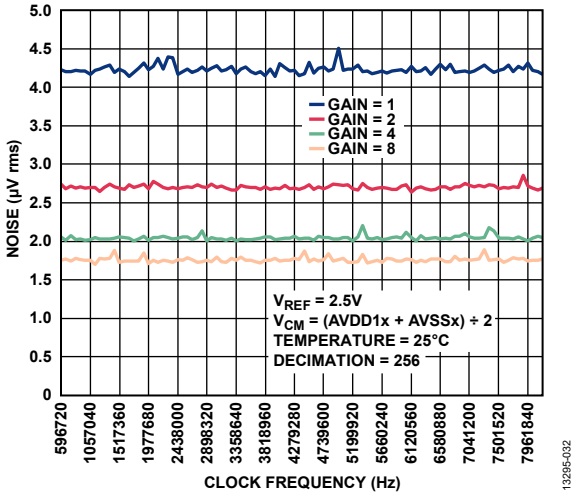

Figure 21. Noise vs. Clock Frequency, High Resolution Mode, Decimation = 256

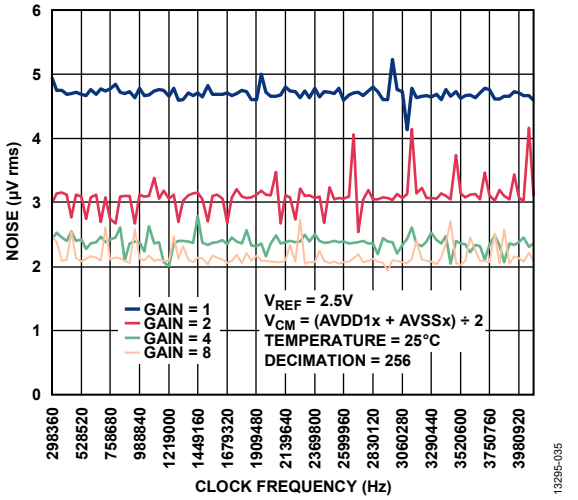

Figure 24. Noise vs. Clock Frequency at 2 kSPS, Low Power Mode, Decimation = 256

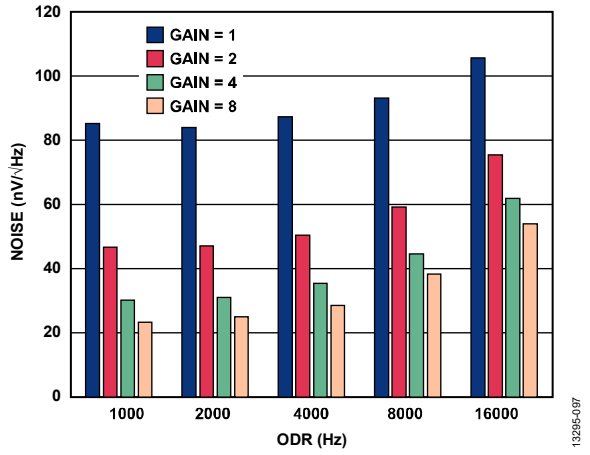

Figure 22. Noise vs. ODR, High Resolution Mode

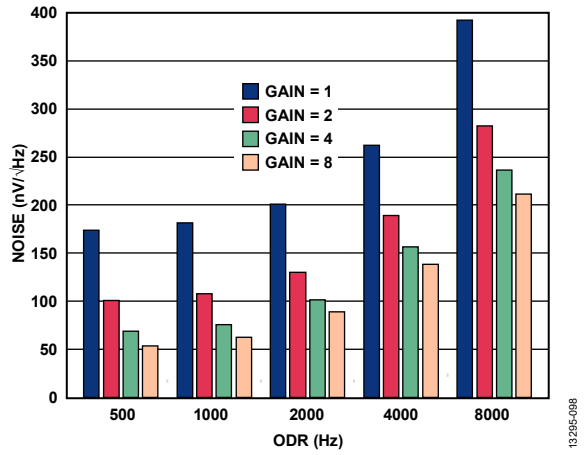

Figure 25. Noise vs. ODR, Low Power Mode

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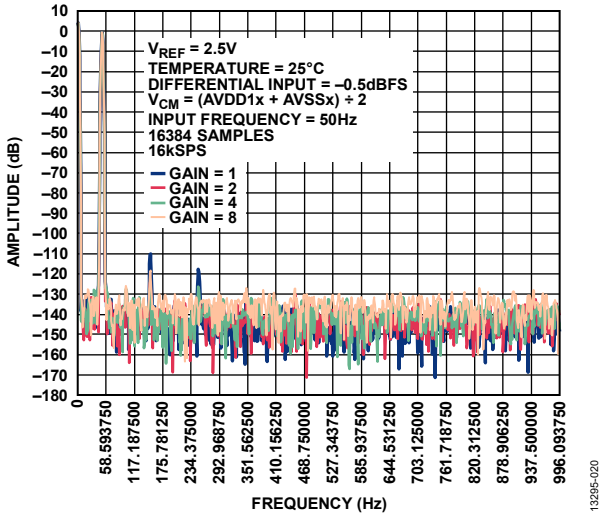

Figure 26. FFT Plot at 16 kSPS, High Resolution Mode, Input Frequency (f_{IN}) = 50 Hz (This Plot is a Close Up Perspective of the Original Data)

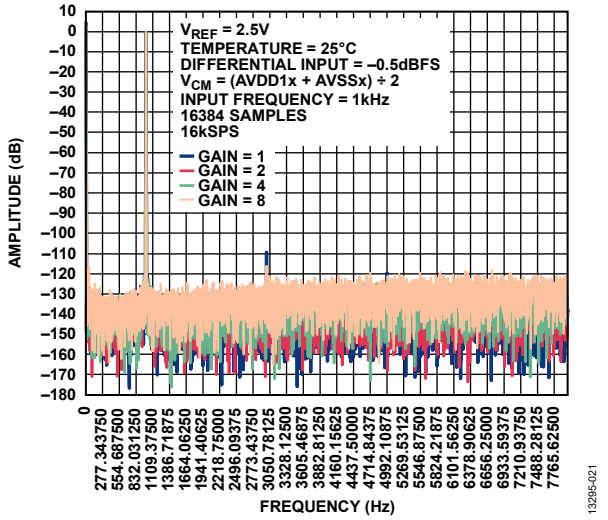

Figure 27. FFT Plot, High Resolution Mode, Input Frequency (f_{IN}) = 1 kHz

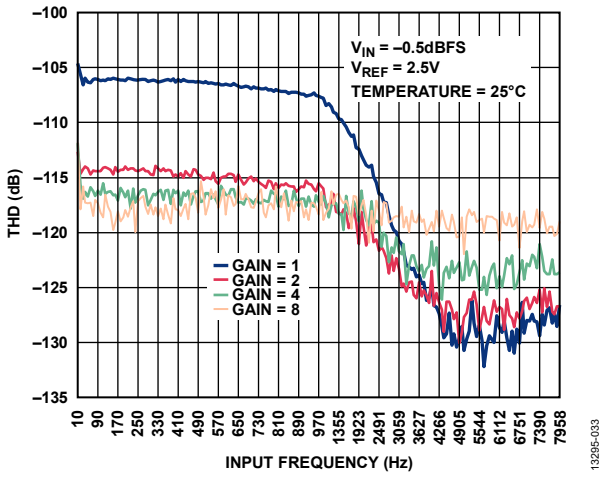

Figure 28. THD vs. Input Frequency at 8 kSPS, High Resolution Mode

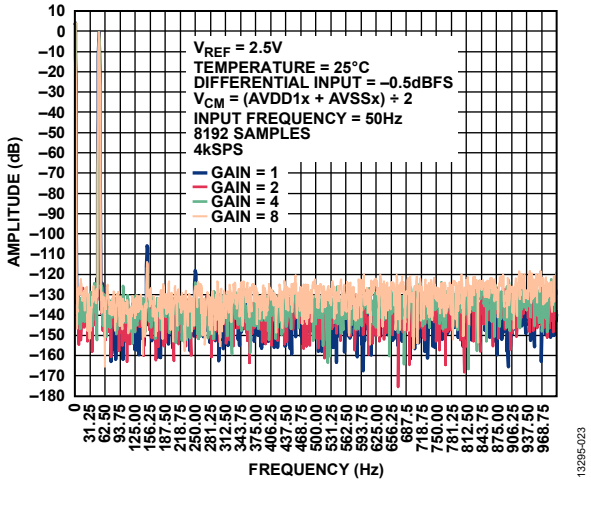

Figure 29. FFT Plot at 4kSPS, Low Power Mode, Input Frequency (f_{IN}) = 50 Hz, (This Plot is a Close Up Perspective of the Original Data)

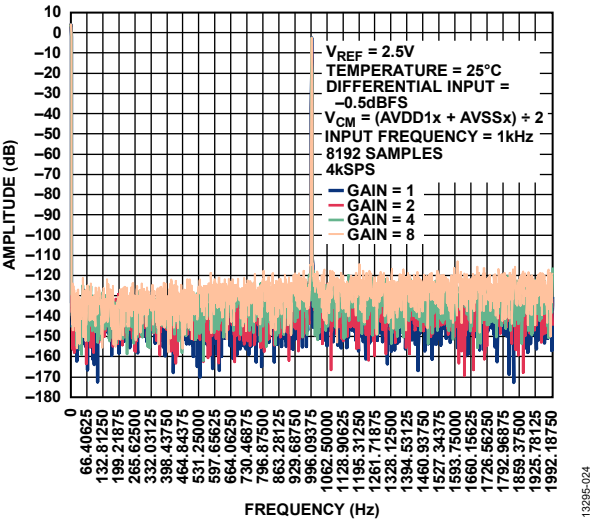

Figure 30. FFT Plot, Low Power Mode, Input Frequency (f_{IN}) = 1 kHz

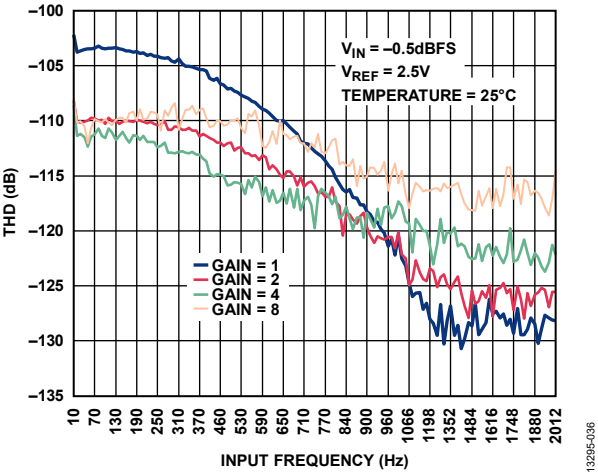

Figure 31. THD vs. Input Frequency at 2 kSPS, Low Power Mode

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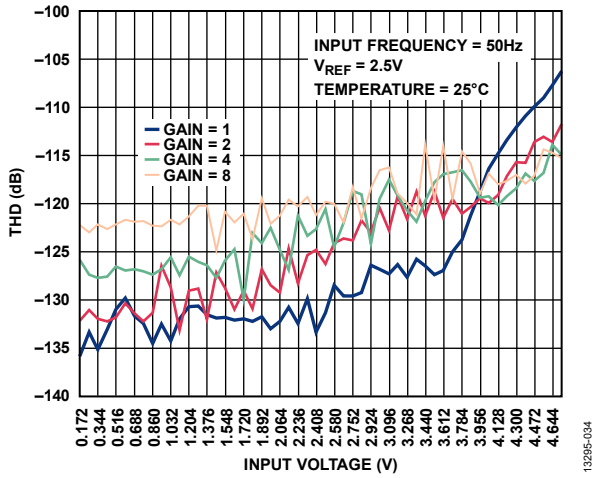

Figure 32. THD vs. Input Voltage at 2 kSPS, High Resolution Mode (Input Frequency = 50 Hz)

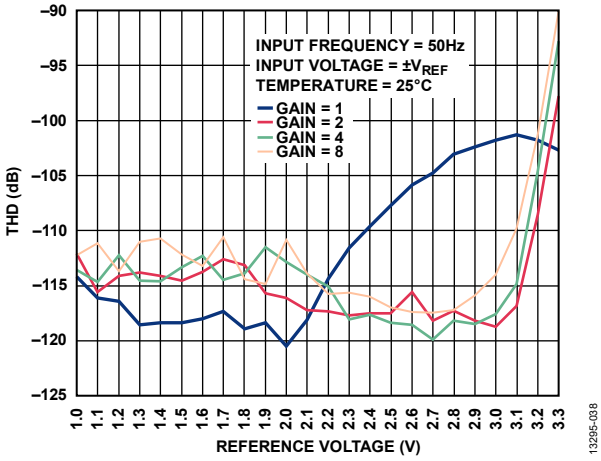

Figure 33. THD vs. Reference Voltage at 8 kSPS, High Resolution Mode (Input Frequency = 50 Hz)

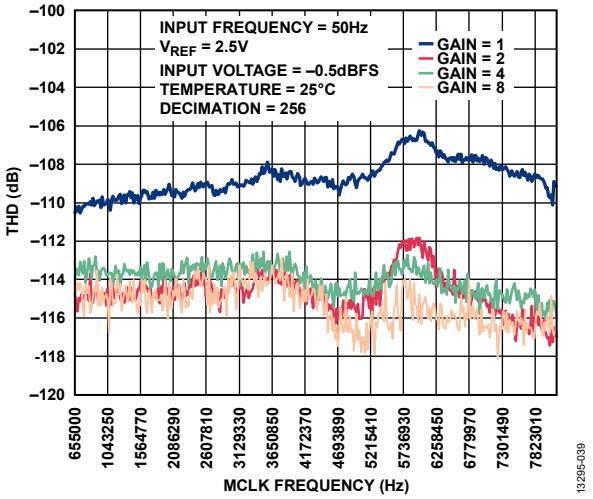

Figure 34. THD vs. MCLK Frequency, High Resolution Mode, Input Frequency (f_{IN}) = 50 Hz, Decimation = 256

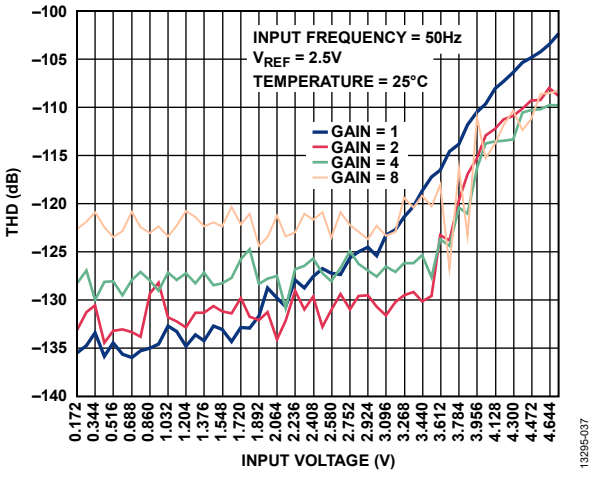

Figure 35. THD vs. Input Voltage at 500 SPS, Low Power Mode (Input Frequency = 50 Hz)

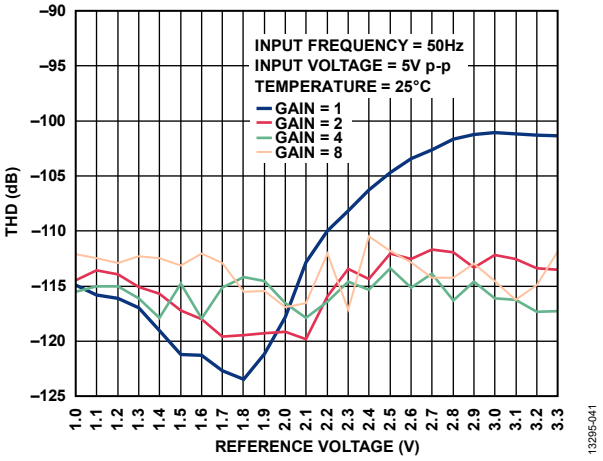

Figure 36. THD vs. Reference Voltage at 2 kSPS, Low Power Mode (Input Frequency = 50 Hz)

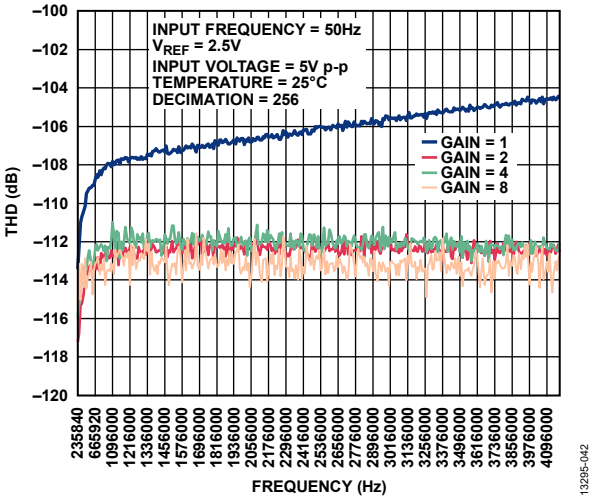

Figure 37. THD vs. MCLK Frequency, Low Power Mode, Input Frequency (f_{IN}) = 50 Hz, Decimation = 256

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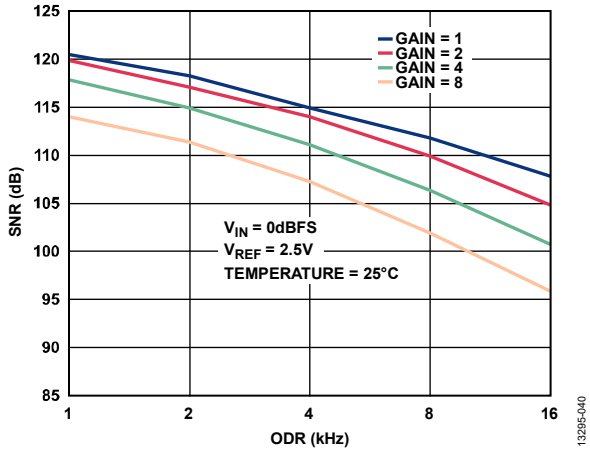

Figure 38. SNR vs. ODR at 8 kSPS, High Resolution Mode

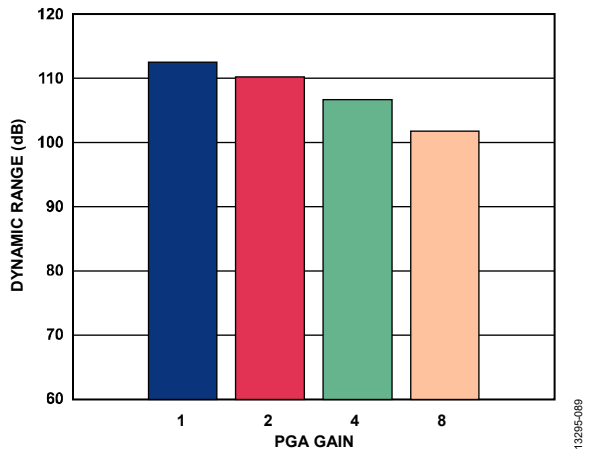

Figure 39. Dynamic Range vs. PGA Gain, High Resolution Mode, ODR = 8 kSPS

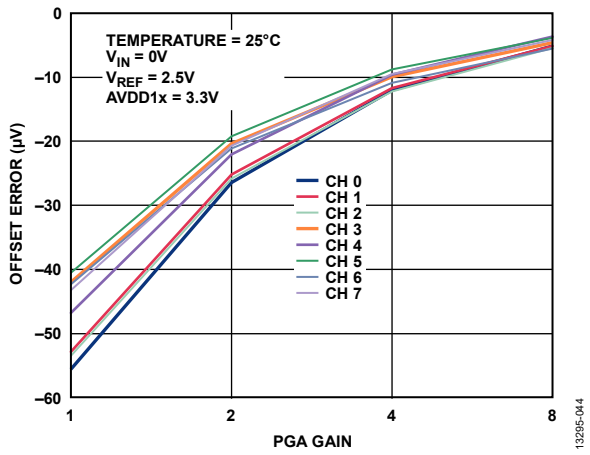

Figure 40. Offset Error vs. PGA Gain, High Resolution Mode

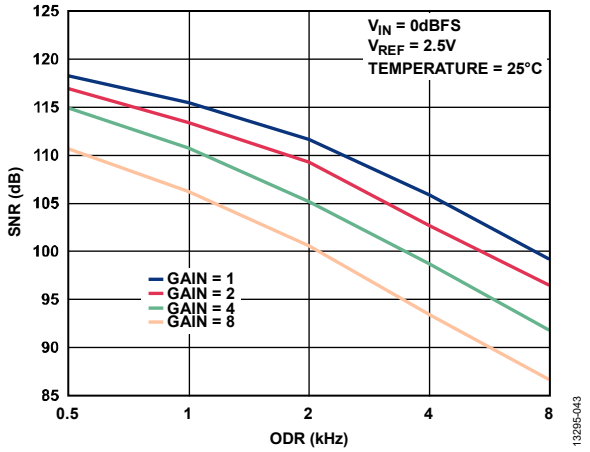

Figure 41. SNR vs. ODR at 2 kSPS, Low Power Mode

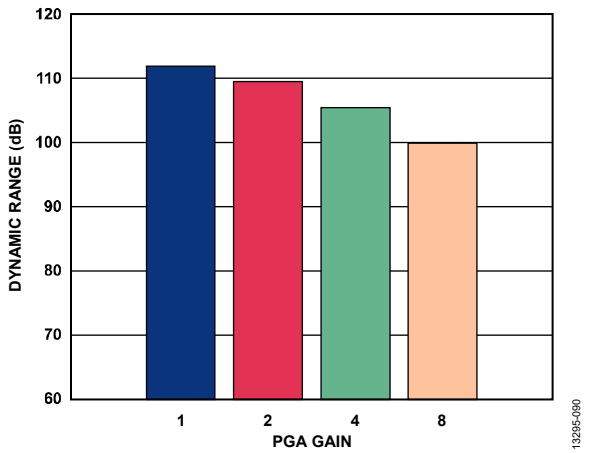

Figure 42. Dynamic Range vs. PGA Gain, Low Power Mode, ODR = 2 kSPS

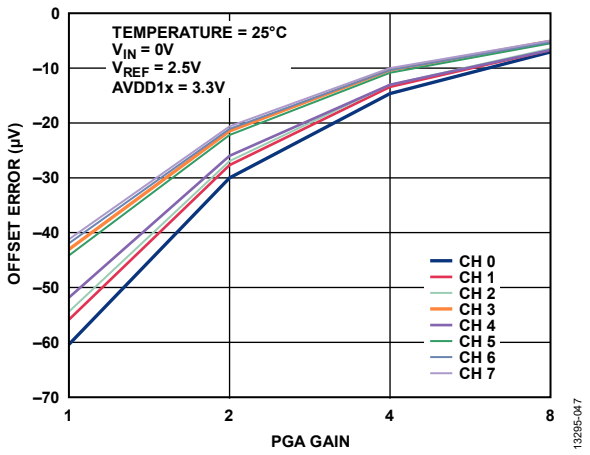

Figure 43. Offset Error vs. PGA Gain, Low Power Mode

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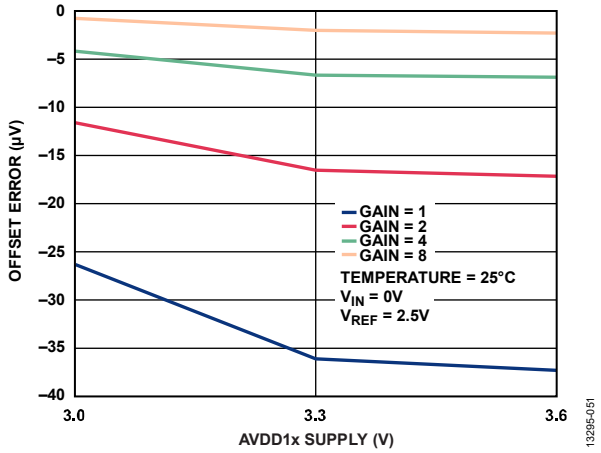

Figure 44. Offset Error vs. Supply Setting, High Resolution Mode

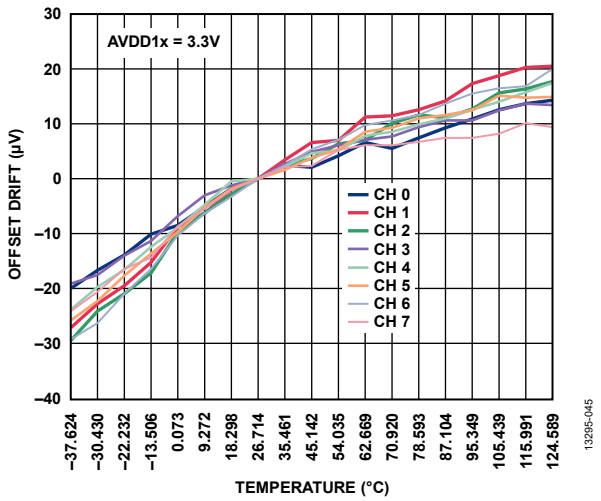

Figure 45. Offset Drift vs. Temperature

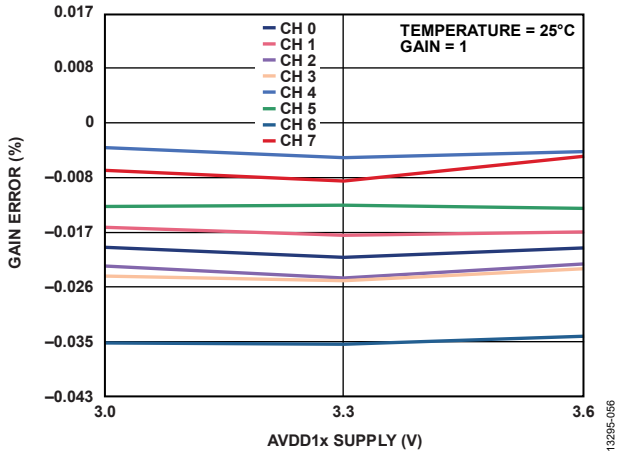

Figure 46. Gain Error vs. AVDD1x Supply, High Resolution Mode

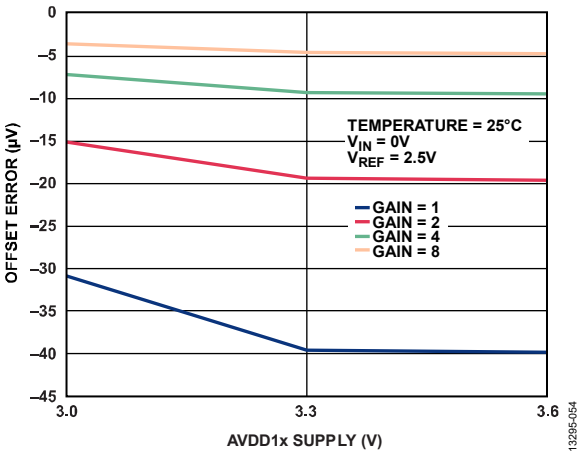

Figure 47. Offset Error vs. Supply Setting, Low Power Mode

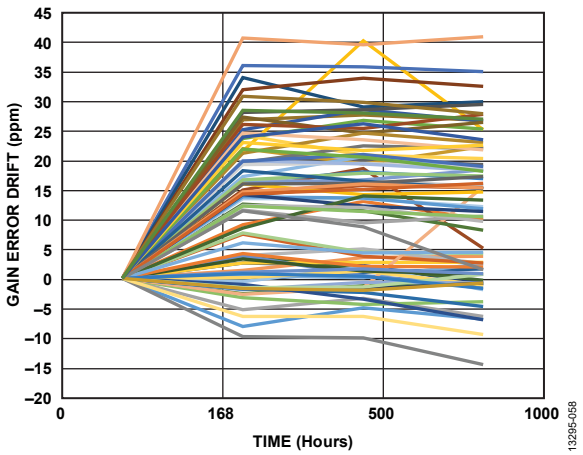

Figure 48. Gain Error Drift vs. Time

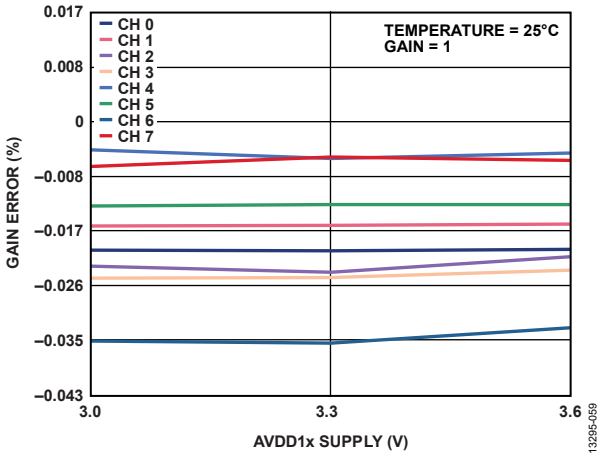

Figure 49. Gain Error vs. AVDD1x Supply, Low Power Mode

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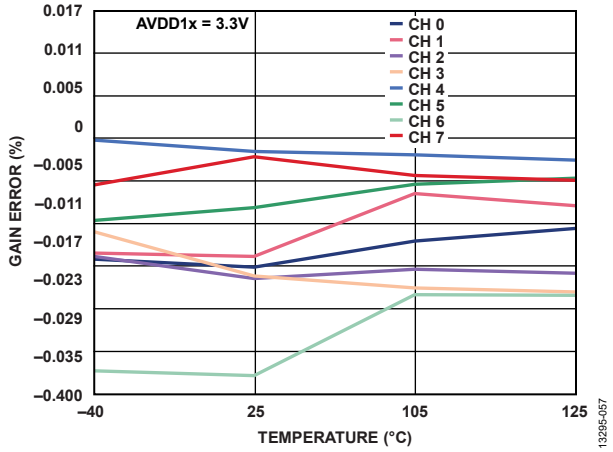

Figure 50. Gain Error vs. Temperature, High Resolution Mode, AVDD1x = 3.3 V

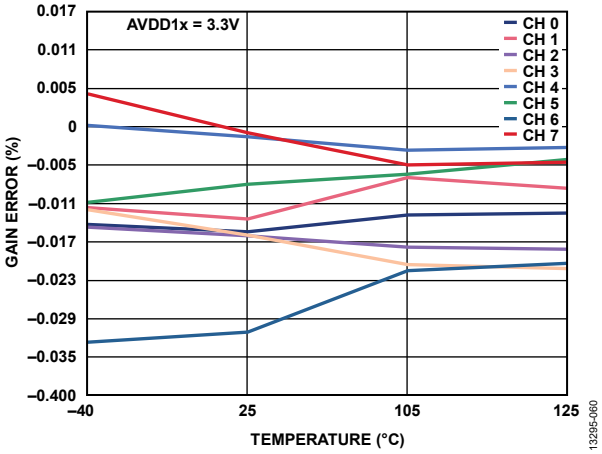

Figure 53. Gain Error vs. Temperature, Low Power Mode, AVDD1x = 3.3 V

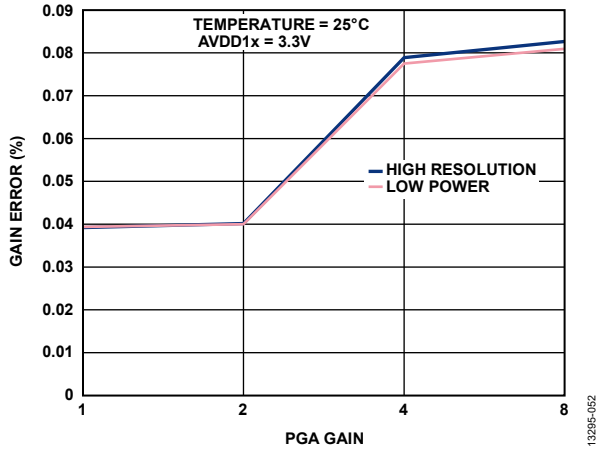

Figure 51. Channel Gain Mismatch, High Resolution Mode

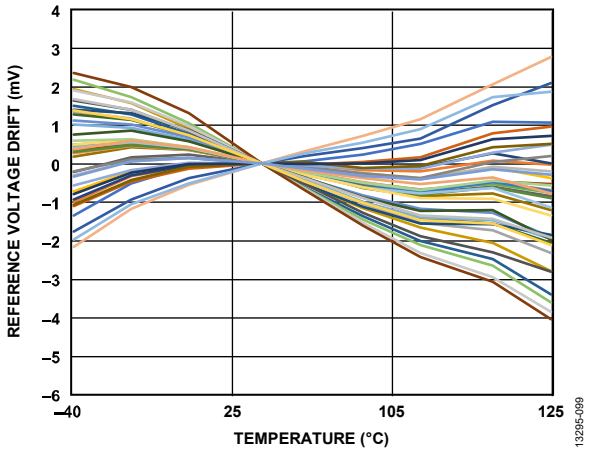

Figure 54. Internal Reference Voltage Drift

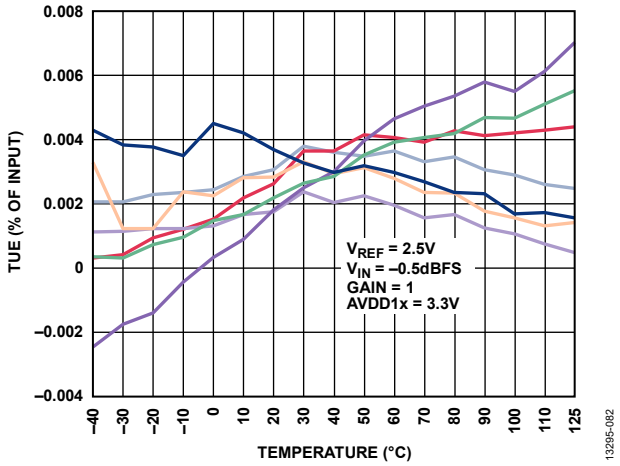

Figure 52. Total Unadjusted Error (TUE) (as % of Input) vs. Temperature, High Resolution Mode

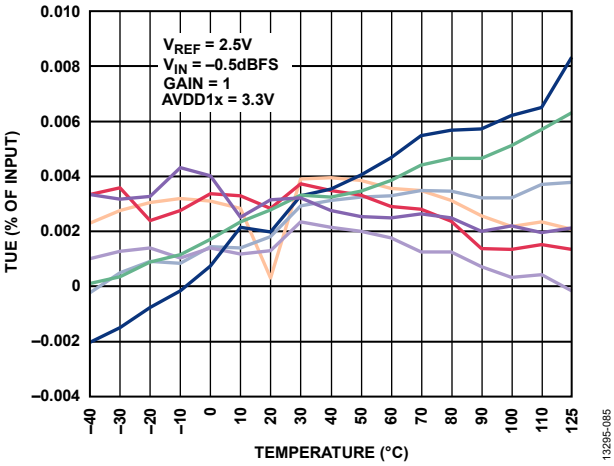

Figure 55. TUE (as % of Input) vs. Temperature, Low Power Mode

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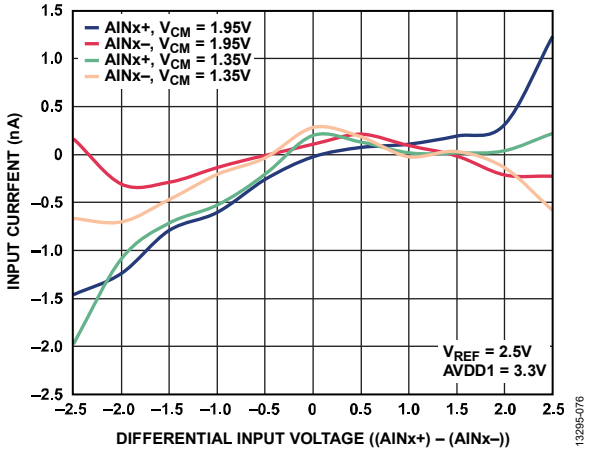

Figure 56. Input Current vs. Differential Input Voltage, High Resolution Mode

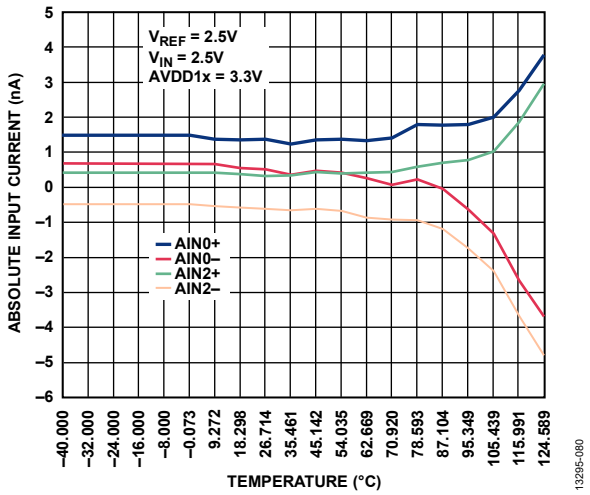

Figure 57. Absolute Input Current vs. Temperature, High Resolution Mode

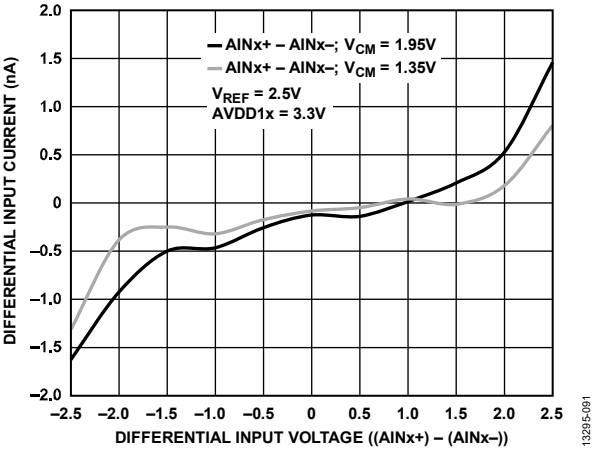

Figure 58. Differential Input Current vs. Differential Input Voltage, High Resolution Mode

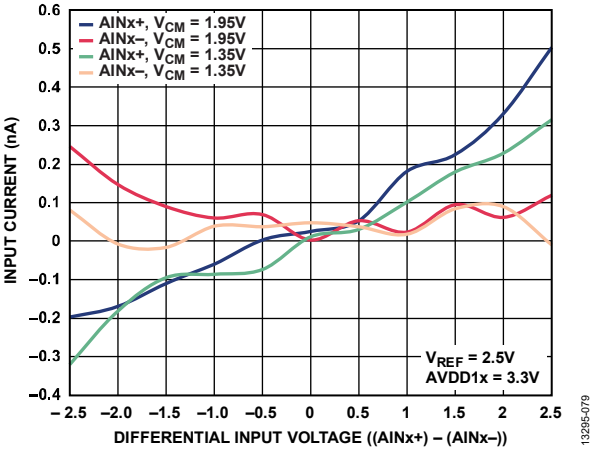

Figure 59. Input Current vs. Differential Input Voltage, Low Power Mode

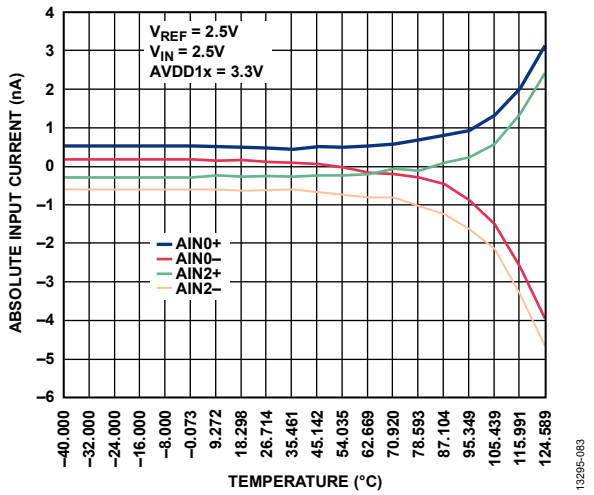

Figure 60. Absolute Input Current vs. Temperature, Low Power Mode

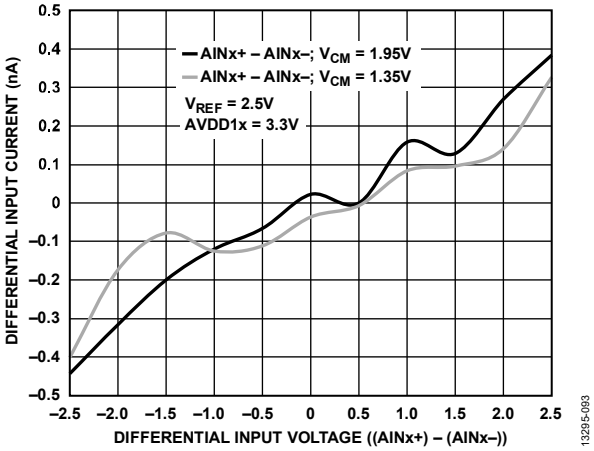

Figure 61. Differential Input Current vs. Differential Input Voltage, Low Power Mode

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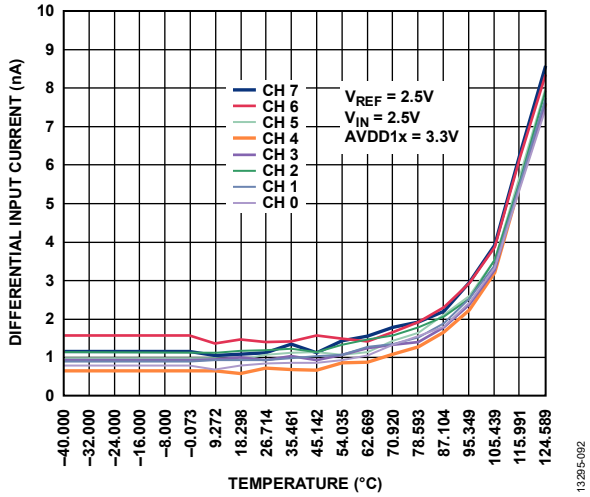

Figure 62. Differential Input Current vs. Temperature, High Resolution Mode

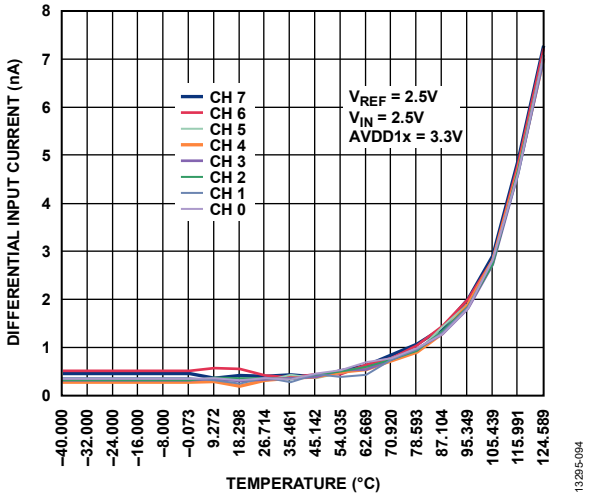

Figure 65. Differential Input Current vs. Temperature, Low Power Mode

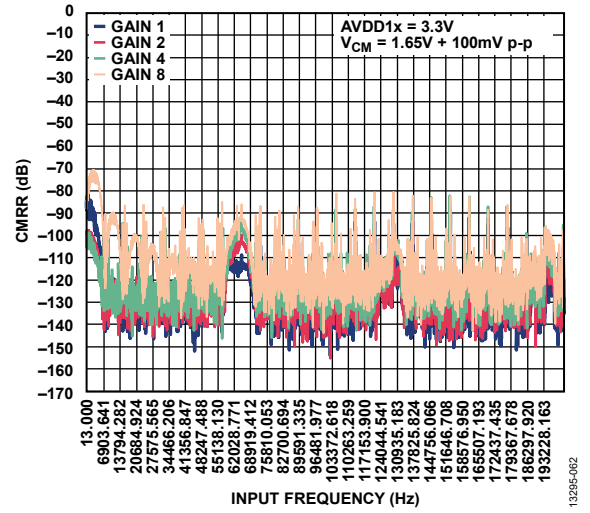

Figure 63. CMRR vs. Input Frequency at 8 kSPS, High Resolution Mode

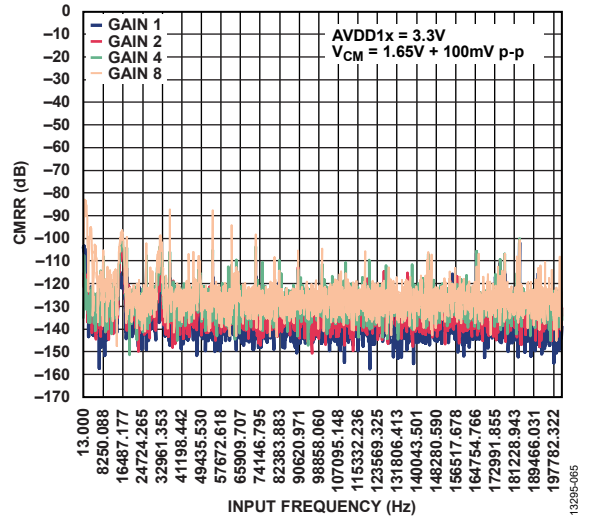

Figure 66. CMRR vs. Input Frequency at 2 kSPS, Low Power Mode

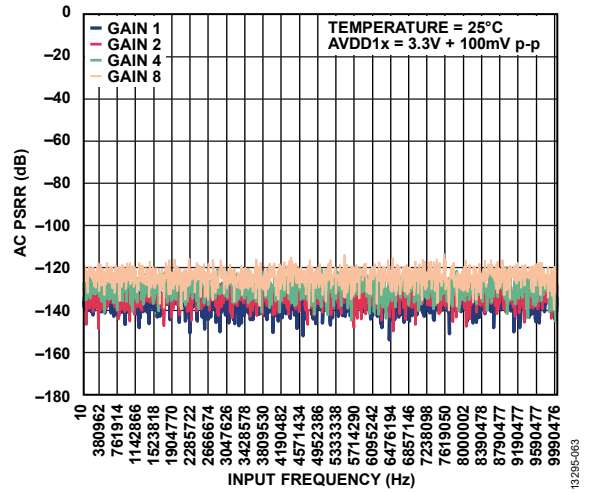

Figure 64. AC PSRR vs. Input Frequency at 8 kSPS, High Resolution Mode

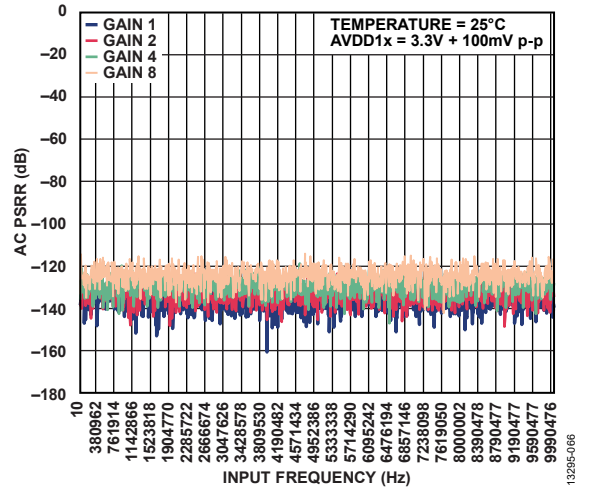

Figure 67. AC PSRR vs. Input Frequency at 2 kSPS, Low Power Mode

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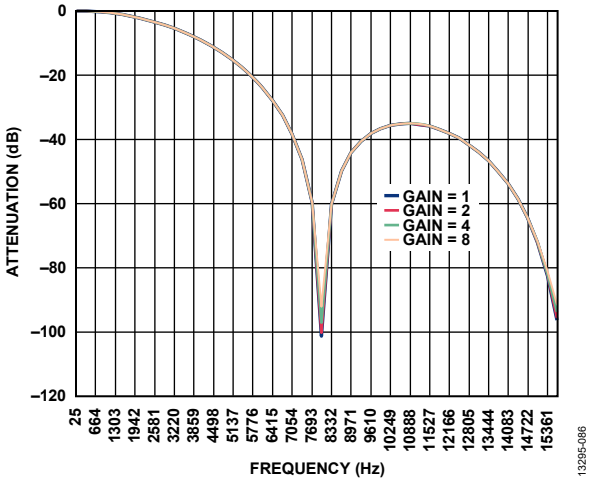

Figure 68. Filter Profiles at 8 kSPS, High Resolution Mode

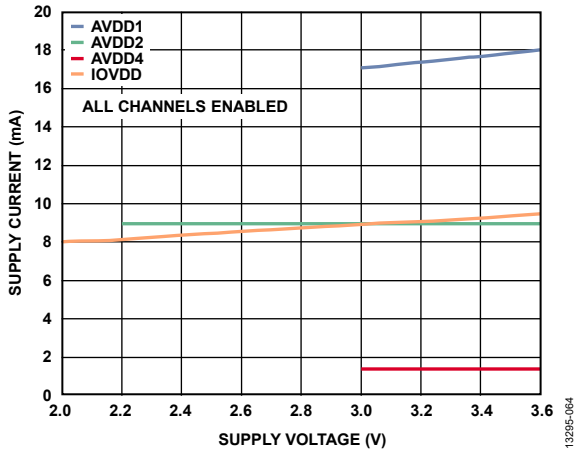

Figure 69. Supply Current vs. Supply Voltage at 8 kSPS, High Resolution Mode

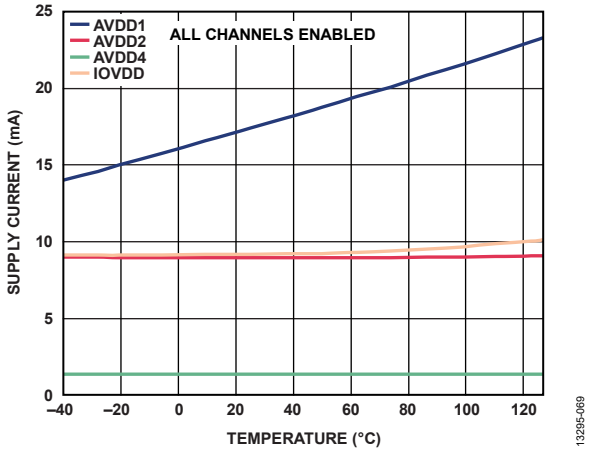

Figure 70. Supply Current vs. Temperature at 8 kSPS, High Resolution Mode

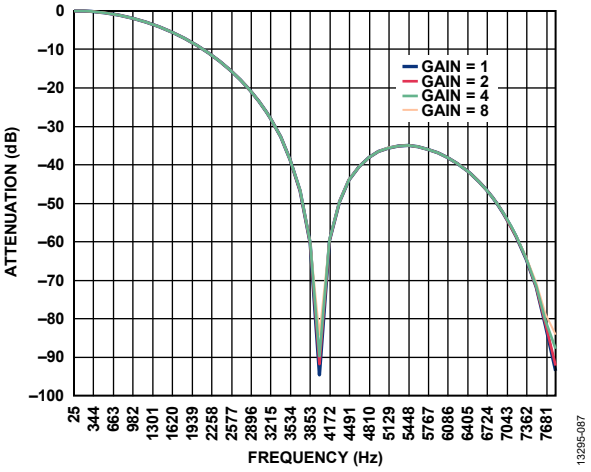

Figure 71. Filter Profiles at 2 kSPS, Low Power Mode

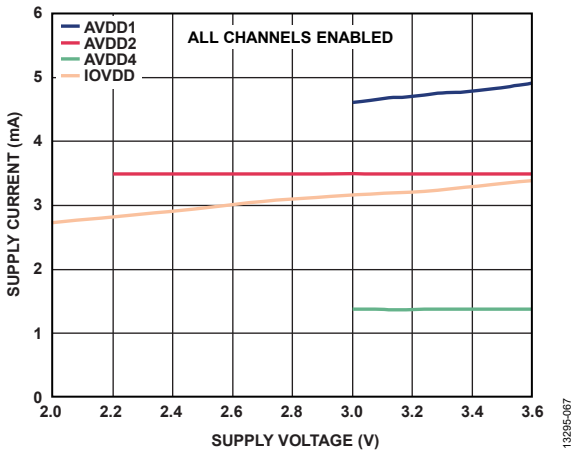

Figure 72. Supply Current vs. Supply Voltage at 2 kSPS, Low Power Mode

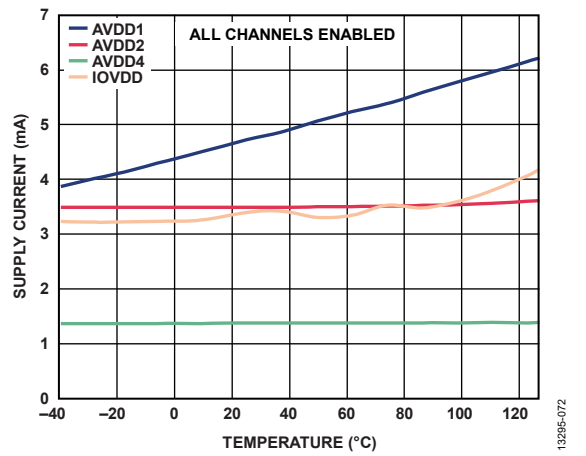

Figure 73. Supply Current vs. Temperature at 2 kSPS, Low Power Mode

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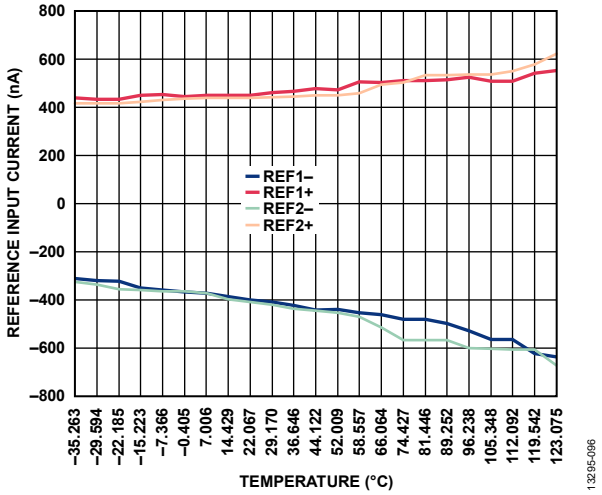

Figure 74. Reference Input Current vs. Temperature, High Resolution Mode

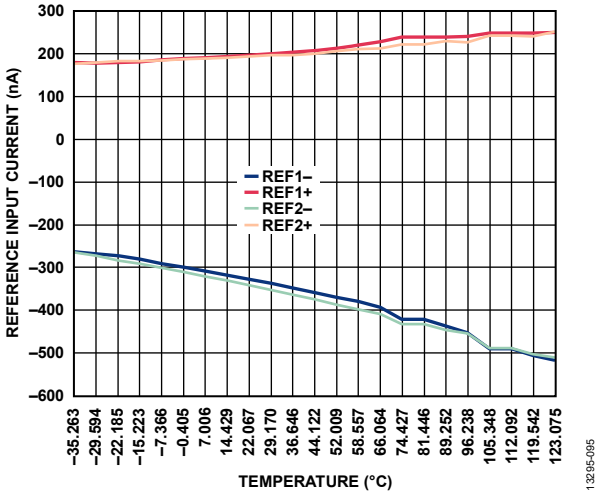

Figure 77. Reference Input Current vs. Temperature, Low Power Mode

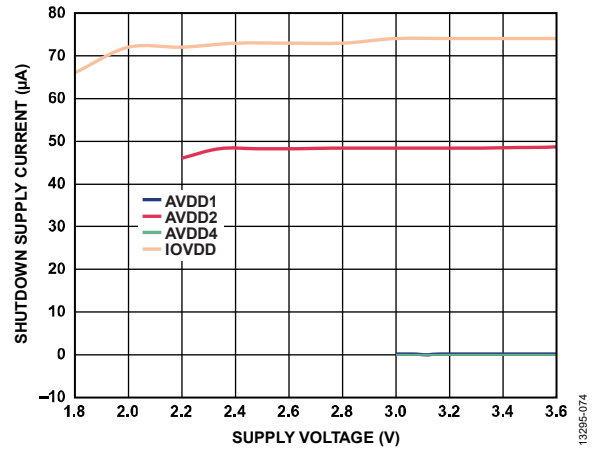

Figure 75. Shutdown Supply Current vs. Supply Voltage

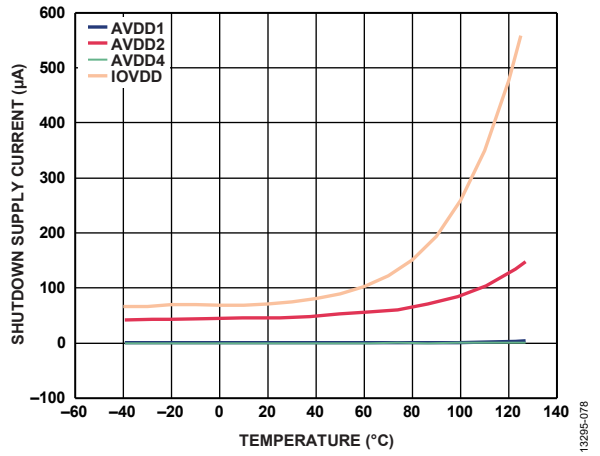

Figure 78. Shutdown Supply Current vs. Temperature

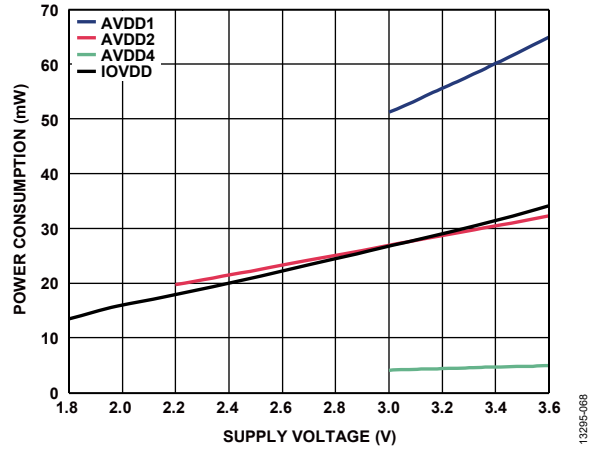

Figure 76. Power Consumption per Channel vs. Supply Voltage at 8 kSPS, High Resolution Mode

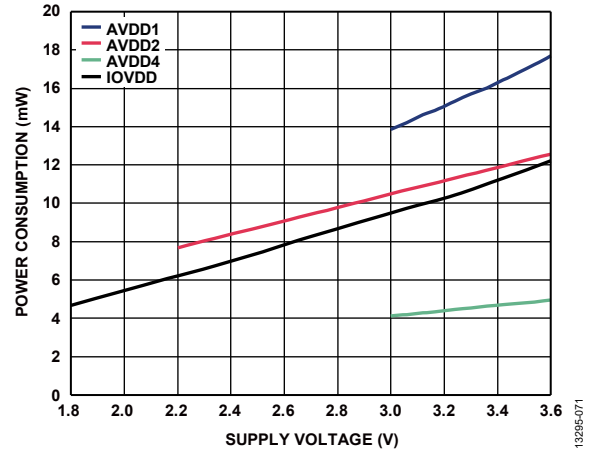

Figure 79. Power Consumption per Channel vs. Supply Voltage at 2 kSPS, Low Power Mode

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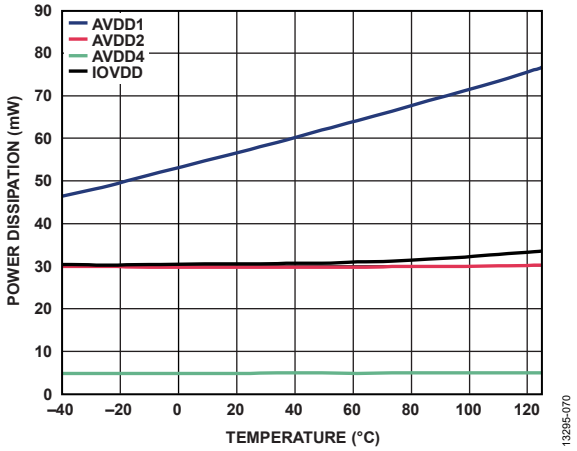

Figure 80. Power Dissipation vs. Temperature at 8 kSPS, High Resolution Mode

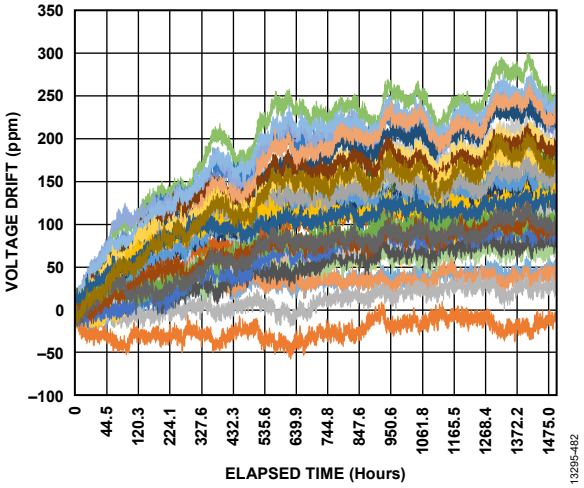

Figure 82. Internal Reference Long Term Drift from 0 Hours to 1500 Hours

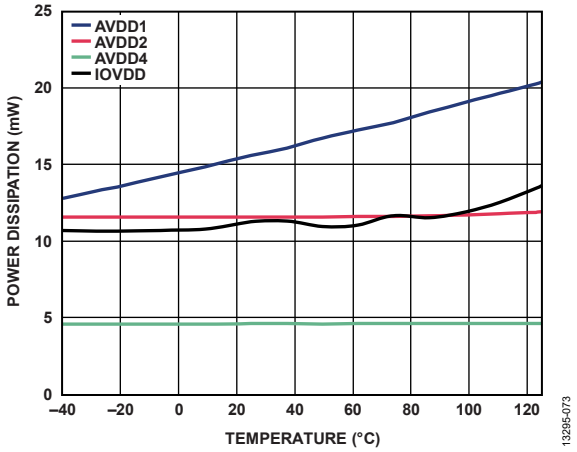

Figure 81. Power Dissipation vs. Temperature at 2 kSPS, Low Power Mode

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TERMINOLOGY

Common-Mode Rejection Ratio (CMRR)
CMRR is the ratio of the power in the ADC output of a 100 mV p-p differential input (AINx+ or AINx−) at a fixed frequency (f = 1 kHz) to the power of a 100 mV p-p sine wave applied to the common-mode voltage of AINx+ and AINx− at frequency f_S.

$$CMRR\ (\text{dB}) = 10 \log(Pf/Pf_S)$$

where:
Pf is the power at frequency, f, in the ADC output.
Pf_S is the power at frequency, f_S, in the ADC output.

Differential Nonlinearity (DNL) Error
In an ideal ADC, code transitions are 1 LSB apart. Differential nonlinearity is the maximum deviation from this ideal value. DNL error is often specified in terms of resolution for which no missing codes are guaranteed.

Integral Nonlinearity (INL) Error
Integral nonlinearity error refers to the deviation of each individual code from a line drawn from negative full scale through positive full scale. The point used as negative full scale occurs ½ LSB before the first code transition. Positive full scale is a level 1½ LSB beyond the last code transition. The deviation is measured from the middle of each code to the true straight line.

Dynamic Range
Dynamic range is the ratio of the rms value of the full-scale input signal to the rms noise measured for an input. The value for dynamic range is expressed in decibels.

Channel to Channel Isolation
Channel to channel isolation is a measure of the level of crosstalk between channels. It is measured by applying a full-scale frequency sweep sine wave signal to all seven nonselected input channels and determining how much that signal is attenuated in the selected channel. The figure is given for worst case scenarios across all eight channels of the AD7779.

Intermodulation Distortion
With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities creates distortion products at sum and difference frequencies of mfa and nfb, where m, n = 0, 1, 2, 3, and so on. Intermodulation distortion terms are those for which neither m nor n are equal to 0. For example, the second-order terms include (fa + fb) and (fa − fb), and the third-order terms include (2fa + fb), (2fa − fb), (fa + 2fb), and (fa − 2fb). The AD7779 is tested using the CCIF standard, where two input frequencies near the top end of the input bandwidth are used. In this case, the second-order terms are usually distanced in frequency from the original sine waves, and the third-order terms are usually at a frequency close to the input frequencies. As a result, the second- and third-order terms are specified separately. The calculation of the intermodulation distortion is per the THD specification, where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the sum of the fundamentals, expressed in decibels.

Gain Error
The first transition (from 100 … 000 to 100 … 001) occurs at a level ½ LSB above nominal negative full scale (−2.49999 V for the ±2.5 V range). The last transition (from 011 … 110 to 011 … 111) occurs for an analog voltage 1½ LSB below the nominal full scale (2.49999 V for the ±2.5V range). The gain error is the deviation of the difference between the actual level of the last transition and the actual level of the first transition from the difference between the ideal levels.

Gain Error Drift
Gain error drift is the ratio of the gain error change due to a temperature change of 1°C and the full-scale range (2^N). It is expressed in parts per million.

Least Significant Bit (LSB)
The least significant bit, or LSB, is the smallest increment that can be represented by a converter. For a fully differential input ADC with N bits of resolution, the LSB expressed in volts is

$$LSB\ (\text{V}) = \frac{2 \times V_{REF}}{2^N}$$

The LSB referred to the input is

$$LSB\ (V_{IN}) = \frac{\frac{2 \times V_{REF}}{PGA_{GAIN}}}{2^N}$$

Power Supply Rejection Ratio (PSRR)
Variations in power supply affect the full-scale transition but not the linearity of the converter. PSRR is the maximum change in the full-scale transition point due to a change in the power supply voltage from the nominal value.

Signal-to-Noise Ratio (SNR)
SNR is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, excluding harmonics and dc. The value for SNR is expressed in decibels.

Signal-to-(Noise + Distortion) Ratio (SINAD)
SINAD is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for SINAD is expressed in decibels.

Spurious-Free Dynamic Range (SFDR)
SFDR is the difference, in decibels, between the rms amplitude of the input signal and the peak spurious signal (including harmonics).

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Total Harmonic Distortion (THD)
THD is the ratio of the rms sum of the first five harmonic components to the rms value of a full-scale input signal and is expressed in decibels.

Offset Error
Offset error is the difference between the ideal midscale input voltage (0 V) and the actual voltage producing the midscale output code.

Offset Error Drift
Offset error drift is the ratio of the offset error change due to a temperature change of 1°C and the full-scale code range (2^N). It is expressed in µV/°C.

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RMS NOISE AND RESOLUTION

Table 10 through Table 12 show the dynamic range (DR), rms noise (RTI), effective number of bits (ENOB), and effective resolution (ER) of the AD7779 for various output data rates and gain settings. The numbers given are for the bipolar input range with an external 2.5 V reference. These numbers are typical and are generated with a differential input voltage of 0 V when the ADC is continuously converting on a single channel.

It is important to note that the effective resolution is calculated using the rms noise; 16,384 consecutives samples were used to calculate the rms noise.

$$Effective\ Resolution = \log2(Input\ Range/RMS\ Noise)$$

$$ENOB = (DR - 1.78)/6$$

HIGH RESOLUTION MODE

Table 10. DR (dB) and RTI (μV_{RMS}) for High Resolution Mode

Decimation Rate	Output Data Rate (SPS)	f_{-3dB} (Hz)	Gain							
			1		2		4		8	
			DR	RTI	DR	RTI	DR	RTI	DR	RTI
128	16000	5029.99	108.28	6.80	105.13	4.80	101	3.95	95.86	3.46
256	8000	2521.99	112.5	4.12	110.21	2.63	106.8	2.01	102	1.72
512	4000	1267.99	116.12	2.70	114.7	1.59	111.6765	1.11	107.61	0.93
1024	2000	640.99	119.5	1.87	118.3	1.07	115.82	0.70	112	0.57
2048	1000	327.49	122.37	1.33	121.55	0.74	119	0.49	115.5	0.38

Table 11. ENOB and ER for High Resolution Mode

Decimation Rate	Output Data Rate (SPS)	f_{-3dB} (Hz)	Gain							
			1		2		4		8	
			ENOB	ER	ENOB	ER	ENOB	ER	ENOB	ER
128	16000	5029.99	17.75	19.49	17.23	18.99	16.54	18.27	15.68	17.46
256	8000	2521.99	18.46	20.21	18.08	19.86	17.51	19.25	16.71	18.47
512	4000	1267.99	19.06	20.82	18.82	20.58	18.32	20.10	17.64	19.36
1024	2000	640.99	19.62	21.35	19.42	21.16	19.01	20.76	18.37	20.08
2048	1000	327.49	20.1	21.84	19.97	21.69	19.54	21.28	18.96	20.66

LOW POWER MODE

Table 12. DR and RTI (μV_{RMS}) for Low Power Mode

Decimation Rate	Output Data Rate (SPS)	f_{-3dB} (Hz)	Gain							
			1		2		4		8	
			DR	RTI	DR	RTI	DR	RTI	DR	RTI
64	8000	2521.99	100	19.1	96	13.4	92	11.2	87	10.3
128	4000	1267.99	106	8.82	103	6.18	98.5	5.2	94	4.65
256	2000	640.99	112	4.53	108.5	3.03	106	2.32	100.5	2.05
512	1000	327.49	116	2.89	114	1.77	111	1.24	107	1.04

Table 13. ENOB and ER for Low Power Mode

Decimation Rate	Output Data Rate (SPS)	f_{-3dB} (Hz)	Gain							
			1		2		4		8	
			ENOB	ER	ENOB	ER	ENOB	ER	ENOB	ER
64	8000	2521.99	16.37	18.00	15.71	17.51	15.04	16.77	14.21	15.89
128	4000	1267.99	17.37	19.11	16.87	18.63	16.12	17.87	15.37	17.04
256	2000	640.99	18.37	20.07	17.79	19.65	17.37	19.04	16.46	18.22
512	1000	327.49	19.04	20.72	18.71	20.43	18.21	19.94	17.54	19.20

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THEORY OF OPERATION

The AD7779 is an 8-channel, simultaneously sampling, low noise, 24-bit Σ-Δ ADC with integrated digital filtering per channel and SRC.

The AD7779 offers two operation modes: high resolution mode, which offers up to 16 kSPS, and low power mode, which offers up to 8 kSPS. In low power mode, the specifications are guaranteed up to 4 kSPS, with performance degradation expected at ODRs higher than 4 kSPS.

The AD7779 employs a Σ-Δ conversion technique to convert the analog input signal into an equivalent digital word. The overview of the Σ-Δ technique is that the modulator samples the input waveform and outputs an equivalent digital word at the input clock frequency, f_{CLKIN}.

Due to the high oversampling rate, this technique spreads the quantization noise from 0 to $f_{CLKIN}/2$ (in the case of the AD7779, f_{CLKIN} relates to the external clock); therefore, the noise energy contained in the band of interest is reduced (see Figure 83). To further reduce the quantization noise, a high order modulator is employed to shape the noise spectrum so that most of the noise energy is shifted out of the band of interest (see Figure 84). The digital filter that follows the modulator removes the large out of band quantization noise (see Figure 85).

For more information on basic and advanced concepts of Σ-Δ ADCs, see the MT-022 and MT-023.

Digital filtering has certain advantages over analog filtering. Because digital filtering occurs after the analog-to-digital conversion process, it can remove noise injected during the conversion. Analog filtering cannot remove noise injected during conversion.

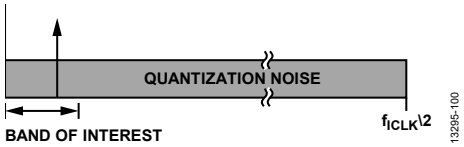

Figure 83. Σ-Δ ADC Operation, Reduction of Noise Energy Contained in the Band of Interest (Linear Scale X-Axis)

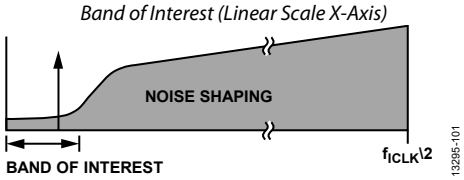

Figure 84. Σ-Δ ADC Operation, Majority of Noise Energy Shifted Out of the Band of Interest (Linear Scale X-Axis)

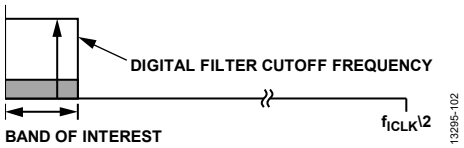

Figure 85. Σ-Δ ADC Operation, Removal of Noise Energy from the Band of Interest (Linear Scale X-Axis)

The Σ-Δ ADC starts the conversions of the input signal after the supplies generated by the internal LDOs become stable. An external signal is not required to generate the conversions.

ANALOG INPUTS

The AD7779 can be operated in bipolar or unipolar modes and accepts true differential, pseudo differential, and single-ended input signals, as shown in Figure 86 through Figure 89.

Table 14 summarizes the maximum differential input signal and dynamic range for the different input modes.

Table 14. Input Signal Modes

Input Signal Mode	PGA Gain	Maximum Differential Signal	Maximum Peak-to-Peak Signal
True Differential	All gains	$\pm(V_{REF}/PGA_{GAIN})$	$2 \times V_{REF}/PGA_{GAIN}$
Pseudo Differential	All gains	$\pm(V_{REF}/PGA_{GAIN})$	$2 \times V_{REF}/PGA_{GAIN}$
Single-Ended	All gains	V_{REF}/PGA_{GAIN}	V_{REF}/PGA_{GAIN}

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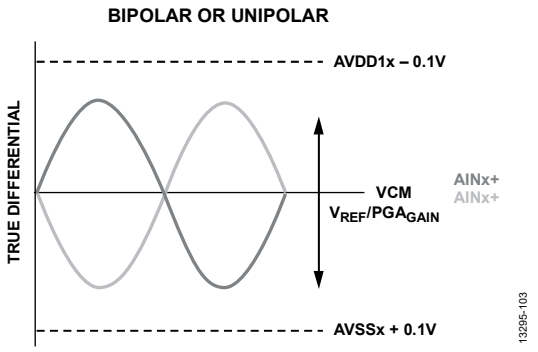

Figure 86. Σ-Δ ADC Input Signal Configuration, True Differential

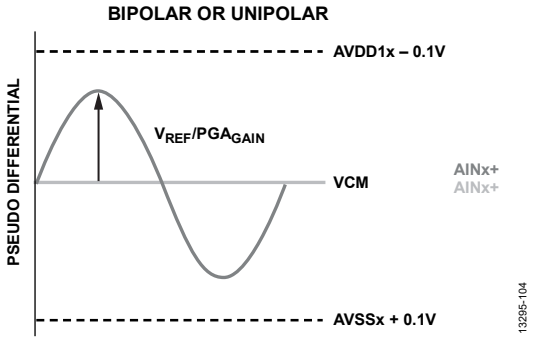

Figure 87. Σ-Δ ADC Input Signal Configuration, Pseudo Differential

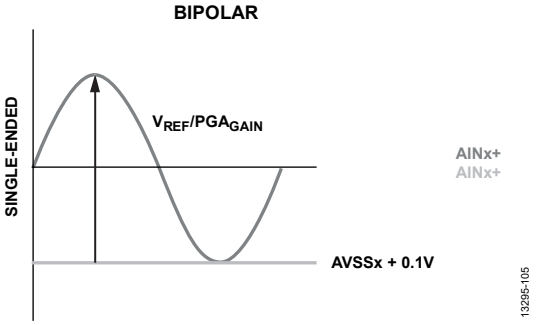

Figure 88. Σ-Δ ADC Input Signal Configuration, Single-Ended Bipolar

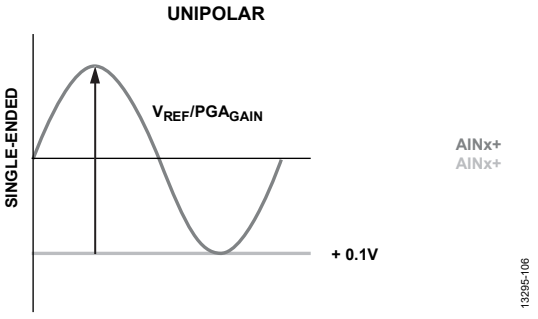

Figure 89. Σ-Δ ADC Input Signal Configuration, Single-Ended Unipolar

The input signal common mode is not limited, but keep the absolute input signal voltage on any AINx± pin between AVSSx + 100 mV and AVDD1x – 100 mV; otherwise, the input signal linearity degrades and, if the signal voltage exceeds the absolute maximum signal rating, damages the device.

Figure 90 shows the maximum and minimum voltage common-mode range at different PGA gains for a maximum differential input voltage.

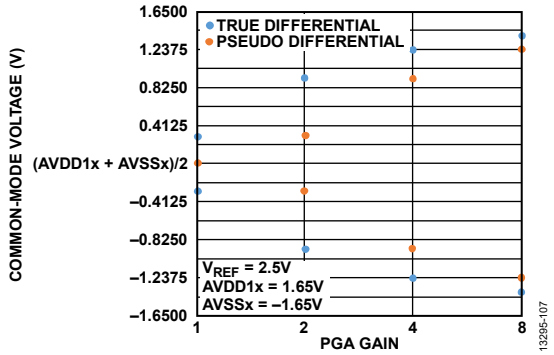

Figure 90. Maximum Common-Mode Voltage Range for a Maximum Differential Input Signal

The AD7779 provides a common-mode voltage pin (AVDD1x + AVSSx)/2), VCM, for the single-supply, pseudo differential, or true differential input configurations.

TRANSFER FUNCTION

The AD7779 can operate with up to a 3.6 V reference, typical at 2.5 V, and converts the differential voltage between the analog inputs (AINx+ and AINx–) into a digital output. The ADC converts the voltage difference between the analog input pins (AINx+ – AINx–) into a digital code on the output. The 24-bit conversion result is in MSB first, twos complement format, as shown in Table 15 and Figure 91.

Table 15. Output Codes and Ideal Input Voltages for PGA = 1×

Condition	Analog Input (AINx+ – AINx–), V_{REF} = 2.5 V	Digital Output Code, Twos Complement (Hex)
FS – 1 LSB	+2.499999702 V	0x7FFFFF
Midscale + 1 LSB	+298 nV	0x000001
Midscale	0 V	0x000000
Midscale – 1 LSB	–298 nV	0xFFFFFF
–FS + 1 LSB	–2.499999702 V	0x800001
–FS	–2.5 V	0x800000

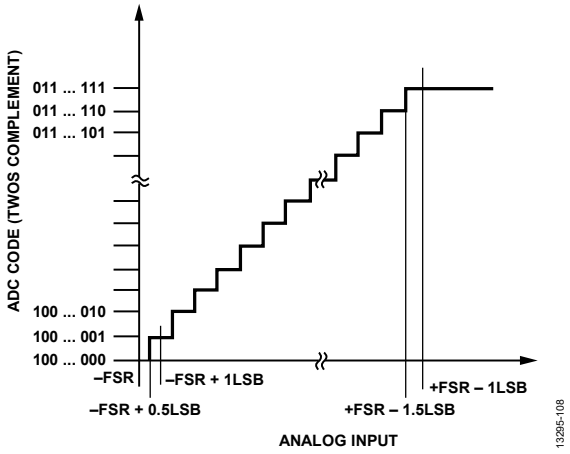

Figure 91. Transfer Function

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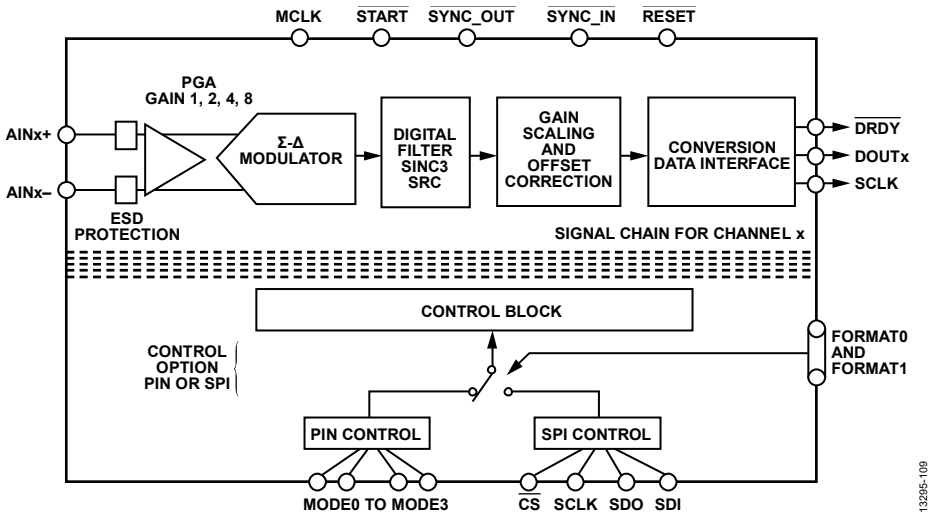

Figure 92. Top Level Core Signal Chain

CORE SIGNAL CHAIN

Each Σ-Δ ADC channel on the AD7779 has an identical signal path from the analog input pins to the digital output pins. Figure 92 shows a top level implementation of this signal chain. Prior to each Σ-Δ ADC, a PGA maps sensor outputs into the ADC inputs, providing low input current in dc (±4 nA, input current, and ±1.5 nA differential input current), an 8 pF input capacitance in ac, and configurable gains of 1, 2, 4, and 8. Each ADC channel has its own Σ-Δ modulator, which oversamples the analog input and passes the digital representation to the digital filter block. The data is filtered, scaled for gain and offset, and is then output on the data interface.

To minimize power consumption, individually disable the channels.

CAPACITIVE PGA

Each Σ-Δ ADC has a dedicated PGA, offering gain ranges of 1, 2, 4, and 8. This PGA reduces the need for an external input buffer and allows the user to amplify small sensor signals to use the full dynamic range of the AD7779.

The PGA maximize the signal chain dynamic range for small sensor output signals.

The AD7779 uses chopping of the PGA to minimize offset and offset drift in the input amplifier, reducing the 1/f noise as well. For the AD7779, the chopping frequency is set to 64 kHz for high resolution mode, and 16 kHz for low power mode. See the AN-1392 Application Note for more information. The chopping tone is rejected by the SINC filter.

To minimize intermodulation effects that may cause image in the band of interest, it is recommended to limit the input signal bandwidth to 2/3 of the chop frequency.

The capacitive PGA common-mode voltage does not depend on the gain, and can be any value as long as the input signal voltage is within AVSSx + 100 mV to AVDD1x – 100 mV. See Figure 90 for the maximum common-mode voltage at maximum differential input signals.

INTERNAL REFERENCE AND REFERENCE BUFFERS

The AD7779 integrates a 2.5 V, 10 ppm/°C typical, voltage reference that is disabled at power-up. The buffered reference is available at Pin 49 and offers up to 10 mA of continuous current. A 100 nF capacitor is required if the reference is enabled.

In applications where a low noise reference is required, it is recommended to add a low-pass filter (LPF) with a cutoff frequency (f_{CUTOFF}) below 10 Hz to the REF_OUT pin. Connect the output of this filter to REFx+, and connect AVSSx to REFx–. In this scenario, configure the Σ-Δ reference externally by configuring the reference buffers in enable or precharge mode. An example of performance with and without the output filter is shown in Figure 93.

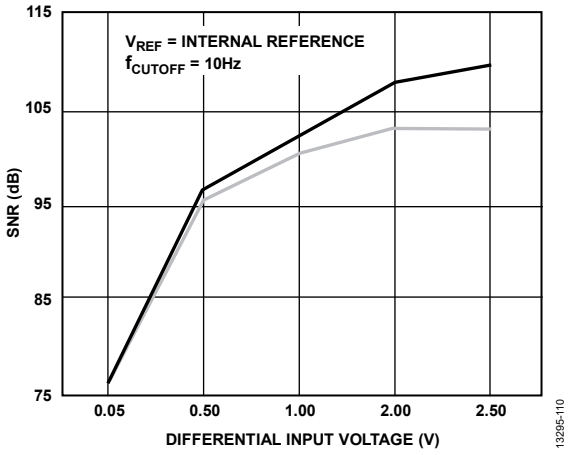

Figure 93. SNR Adding External LPF with V_{REF} = Internal Reference and f_{CUTOFF} = 10 Hz

The AD7779 can be used with an external reference connected between the REFx+ and REFx– pins. Recommended reference voltage sources for the AD7779 include the ADR441 and ADR4525 family of low noise, high accuracy voltage references.

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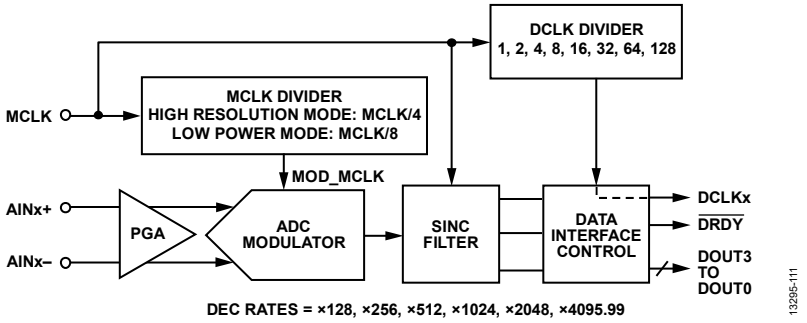

Figure 94. Clock Generation on the AD7779

The reference buffers can be operated in three different modes: buffer enabled mode, buffer bypassed mode, and buffer precharged mode.

In buffer enabled mode, the buffer is fully enabled, minimizing the current requirements from the external references. Note that the buffer output voltage headroom is ±100 mV from the rails.

In buffer bypassed mode, the external reference is directly connected to the ADC reference capacitors; the reference must provide enough current to correctly charge the internal ADC reference capacitors. In this mode of operation, a degradation in crosstalk is expected because the ADC channels are not isolated from each other.

Buffer precharged (pre-Q) mode is the default operation mode. It is a hybrid mode where the internal reference buffers are connected during the initial acquisition time to precharge the internal ADC reference capacitors. During the final phase of the acquisition, the reference is connected directly to the ADC capacitors. This mode has some benefits compared to the buffer enabled and buffer bypassed modes. In buffer precharged mode, the reference current requirements are minimized compared to buffer bypassed mode the noise contribution from the internal reference buffers is removed (compared to buffer enabled mode).

In buffer precharged mode, the headroom/footroom of the buffer reference is not applicable because the reference sets the final voltage in the ADC reference capacitors.

INTEGRATED LDOs

The AD7779 has three internal LDOs to regulate the internal supplies: two LDOs for the analog block and one LDO for the digital core. The internal LDOs requires an external 1 µF decoupling capacitor on the DREGCAP, AREG1CAP, and the AREG2CAP pins. The LDO slew rate may be low because it depends on the main supply slew rate; therefore, a hardware reset generated by pulsing the $\overline{\text{RESET}}$ pin at power-up is required to guarantee that the digital block initializes correctly.

CLOCKING AND SAMPLING

The AD7779 includes eight Σ-Δ ADC cores. Each ADC receives the same master clock signal. The AD7779 requires a maximum external MCLK frequency of 8192 kHz for high resolution mode and 4096 kHz for low power mode. The MCLK is internally divided by 4 in high resolution mode and by 8 in low power mode to produce the modulator MCLK (MOD_MCLK) signal used as the modulator sampling clock for the ADCs. The MCLK can be decreased to accommodate lower ODRs if the minimum ODR selected by the SINC filter is not low enough. If the external clock is lower than 250 kHz, set the CLK_QUAL_DIS bit (in SPI control mode only).

The AD7779 integrates an internal oscillator clock that initializes the internal registers at power-up. The CLK_SEL pin defines the external clock used after initialization (see Table 16).

Table 16. Clock Sources

CLK_SEL State	Clock Source	Connection
0	CMOS	Input to XTAL2/MCLK, IOVDD logic level. XTAL1 must be tied to DGND.
1	Crystal	Connected between XTAL1 and XTAL2/MCLK.

The MCLK signal generates the DCLK output signal, which in turn clocks the Σ-Δ conversion data from the AD7779, as shown in Figure 94.

DIGITAL RESET AND SYNCHRONIZATION PINS

An external pulse in the $\overline{\text{SYNC_IN}}$ pin generates the internal reset of the digital block; this pulse does not affect the data programmed in the internal registers. A pulse in this pin is required in two cases as follows:

- After updating one or more registers directly related to the sinc3 filter. These are power mode, offset, gain, and phase compensation.
- To synchronize multiple devices, the pulse in the $\overline{\text{SYNC_IN}}$ pin must be synchronous with MCLK.

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There are two different ways to achieve a synchronous pulse if the controller/processor cannot generate it, as follows:

- Applying an asynchronous pulse on the $\overline{\text{START}}$ pin, which is then internally synchronized with the external MCLK clock, and the resulting synchronous signal is output on the $\overline{\text{SYNC_OUT}}$ pin.
- Triggering the $\overline{\text{SYNC_OUT}}$ internally. When the AD7779 is configured in SPI control mode, toggling Bit 0 in the GEN_USER_CONFIG_2 register generates a synchronous pulse that is output on the $\overline{\text{SYNC_OUT}}$ pin.

The $\overline{\text{SYNC_IN}}$ and $\overline{\text{SYNC_OUT}}$ pins must be externally connected if internal synchronization is used.

If multiple AD7779 devices must be synchronized, the $\overline{\text{SYNC_OUT}}$ pin of one device can be connected to multiple devices. This synchronization method requires the use of a common MCLK signal for all the AD7779 devices connected, as shown in Figure 95.

If the $\overline{\text{START}}$ pin is not used, tie it to IOVDD.

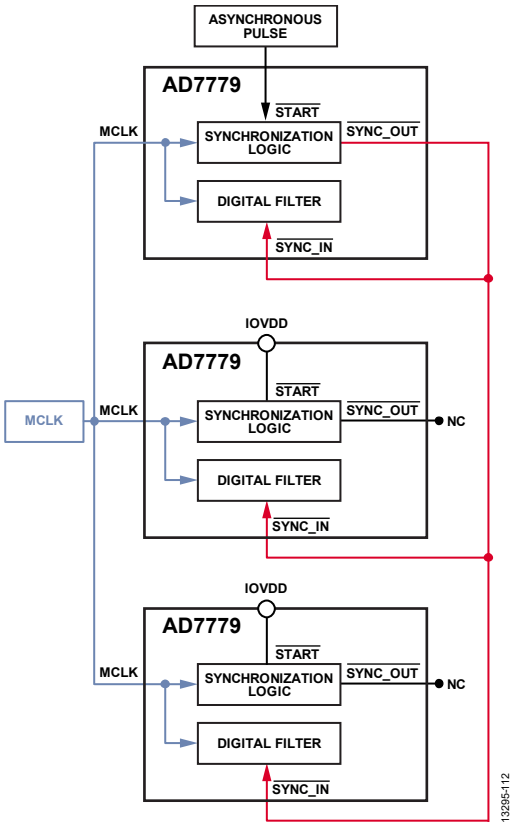

Figure 95. Multiple AD7779 Synchronization

DIGITAL FILTERING

The AD7779 offers a low latency sinc3 filter. Most precision Σ-Δ ADCs use sinc3 filters because the sinc3 filter offers a low latency path for applications requiring low bandwidth signals, for example, in control loops or where application specific post processing is required. The digital filter adds notches at multiples of the sampling frequency.

The digital filter implements three main notches, one at the maximum ODR (16 kHz or 8 kHz, depending on the power mode) and another two at the ODR frequency selected to stop noise aliasing into the pass band.

Figure 96 shows the typical filter transfer function for the high resolution and low power modes using a decimation rate of 256 samples.

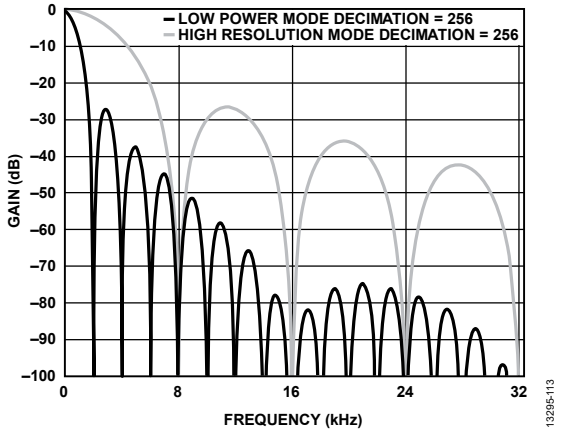

Figure 96. Sinc3 Frequency Response

The sample rate converter featured allows fine tuning of the decimation rate, even for noninteger multiples of the decimation rate. See the Sample Rate Converter (SRC) section for more information on filter profiles for noninteger decimation rates.

SHUTDOWN MODE

The AD7779 can be placed in shutdown mode by pulling AVDD2 to ground and connecting 1 MΩ resistance, pulled low, to XTAL2. In this mode, the average current consumption is reduced to 1 mA, as shown in Figure 97.

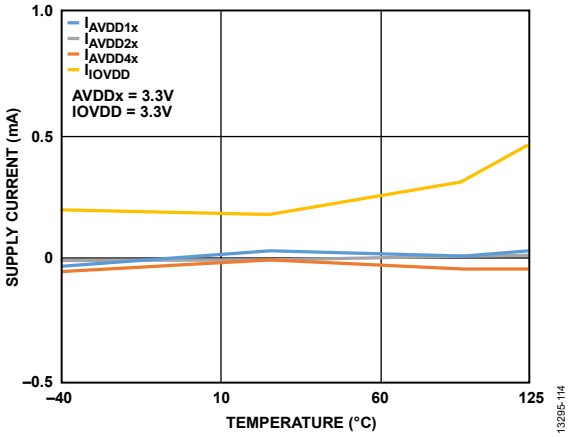

Figure 97. Shutdown Current

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CONTROLLING THE AD7779

The AD7779 can be controlled using either pin control mode or SPI control mode.

Pin control mode allows the AD7779 to be hardwired to predefined settings that offer a subset of the overall functionality of the AD7779. In this mode, the SRC and diagnostic features or extended errors source are not available.

Controlling the AD7779 over the SPI interface allows the user access to the full monitoring, diagnostic, and Σ-Δ control functionality. SPI control offers additional functionality such as offset, gain, and phase correction per channel, in addition to access to the flexible SRC to achieve a coherent sampling.

See Table 17 for more details about these different configurations.

PIN CONTROL MODE

In pin control mode, the AD7779 is configured at power-up based on the level of the mode pins, MODE 0, MODE1, MODE2, and MODE3. These four pins set the following functions on the AD7779: the mode of operation, the decimation rate/ODR, the PGA gain, and the reference source, as shown in Table 18.

Due to the limited number of mode pins and the number of options available, the PGA gain control is grouped into blocks of 4, and the ODR is selected for the maximum value defined by the decimation rate; ODR (kSPS) = 2048/decimation for high resolution mode, and ODR (kSPS) = 512/decimation for low power mode.

Depending on the mode selected, the device is configured to use an external or an internal reference.

The conversion data can be read back using the SPI interface or the data output interface, as shown in Table 17. If the data output interface is used to read back the data from the conversions, the number of DOUTx lines enabled and the number of clocks required for the Σ-Δ data transfer are determined by the logic level of the CONV_SAR, FORMAT0, and FORMAT1 pins. In this case, the DCLK2, DCLK1, and DCLK0 pins select the Σ-Δ output interface and control the DCLKx divide function, which is a submultiple of MCLK, as shown in Table 19. The DCLKx divide function sets the frequency of the data output interface DCLKx signal. The DCLK minimum frequency depends on the decimation rate and operation mode. See the Data Output Interface section for more details about the minimum DCLKx frequency.

All the pins that define the AD7779 configuration mode are reevaluated each time the $\overline{\text{SYNC_IN}}$ pin is pulsed. The typical connection diagram for pin control mode is shown in Figure 98.

Table 17. Format of the Data Interface

CONV_SAR State	FORMAT1	FORMAT0	Control Mode	Data Output Mode
1	0	0	Pin	SPI output
	0	1	Pin	SPI output
	1	0	Pin	SPI output
	1	1	SPI	Defined in Register 0x013 and/or Register 0x014
0	0	0	Pin	DOUT0, Channel 0 to Channel 1 DOUT1, Channel 2 to Channel 3 DOUT2, Channel 4 to Channel 5 DOUT3, Channel 5 to Channel 7
	0	1	Pin	DOUT0, Channel 0 to Channel 3 DOUT1, Channel 4 to Channel 7
	1	0	Pin	DOUT0, Channel 0 to Channel 7
	1	1	SPI	Defined in Register 0x013 and/or Register 0x014

Table 18. Pin Mode Options

Pin State						PGA Gain Channel		
MODE3	MODE2	MODE1	MODE0	Decimation Rate	Power Mode	0 to 3	4 to 7	Reference Type
0	0	0	0	1024	High resolution	1	1	External
0	0	0	1	512	High resolution	1	1	External
0	0	1	0	256	High resolution	1	1	External
0	0	1	1	128	High resolution	1	1	External
0	1	0	0	256	High resolution	1	2	External
0	1	0	1	512	High resolution	1	4	External
0	1	1	0	256	High resolution	1	4	External
0	1	1	1	128	High resolution	1	4	External

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Pin State						PGA Gain Channel		
MODE3	MODE2	MODE1	MODE0	Decimation Rate	Power Mode	0 to 3	4 to 7	Reference Type
1	0	0	0	512	High resolution	1	1	Internal
1	0	0	1	256	High resolution	1	1	Internal
1	0	1	0	128	High resolution	1	1	Internal
1	0	1	1	512	Low power	1	1	External
1	1	0	0	256	Low power	1	1	External
1	1	0	1	128	Low power	1	1	External
1	1	1	0	128	Low power	1	1	Internal
1	1	1	1	256	Low power	1	1	Internal

Table 19. DCLKx Selection for Pin Control Mode

State			
DCLK2/SCLK	DCLK1/SDI	DCLK0/SDO	MCLK Divider
0	0	0	1
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	16
1	0	1	32
1	1	0	64
1	1	1	128

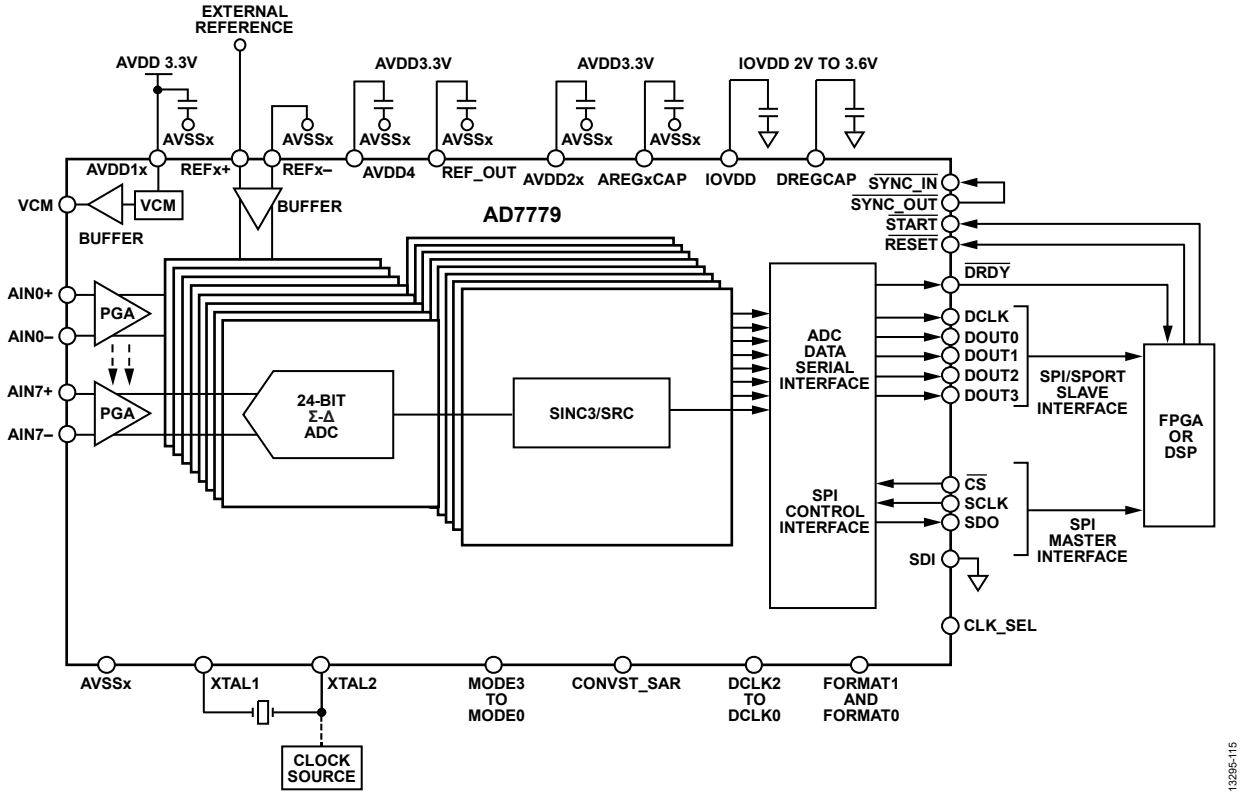

Figure 98. Pin Mode Connection Diagram with External Reference

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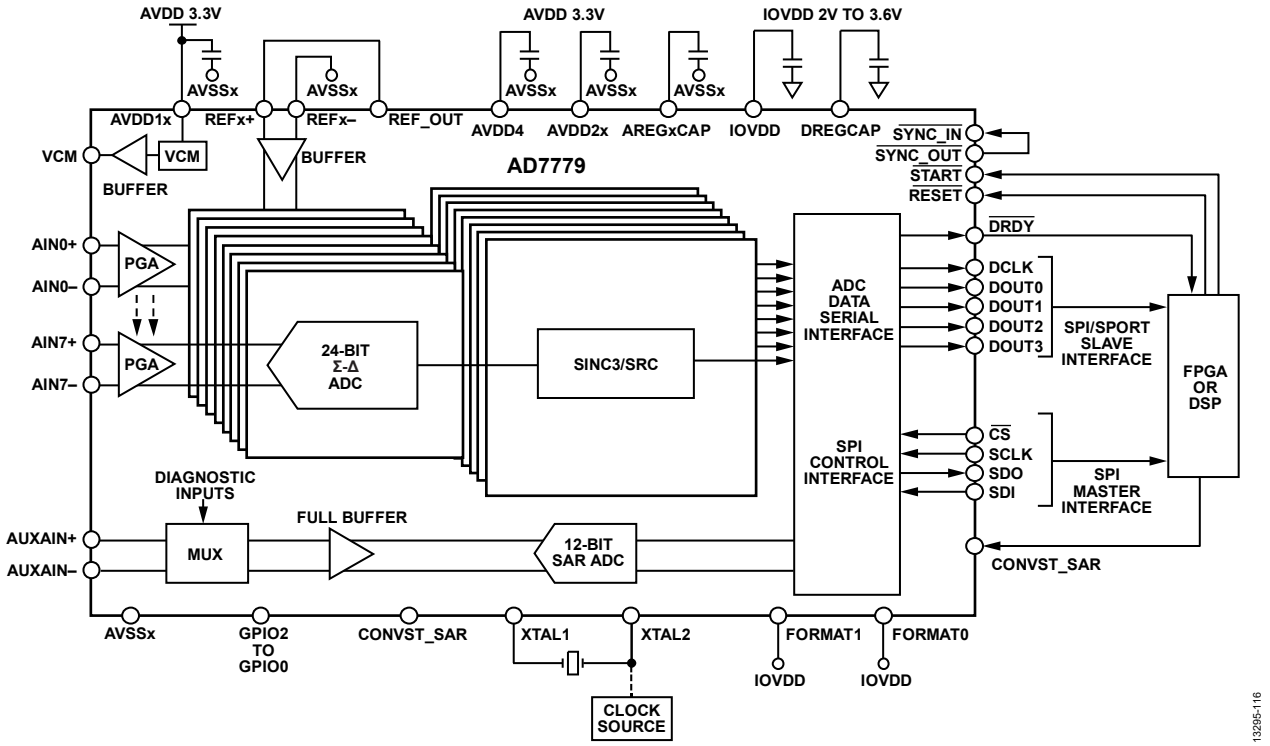

Figure 99. SPI Control Mode Connection Diagram with Internal Reference

SPI CONTROL

The second option for control and monitoring the AD7779 is via the SPI interface. This option allows access to the full functionality on the AD7779, including access to the SAR converter, phase synchronization, offset and gain adjustment, diagnostics and the SRC. To use the SPI control, set the FORMAT0 and FORMAT1 pins to logic high.

In this mode, the SPI interface can also be used to read the Σ-Δ conversation data by setting the SPI_SLAVEMODE_EN bit.

The typical connection diagram for SPI control mode is shown in Figure 99.

Functionality Available in SPI Mode

SPI control of the AD7779 offers the super set of the functions and diagnostics. The SPI Control Functionality section describes the functionality and diagnostics offered when in SPI control mode.

Offset and Gain Correction

Offset and gain registers are available for system calibration. The gain register is preprogrammed during final production for a PGA gain of 1, but can be overwritten with a new value if required.

The gain register is 24 bits long and is split across three registers, CHx_GAIN_UPPER_BYTE, CHx_GAIN_MID_BYTE, and CHx_GAIN_LOWER_BYTE, which set the gain on a per channel basis.

The gain value is relative to 0x555555, which represents a gain of 1.

The offset register is 24 bits long and is spread across three byte registers, CHx_OFFSET_UPPER_BYTE, CHx_OFFSET_MID_BYTE, and CHx_OFFSET_LOWER_BYTE. The default value is 0x000000 at power-up. Program the offset as a twos complement, signed 24-bit number. If the channel gain is set to its nominal value of 0x555555, an LSB of offset register adjustment changes the digital output by −4/3 LSBs.

As an example of calibration, the offset measured is −200 LSB (with both AINx± pins connected to the same potential).

An offset adjustment of −150 changes the digital output by −150 × (−4/3) = 200 LSBs (gain value = 0x555555), representing this number as two complement, 0xFFFFFF − 0x96 + 1 = 0xFFFF70.

- CHx_OFFSET_UPPER_BYTE = 0xFF
- CHx_OFFSET_MID_BYTE = 0xFF
- CHx_OFFSET_LOWER_BYTE = 0x70

Note that the offset compensation is performed before the gain compensation. The gain is programmed during final testing for PGA_{GAIN} = 1. The gain register values can be overwritten; however, after a reset or power cycle, the gain register values revert to the hard coded programmed factory setting.

If the gain required is 0.75 of the nominal value (0x555555), the value that must be programmed is

0x555555 × 0.75 = 0x400000

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Then, an LSB of the offset register adjustment changes the digital output by −4/3 × 0.75 = 1 LSB.

- CHx_GAIN_UPPER_BYTE = 0x40
- CHx_GAIN_MID_BYTE = 0x00
- CHx_GAIN_LOWER_BYTE = 0x00

SPI Control Functionality

Global Control Functions

The following list details the global control functions of the AD7779:

- High resolution and low power modes of operation
- Output data rate: sample rate converter (SRC)
- VCM buffer power-down
- Internal/external reference selection
- Enable, precharged, or bypassed reference buffer modes
- Internal reference power-down
- SAR diagnostic mux
- SAR power-down
- GPIO write/read
- SPI SAR conversion readback
- SPI slave mode—read Σ-Δ results
- SDO and DOUT drive strength
- DOUT mode
- DCLK division
- Internal LDO bypassed
- CRC protection: enabled or disabled

Per Channel Functions

The following list details the per channel functions of the AD7779:

- PGA gain.
- Σ-Δ channel power-down.
- Phase delay: synchronization phase offset per channel.
- Calibration of offset.
- Calibration of gain.
- Σ-Δ input signal mux.
- Channel error register.
- PGA gain.

Phase Adjustment

The AD7779 phase delay can be adjusted to compensate for phase mismatches between channels due to sensors or signal channel phase errors connected to the AD7779. Achieve phase adjustment by programming the CHx_SYNC_OFFSET register. This programming delays the synchronization signal by a certain number of modulator clocks, MOD_CLKs, to individually initiate the digital filter for each Σ-Δ ADC. In other words, program the channel with a higher phase to Phase 0 and delay the channel with a lower phase to compensate the phase mismatch.

The phase adjustment register is read after a pulse on the SYNC_IN pin. Any further changes on the register have no effect unless another pulse is generated. See the Digital Reset and Synchronization Pins section for more information on how to generate a pulse in the pin.

The phase offset register is multiplied internally by a factor (n), that depends on the decimation rate, as shown in Table 20.

Table 20. Phase Adjustment vs. Decimation Rate

Phase Adjustment Compensation (n)	Decimation Rate
×1	≤255
×2	≤511
×4	≤1023
×8	≤2047
×16	≤4095

The maximum phase delay cannot be equal to or greater than the decimation rate. If this is the case, the value changes internally to the decimation rate value minus 1.

When the CHx_SYNC_OFFSET register is written it automatically overwrites itself multiplied by the corresponding factor (n), as defined in Table 20. As CHx_SYNC_OFFSET is only 8 bits long, the resulting value will be scaled down to fit 8 bits. To know whether the phase adjustment has clipped or not, see Table 21.

Table 21.

CHx_SYNC_OFFSET × n	CHx_SYNC_OFFSET Overwrite
≤255	CHx_SYNC_OFFSET × n
≤511	CHx_SYNC_OFFSET × n/2
≤1023	CHx_SYNC_OFFSET × n/4
≤2047	CHx_SYNC_OFFSET × n/8
≤4095	CHx_SYNC_OFFSET × n/16

As an example, the phase mismatch between Channel 0 and Channel 1 is 5°, and the ODR is 5 kSPS in high resolution mode. In this case, the decimation rate is 2048 kHz/5 kHz = 409.6, which means that the offset register value is multiplied internally by 2.

Assuming an input signal of 50 Hz, the number of MOD_MCLK pulses required to sample a full period is 2048 kHz/50 Hz = 40960 > 360°/40960 = 0.00878°.

If a 5° delay is required, the number of MOD_MCLK delays must be 569 (5°/0.00878°) because the offset register is multiplied by 2; the final offset register value is 409.6/2 − 569/2, which gives a negative value. In this case, if the offset value programmed to the register is higher than 204 (for example, 210 × 2 = 420), the value is internally changed to 408, resulting in a phase compensation of 408 × 0.00878° = 3.58°.

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PGA Gain

The PGA gain can be selected individually by appropriately selecting Bits[7:6] in the CHx_CONFIG register, see Table 22.

Table 22. PGA Gain Settings via CHx_CONFIG

CHx_CONFIG, Bits[7:6] Setting	PGA Gain Setting
00	×1
01	×2
10	×4
11	×8

If the Σ-Δ reference is updated, it is recommended to apply a pulse on the $\overline{\text{SYNC_IN}}$ pin to remove invalid samples during the transition of the reference.

Decimation

The decimation defines the sampling frequency as follows:

- In high resolution mode, the sampling frequency = MCLK/(4 × decimation)
- In low power mode, the sampling frequency = MCLK/(8 × decimation)

Refer to the Sample Rate Converter (SRC) section for more information.

GPIO Pins

If the AD7779 operates in SPI control mode, the mode pins operate as GPIO pins, as shown in Figure 100. The GPIO pins can be configured as inputs or outputs in any order.

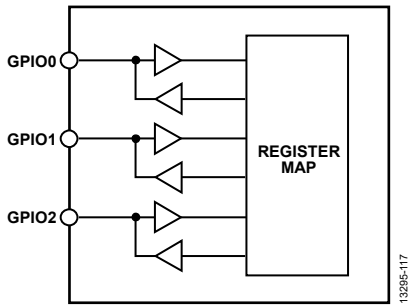

Figure 100. GPIO Pin Functionality

Configuration control and readback of the GPIO pins are dealt with by Bits[2:0] in the GPIO_CONFIG register (0 = input, 1 = output) and the GPIO_DATA register. Among other uses, the GPIOs can control an external mux connected to the auxiliary inputs of the SAR ADC. Use this mux to verify the results on the Σ-Δ ADCs.

In addition, the GPIO pins can be used to externally trigger a new decimation rate. Refer to the Sample Rate Converter (SRC) section for more information about this functionality.

Σ-Δ Reference Configuration

The AD7779 can operate with internal or external references. In addition, for diagnostic purposes, the analog supply can be used as a reference, as shown in Table 23.

Table 23. Σ-Δ References

Setting for ADC_MUX_CONFIG, Bits[7:6]	Channel 0 to Channel 3	Channel 4 to Channel 7
00	REF1+/REF1−	REF2+/REF2−
01	Internal reference	Internal reference
10	AVDD1A/AVSS1A	AVDD1B/AVSS1B
11	REF1−/REF1+	REF2−/REF2+

Reference buffer operation is described in Table 24. The selected reference and buffer operation mode affect all channels.

If the Σ-Δ reference is updated, it is recommended to apply a pulse on the $\overline{\text{SYNC_IN}}$ pin to remove invalid samples during the transition of the reference.

Table 24. Reference Buffer Operation Modes

Reference Buffer Operation Mode	REFx+	REFx−
Enabled	BUFFER_CONFIG_1, Bit 4 = 1; BUFFER_CONFIG_2, Bit 7 = 0	BUFFER_CONFIG_1, Bit 3 = 1; BUFFER_CONFIG_2, Bit 6 = 0
Precharged	BUFFER_CONFIG_1, Bit 4 = 1; BUFFER_CONFIG_2, Bit 7 = 1	BUFFER_CONFIG_1, Bit 3 = 1; BUFFER_CONFIG_2, Bit 6 = 1
Disabled	BUFFER_CONFIG_1, Bit 4 = 0	BUFFER_CONFIG_1, Bit 3 = 0

Table 25. Additional Disable Power-Down Blocks

Block	Register	Notes
VCM	GENERAL_USER_CONFIG_1, Bit 5	Enable by default
Reference Buffer	BUFFER_CONFIG_1, Bits[4:3]	Precharge mode by default
Internal Reference Buffer	GENERAL_USER_CONFIG_1, Bit 4	Disable by default
Σ-Δ Channel	CH_DISABLE, Bits[7:0]	All channels enable
SAR	GENERAL_USER_CONFIG_1, Bit 3	Disable by default
Internal Oscillator	GENERAL_USER_CONFIG_1, Bit 2	Enable by default

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Power Modes

The AD7779 offers different power modes to improve the power efficiency, high resolution and low power mode, which can be controlled via GENERAL_USER_CONFIG_1, Bit 6. To further reduce the power, additional blocks can be disabled independently, as described in Table 25.

If the power mode changes, a pulse on the $\overline{\text{SYNC_IN}}$ pin is required.

LDO Bypassing

The internal LDOs can be individually bypassed and an external supply can be applied directly to AREG1CAP, AREG2CAP, or DREGCAP pins. Table 26 shows the absolute minimum and maximum supplies for these pins, as well as the associated register used to bypass the regulator.

Table 26. LDO Bypassing

LDO	BUFFER_CONFIG_2, Bits[2:0][1]	Supply	
		Max (V)	Min (V)
AREG1CAP	1XX	1.9	1.85
AREG2CAP	X1X	1.9	1.85
DREGCAP	XX1	1.98	1.65

[1] X means don't care.

DIGITAL SPI INTERFACE

The SPI serial interface on the AD7779 consists of four signals: $\overline{\text{CS}}$, SDI, SCLK, and SDO. A typical connection diagram of the SPI interface is shown in Figure 101.

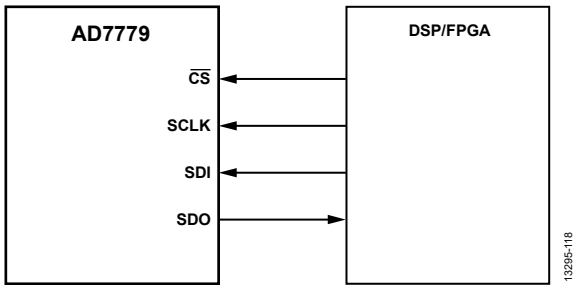

Figure 101. SPI Control Interface—AD7779 is the SPI Slave, Digital Signal Processor (DSP)/Field Programmable Gate Array (FPGA) is the Master

The SPI interfaces operates in Mode 0 and Mode 3, CPOL = 0, CPHA = 0 (Mode 0) or CPOL = 1, CPHA = 1 (Mode 3).

In pin control mode, the SDO can be used to read back the Σ-Δ results, depending on the level of the CONV_SAR pin, as described in Table 17.

In SPI control mode, the SPI interface transfers data into the on-chip registers while the SDO pin reads back data from the on-chip registers or reads the SAR or the Σ-Δ conversions results, depending on the selected operation mode.

The SDO data source in SPI control mode is defined by the GENERAL_USER_CONFIG_2 and GENERAL_USER_CONFIG_3 registers, as described in Table 27.

Table 27. SPI Operation Mode in SPI Control Mode

GENERAL_USER_CONFIG_2, Bit 5 Setting	GENERAL_USER_CONFIG_3, Bit 4 Setting	Mode
0	0	Internal register
0	1	Σ-Δ data conversion
1	X	SAR conversion

In SPI control mode, there are four different levels of I/O strength on the SDO pin, which can be selected in GENERAL_USER_CONFIG_2, Bits[4:3], as described in Table 28.

Table 28. SDO Strength

GENERAL_USER_CONFIG_2, Bits[4:3] Setting		Mode
0	0	Nominal
0	1	Strong
1	0	Weak
1	1	Extra strong

SCLK is the serial clock input for the device. All data transfers (on either SDO or SDI) occur with respect to this SCLK signal.

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The SPI interface can operate in multiples of eight bits. For example, in SPI control mode, if the SDO pin is used to read back the data from the internal register or the SAR ADC, the data frame is 16 bits wide (CRC disabled), as shown in Figure 102, or 24 bits wide (CRC enabled), as shown in Figure 103. In this case, the controller can generate one frame of 16 bits/24 bits (with and without the CRC enabled), or 2/3 frames of 8 bits (with and without the CRC enabled). When the SDO pin is used to read back the data from the Σ-Δ channels, 64 bits must be read back from the controller (in this case, the controller can generate a frame of 64 bits: either 2 × 32 bits, 4 × 16 bits, or 8 × 8 bits).

SPI CRC—Checksum Protection (SPI Control Mode)

The AD7779 has a checksum mode that improves SPI interface robustness in SPI control mode. Using the checksum ensures that only valid data is written to a register and allows data read from the device to be validated. The SPI CRC can be enabled by setting the SPI_CRC_TEST_EN bit. If an error occurs during a register write, the SPI_CRC_ERR is set in the error register.

Enabling the SPI_CRC_TEST_EN bit results in a CRC checksum being performed on all the R/$\overline{W}$ operations. When SPI_CRC_TEST_EN is enabled, an 8-bit CRC word is appended to every SPI transaction for SAR and register map operations. For more information on Σ-Δ readback operations, see the CRC Header section.

To ensure that the register write is successful, it is recommended to read back the register and verify the checksum.

For CRC checksum calculations, the following polynomial is always used: $x^8 + x^2 + x + 1$. See the SPI Control Mode Checksum section for more information.

SPI Read/Write Register Mode (SPI Control Mode)

The AD7779 has on-board registers to configure and control the device.

The registers have 7-bit addresses—the 7-bit register address on the SDI line selects the register for the read/write function. The 7-bit register address follows the R/$\overline{W}$ bit in the SDI data. The 8 bits on the SDI line following the 7-bit register address are the data to be written to the selected register if the SPI is a write transfer. Data on the SDI line is clocked into the AD7779 on the rising edge of SCLK, as shown in Figure 3.

The data on the SDO line during the SPI transfer contains the 8-bit 0010 0000 header: 8 bits of register data in the case of a read (R) operation, or 8 zeros in the case of a write ($\overline{W}$) operation.

With the CRC disabled, the basic data frame on the SDI line during the transfer is 16 bits long, as shown in Figure 102. When the CRC is enabled, a minimum frame length of 24 SCLKs is required on SPI transfers. The 24 bits of data on the SDO line consist of an 8-bit header (0010 0000), 8 bits of data, and an 8-bit CRC (see Figure 103).

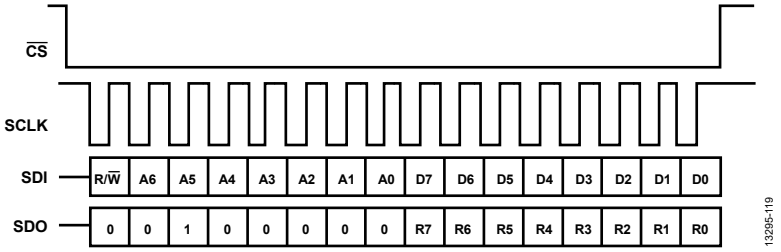

Figure 102. 16-Bit SPI Transfer—CRC Disabled

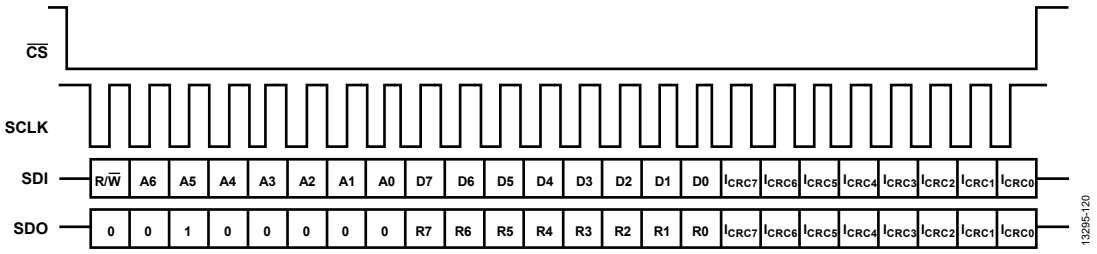

Figure 103. 24-Bit SPI Transfer—CRC Enabled

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SPI SAR Diagnostic Mode (SPI Control Mode)

Setting Bit 5 in the GENERAL_USER_CONFIG_2 register configures the SDO line to shift out data from the SAR ADC conversions, as described in Table 27. The SAR ADC is disabled at power-up. To enable this ADC, set the PDB_SAR bit.

In SAR mode, the AD7779 internal registers can be written to, but any readback command is ignored because the SDO data frame is dedicated to shift out the conversion results from the SAR ADC.

To exit this mode of operation, reset Bit 5 in the GENERAL_ USER_CONFIG_2 register.

The data on the SDO line during the SPI transfer contains a 4-bit 0010 header and 12 bits of the SAR conversion result if the CRC is disabled.

When the CRC is enabled, a minimum frame length of 24 SCLKs is required on SPI transfers. The 24 bits of data on the SDO line consist of a 4-bit header (0010), 12 bits of data, and an 8-bit CRC, as shown in Figure 104.

Per the SPI read/write register mode (see the SPI Read/Write Register Mode section), the SDI line contains the R/$\overline{W}$ bit, a 7-bit register address, 8 bits of data, and an 8-bit CRC (if enabled). To avoid unwanted writes to the internal register while the SAR conversions are read back through the SDO line, it is recommended to send a readback command, for example, 0x8000, to the device, which is ignored because the SDO pin is used to shift out the content of the SAR ADC.

If consecutives conversion are performed in the SAR ADC, read back the result from the previous conversion before a new conversion is generated. Otherwise, the results are corrupted.

Σ-Δ Data, ADC Mode

In pin control mode, the SPI interface can be used to read back the Σ-Δ conversions as described in Table 17. In SPI control mode, the SPI interface reads back the Σ-Δ conversions by setting GENERAL_USER_CONFIG_3, Bit 4, as described in Table 27; in this mode, the AD7779 internal register can be written to, but any readback command is ignored because the SDO data frame is dedicated to shifting out the conversion results from the Σ-Δ ADCs. To avoid unwanted writes to the internal register, it is recommended to send a readback command, for example, 0x8000, to the device, which is ignored because the SDO pin is used to shift out the content of the Σ-Δ ADC.

The SDO pin data can be read back in any multiple of 8 bits, for example, as 64 bits, 2 × 32 bits, 4 × 16 bits, or 8 × 8 bits.

SPI Software Reset

Keeping the SDI pin high during 64 consecutives clocks generates a software reset.

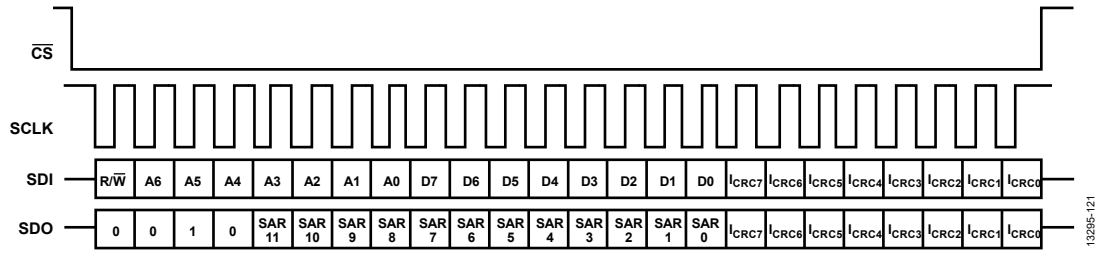

Figure 104. SAR ADC/Diagnostic Mode—CRC Enabled

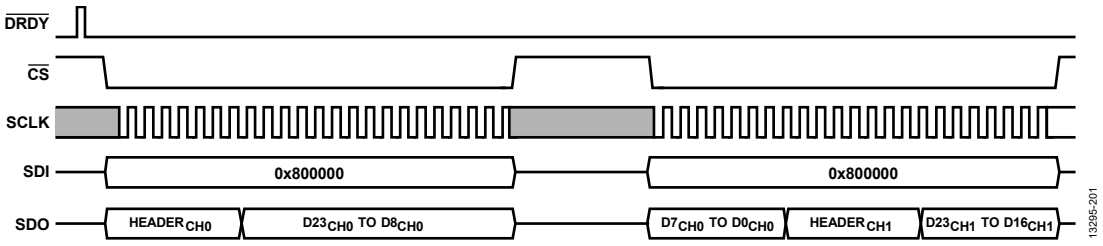

Figure 105. SPI Used to Read Back the Σ-Δ ADC Data, in 24-Bit Frames

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DIAGNOSTICS AND MONITORING

SELF DIAGNOSTICS ERROR

The AD7779 includes self diagnostic features to guarantee the correct operation. If an error is detected, the ALERT pin is pulled high to generate an external interruption to the controller. In addition, the header of the Σ-Δ output data contains a bit used to inform the controller of a chip error (see the ADC Conversion Output—Header and Data section).

Both the ALERT pin and the bit (status header) are automatically cleared if the error is no longer present. The errors related to the SPI interface do not recover automatically; read back the appropriate register to clear the error, resetting both the ALERT pin and the bit.

If an error detector is manually disabled, it does not generate an internal error and, consequently, the register map or the ALERT pin and bit are not triggered.

There are different sources of errors, as described in Table 29. In pin control mode, it is not possible to check the error source, and some sources of error are not enabled. In SPI control mode, check the source of an error by reading the appropriate register bit.

The STATUS_REG_x register bits identify the register that generates an error, as summarized in Table 29.

Table 29. Register Error Source

Bit Name	Register Source
ERR_LOC_GEN2	GEN_ERR_REG_2
ERR_LOC_GEN1	GEN_ERR_REG_1
ERR_LOC_CH7	CH7_ERR_REG
ERR_LOC_CH6	CH6_ERR_REG
ERR_LOC_CH5	CH5_ERR_REG
ERR_LOC_CH4	CH4_ERR_REG
ERR_LOC_CH3	CH3_ERR_REG
ERR_LOC_CH2	CH2_ERR_REG
ERR_LOC_CH1	CH1_ERR_REG
ERR_LOC_CH0	CH0_ERR_REG
ERR_LOC_SAT_CH6_7	CH6_7_SAT_ERR
ERR_LOC_SAT_CH4_5	CH4_5_SAT_ERR
ERR_LOC_SAT_CH2_3	CH2_3_SAT_ERR
ERR_LOC_SAT_CH0_1	CH0_1_SAT_ERR

In addition, STATUS_REG_x has a bit that indicates if any internal error bit is set. This bit clears if the error is no longer present and the register is read back.

The INIT_COMPLETE bit in the STATUS_REG_3 indicates that the device is initialized correctly. This bit is not an error but an indicator.

General Errors

MCLK Switch Error (SPI Control Mode)

After power-up, the AD7779 initiates a clocking handover sequence to pass clocking control to the external oscillator, or the CMOS clock. In SPI mode, if an error occurs in the handover, the EXT_MCLK_SWITCH_ERR bit is set in the general error register, GEN_ERR_REG_2.

If EXT_MCLK_SWITCH_ERR is set, this means that the device is operating off the internal oscillator.

To use a slow external clock (<265 kHz), set the CLK_QUAL_DIS bit. Setting this bit also clears the error bit.

If the external clock is between 132 kHz and 265 kHz, depending on the internal synchronization between internal oscillator and external clock, the error may not trigger. However, it is still recommended to set the CLK_QUAL_DIS bit.

If a slow clock is not in use and the error triggers, a reset is required.

Reset Detection

The AD7779 general error register contains a RESET_DETECTED bit. This bit is asserted if a reset pulse is applied to the AD7779 and is cleared by reading the general error register. This bit indicates that the power-on reset (POR) initialized correctly on the device. In addition, this pin can be used to detect an unexpected device reset or glitch on the $\overline{\text{RESET}}$ pin. To reset this error signal in SPI control mode, toggle the $\overline{\text{SYNC_IN}}$ pin or read from the general error register, GEN_ERR_REG_2. To reset this error signal in pin control mode, toggle the $\overline{\text{SYNC_IN}}$ pin.

Internal LDO Status

The AD7779 has three internal LDOs to regulate the internal analog and digital supply rails. The LDOs have internal power supply monitors. Internal comparators monitor and flag errors with these supplies after they pass a predetermined limit.

The ALDO1_PSM_ERR, ALDO2_PSM_ERR, and DLDO_PSM_ERR bits indicate either an LDO malfunction, or, if the LDOs are bypassed, an incorrect external supply.

The internal analog and digital voltage monitors can be disabled by appropriately selecting the LDO_PSM_TEST_EN bits.

Use the SAR ADC to verify the error.

Additionally, the levels of the internal monitors can be manually triggered to check if the detector works correctly by appropriately setting the bits in the LDO_PSM_TRIP_TEST_EN register. These bits increase the comparator window threshold above the LDO outputs, forcing the comparator to trigger.

ROM and MEMMAP CRC

If an error is found at power-up during the ROM verification, or if the internal memory map is corrupted, the AD7779 generates an error and sets MEMMAP_CRC_ERR or ROM_CRC_ERR, depending on the source of the error.

The checker can be disabled by clearing the MEMMAP_CRC_TEST_EN and ROM_CRC_TEST_EN bits.

The device must be reset if any of these errors trigger.

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Σ-Δ ADC Errors

Reference Detect (SPI Control Mode)

In SPI control mode, the AD7779 includes on-chip circuitry to detect if there is a valid reference for conversions or calibrations. If the voltage between the selected REFx+ and REFx– pins goes below 0.7 V, the AD7779 detects that it no longer has a valid reference. CHx_ERR_REF_DET can be interrogated to identify the affected channel, which clears the bit register if the error is no longer present. The voltage detector can be disabled by clearing the REF_DET_TEST_EN bit.

Use the Σ-Δ ADC diagnostic or the SAR ADC to verify the error.

Overvoltage and Undervoltage Events

The AD7779 includes on-chip overvoltage/undervoltage circuitry on each analog input pin. When the voltage on an analog input pin goes above AVDD1x + 40 mV, the CHx_ERR_AINx_OV bit is set. The error disappears if the input voltage falls below AVDD1x – 40 mV.

If an undervoltage event occurs (AVSSx – 40 mV), the CHx_ERR_AINx_UV bit is set. The error disappears if the input voltage increases to AVSSx + 40 mV.

The CHx_ERR_AINM_UV, CHx_ERR_AINM_OV, CHx_ERR_AINP_UV, and CHx_ERR_AINP_OV bits can be read back to verify the affected channel input, which clears the bit register if the error is no longer present. The overvoltage and undervoltage detection can be disabled independently by clearing the AINM_UV_TEST_EN, AINM_OV_TEST_EN, AINP_UV_TEST_EN, or AINP_OV_TEST_EN bits.

The input voltage can be checked independently with the SAR ADC.

Modulator Saturation

The AD7779 includes modulator saturation detection on each of the Σ-Δ ADCs. If 20 consecutive codes for the modulator are either all 1s or 0s, this is flagged as a modulator saturation event. Reading the CHx_ERR_MOD_SAT register clears the bit if the error corrects itself.

Modulator saturation detection can be disabled by clearing the MOD_SAT_TEST_EN bit.

The modulator input voltage is attenuated internally, which means that a modulator output of all 1s or 0s represents a modulator that is out of bounds and that a $\overline{\text{RESET}}$ pulse is required.

Filter Saturation

TheAD7779 includes digital filter saturation detection on each Σ-Δ ADC channel. This detection indicates that the filter output is out of bounds, which represents an output code approximately 20% higher than positive or negative full scale. Reading the CHx_ERR_FILTER_SAT bit clears the bit if the error corrects itself.

Clear the FILTER_SAT_TEST_EN bit to disable the detection.

Output Saturation

An output saturation event can occur when gain and offset calibration causes the output from the digital filter to clip at either positive or negative full scale. The output does not wrap. Reading the CHx_ERR_OUTPUT_SAT bit clears the bit if the error corrects itself.

The detection can be disabled by clearing OUTPUT_SAT_TEST_EN bit.

SPI Transmission Errors (SPI Control Mode)

All SPI errors clear after reading GEN_ERR_REG_1, which contains the SPI errors. These errors are not recovered automatically and, consequently, the ALERT pin and the ALERT bit remain set until the error register is read back, and new SPI frame is generated.

CRC Checksum Error

If the CRC checksum is enabled by setting the SPI_CRC_TEST_EN bit, an error bit, SPI_CRC_ERR, is raised if the CRC message does not match the message computed by the AD7779 internal CRC block. If the CRC message does not match the internally computed message, the register is not updated.

SCLK Counter

If the number of clocks generated by the controller is not a multiple of 8 after $\overline{\text{CS}}$ is pulled high, an error bit, SPI_CLK_COUNT_ERR is raised. The last command multiple of 8 is executed; however, the SCLK counter can be disabled by setting the SPI_CLK_COUNT_TEST_EN bit.

Invalid Read

When an invalid register is trying to read back, the SPI_INVALID_READ_ERR bit is set.

The invalid readback address detection can be disabled by setting the SPI_INVALID_READ_TEST_EN bit.

Invalid Write

When an invalid register is trying to write, the SPI_INVALID_WRITE_ERR bit is set.

The invalid write address detection can be disabled by setting the SPI_INVALID_WRITE_TEST_EN bit.

MONITORING USING THE AD7779 SAR ADC (SPI CONTROL MODE)

The AD7779 contains an on-chip SAR ADC for chip diagnostics, system diagnostics, or measurement verification. The SAR ADC has a 12-bit resolution. The AVDD4 and AVSS4 pins operate in complete independence of the Σ-Δ ADC supplies and, therefore, can be used for chip diagnostics in systems where functional safety is important. The reference for the SAR conversion process is taken from the SAR ADC supply voltage (AVDD4/AVSS4) and, therefore, the SAR analog input range is from AVSS4 to AVDD4.

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The SAR ADC has a maximum throughput rate of 256 kSPS. The CONVST_SAR pin initiates a conversion on the SAR ADC. The maximum allowable frequency of the CONVST_SAR pin is 256 kHz. If consecutives conversion are performed in the SAR ADC, read back the result from the previous conversion before a new conversion is generated. Otherwise, the results are corrupted.

The SAR ADC is only available in SPI control mode. To read conversion results from the SAR ADC, set the SAR_DIAG_MODE_EN bit. After this bit is set, all data shift out from the SDO pin are from the SAR ADC register, as shown in Figure 106.

The CONVST_SAR signal can be internally deglitched to avoid false triggers.

Table 30. SAR Synchronization and Deglitching

CONVST_DEGLITCH_DIS	Effect on CONVST_SAR
11	CONVST_SAR goes directly to the SAR
10	CONVST_SAR reaches the SAR when it is 1.5 MCLK cycles wide

Increase the acquisition time by 1.5/MCLK when the deglitch circuitry is enabled.

Prior to the SAR ADC, the AD7779 contains an internal multiplexer. This multiplexer can be configured over the SPI interface to set the inputs to the SAR ADC to be either internal circuit nodes in the case of diagnostics or to select the external AUXAIN+ and AUXAIN− pins.

Along with converting external voltages, the SAR ADC can be used to monitor the internal nodes on the AVDD, IOVDD, and DGND pins, and can monitor the DLDO and ALDO outputs. Some voltages are internally attenuated by 6, and the resulting voltage is applied to the SAR ADC, as shown in Table 31. This is useful because variations in the power supply voltage can be monitored.

The input multiplexer of the SAR is controlled by the GLOBAL_MUX_CONFIG register, and the different inputs available are described in Table 31.

The SAR ADC also contains an ADC driver amplifier, as shown in Figure 107. This amplifier settles the SAR input to 12-bit accuracy within the t_{33} time. This driver amplifier helps minimize the kickback from the SAR converter to the global diagnostic mux input circuit nodes.

Use the auxiliary inputs, AUXAIN+ and AUXAIN−, to validate the Σ-Δ measurements. While operating in SPI control mode, the AD7779 has three available GPIO ports controlled via the SPI interface. The GPIO pins can be used to control an external, dual 8:1 multiplexer, which in turn is used to sample the eight Σ-Δ channels. Use this diagnostic in applications where functional safety is required. This diagnostic aids in removing the need for a secondary external ADC to validate primary measurements on the Σ-Δ channels.

Temperature Sensor

The internal die temperature can be measured with an error of ±2°C. DV_{BE} is proportional to the temperature measured referred to 25°C.

$$DV_{BE} = \frac{AVDD4 - AVSS4}{2^{n-1}}\left(ADC_{CODE} - 2^{n-1}\right)$$

$$Temperature\ (°C) = 25 + \frac{DV_{BE} - 0.6}{0.002}$$

Table 31. SAR Mux Inputs

	Signal		
SAR Input	Positive	Negative	Attenuation ÷ 6
0	AUXAIN+	AUXAIN−	No
1	DV_{BE}	AVSSx	No
2	REF1+	REF1−	No
3	REF2+	REF2−	No
4	REF_OUT	AVSSx	No
5	VCM	AVSSx	No
6	AREG1CAP	AVSSx	Yes
7	AREG2CAP	AVSSx	Yes
8	DREGCAP	DGND	Yes
9	AVDD1A	AVSSx	Yes
10	AVDD1B	AVSSx	Yes
11	AVDD2A	AVSSx	Yes
12	AVDD2B	AVSSx	Yes
13	IOVDD	DGND	Yes
14	AVDD4	AVSSx	No
15	DGND	AVSSx	Yes
16	DGND	AVSSx	Yes
17	DGND	AVSSx	Yes
18	AVDD4	AVSSx	Yes
19	REF1+	AVSSx	No
20	REF2+	AVSSx	No
21	AVSSx	AVDD4	Yes

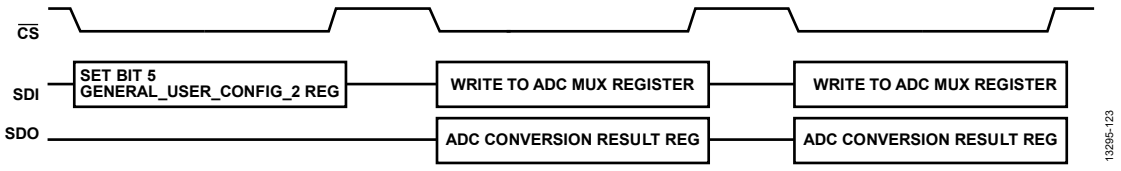

Figure 106. Configuring the AD7779 to Operate the SPI to Read from the SAR ADC

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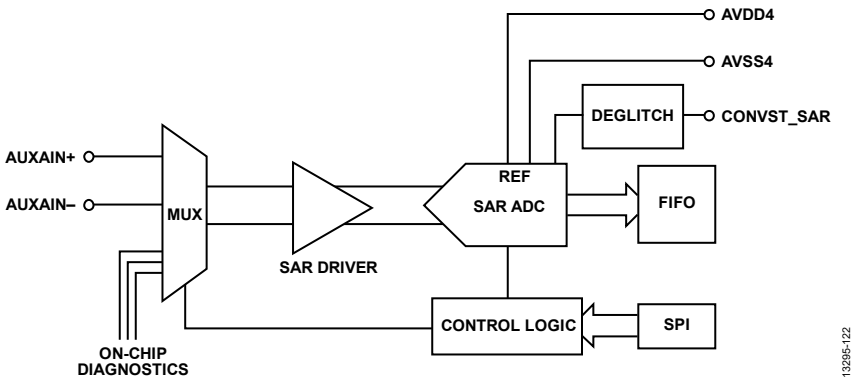

Figure 107. SAR ADC Configuration and Control

Table 32. Σ-Δ Diagnostic

Input	Voltage	Recommended Voltage Reference	Notes/Result
0	Floating	Not applicable	Not applicable
1	Floating	Not applicable	Not applicable
2	280 mV differential signal	Internal/External	PGA gain calibration
3	External reference, positive/negative	External	Positive full scale
4	External reference, negative/positive	External	Negative full scale
5	External reference, negative/ negative	External	Zero scale
6	Internal reference, positive/negative	Internal	Positive Full scale
7	Internal reference, negative/positive	Internal	Negative full scale
8	Internal reference, positive/ positive	Internal	Zero scale
9	External reference, positive/ positive	External	Zero scale

Σ-Δ ADC DIAGNOSTICS (SPI CONTROL MODE)

The AD7779 Σ-Δ ADC diagnostic functions are accessible through the SPI interface. The internal mux placed before the PGA has different inputs, allowing the user to select a zero-scale, positive full-scale, or negative full-scale input to the Σ-Δ ADC, which can be converted to verify the correct operation of the Σ-Δ ADC channel.

The diagnostic mux control signals are shared across all the Σ-Δ channels. Depending on the diagnostic selected, connect the Σ-Δ ADC reference to a different reference source to guarantee that the conversion is within the measurable range.

There are two different ways to enable the diagnostic mux:

- Setting the CHx_RX bit. This bit enables the input Σ-Δ mux. The multiplexer inputs are described in Table 32. The reference used during the conversions are controlled by the REF_MUX_CTRL bits.
- Setting CHx_REF_MONITOR. This bit has the same effect as enabling the CHx_RX bit and selects the VDD1x/AVSSx supplies as the main reference.

If the AINx± pin is connected to AVSSx, the input range is outside range (AVSSx + 100 mV); therefore, results may differ slightly from the expected value.

The inputs can be used alternatively to calibrate gain and offset errors.

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Σ-Δ OUTPUT DATA

ADC CONVERSION OUTPUT—HEADER AND DATA

The AD7779 Σ-Δ conversion results are output on the DOUT0 to DOUT3 pins or over the SPI, depending on the selected interface. If the DOUTx interface is selected, the AD7779 acts as the master in the transmission. If the SPI interface is selected, the controller is the master.

The $\overline{\text{DRDY}}$ signal indicates the end of conversion independently of the interface selected to read back the Σ-Δ conversion. When the SPI is used to read back the Σ-Δ conversion, if a new conversion is completed ($\overline{\text{DRDY}}$ falling edge) before the previous conversion is read back, the results from previous conversion are overwritten and, consequently, the previous conversion data is corrupted.

For each channel, the width is 32 bits long: 8 bits for the header and 24 bits for the Σ-Δ conversion, as shown in Figure 108.

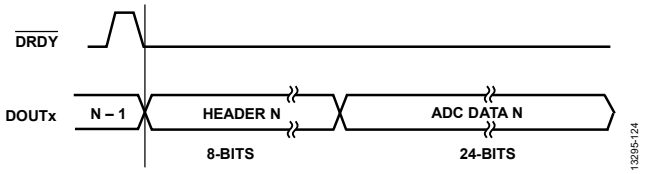

Figure 108. ADC Output—8-Bit Header + 24-Bit Conversion Data

In pin control mode, the header is fixed to the CRC while in SPI mode, and can be selected between CRC or error headers.

CRC Header

The CRC header is the header generated in pin control mode or in SPI mode if DOUT_HEADER_FORMAT is set.

As shown in Figure 109, the header consists of an alert bit, three bits for the ADC channel, as shown in Table 33, and four bits for the CRC.

The alert bit is set high if an error is detected in any channel, as explained in the General Errors section. The alert bit remains 1 until the error disappears.

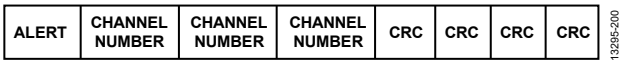

Figure 109. CRC Header

Table 33. Channel ID

Channel	Channel ID 2	Channel ID 1	Channel ID 0
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

The CRC generated is eight bits long; the CRC 4 MSBs are placed on the header for the first channel in the pairing and the 4 LSBs on the header of the second channel in the pairing, as shown in Table 34. If a channel is disabled, the 24-bit output data for this channel is 0x000000.

Table 34. 8-Bit CRC, Header Configuration (Channel 2)

Channel 2 Header							
Alert	0	1	0	CRC7	CRC6	CRC5	CRC4

Table 35. 8-Bit CRC, Header Configuration (Channel 3)

Channel 3 Header							
Alert	0	1	1	CRC3	CRC2	CRC1	CRC0

ERROR Header (SPI Control Mode)

In SPI control mode, the default header can be replaced by an error header. If the Σ-Δ conversion is read back through the SPI interface, disable the CRC by clearing the SPI_CRC_TEST_EN bit. If the DOUTx interface is used, clear the DOUT_HEADER_FORMAT bit.

The error header provides information of common error sources specific for each channel, as shown in Table 36. Modulator and filter errors are indicated even if the checker for this error has been specifically disabled, as described in the Σ-Δ ADC Errors section.

Table 36. Status Header Output

Bits	Name	Description
7	Alert	This bit is set high if any of the enabled diagnostic functions have detected an error, including an external clock not detected, a memory map bit flip, or an internal CRC error. This bit is not channel specific. The bit clears if the error is no longer present.
[6:4]	CH_ID_[2:0]	These bits indicate which ADC channel the following conversion data came from (see Table 33).
3	RESET_DETECTED	This bit indicates if a reset condition occurs. This bit is not channel specific.
2	MODULATOR_SATURATE	This bit indicates that the modulator output 20 consecutive 0s or 1s. The bit resets automatically after the error is no longer present.
1	FILTER_SATURATE	This bit indicates that the filter output is out of bounds. The bit resets automatically after the error is no longer present.
0	AIN_OV_UVERROR	This bit indicates that there is an AINx± overvoltage/undervoltage condition on the inputs. This bit is set until the appropriate register is read back and the error is no longer present.

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SAMPLE RATE CONVERTER (SRC) (SPI CONTROL MODE)

The AD7779 implements a patented featured called the SRC on each Σ-Δ channel, which allows the user to configure the output data rate or sampling frequency to any desired value, including noninteger values. The SRC achieves fine resolution control over the decimation ratio, up to 15.26×10^{-6}. In applications where the ODR must change based on changes in the input signal to maintain sampling coherency, the SRC provides fine control over the ODR. For example, to achieve the highest classification standard, Class A, in power quality applications, coherency must be maintained for 0.01 Hz changes in the input power line. The SRC can be used to achieve this sampling frequency accuracy.

In the pin control mode, the ODR is fixed per the predefined pin control options. Consequently, a noninteger number cannot be selected, as shown in Table 17.

To set the ODR, the user must program up to four registers, depending on the decimation value: two registers to program the integer value, N (the effective decimation rate), and two registers to program the decimal value, IF (the interpolation factor).

The integer value registers are SRC_N_MSB, Bits[3:0] and SRC_N_LSB, Bits[7:0]. The decimal part value registers are SRC_IF_MSB, Bits[7:0] and SRC_IF_LSB, Bits[7:0].

As an example, if an output data rate of 2.8 kSPS is required, the decimation rate is as follows:

- In HR mode = (8192/4)/2.8 = 731.428
- In LP mode = (4096/8)/2.8 = 182.857

The register values for HR mode are as follows:

- 731d = 0x2DB
- SRC_N_MSB[3:0] = 0x02
- SRC_N_LSB[7:0] = 0xDB
- 0.428d = 0.428 × 2^{16} = 28049d = 0x6D91
- SRC_IF_MSB[7:0] = 0x6D
- SRC_IF_LSB[7:0] = 0x91

The ODR can be updated on the fly, but a new ODR is effective in three conversion cycles of the Σ-Δ ADCs. This guarantees a smooth transition with no conversion results out of range.

There are two different ways to change the ODR after a new value is written in the SRC registers: via software or via hardware, depending on SRC_UPDATE, Bit 7.

If the SRC_LOAD_SOURCE bit is clear, the new ODR value is updated by setting the SRC_LOAD_UPDATE bit to 1. This bit must be held high for at least two MLCK periods; return the bit to 0 before attempting another update.

If SRC_LOAD_SOURCE is set, the ODR update is controlled externally by the GPIO0 pin. Apply a pulse in the GPIO2 pin, which is then internally synchronized with the external MCLK, and the resultant synchronous signal is output on the GPIO1 pin.

The GPIO1 and GPIO0 pins must be externally connected.

If multiple AD7779 must be synchronized, the GPIO1 pin of one device can be connected to multiple devices. This synchronization method requires the use of a common MCLK signal for all the AD7779 devices connected, as shown in Figure 110.

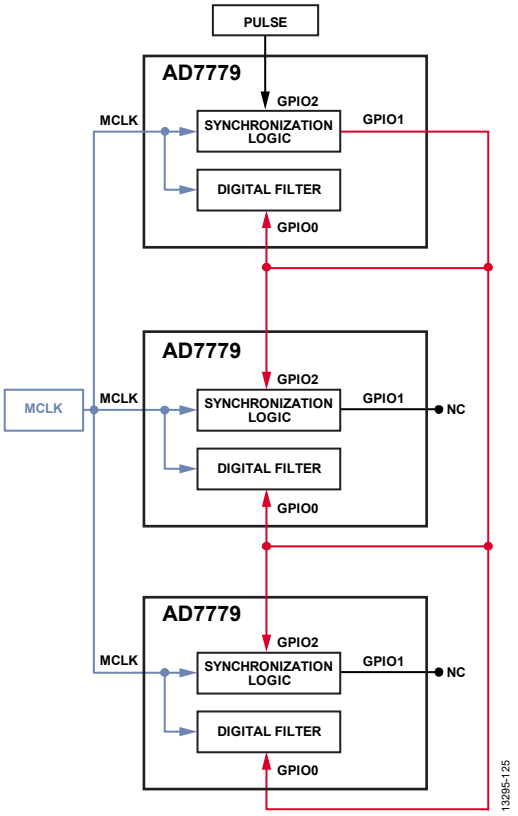

Figure 110. Hardware ODR

SRC Bandwidth

The SINC filter architecture allows the user to select a noninteger value as the decimation range. This versatility means that the filter notches must be adjusted dynamically: two notches at the variable frequency, and one fixed notch to remove the PGA chopping tone. Consequently, the traditional formula for the −0.1 dB and −3 dB bandwidth must be adjusted depending on the selected decimation rate.

The bandwidth transfer function is not linear but can be approximated by using a linear function.

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Figure 111 and Figure 112 show the correction factor for the −0.1 dB and −3 dB bandwidth, respectively in high resolution and low power modes. For example, when the ODR = 1000 in HR mode, the −0.1 dB point is BW = 0.0474 × 1000 + 31.667 = 79.067 Hz.

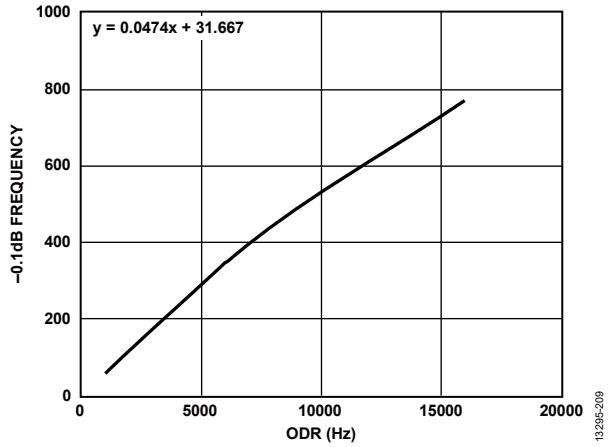

Figure 111. −0.1 dB Correction Factor, HR Mode

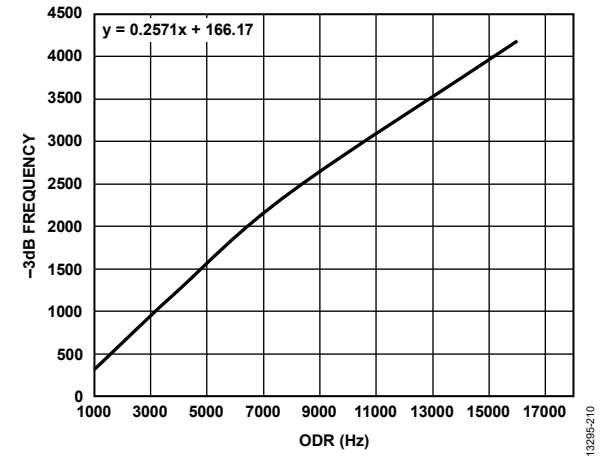

Figure 112. −3 dB Correction Factor, HR Mode

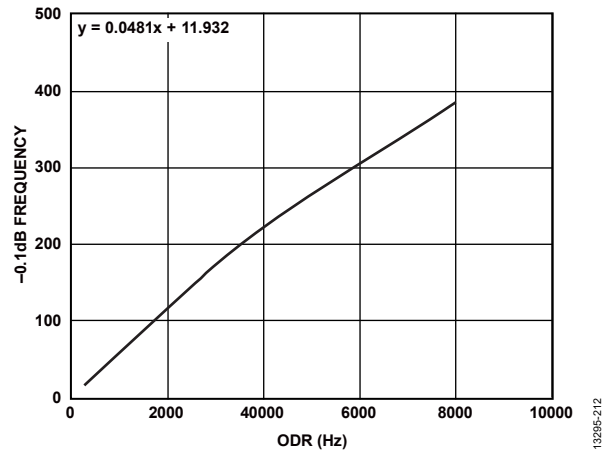

Figure 113. −0.1 dB Correction Factor, LP Mode

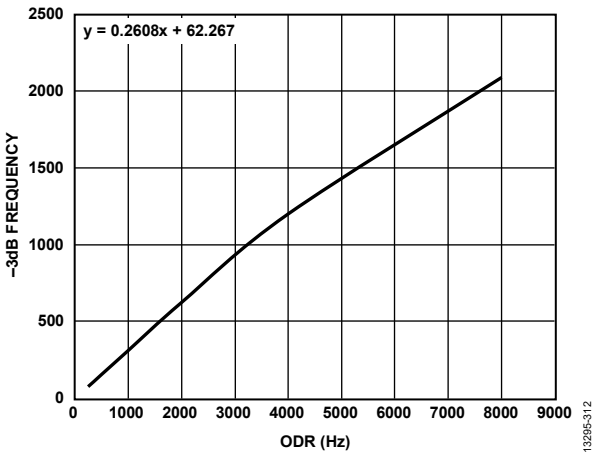

Figure 114. −3 dB Correction Factor, LP Mode

SRC Group Delay and Latency

The SRC group delay depends on the selected ODR and the power mode, and is defined by the following equation:

$$Group\ Delay = \frac{PM + SRC_N}{SRC_N \times ODR}$$

where:
PM is a value that depends on the power mode, either 64 for high resolution mode or 32 for low power mode.
SRC_N is the integer value of the programmed ODR.
ODR is the programmed output data rate.

The latency is the contribution of the group delay and the calibration time.

$$Latency = Group\ Delay + t_{CAL}$$

where t_{CAL} = 62 × t_{MCLK}, with a maximum error of 2 × t_{MCLK}, in high resolution mode; or 121 × t_{MCLK}, with a maximum error of 4 × t_{MCLK}, in low power mode.

t_{MCLK} is the modulator period, MCLK/4 in high resolution mode and MCLK/8 in low power mode.

Settling Time

The settling time is defined by the contribution of all the internal stages, the filter delay, and the block calibration.

The filter delay is defined as 3/ODR. In some extreme cases, as when an external pulse is applied, this value may increase to 4/ODR.

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DATA OUTPUT INTERFACE

The Σ-Δ output data interface is defined by the CONV_SAR, FORMAT0, and FORMAT1 pins in pin control mode at power-up. The FORMATx pins cannot be changed dynamically. Table 18 shows the available options for pin control mode. If the device is configured in SPI control mode, the SPI_SLAVE_MODE_EN bit enables the SPI interface to transmit the Σ-Δ ADC conversion results, as shown in Table 27.

DOUT3 to DOUT0 Data Interface

Standalone Mode

In standalone mode, the AD7779 interface acts as a master. There are three different DOUT configurations, configurable through the FORMATx pins in pin control mode, as shown in Figure 115 through Figure 117, or via the DOUT_FORMAT bits, Bits[7:6], in SPI control mode, as described in Table 37.

Figure 118, Figure 119, and Figure 120 show the expected data outputs for different DOUTx output modes.

Table 37. DOUTx Channels

DOUT_FORMAT Bits/FORMATx Pins	Number of DOUTx Lines Enabled	Associated Channels
00	4	DOUT0—Channel 0 and Channel 1 DOUT1—Channel 2 and Channel 3 DOUT2—Channel 4 and Channel 5 DOUT3—Channel 6 and Channel 7
01	2	DOUT0—Channel 0, Channel 1, Channel 2, and Channel 3 DOUT1—Channel 4, Channel 5, Channel 6, and Channel 7
10	1	DOUT0—Channel 0, Channel 1, Channel 2, Channel 3, Channel 4, Channel 5, Channel 6, and Channel 7

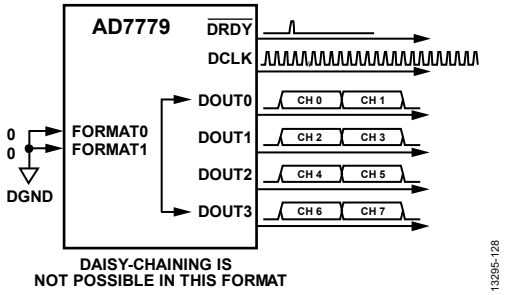

Figure 115. FORMATx Pin Configuration—FORMAT0 = 0, FORMAT1 = 0

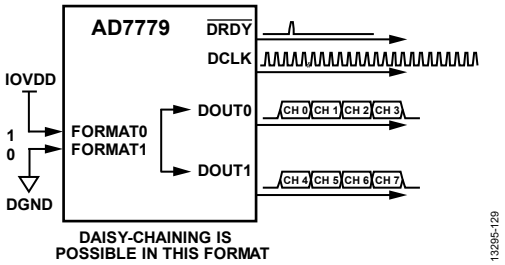

Figure 116. FORMATx Pin Configuration—FORMAT0 = 1, FORMAT1 = 0

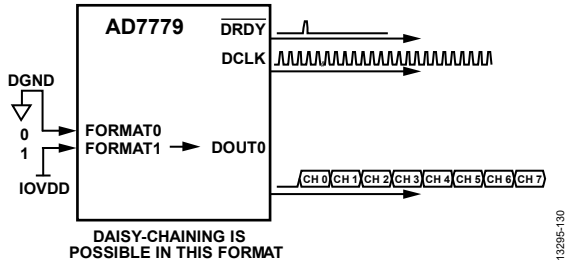

Figure 117. FORMATx Pin Configuration—FORMAT0 = 0, FORMAT1 = 1

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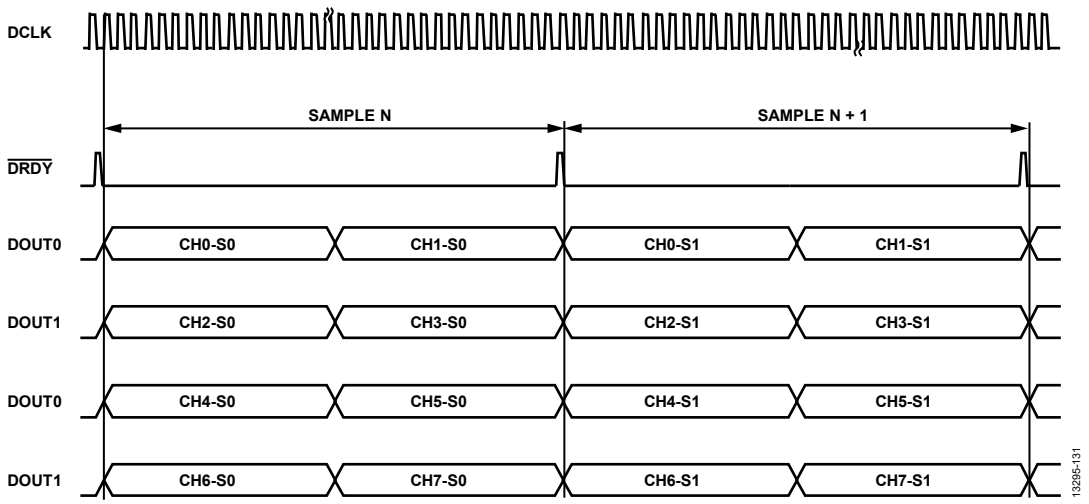

Figure 118. FORMAT0 = 0, FORMAT1 = 0—Each DOUTx Outputs Two ADC Conversions (S0 Means Sample 0 and S1 Means Sample 1)

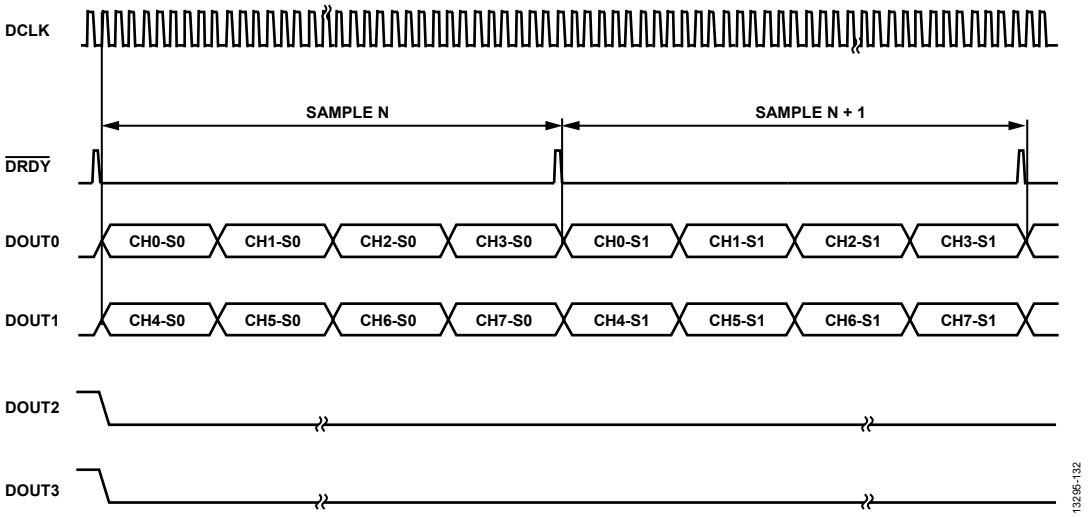

Figure 119. FORMAT0 = 0, FORMAT1 = 1—Channel 0 to Channel 3 Share DOUT0, and Channel 4 to Channel 7 Share DOUT1 (S0 Means Sample 0 and S1 Means Sample 1)

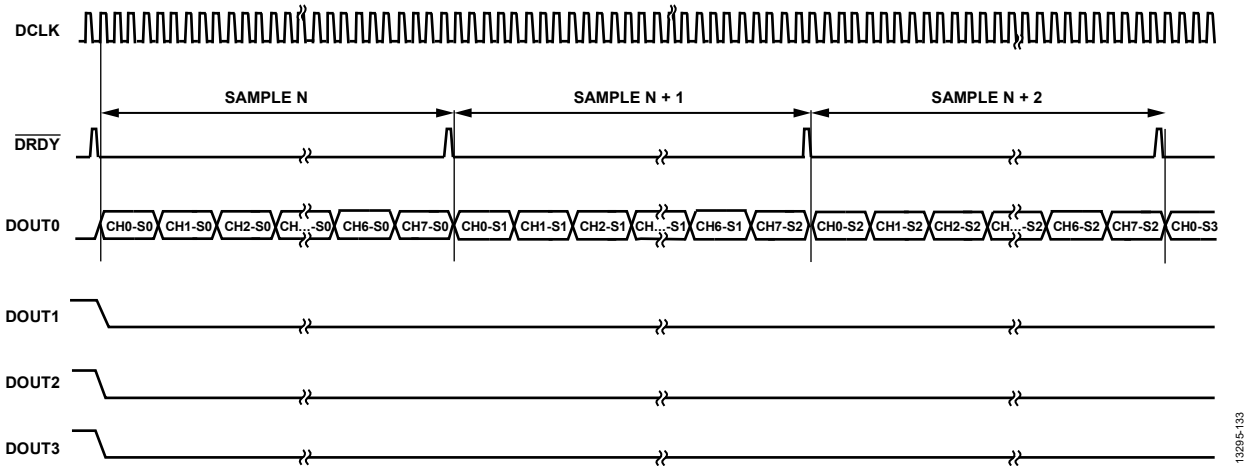

Figure 120. FORMAT0 = 1, FORMAT1 = 0—Channel 0 to Channel 7 Output on DOUT0 Only (S0 Means Sample 0 and S1 Means Sample 1)

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Daisy-Chain Mode

Daisy-chaining devices allows numerous devices to use the same data interface lines by cascading the outputs of multiple ADCs from separate AD7779 devices. In daisy-chain configuration, only one device has direct connection between the DOUTx interface and the digital host. For the AD7779, daisy-chain capability is implemented by cascading DOUT0 and DOUT1 through a number of devices, or by just using DOUT0 (this depends on the selected DOUTx mode). The ability to daisy chain devices and the limit on the number of devices that can be handled by the chain is dependent on the selected DOUTx mode and the decimation rate employed.

When operating in daisy-chain mode, it is required that all AD7779 devices in the chain are correctly synchronized. See the Digital Reset and Synchronization Pins section for more information.

This feature is especially useful for reducing the component count and wiring connections in, for example, isolated multiconverter applications or for systems with a limited interfacing capacity.

For daisy-chain operation, there are two different configurations possible, as described in Table 38.

Using the DOUTx = 10 mode DOUT2 acts as input pins, as shown in Figure 121. In this case, the DOUT0 pin of the AD7779 devices is cascaded to the DOUT2 pin of the next device in the chain. Data readback is analogous to clocking a shift register where data is clocked on the rising edge of DCLK.

Table 38. DOUTx Modes in Daisy-Chain Operation

DOUT_FORMAT Bits/ FORMATx Pins	Number of DOUTx Lines Enabled	Associated Channels
01	2	DOUT0—Channel 0 to Channel 3 and DOUT2 DOUT1—Channel 4 to Channel 7 and DOUT3 DOUT2—input channel DOUT3—input channel
10	1	DOUT0—Channel 0 to Channel 7 and DOUT2 DOUT2—input Channel

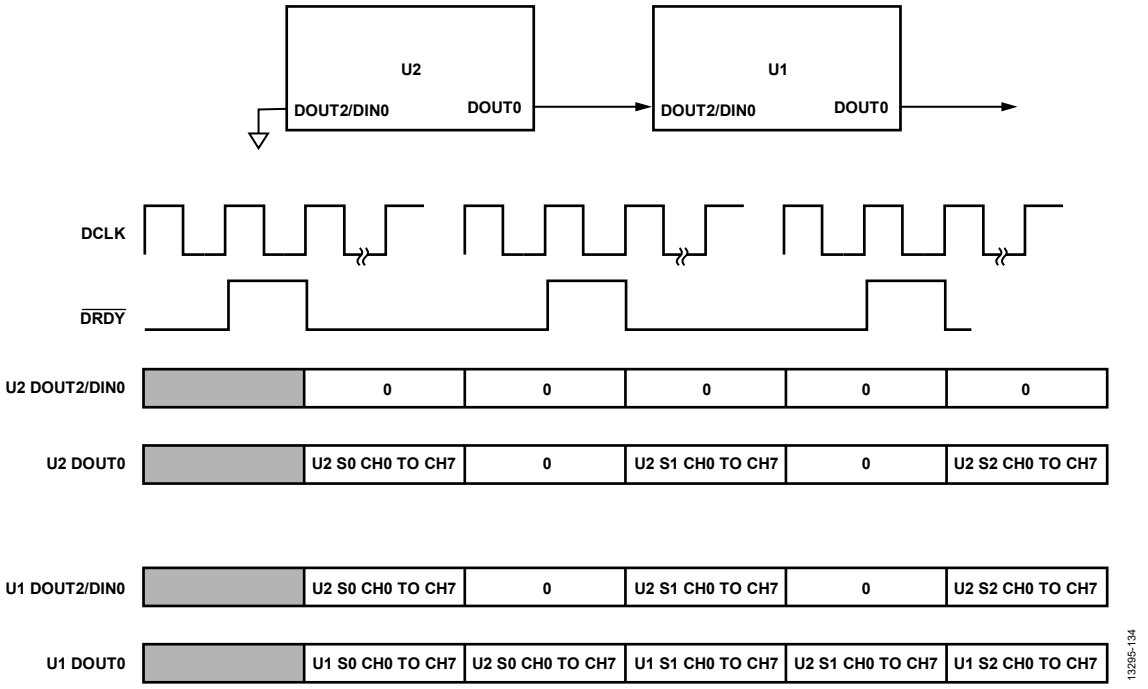

Figure 121. Daisy-Chain Connection Mode, FORMAT0 = 1, FORMAT1 = 0 (S0 Means Sample 0 and S1 Means Sample 1); When Connected in Daisy-Chain Mode, DOUT2 Acts as an Input Pin, Represented by DIN0

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Minimum DCLKx Frequency

Select the DCLKx frequency ratio in such a way that the data is completely shifted out before a new conversion is completed, otherwise the previous conversion is overwritten and the transmission becomes corrupt. The minimum DCLKx frequency ratio is defined by the decimation rate, the operation mode, and the lines enabled on the DOUT3 to DOUT0 data interface as described in the following equations:

In standalone mode,

$$High\ Resolution\ Mode - DCLK_{MIN_RATIO} < Decimation/(8 \times CHANNELS_PER_DOUT)$$

$$Low\ Power\ Mode - DCLK_{MIN_RATIO} < Decimation/(4 \times CHANNELS_PER_DOUT)$$

In daisy-chain mode,

$$High\ Resolution\ Mode - DCLK_{MIN_RATIO} < Decimation/(8 \times Devices \times DOUTx\ Channels)$$

$$Low\ Power\ Mode - DCLK_{MIN_RATIO} < Decimation/(4 \times Devices \times DOUTx\ Channels)$$

As an example, when operating in master interface mode, DOUTx = 01, the DOUT0 and DOUT1 pins shift out four Σ-Δ channels each and, assuming a maximum output rate in high resolution mode, the decimation = 128.

$$DCLK_{MIN} < 128/(8 \times 4) = 4$$

If the $DCLK_{MIN_RATIO}$ is selected above the necessary minimum, a Logic 0 is continuously transmitted until a new sample is available.

An example in daisy-chain mode, assuming DOUTx = 01, and with three devices connected and a decimation rate of 256 in high resolution mode, is as follows:

$$DCLK_{MIN_RATIO} < 256/(8 \times 3 \times 4) = 2.66 = 2$$

The different ratios are summarized in Table 39.

Table 39. Available DCLK Ratios

DCLK_CLK_DIV (SPI Control Mode), DCLKx (Pin Control Mode)	DCLKx Ratio
000	1
001	2
010	4
011	8
100	16
101	32
110	64
111	128

There are maximum achievable ODRs and minimum DCLKx frequencies required for a given DOUTx pin configuration, as shown in Table 40 and Table 41.

Table 40. Maximum ODRs and Minimum DCLKx Frequencies in High Resolution Mode

Decimation Rate	ODR (kSPS)	Minimum DCLKx (kHz)		
		1 DOUTx	2 DOUTx	4 DOUTx
4095	0.500122	128	64	32
2048	1	256	128	64
1024	2	512	256	128
512	4	1024	512	256
256	8	2048	1024	512
128	16	4096	2048	1024

Table 41. Maximum ODRs and Minimum DCLK Frequencies in Low Power Mode

Decimation Rate	ODR (kSPS)	Minimum DCLK (kHz)		
		1 DOUT	2 DOUT	4 DOUT
2048	0.25	64	32	16
1024	0.5	128	64	32
512	1	256	128	64
256	2	512	256	128
128	4	1024	512	256
64	8	2048	1024	512

If the AD7779 operates in SPI control mode, it is possible to adjust the DOUTx strength, which can be selected in the DOUT_DRIVE_STR bits, as described in Table 42.

Table 42. DOUTx Strength

GENERAL_USER_CONFIG2, Bits[2:1]		Mode
0	0	Nominal
0	1	Strong
1	0	Weak
1	1	Extra strong

SPI Interface

The SPI interfaces gives the user flexibility to read the conversion from the Σ-Δ ADC where the processor or microcontroller is the master.

When a new conversion is completed, the $\overline{DRDY}$ signal is toggled to indicate that data can be accessed. When $\overline{DRDY}$ toggles, the internal channel counter is reset and the next SPI read is from Channel 0 again. Conversely, after the last channel data is read, all succeeding reads before the next $\overline{DRDY}$ signal are from Channel 7 (LSB).

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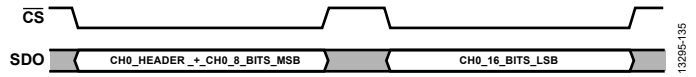

Figure 122. SPI Readback, 16 Bits per Frame

Figure 123. SPI Readback, 24 Bits per Frame

The SPI operates in multiples of 8 bits per frame; Figure 122 shows a readback example in 16 bits per frames, whereas Figure 123 shows a readback in 24 bits per frame.

Note that if the device is configured in SPI control mode, the AD7779 generates a software reset if the SDI pin is sampled high for 64 consecutive clocks. To avoid a reset or unwanted register writes, it is recommended to transfer a 0x8000 command, which generates a readback command that is ignored by the device, as explained in the SPI Software Reset section.

CALCULATING THE CRC CHECKSUM

The AD7779 implements two different CRC checksum generators, one for the Σ-Δ results and another for the SPI control mode.

The AD7779 uses a CRC polynomial to calculate the CRC checksum value. The 8-bit CRC polynomial used is $x^8 + x^2 + x + 1$.

To replicate the polynomial division in the hardware, the data is left shifted by eight bits to create a number ending in eight Logic 0s. The polynomial is aligned so that its MSB is adjacent to the leftmost Logic 1 of the data. An XOR (exclusive OR) function is applied to the data to produce a new, shorter number. The polynomial is again aligned so that its MSB is adjacent to the leftmost Logic 1 of the new result, and the procedure is repeated. This process is repeated until the original data is reduced to a value less than the polynomial. This is the 8-bit checksum.

Note that the AD7779 CRC block presets the input shift registers to 1, which means that the 8 MSBs of user data must be inverted before computing the algorithm.

As an example of CRC calculation for 16-bit data using the XOR is shown in Table 43.

Table 43. Example CRC Calculation for 16-Bit Data[1, 2]

Data	**0**	**0**	**0**	**0**	**0**	**1**	**1**	**0**	**0**	**1**	**0**	**0**	**1**	**1**	**1**	**0**	**N/A**	**N/A**	**N/A**	**N/A**	**N/A**	**N/A**	**N/A**	**N/A**
Process Data	**1**	**1**	**1**	**1**	**1**	**0**	**0**	**1**	**0**	**1**	**0**	**0**	**1**	**1**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Polynomial	1	0	0	0	0	0	1	1	1															
		1	1	1	1	0	1	0	1	1														
		1	0	0	0	0	0	1	1	1														
			1	1	1	0	1	1	0	0	0													
			1	0	0	0	0	0	1	1	1													
				1	1	0	1	1	1	1	1	0												
				1	0	0	0	0	0	1	1	1												
					1	0	1	1	1	0	0	1	1											
					1	0	0	0	0	0	1	1	1											
						1	1	1	0	1	0	0	0	1	1									
						1	0	0	0	0	0	1	1	1	1									
							1	1	0	1	0	0	1	0	1	1								
							1	0	0	0	0	0	0	1	1	1								
								1	1	0	0	1	0	0	0	1	0							
								1	0	0	0	0	0	1	1	1	1							
									1	0	0	1	0	0	1	1	0							
									1	0	0	0	0	1	1	1	1							
										1	0	1	0	0	0	0	1	1	0	1	0	0		
										1	0	0	0	0	0	1	1	1	1	1	1	1		
											1	0	1	1	0	0	0	0	1	0	1	1	0	1
											1	0	0	0	0	0	0	1	1	0	0	1	1	1
												1	0	0	0	0	0	0	1	1	0	0	1	1
													1	0	0	0	0	0	0	0	1	1	0	1
CRC																	0	1	0	0	0	1	0	0

[1] This table represents the division of the data; blank cells are for formatting purposes.
[2] N/A means not applicable.

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Σ-Δ CRC Checksum

The CRC message is calculated internally by the AD7779 on ADC pairs. The CRC is calculated using the ADC output data from two ADCs and Bits[7:4] from the header. Therefore, 56 bits are used to calculate the 8-bit CRC. This CRC is split between the two channel headers. The CRC data covers channel pairings as follows: Channel 0 and Channel 1, Channel 2 and Channel 3, Channel 4 and Channel 5, Channel 6 and Channel 7.

The CRC is calculated from 56 bits across two consecutive/ channel pairings (Channel 0 and Channel 1, Channel 2 and Channel 3, Channel 4 and Channel 5, Channel 6 and Channel 7). The 56 bits consist of the chip error, the 3 bits for the first ADC pairing channel, and the 24 bits of data of each pairing channel.

For example, for the second channel pairing, Channel 2 and Channel 3,

56 *Bits = Chip Error + 3 ADC Channel Bits (010) + 24 Data Bits (Channel 2) + Chip Error + 3 ADC Channel Bits (011) + 24 Data Bits (Channel 3)*

SPI Control Mode Checksum

The CRC message is calculated internally by the AD7779. The data transferred to the AD7779 uses the R/W bit, a 7-bit address, and 8 bits of data for the CRC calculation.

The CRC calculated and appended to the data that it is shifted out uses the previously transmitted R/$\overline{W}$ bit, the 7-bit register address, and the 8 bits of data from the readback register.

If the SAR ADC is read back, the CRC algorithm uses the b0000 header and the 12 bits of SAR conversion data.

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REGISTER SUMMARY

Table 44. AD7779 Register Summary

Reg.	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	R/W
0x000	CH0_CONFIG	[7:0]	CH0_GAIN		CH0_REF_ MONITOR	CH0_RX	RESERVED				0x00	/W R
0x001	CH1_CONFIG	[7:0]	CH1_GAIN		CH1_REF_ MONITOR	CH1_RX	RESERVED				0x00	R/W
0x002	CH2_CONFIG	[7:0]	CH2_GAIN		CH2_REF_ MONITOR	CH2_RX	RESERVED				0x00	R/W
0x003	CH3_CONFIG	[7:0]	CH3_GAIN		CH3_REF_ MONITOR	CH3_RX	RESERVED				0x00	R/W
0x004	CH4_CONFIG	[7:0]	CH4_GAIN		CH4_REF_ MONITOR	CH4_RX	RESERVED				0x00	R/W
0x005	CH5_CONFIG	[7:0]	CH5_GAIN		CH5_REF_ MONITOR	CH5_RX	RESERVED				0x00	R/W
0x006	CH6_CONFIG	[7:0]	CH6_GAIN		CH6_REF_ MONITOR	CH6_RX	RESERVED				0x00	R/W
0x007	CH7_CONFIG	[7:0]	CH7_GAIN		CH7_REF_ MONITOR	CH7_RX	RESERVED				0x00	R/W
0x008	CH_DISABLE	[7:0]	CH7_ DISABLE	CH6_ DISABLE	CH5_DISABLE	CH4_DISABLE	CH3_ DISABLE	CH2_ DISABLE	CH1_ DISABLE	CH0_ DISABLE	0x00	R/W
0x009	CH0_SYNC_ OFFSET	[7:0]	CH0_SYNC_OFFSET								0x00	R/W
0x00A	CH1_SYNC_ OFFSET	[7:0]	CH1_SYNC_OFFSET								0x00	R/W
0x00B	CH2_SYNC_ OFFSET	[7:0]	CH2_SYNC_OFFSET								0x00	R/W
0x00C	CH3_SYNC_ OFFSET	[7:0]	CH3_SYNC_OFFSET								0x00	R/W
0x00D	CH4_SYNC_ OFFSET	[7:0]	CH4_SYNC_OFFSET								0x00	R/W
0x00E	CH5_SYNC_ OFFSET	[7:0]	CH5_SYNC_OFFSET								0x00	R/W
0x00F	CH6_SYNC_ OFFSET	[7:0]	CH6_SYNC_OFFSET								0x00	R/W
0x010	CH7_SYNC_ OFFSET	[7:0]	CH7_SYNC_OFFSET								0x00	R/W
0x011	GENERAL_ USER_ CONFIG_1	[7:0]	ALL_ CH_DIS_ MCLK_ EN	POWER-MODE	PDB_VCM	PDB_ REFOUT_ BUF	PDB_ SAR	PDB_ RC_OSC	SOFT_RESET		0x24	R/W
0x012	GENERAL_ USER_ CONFIG_2	[7:0]	RESERVED		SAR_DIAG_ MODE_EN	SDO_DRIVE_STR		DOUT_DRIVE_STR		SPI_SYNC	0x09	R/W
0x013	GENERAL_ USER_ CONFIG_3	[7:0]	CONVST_ DEGLITCH_DIS		RESERVED	SPI_SLAVE_ MODE_EN	RESERVED			CLK_ QUAL_DIS	0x80	R/W
0x014	DOUT_ FORMAT	[7:0]	DOUT_FORMAT		DOUT_ HEADER_ FORMAT	RESERVED	DCLK_CLK_DIV			RESERVED	0x20	R/W
0x015	ADC_MUX_ CONFIG	[7:0]	REF_MUX_CTRL		MTR_MUX_CTRL				RESERVED		0x00	R/W
0x016	GLOBAL_MUX_ CONFIG	[7:0]	GLOBAL_MUX_CTRL					RESERVED			0x00	R/W
0x017	GPIO_CONFIG	[7:0]	RESERVED					GPIO_OP_EN			0x00	R/W
0x018	GPIO_DATA	[7:0]	RESERVED		GPIO_READ_DATA			GPIO_WRITE_DATA			0x00	R/W
0x019	BUFFER_ CONFIG_1	[7:0]	RESERVED			REF_BUF_ POS_EN	REF_ BUF_ NEG_EN	RESERVED			0x38	R/W

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Reg.	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	R/W
0x01A	BUFFER_ CONFIG_2	[7:0]	REF- BUFP_ PREQ	REF- BUFN_ PREQ	RESERVED			PDB_ALDO 1_OVRDRV	PDB_ ALDO2_ OVRDRV	PDB_ DLDO_ OVRDRV	0xC0	R/W
0x01C	CH0_OFFSET_ UPPER_BYTE	[7:0]	CH0_OFFSET_ALL[23:16]								0x00	R/W
0x01D	CH0_OFFSET_ MID_BYTE	[7:0]	CH0_OFFSET_ALL[15:8]								0x00	R/W
0x01E	CH0_OFFSET_ LOWER_BYTE	[7:0]	CH0_OFFSET_ALL[7:0]								0x00	R/W
0x01F	CH0_GAIN_ UPPER_BYTE	[7:0]	CH0_GAIN_ALL[23:16]								0x00	R/W
0x020	CH0_GAIN_ MID_BYTE	[7:0]	CH0_GAIN_ALL[15:8]								0x00	R/W
0x021	CH0_GAIN_ LOWER_BYTE	[7:0]	CH0_GAIN_ALL[7:0]								0x00	R/W
0x022	CH1_OFFSET_ UPPER_BYTE	[7:0]	CH1_OFFSET_ALL[23:16]								0x00	R/W
0x023	CH1_OFFSET_ MID_BYTE	[7:0]	CH1_OFFSET_ALL[15:8]								0x00	R/W
0x024	CH1_OFFSET_ LOWER_BYTE	[7:0]	CH1_OFFSET_ALL[7:0]								0x00	R/W
0x025	CH1_GAIN_ UPPER_BYTE	[7:0]	CH1_GAIN_ALL[23:16]								0x00	R/W
0x026	CH1_GAIN_ MID_BYTE	[7:0]	CH1_GAIN_ALL[15:8]								0x00	R/W
0x027	CH1_GAIN_ LOWER_BYTE	[7:0]	CH1_GAIN_ALL[7:0]								0x00	R/W
0x028	CH2_OFFSET_ UPPER_BYTE	[7:0]	CH2_OFFSET_ALL[23:16]								0x00	R/W
0x029	CH2_OFFSET_ MID_BYTE	[7:0]	CH2_OFFSET_ALL[15:8]								0x00	R/W
0x02A	CH2_OFFSET_ LOWER_BYTE	[7:0]	CH2_OFFSET_ALL[7:0]								0x00	R/W
0x02B	CH2_GAIN_ UPPER_BYTE	[7:0]	CH2_GAIN_ALL[23:16]								0x00	R/W
0x02C	CH2_GAIN_ MID_BYTE	[7:0]	CH2_GAIN_ALL[15:8]								0x00	R/W
0x02D	CH2_GAIN_ LOWER_BYTE	[7:0]	CH2_GAIN_ALL[7:0]								0x00	R/W
0x02E	CH3_OFFSET_ UPPER_BYTE	[7:0]	CH3_OFFSET_ALL[23:16]								0x00	R/W
0x02F	CH3_OFFSET_ MID_BYTE	[7:0]	CH3_OFFSET_ALL[15:8]								0x00	R/W
0x030	CH3_OFFSET_ LOWER_BYTE	[7:0]	CH3_OFFSET_ALL[7:0]								0x00	R/W
0x031	CH3_GAIN_ UPPER_BYTE	[7:0]	CH3_GAIN_ALL[23:16]								0x00	R/W
0x032	CH3_GAIN_ MID_BYTE	[7:0]	CH3_GAIN_ALL[15:8]								0x00	R/W
0x033	CH3_GAIN_ LOWER_BYTE	[7:0]	CH3_GAIN_ALL[7:0]								0x00	R/W
0x034	CH4_OFFSET_ UPPER_BYTE	[7:0]	CH4_OFFSET_ALL[23:16]								0x00	R/W
0x035	CH4_OFFSET_ MID_BYTE	[7:0]	CH4_OFFSET_ALL[15:8]								0x00	R/W
0x036	CH4_OFFSET_ LOWER_BYTE	[7:0]	CH4_OFFSET_ALL[7:0]								0x00	R/W
0x037	CH4_GAIN_ UPPER_BYTE	[7:0]	CH4_GAIN_ALL[23:16]								0x00	R/W

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Reg.	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	R/W
0x038	CH4_GAIN_MID_BYTE	[7:0]	CH4_GAIN_ALL[15:8]								0x00	R/W
0x039	CH4_GAIN_LOWER_BYTE	[7:0]	CH4_GAIN_ALL[7:0]								0x00	R/W
0x03A	CH5_OFFSET_UPPER_BYTE	[7:0]	CH5_OFFSET_ALL[23:16]								0x00	R/W
0x03B	CH5_OFFSET_MID_BYTE	[7:0]	CH5_OFFSET_ALL[15:8]								0x00	R/W
0x03C	CH5_OFFSET_LOWER_BYTE	[7:0]	CH5_OFFSET_ALL[7:0]								0x00	R/W
0x03D	CH5_GAIN_UPPER_BYTE	[7:0]	CH5_GAIN_ALL[23:16]								0x00	R/W
0x03E	CH5_GAIN_MID_BYTE	[7:0]	CH5_GAIN_ALL[15:8]								0x00	R/W
0x03F	CH5_GAIN_LOWER_BYTE	[7:0]	CH5_GAIN_ALL[7:0]								0x00	R/W
0x040	CH6_OFFSET_UPPER_BYTE	[7:0]	CH6_OFFSET_ALL[23:16]								0x00	R/W
0x041	CH6_OFFSET_MID_BYTE	[7:0]	CH6_OFFSET_ALL[15:8]								0x00	R/W
0x042	CH6_OFFSET_LOWER_BYTE	[7:0]	CH6_OFFSET_ALL[7:0]								0x00	R/W
0x043	CH6_GAIN_UPPER_BYTE	[7:0]	CH6_GAIN_ALL[23:16]								0x00	R/W
0x044	CH6_GAIN_MID_BYTE	[7:0]	CH6_GAIN_ALL[15:8]								0x00	R/W
0x045	CH6_GAIN_LOWER_BYTE	[7:0]	CH6_GAIN_ALL[7:0]								0x00	R/W
0x046	CH7_OFFSET_UPPER_BYTE	[7:0]	CH7_OFFSET_ALL[23:16]								0x00	R/W
0x047	CH7_OFFSET_MID_BYTE	[7:0]	CH7_OFFSET_ALL[15:8]								0x00	R/W
0x048	CH7_OFFSET_LOWER_BYTE	[7:0]	CH7_OFFSET_ALL[7:0]								0x00	R/W
0x049	CH7_GAIN_UPPER_BYTE	[7:0]	CH7_GAIN_ALL[23:16]								0x00	R/W
0x04A	CH7_GAIN_MID_BYTE	[7:0]	CH7_GAIN_ALL[15:8]								0x00	R/W
0x04B	CH7_GAIN_LOWER_BYTE	[7:0]	CH7_GAIN_ALL[7:0]								0x00	R/W
0x04C	CH0_ERR_REG	[7:0]	RESERVED			CH0_ERR_AINM_UV	CH0_ERR_AINM_OV	CH0_ERR_AINP_UV	CH0_ERR_AINP_OV	CH0_ERR_REF_DET	0x00	R
0x04D	CH1_ERR_REG	[7:0]	RESERVED			CH1_ERR_AINM_UV	CH1_ERR_AINM_OV	CH1_ERR_AINP_UV	CH1_ERR_AINP_OV	CH1_ERR_REF_DET	0x00	R
0x04E	CH2_ERR_REG	[7:0]	RESERVED			CH2_ERR_AINM_UV	CH2_ERR_AINM_OV	CH2_ERR_AINP_UV	CH2_ERR_AINP_OV	CH2_ERR_REF_DET	0x00	R
0x04F	CH3_ERR_REG	[7:0]	RESERVED			CH3_ERR_AINM_UV	CH3_ERR_AINM_OV	CH3_ERR_AINP_UV	CH3_ERR_AINP_OV	CH3_ERR_REF_DET	0x00	R
0x050	CH4_ERR_REG	[7:0]	RESERVED			CH4_ERR_AINM_UV	CH4_ERR_AINM_OV	CH4_ERR_AINP_UV	CH4_ERR_AINP_OV	CH4_ERR_REF_DET	0x00	R

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Reg.	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	R/W
0x051	CH5_ERR_REG	[7:0]	RESERVED			CH5_ERR_AINM_UV	CH5_ERR_AINM_OV	CH5_ERR_AINP_UV	CH5_ERR_AINP_OV	CH5_ERR_REF_DET	0x00	R
0x052	CH6_ERR_REG	[7:0]	RESERVED			CH6_ERR_AINM_UV	CH6_ERR_AINM_OV	CH6_ERR_AINP_UV	CH6_ERR_AINP_OV	CH6_ERR_REF_DET	0x00	R
0x053	CH7_ERR_REG	[7:0]	RESERVED			CH7_ERR_AINM_UV	CH7_ERR_AINM_OV	CH7_ERR_AINP_UV	CH7_ERR_AINP_OV	CH7_ERR_REF_DET	0x00	R
0x054	CH0_1_SAT_ERR	[7:0]	RESERVED		CH1_ERR_MOD_SAT	CH1_ERR_FILTER_SAT	CH1_ERR_OUT-PUT_SAT	CH0_ERR_MOD_SAT	CH0_ERR_FILTER_SAT	CH0_ERR_OUTPUT_SAT	0x00	R
0x055	CH2_3_SAT_ERR	[7:0]	RESERVED		CH3_ERR_MOD_SAT	CH3_ERR_FILTER_SAT	CH3_ERR_OUT-PUT_SAT	CH2_ERR_MOD_SAT	CH2_ERR_FILTER_SAT	CH2_ERR_OUTPUT_SAT	0x00	R
0x056	CH4_5_SAT_ERR	[7:0]	RESERVED		CH5_ERR_MOD_SAT	CH5_ERR_FILTER_SAT	CH5_ERR_OUT-PUT_SAT	CH4_ERR_MOD_SAT	CH4_ERR_FILTER_SAT	CH4_ERR_OUTPUT_SAT	0x00	R
0x057	CH6_7_SAT_ERR	[7:0]	RESERVED		CH7_ERR_MOD_SAT	CH7_ERR_FILTER_SAT	CH7_ERR_OUT-PUT_SAT	CH6_ERR_MOD_SAT	CH6_ERR_FILTER_SAT	CH6_ERR_OUTPUT_SAT	0x00	R
0x058	CHX_ERR_REG_EN	[7:0]	OUTPUT_SAT_TEST_EN	FILTER_SAT_TEST_EN	MOD_SAT_TEST_EN	AINM_UV_TEST_EN	AINM_OV_TEST_EN	AINP_UV_TEST_EN	AINP_OV_TEST_EN	REF_DET_TEST_EN	0xFE	R/W
0x059	GEN_ERR_REG_1	[7:0]	RESERVED		MEMMAP_CRC_ERR	ROM_CRC_ERR	SPI_CLK_COUNT_ERR	SPI_INVALID_READ_ERR	SPI_INVALID_WRITE_ERR	SPI_CRC_ERR	0x00	R
0x05A	GEN_ERR_REG_1_EN	[7:0]	RESERVED		MEMMAP_CRC_TEST_EN	ROM_CRC_TEST_EN	SPI_CLK_COUNT_TEST_EN	SPI_INVALID_READ_TEST_EN	SPI_INVALID_WRITE_TEST_EN	SPI_CRC_TEST_EN	0x3E	R/W
0x05B	GEN_ERR_REG_2	[7:0]	RESERVED		RESET_DETECTED	EXT_MCLK_SWITCH_ERR	RE-SERVED	ALDO1_PSM_ERR	ALDO2_PSM_ERR	DLDO_PSM_ERR	0x00	R
0x05C	GEN_ERR_REG_2_EN	[7:0]	RESERVED		RESET_DETECT_EN	RESERVED	LDO_PSM_TEST_EN		LDO_PSM_TRIP_TEST_EN		0x3C	R/W
0x05D	STATUS_REG_1	[7:0]	RESERVED		CHIP_ERROR	ERR_LOC_CH4	ERR_LOC_CH3	ERR_LOC_CH2	ERR_LOC_CH1	ERR_LOC_CH0	0x00	R
0x05E	STATUS_REG_2	[7:0]	RESERVED		CHIP_ERROR	ERR_LOC_GEN2	ERR_LOC_GEN1	ERR_LOC_CH7	ERR_LOC_CH6	ERR_LOC_CH5	0x00	R
0x05F	STATUS_REG_3	[7:0]	RESERVED		CHIP_ERROR	INIT_COMPLETE	ERR_LOC_SAT_CH6_7	ERR_LOC_SAT_CH4_5	ERR_LOC_SAT_CH2_3	ERR_LOC_SAT_CH0_1	0x00	R

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Reg.	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	R/W
0x060	SRC_N_MSB	[7:0]	RESERVED				SRC_N_ALL[11:8]				0x00	R/W
0x061	SRC_N_LSB	[7:0]	SRC_N_ALL[7:0]								0x80	R/W
0x062	SRC_IF_MSB	[7:0]	SRC_IF_ALL[15:8]								0x00	R/W
0x063	SRC_IF_LSB	[7:0]	SRC_IF_ALL[7:0]								0x00	R/W
0x064	SRC_UPDATE	[7:0]	SRC_ LOAD_ SOURCE	RESERVED						SRC_ LOAD_ UPDATE	0x00	R/W

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REGISTER DETAILS

CHANNEL 0 CONFIGURATION REGISTER

Address: 0x000, Reset: 0x00, Name: CH0_CONFIG

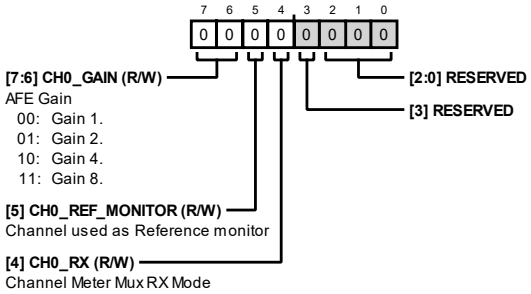

Table 45. Bit Descriptions for CH0_CONFIG

Bits	Bit Name	Settings	Description	Reset	Access
[7:6]	CH0_GAIN		AFE Gain	0x0	R/W
		00	Gain 1		
		01	Gain 2		
		10	Gain 4		
		11	Gain 8		
5	CH0_REF_MONITOR		Channel Used as Reference Monitor	0x0	R/W
4	CH0_RX		Channel Meter Mux Rx Mode	0x0	R/W
[3:0]	RESERVED		Reserved	0x0	R/W

CHANNEL 1 CONFIGURATION REGISTER

Address: 0x001, Reset: 0x00, Name: CH1_CONFIG

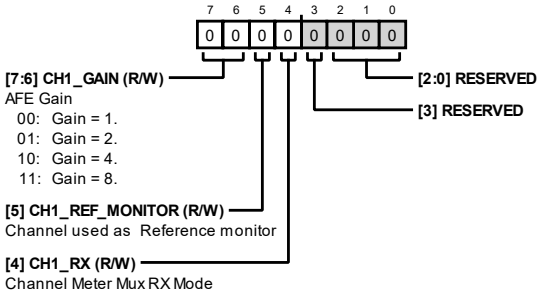

Table 46. Bit Descriptions for CH1_CONFIG

Bits	Bit Name	Settings	Description	Reset	Access
[7:6]	CH1_GAIN		AFE Gain	0x0	R/W
		00	Gain = 1		
		01	Gain = 2		
		10	Gain = 4		
		11	Gain = 8		
5	CH1_REF_MONITOR		Channel Used as Reference Monitor	0x0	R/W
4	CH1_RX		Channel Meter Mux Rx Mode	0x0	R/W
[3:0]	RESERVED		Reserved	0x0	R/W

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CHANNEL 2 CONFIGURATION REGISTER

Address: 0x002, Reset: 0x00, Name: CH2_CONFIG

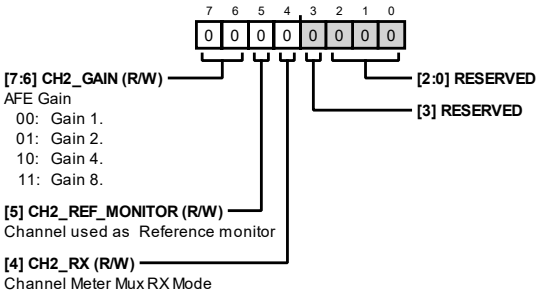

Table 47. Bit Descriptions for CH2_CONFIG

Bits	Bit Name	Settings	Description	Reset	Access
[7:6]	CH2_GAIN		AFE Gain	0x0	R/W
		00	Gain 1		
		01	Gain 2		
		10	Gain 4		
		11	Gain 8		
5	CH2_REF_MONITOR		Channel Used as Reference Monitor	0x0	R/W
4	CH2_RX		Channel Meter Mux Rx Mode	0x0	R/W
[3:0]	RESERVED		Reserved	0x0	R/W

CHANNEL 3 CONFIGURATION REGISTER

Address: 0x003, Reset: 0x00, Name: CH3_CONFIG

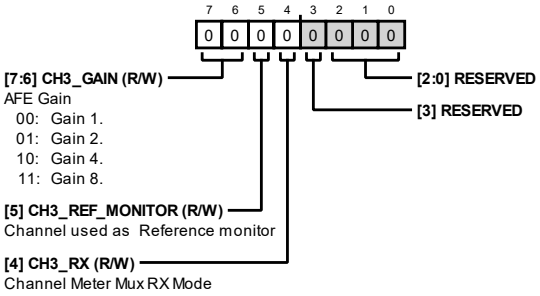

Table 48. Bit Descriptions for CH3_CONFIG

Bits	Bit Name	Settings	Description	Reset	Access
[7:6]	CH3_GAIN		AFE Gain	0x0	R/W
		00	Gain 1		
		01	Gain 2		
		10	Gain 4		
		11	Gain 8		
5	CH3_REF_MONITOR		Channel Used as Reference Monitor	0x0	R/W
4	CH3_RX		Channel Meter Mux Rx Mode	0x0	R/W
[3:0]	RESERVED		Reserved	0x0	R/W

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CHANNEL 4 CONFIGURATION REGISTER

Address: 0x004, Reset: 0x00, Name: CH4_CONFIG

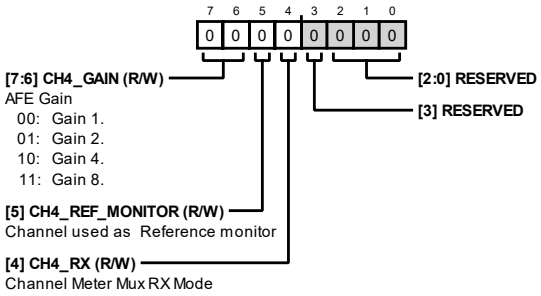

Table 49. Bit Descriptions for CH4_CONFIG

Bits	Bit Name	Settings	Description	Reset	Access
[7:6]	CH4_GAIN		AFE Gain	0x0	R/W
		00	Gain 1		
		01	Gain 2		
		10	Gain 4		
		11	Gain 8		
5	CH4_REF_MONITOR		Channel Used as Reference Monitor	0x0	R/W
4	CH4_RX		Channel Meter Mux Rx Mode	0x0	R/W
[3:0]	RESERVED		Reserved	0x0	R/W

CHANNEL 5 CONFIGURATION REGISTER

Address: 0x005, Reset: 0x00, Name: CH5_CONFIG

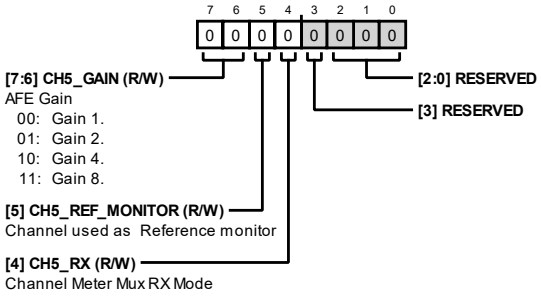

Table 50. Bit Descriptions for CH5_CONFIG

Bits	Bit Name	Settings	Description	Reset	Access
[7:6]	CH5_GAIN		AFE Gain	0x0	R/W
		00	Gain 1		
		01	Gain 2		
		10	Gain 4		
		11	Gain 8		
5	CH5_REF_MONITOR		Channel Used as Reference Monitor	0x0	R/W
4	CH5_RX		Channel Meter Mux Rx Mode	0x0	R/W
[3:0]	RESERVED		Reserved	0x0	R/W

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CHANNEL 6 CONFIGURATION REGISTER

Address: 0x006, Reset: 0x00, Name: CH6_CONFIG

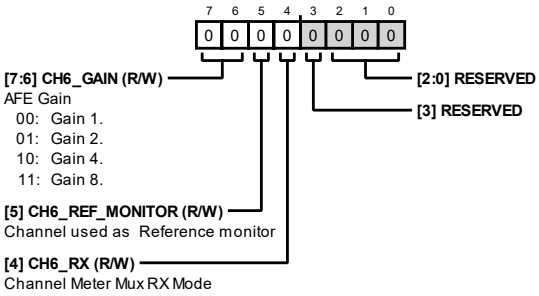

Table 51. Bit Descriptions for CH6_CONFIG

Bits	Bit Name	Settings	Description	Reset	Access
[7:6]	CH6_GAIN		AFE Gain	0x0	R/W
		00	Gain 1		
		01	Gain 2		
		10	Gain 4		
		11	Gain 8		
5	CH6_REF_MONITOR		Channel Used as Reference Monitor	0x0	R/W
4	CH6_RX		Channel Meter Mux Rx Mode	0x0	R/W
[3:0]	RESERVED		Reserved	0x0	R/W

CHANNEL 7 CONFIGURATION REGISTER

Address: 0x007, Reset: 0x00, Name: CH7_CONFIG

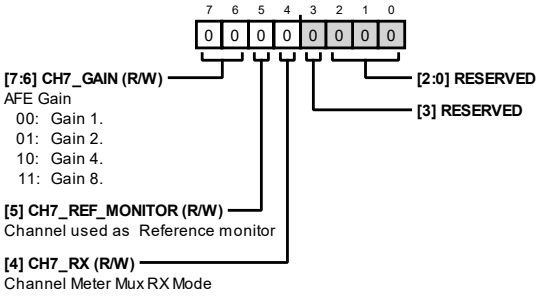

Table 52. Bit Descriptions for CH7_CONFIG

Bits	Bit Name	Settings	Description	Reset	Access
[7:6]	CH7_GAIN		AFE Gain	0x0	R/W
		00	Gain 1		
		01	Gain 2		
		10	Gain 4		
		11	Gain 8		
5	CH7_REF_MONITOR		Channel Used as Reference Monitor	0x0	R/W
4	CH7_RX		Channel Meter Mux Rx Mode	0x0	R/W
[3:0]	RESERVED		Reserved	0x0	R/W

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DISABLE CLOCKS TO ADC CHANNEL REGISTER

Address: 0x008, Reset: 0x00, Name: CH_DISABLE

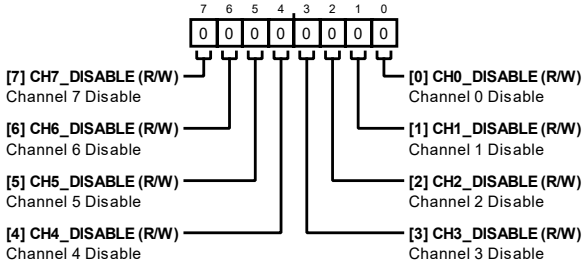

Table 53. Bit descriptions for CH_DISABLE

Bits	Bit Name	Settings	Description	Reset	Access
7	CH7_DISABLE		Channel 7 Disable	0x0	R/W
6	CH6_DISABLE		Channel 6 Disable	0x0	R/W
5	CH5_DISABLE		Channel 5 Disable	0x0	R/W
4	CH4_DISABLE		Channel 4 Disable	0x0	R/W
3	CH3_DISABLE		Channel 3 Disable	0x0	R/W
2	CH2_DISABLE		Channel 2 Disable	0x0	R/W
1	CH1_DISABLE		Channel 1 Disable	0x0	R/W
0	CH0_DISABLE		Channel 0 Disable	0x0	R/W

CHANNEL 0 SYNC OFFSET REGISTER

Address: 0x009, Reset: 0x00, Name: CH0_SYNC_OFFSET

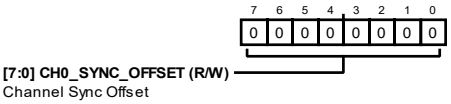

Table 54. Bit Descriptions for CH0_SYNC_OFFSET

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	CH0_SYNC_OFFSET		Channel Sync Offset	0x0	R/W

CHANNEL 1 SYNC OFFSET REGISTER

Address: 0x00A, Reset: 0x00, Name: CH1_SYNC_OFFSET

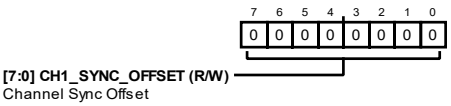

Table 55. Bit Descriptions for CH1_SYNC_OFFSET

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	CH1_SYNC_OFFSET		Channel Sync Offset	0x0	R/W

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CHANNEL 2 SYNC OFFSET REGISTER

Address: 0x00B, Reset: 0x00, Name: CH2_SYNC_OFFSET

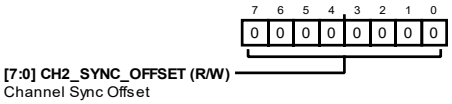

Table 56. Bit Descriptions for CH2_SYNC_OFFSET

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	CH2_SYNC_OFFSET		Channel Sync Offset	0x0	R/W

CHANNEL 3 SYNC OFFSET REGISTER

Address: 0x00C, Reset: 0x00, Name: CH3_SYNC_OFFSET

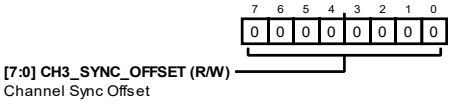

Table 57. Bit Descriptions for CH3_SYNC_OFFSET

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	CH3_SYNC_OFFSET		Channel Sync Offset	0x0	R/W

CHANNEL 4 SYNC OFFSET REGISTER

Address: 0x00D, Reset: 0x00, Name: CH4_SYNC_OFFSET

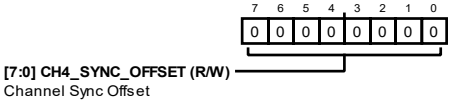

Table 58. Bit Descriptions for CH4_SYNC_OFFSET

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	CH4_SYNC_OFFSET		Channel Sync Offset	0x0	R/W

CHANNEL 5 SYNC OFFSET REGISTER

Address: 0x00E, Reset: 0x00, Name: CH5_SYNC_OFFSET

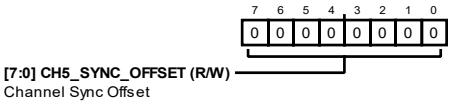

Table 59. Bit Descriptions for CH5_SYNC_OFFSET

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	CH5_SYNC_OFFSET		Channel Sync Offset	0x0	R/W

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CHANNEL 6 SYNC OFFSET REGISTER

Address: 0x00F, Reset: 0x00, Name: CH6_SYNC_OFFSET

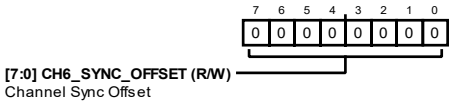

Table 60. Bit Descriptions for CH6_SYNC_OFFSET

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	CH6_SYNC_OFFSET		Channel Sync Offset	0x0	R/W

CHANNEL 7 SYNC OFFSET REGISTER

Address: 0x010, Reset: 0x00, Name: CH7_SYNC_OFFSET

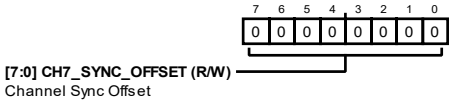

Table 61. Bit Descriptions for CH7_SYNC_OFFSET

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	CH7_SYNC_OFFSET		Channel Sync Offset	0x0	R/W

GENERAL USER CONFIGURATION 1 REGISTER

Address: 0x011, Reset: 0x24, Name: GENERAL_USER_CONFIG_1

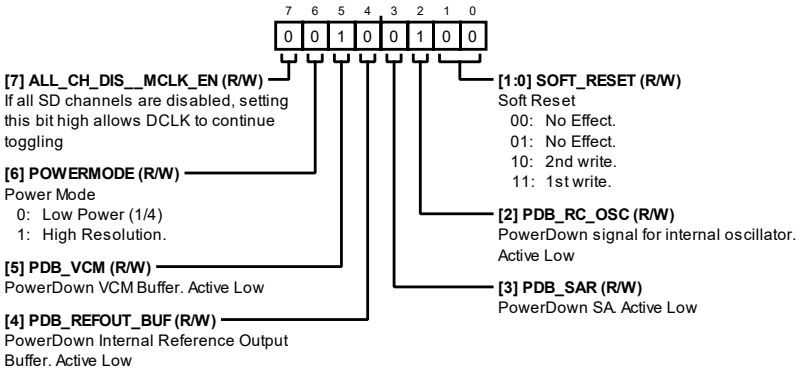

Table 62. Bit Descriptions for GENERAL_USER_CONFIG_1

Bits	Bit Name	Settings	Description	Reset	Access
7	ALL_CH_DIS_MCLK_EN		If all Σ-Δ channels are disabled, setting this bit high allows DCLK to continue toggling.	0x0	R/W
6	POWERMODE		Power Mode.	0x0	R/W
		0	Low power (1/4).		
		1	High resolution.		
5	PDB_VCM		Power Down VCM Buffer. Active low.	0x1	R/W
4	PDB_REFOUT_BUF		Power Down Internal Reference Output Buffer. Active low.	0x0	R/W
3	PDB_SAR		Power Down SAR. Active low.	0x0	R/W
2	PDB_RC_OSC		Power Down Signal for Internal Oscillator. Active low.	0x1	R/W

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Bits	Bit Name	Settings	Description	Reset	Access
[1:0]	SOFT_RESET		Soft Reset	0x0	R/W
		00	No effect		
		01	No effect		
		10	2nd write		
		11	1st write		

GENERAL USER CONFIGURATION 2 REGISTER

Address: 0x012, Reset: 0x09, Name: GENERAL_USER_CONFIG_2

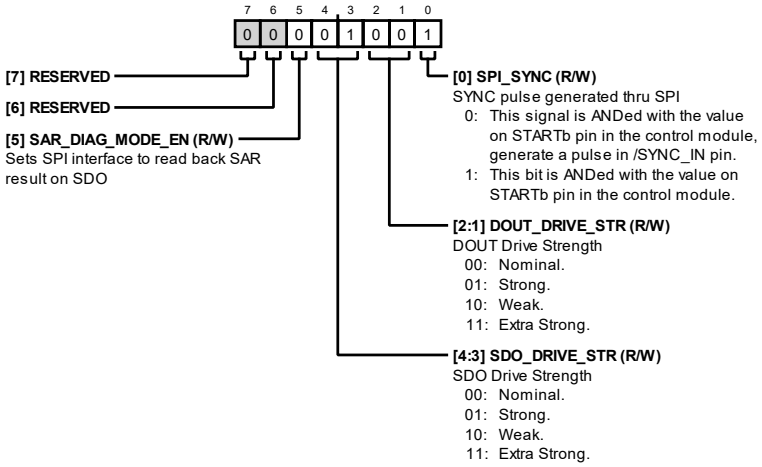

Table 63. Bit Descriptions for GENERAL_USER_CONFIG_2

Bits	Bit Name	Settings	Description	Reset	Access
[7:6]	RESERVED		Reserved.	0x0	R/W
5	SAR_DIAG_MODE_EN		Sets SPI Interface to Read Back SAR Result on SDO.	0x0	R/W
[4:3]	SDO_DRIVE_STR		SDO Drive Strength.	0x1	R/W
		00	Nominal.		
		01	Strong.		
		10	Weak.		
		11	Extra strong.		
[2:1]	DOUT_DRIVE_STR		DOUTx Drive Strength.	0x0	R/W
		00	Nominal.		
		01	Strong.		
		10	Weak.		
		11	Extra strong.		
0	SPI_SYNC		SYNC Pulse Generated Through SPI.	0x1	R/W
		0	This signal is AND'ed with the value on the $\overline{\text{START}}$ pin in the control module and generates a pulse in the $\overline{\text{SYNC_IN}}$ pin.		
		1	This bit is AND'ed with the value on $\overline{\text{START}}$ pin in the control module.		

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GENERAL USER CONFIGURATION 3 REGISTER

Address: 0x013, Reset: 0x80, Name: GENERAL_USER_CONFIG_3

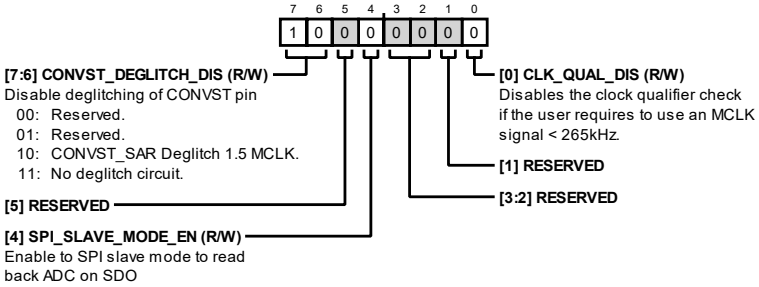

Table 64. Bit descriptions for GENERAL_USER_CONFIG_3

Bits	Bit Name	Settings	Description	Reset	Access
[7:6]	CONVST_DEGLITCH_DIS		Disable deglitching of CONVST_SAR pin	0x2	R/W
		00	Reserved.		
		01	Reserved.		
		10	CONVST_SAR Deglitch 1.5 MCLK.		
		11	No deglitch circuit.		
5	RESERVED		Reserved.	0x0	R/W
4	SPI_SLAVE_MODE_EN		Enable to SPI slave mode to read back ADC on SDO	0x0	R/W
[3:2]	RESERVED		Reserved.	0x0	R/W
1	RESERVED		Reserved.	0x0	R/W
0	CLK_QUAL_DIS		Disables the clock qualifier check if the user requires to use an MCLK signal <265 kHz.	0x0	R/W

DATA OUTPUT FORMAT REGISTER

Address: 0x014, Reset: 0x20, Name: DOUT_FORMAT

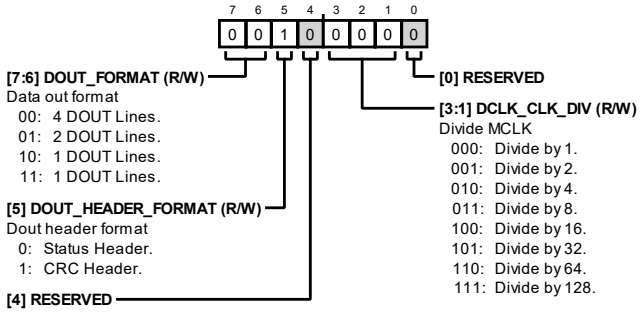

Table 65. Bit Descriptions for DOUT_FORMAT

Bits	Bit Name	Settings	Description	Reset	Access
[7:6]	DOUT_FORMAT		Data Out Format.	0x0	R/W
		00	4 DOUT lines		
		01	2 DOUT lines		
		10	1 DOUT lines		
		11	1 DOUT lines		

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Bits	Bit Name	Settings	Description	Reset	Access
5	DOUT_HEADER_FORMAT		DOUT Header Format	0x1	R/W
		0	Status header		
		1	CRC header		
4	RESERVED		Reserved.	0x0	R/W
[3:1]	DCLK_CLK_DIV		Divide MCLK	0x0	R/W
		000	Divide by 1		
		001	Divide by 2		
		010	Divide by 4		
		011	Divide by 8		
		100	Divide by 16		
		101	Divide by 32		
		110	Divide by 64		
		111	Divide by 128		
0	RESERVED		Reserved.	0x0	R/W

MAIN ADC METER AND REFERENCE MUX CONTROL REGISTER

Address: 0x015, Reset: 0x00, Name: ADC_MUX_CONFIG

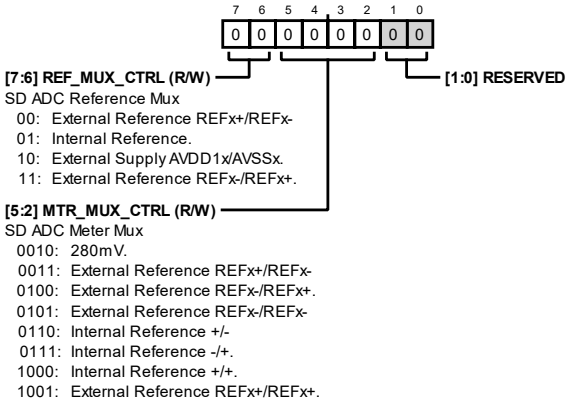

Table 66. Bit Descriptions for ADC_MUX_CONFIG

Bits	Bit Name	Settings	Description	Reset	Access
[7:6]	REF_MUX_CTRL		SD ADC Reference Mux	0x0	R/W
		00	External reference REFx+/REFx−		
		01	Internal reference.		
		10	External supply AVDD1x/AVSSx.		
		11	External reference REFx−/REFx+.		
[5:2]	MTR_MUX_CTRL		SD ADC Meter Mux	0x0	R/W
		0010	280 mV		
		0011	External reference REFx+/REFx−		
		0100	External reference REFx−/REFx+		
		0101	External reference REFx−/REFx−		
		0110	Internal reference +/−		

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Bits	Bit Name	Settings	Description	Reset	Access
		0111	Internal reference −/+		
		1000	Internal reference +/+		
		1001	External reference REFx+/REFx+		
[1:0]	RESERVED		Reserved.	0x0	R/W

GLOBAL DIAGNOSTICS MUX REGISTER

Address: 0x016, Reset: 0x00, Name: GLOBAL_MUX_CONFIG

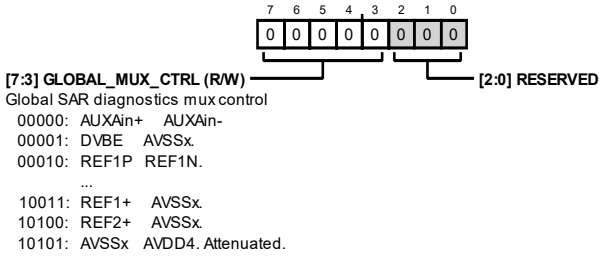

Table 67. Bit Descriptions for GLOBAL_MUX_CONFIG

Bits	Bit Name	Settings	Description	Reset	Access
[7:3]	GLOBAL_MUX_CTRL		Global SAR Diagnostics Mux Control.	0x0	R/W
		00000	AUXAIN+/AUXAIN−.		
		00001	DV_{BE}/AVSSx.		
		00010	REF1+/REF1−.		
		00011	REF2+/REF2−.		
		00100	REF_OUT/AVSSx.		
		00101	VCM/AVSSx.		
		00110	AREG1CAP/AVSSx.		
		00111	AREG2CAP/AVSSx.		
		01000	DREGCAP/DGND.		
		01001	AVDD1A/AVSSx.		
		01010	AVDD1B/AVSSx.		
		01011	AVDD2A/AVSSx.		
		01100	AVDD2B/AVSSx.		
		01101	IOVDD/DGND.		
		01110	AVDD4/AVSSx.		
		01111	DGND/AVSS1A.		
		10000	DGND/AVSS1B.		
		10001	DGND/AVSSx.		
		10010	AVDD4/AVSSx.		
		10011	REF1+/AVSSx.		
		10100	REF2+/AVSSx.		
		10101	AVDD4/AVSSx. Attenuated.		
[2:0]	RESERVED		Reserved.	0x0	R/W

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GPIO CONFIGURATION REGISTER

Address: 0x017, Reset: 0x00, Name: GPIO_CONFIG

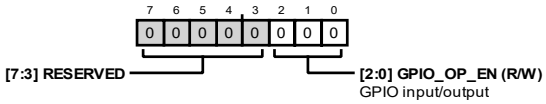

Table 68. Bit Descriptions for GPIO_CONFIG

Bits	Bit Name	Settings	Description	Reset	Access
[7:3]	RESERVED		Reserved.	0x0	R/W
[2:0]	GPIO_OP_EN		GPIO Input/Output	0x0	R/W

GPIO DATA REGISTER

Address: 0x018, Reset: 0x00, Name: GPIO_DATA

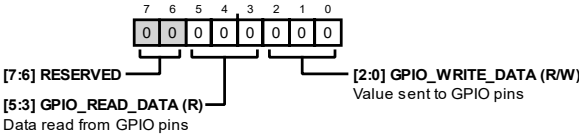

Table 69. Bit Descriptions for GPIO_DATA

Bits	Bit Name	Settings	Description	Reset	Access
[7:6]	RESERVED		Reserved.	0x0	R/W
[5:3]	GPIO_READ_DATA		Data Read from the GPIO Pins	0x0	R
[2:0]	GPIO_WRITE_DATA		Value Sent to the GPIO Pins	0x0	R/W

BUFFER CONFIGURATION 1 REGISTER

Address: 0x019, Reset: 0x38, Name: BUFFER_CONFIG_1

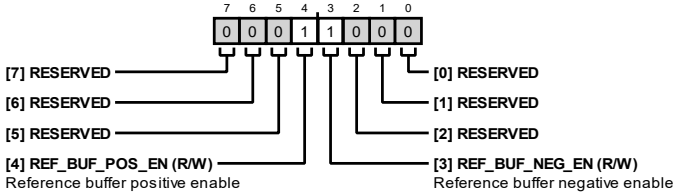

Table 70. Bit Descriptions for BUFFER_CONFIG_1

Bits	Bit Name	Settings	Description	Reset	Access
[7:5]	RESERVED		Reserved	0x0	R/W
4	REF_BUF_POS_EN		Reference Buffer Positive Enable	0x1	R/W
3	REF_BUF_NEG_EN		Reference Buffer Negative Enable	0x1	R/W
[2:0]	RESERVED		Reserved	0x0	R/W

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BUFFER CONFIGURATION 2 REGISTER

Address: 0x01A, Reset: 0xC0, Name: BUFFER_CONFIG_2

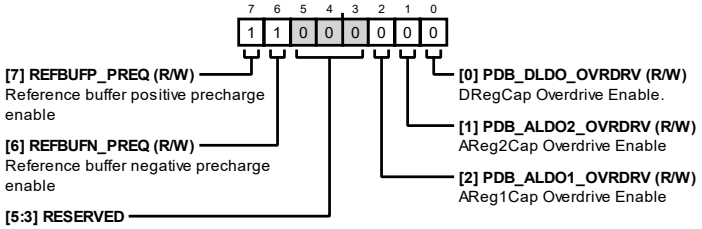

Table 71. Bit Descriptions for BUFFER_CONFIG_2

Bits	Bit Name	Settings	Description	Reset	Access
7	REFBUFP_PREQ		Reference Buffer Positive Precharge Enable	0x1	R/W
6	REFBUFN_PREQ		Reference Buffer Negative Precharge Enable	0x1	R/W
[5:3]	RESERVED		Reserved.	0x0	R/W
2	PDB_ALDO1_OVRDRV		AREG1CAP Overdrive Enable	0x0	R/W
1	PDB_ALDO2_OVRDRV		AREG2CAP Overdrive Enable	0x0	R/W
0	PDB_DLDO_OVRDRV		DREGCAP Overdrive Enable	0x0	R/W

CHANNEL 0 OFFSET UPPER BYTE REGISTER

Address: 0x01C, Reset: 0x00, Name: CH0_OFFSET_UPPER_BYTE

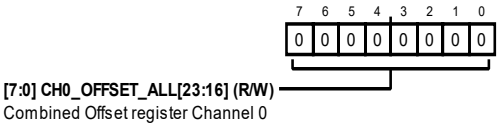

Table 72. Bit Descriptions for CH0_OFFSET_UPPER_BYTE

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	CH0_OFFSET_ALL[23:16]		Combined Offset Register Channel 0	0x0	R/W

CHANNEL 0 OFFSET MIDDLE BYTE REGISTER

Address: 0x01D, Reset: 0x00, Name: CH0_OFFSET_MID_BYTE

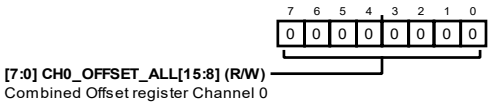

Table 73. Bit Descriptions for CH0_OFFSET_MID_BYTE

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	CH0_OFFSET_ALL[15:8]		Combined Offset Register Channel 0	0x0	R/W

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CHANNEL 0 OFFSET LOWER BYTE REGISTER

Address: 0x01E, Reset: 0x00, Name: CH0_OFFSET_LOWER_BYTE

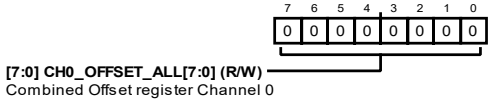

Table 74. Bit Descriptions for CH0_OFFSET_LOWER_BYTE

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	CH0_OFFSET_ALL[7:0]		Combined Offset Register Channel 0	0x0	R/W

CHANNEL 0 GAIN UPPER BYTE REGISTER

Address: 0x01F, Reset: 0x00, Name: CH0_GAIN_UPPER_BYTE

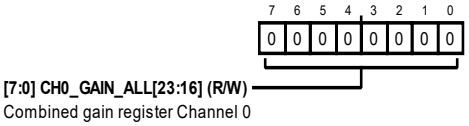

Table 75. Bit Descriptions for CH0_GAIN_UPPER_BYTE

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	CH0_GAIN_ALL[23:16]		Combined Gain Register Channel 0	0x0	R/W

CHANNEL 0 GAIN MIDDLE BYTE REGISTER

Address: 0x020, Reset: 0x00, Name: CH0_GAIN_MID_BYTE

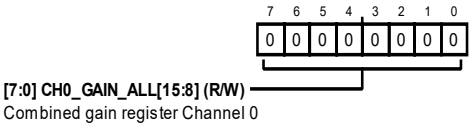

Table 76. Bit Descriptions for CH0_GAIN_MID_BYTE

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	CH0_GAIN_ALL[15:8]		Combined Gain Register Channel 0	0x0	R/W

CHANNEL 0 GAIN LOWER BYTE REGISTER

Address: 0x021, Reset: 0x00, Name: CH0_GAIN_LOWER_BYTE

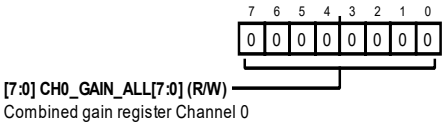

Table 77. Bit Descriptions for CH0_GAIN_LOWER_BYTE

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	CH0_GAIN_ALL[7:0]		Combined Gain Register Channel 0	0x0	R/W

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CHANNEL 1 OFFSET UPPER BYTE REGISTER

Address: 0x022, Reset: 0x00, Name: CH1_OFFSET_UPPER_BYTE

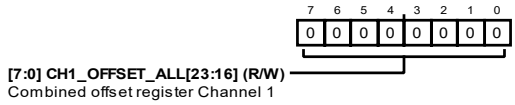

Table 78. Bit Descriptions for CH1_OFFSET_UPPER_BYTE

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	CH1_OFFSET_ALL[23:16]		Combined Offset Register Channel 1	0x0	R/W

CHANNEL 1 OFFSET MIDDLE BYTE REGISTER

Address: 0x023, Reset: 0x00, Name: CH1_OFFSET_MID_BYTE

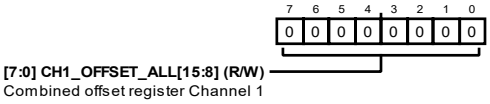

Table 79. Bit Descriptions for CH1_OFFSET_MID_BYTE

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	CH1_OFFSET_ALL[15:8]		Combined Offset Register Channel 1	0x0	R/W

CHANNEL 1 OFFSET LOWER BYTE REGISTER

Address: 0x024, Reset: 0x00, Name: CH1_OFFSET_LOWER_BYTE

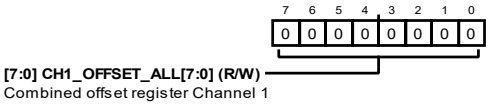

Table 80. Bit Descriptions for CH1_OFFSET_LOWER_BYTE

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	CH1_OFFSET_ALL[7:0]		Combined Offset Register Channel 1	0x0	R/W

CHANNEL 1 GAIN UPPER BYTE REGISTER

Address: 0x025, Reset: 0x00, Name: CH1_GAIN_UPPER_BYTE

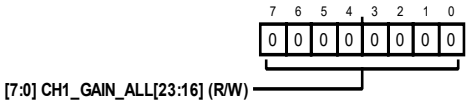

Table 81. Bit Descriptions for CH1_GAIN_UPPER_BYTE

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	CH1_GAIN_ALL[23:16]		Combined Gain Register Channel 1	0x0	R/W

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CHANNEL 1 GAIN MIDDLE BYTE REGISTER

Address: 0x026, Reset: 0x00, Name: CH1_GAIN_MID_BYTE

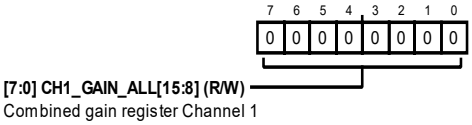

Table 82. Bit Descriptions for CH1_GAIN_MID_BYTE

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	CH1_GAIN_ALL[15:8]		Combined Gain Register Channel 1	0x0	R/W

CHANNEL 1 GAIN LOWER BYTE REGISTER

Address: 0x027, Reset: 0x00, Name: CH1_GAIN_LOWER_BYTE

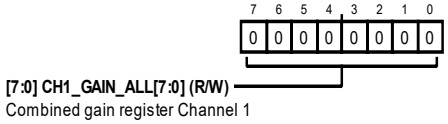

Table 83. Bit Descriptions for CH1_GAIN_LOWER_BYTE

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	CH1_GAIN_ALL[7:0]		Combined Gain Register Channel 1	0x0	R/W

CHANNEL 2 OFFSET UPPER BYTE REGISTER

Address: 0x028, Reset: 0x00, Name: CH2_OFFSET_UPPER_BYTE

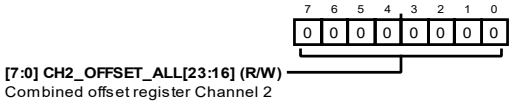

Table 84. Bit Descriptions for CH2_OFFSET_UPPER_BYTE

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	CH2_OFFSET_ALL[23:16]		Combined Offset Register Channel 2	0x0	R/W

CHANNEL 2 OFFSET MIDDLE BYTE REGISTER

Address: 0x029, Reset: 0x00, Name: CH2_OFFSET_MID_BYTE

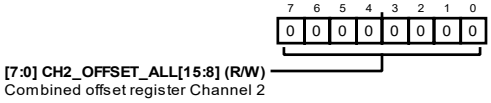

Table 85. Bit Descriptions for CH2_OFFSET_MID_BYTE

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	CH2_OFFSET_ALL[15:8]		Combined Offset Register Channel 2	0x0	R/W

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CHANNEL 2 OFFSET LOWER BYTE REGISTER

Address: 0x02A, Reset: 0x00, Name: CH2_OFFSET_LOWER_BYTE

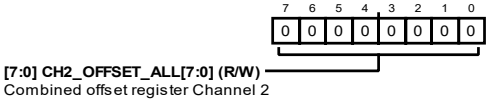

Table 86. Bit Descriptions for CH2_OFFSET_LOWER_BYTE

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	CH2_OFFSET_ALL[7:0]		Combined Offset Register Channel 2	0x0	R/W

CHANNEL 2 GAIN UPPER BYTE REGISTER

Address: 0x02B, Reset: 0x00, Name: CH2_GAIN_UPPER_BYTE

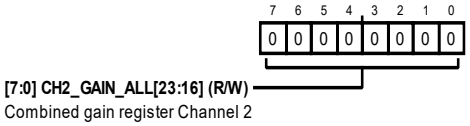

Table 87. Bit Descriptions for CH2_GAIN_UPPER_BYTE

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	CH2_GAIN_ALL[23:16]		Combined Gain Register Channel 2	0x0	R/W

CHANNEL 2 GAIN MIDDLE BYTE REGISTER

Address: 0x02C, Reset: 0x00, Name: CH2_GAIN_MID_BYTE

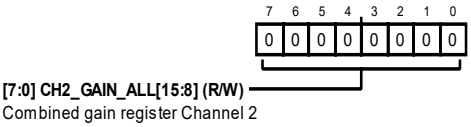

Table 88. Bit Descriptions for CH2_GAIN_MID_BYTE

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	CH2_GAIN_ALL[15:8]		Combined Gain Register Channel 2	0x0	R/W

CHANNEL 2 GAIN LOWER BYTE REGISTER

Address: 0x02D, Reset: 0x00, Name: CH2_GAIN_LOWER_BYTE

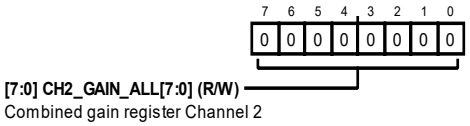

Table 89. Bit Descriptions for CH2_GAIN_LOWER_BYTE

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	CH2_GAIN_ALL[7:0]		Combined Gain Register Channel 2	0x0	R/W

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CHANNEL 3 OFFSET UPPER BYTE REGISTER

Address: 0x02E, Reset: 0x00, Name: CH3_OFFSET_UPPER_BYTE

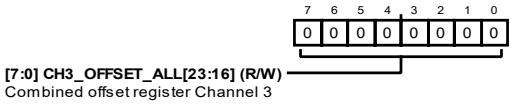

Table 90. Bit descriptions for CH3_OFFSET_UPPER_BYTE

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	CH3_OFFSET_ALL[23:16]		Combined Offset Register Channel 3	0x0	R/W

CHANNEL 3 OFFSET MIDDLE BYTE REGISTER

Address: 0x02F, Reset: 0x00, Name: CH3_OFFSET_MID_BYTE

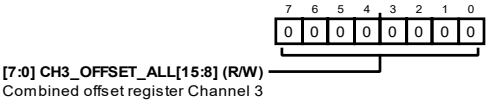

Table 91. Bit Descriptions for CH3_OFFSET_MID_BYTE

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	CH3_OFFSET_ALL[15:8]		Combined Offset Register Channel 3	0x0	R/W

CHANNEL 3 OFFSET LOWER BYTE REGISTER

Address: 0x030, Reset: 0x00, Name: CH3_OFFSET_LOWER_BYTE

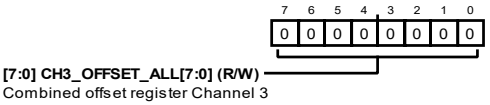

Table 92. Bit Descriptions for CH3_OFFSET_LOWER_BYTE

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	CH3_OFFSET_ALL[7:0]		Combined Offset Register Channel 3	0x0	R/W

CHANNEL 3 GAIN UPPER BYTE REGISTER

Address: 0x031, Reset: 0x00, Name: CH3_GAIN_UPPER_BYTE

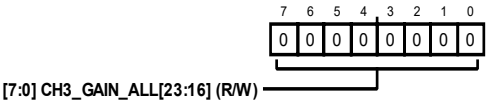

Table 93. Bit Descriptions for CH3_GAIN_UPPER_BYTE

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	CH3_GAIN_ALL[23:16]		Combined Gain Register Channel 3	0x0	R/W

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CHANNEL 3 GAIN MIDDLE BYTE REGISTER

Address: 0x032, Reset: 0x00, Name: CH3_GAIN_MID_BYTE

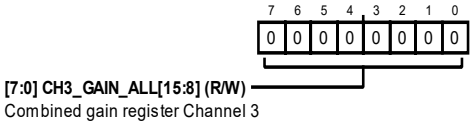

Table 94. Bit Descriptions for CH3_GAIN_MID_BYTE

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	CH3_GAIN_ALL[15:8]		Combined Gain Register Channel 3	0x0	R/W

CHANNEL 3 GAIN LOWER BYTE REGISTER

Address: 0x033, Reset: 0x00, Name: CH3_GAIN_LOWER_BYTE

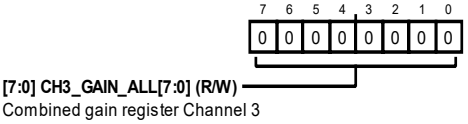

Table 95. Bit Descriptions for CH3_GAIN_LOWER_BYTE

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	CH3_GAIN_ALL[7:0]		Combined Gain Register Channel 3	0x0	R/W

CHANNEL 4 OFFSET UPPER BYTE REGISTER

Address: 0x034, Reset: 0x00, Name: CH4_OFFSET_UPPER_BYTE

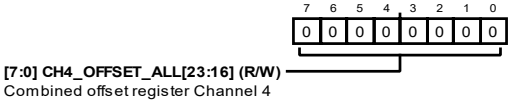

Table 96. Bit Descriptions for CH4_OFFSET_UPPER_BYTE

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	CH4_OFFSET_ALL[23:16]		Combined Offset Register Channel 4	0x0	R/W

CHANNEL 4 OFFSET MIDDLE BYTE REGISTER

Address: 0x035, Reset: 0x00, Name: CH4_OFFSET_MID_BYTE

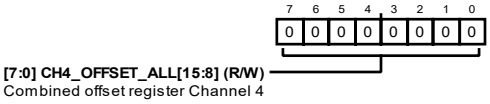

Table 97. Bit Descriptions for CH4_OFFSET_MID_BYTE

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	CH4_OFFSET_ALL[15:8]		Combined Offset Register Channel 4	0x0	R/W

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CHANNEL 4 OFFSET LOWER BYTE REGISTER

Address: 0x036, Reset: 0x00, Name: CH4_OFFSET_LOWER_BYTE

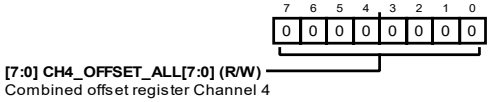

Table 98. Bit Descriptions for CH4_OFFSET_LOWER_BYTE

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	CH4_OFFSET_ALL[7:0]		Combined Offset Register Channel 4	0x0	R/W

CHANNEL 4 GAIN UPPER BYTE REGISTER

Address: 0x037, Reset: 0x00, Name: CH4_GAIN_UPPER_BYTE

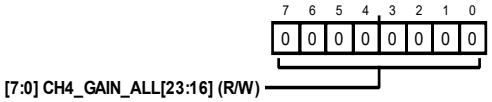

Table 99. Bit Descriptions for CH4_GAIN_UPPER_BYTE

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	CH4_GAIN_ALL[23:16]		Combined Gain Register Channel 4	0x0	R/W

CHANNEL 4 GAIN MIDDLE BYTE REGISTER

Address: 0x038, Reset: 0x00, Name: CH4_GAIN_MID_BYTE

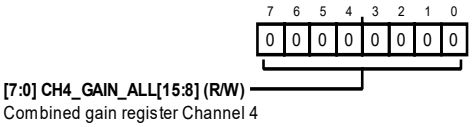

Table 100. Bit Descriptions for CH4_GAIN_MID_BYTE

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	CH4_GAIN_ALL[15:8]		Combined Gain Register Channel 4	0x0	R/W

CHANNEL 4 GAIN LOWER BYTE REGISTER

Address: 0x039, Reset: 0x00, Name: CH4_GAIN_LOWER_BYTE

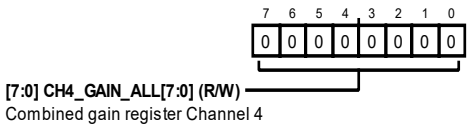

Table 101. Bit Descriptions for CH4_GAIN_LOWER_BYTE

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	CH4_GAIN_ALL[7:0]		Combined Gain Register Channel 4	0x0	R/W

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CHANNEL 5 OFFSET UPPER BYTE REGISTER

Address: 0x03A, Reset: 0x00, Name: CH5_OFFSET_UPPER_BYTE

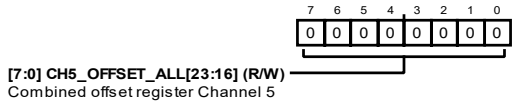

Table 102. Bit Descriptions for CH5_OFFSET_UPPER_BYTE

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	CH5_OFFSET_ALL[23:16]		Combined Offset Register Channel 5	0x0	R/W

CHANNEL 5 OFFSET MIDDLE BYTE REGISTER

Address: 0x03B, Reset: 0x00, Name: CH5_OFFSET_MID_BYTE

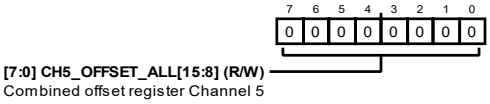

Table 103. Bit Descriptions for CH5_OFFSET_MID_BYTE

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	CH5_OFFSET_ALL[15:8]		Combined Offset Register Channel 5	0x0	R/W

CHANNEL 5 OFFSET LOWER BYTE REGISTER

Address: 0x03C, Reset: 0x00, Name: CH5_OFFSET_LOWER_BYTE

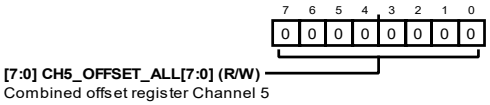

Table 104. Bit Descriptions for CH5_OFFSET_LOWER_BYTE

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	CH5_OFFSET_ALL[7:0]		Combined Offset Register Channel 5	0x0	R/W

CHANNEL 5 GAIN UPPER BYTE REGISTER

Address: 0x03D, Reset: 0x00, Name: CH5_GAIN_UPPER_BYTE

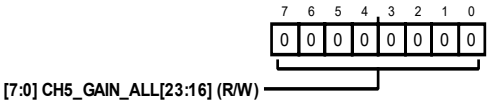

Table 105. Bit Descriptions for CH5_GAIN_UPPER_BYTE

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	CH5_GAIN_ALL[23:16]		Combined Gain Register Channel 5	0x0	R/W

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CHANNEL 5 GAIN MIDDLE BYTE REGISTER

Address: 0x03E, Reset: 0x00, Name: CH5_GAIN_MID_BYTE

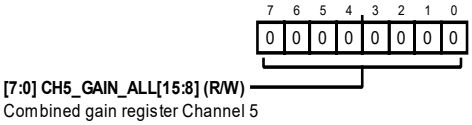

Table 106. Bit Descriptions for CH5_GAIN_MID_BYTE

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	CH5_GAIN_ALL[15:8]		Combined Gain Register Channel 5	0x0	R/W

CHANNEL 5 GAIN LOWER BYTE REGISTER

Address: 0x03F, Reset: 0x00, Name: CH5_GAIN_LOWER_BYTE

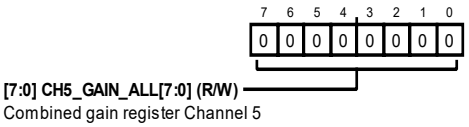

Table 107. Bit Descriptions for CH5_GAIN_LOWER_BYTE

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	CH5_GAIN_ALL[7:0]		Combined Gain Register Channel 5	0x0	R/W

CHANNEL 6 OFFSET UPPER BYTE REGISTER

Address: 0x040, Reset: 0x00, Name: CH6_OFFSET_UPPER_BYTE

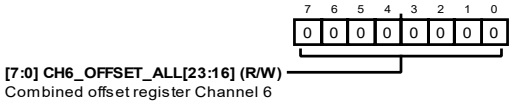

Table 108. Bit Descriptions for CH6_OFFSET_UPPER_BYTE

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	CH6_OFFSET_ALL[23:16]		Combined Offset Register Channel 6	0x0	R/W

CHANNEL 6 OFFSET MIDDLE BYTE REGISTER

Address: 0x041, Reset: 0x00, Name: CH6_OFFSET_MID_BYTE

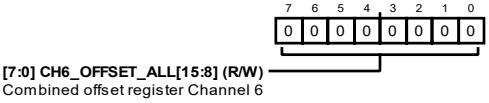

Table 109. Bit Descriptions for CH6_OFFSET_MID_BYTE

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	CH6_OFFSET_ALL[15:8]		Combined Offset Register Channel 6	0x0	R/W

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CHANNEL 6 OFFSET LOWER BYTE REGISTER

Address: 0x042, Reset: 0x00, Name: CH6_OFFSET_LOWER_BYTE

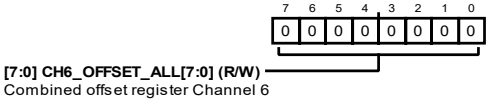

Table 110. Bit Descriptions for CH6_OFFSET_LOWER_BYTE

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	CH6_OFFSET_ALL[7:0]		Combined Offset Register Channel 6	0x0	R/W

CHANNEL 6 GAIN UPPER BYTE REGISTER

Address: 0x043, Reset: 0x00, Name: CH6_GAIN_UPPER_BYTE

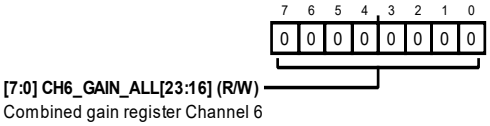

Table 111. Bit Descriptions for CH6_GAIN_UPPER_BYTE

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	CH6_GAIN_ALL[23:16]		Combined Gain Register Channel 6	0x0	R/W

CHANNEL 6 GAIN MIDDLE BYTE REGISTER

Address: 0x044, Reset: 0x00, Name: CH6_GAIN_MID_BYTE

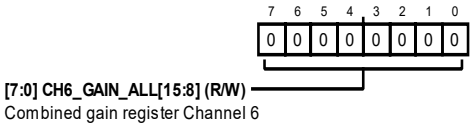

Table 112. Bit Descriptions for CH6_GAIN_MID_BYTE

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	CH6_GAIN_ALL[15:8]		Combined Gain Register Channel 6	0x0	R/W

CHANNEL 6 GAIN LOWER BYTE REGISTER

Address: 0x045, Reset: 0x00, Name: CH6_GAIN_LOWER_BYTE

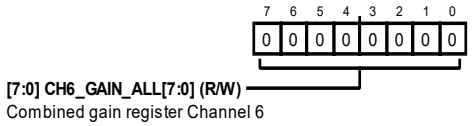

Table 113. Bit Descriptions for CH6_GAIN_LOWER_BYTE

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	CH6_GAIN_ALL[7:0]		Combined Gain Register Channel 6	0x0	R/W

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CHANNEL 7 OFFSET UPPER BYTE REGISTER

Address: 0x046, Reset: 0x00, Name: CH7_OFFSET_UPPER_BYTE

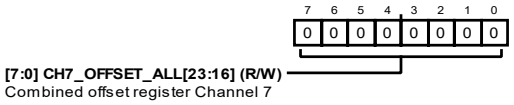

Table 114. Bit Descriptions for CH7_OFFSET_UPPER_BYTE

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	CH7_OFFSET_ALL[23:16]		Combined Offset Register Channel 7	0x0	R/W

CHANNEL 7 OFFSET MIDDLE BYTE REGISTER

Address: 0x047, Reset: 0x00, Name: CH7_OFFSET_MID_BYTE

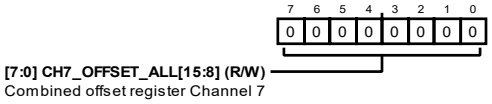

Table 115. Bit Descriptions for CH7_OFFSET_MID_BYTE

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	CH7_OFFSET_ALL[15:8]		Combined Offset Register Channel 7	0x0	R/W

CHANNEL 7 OFFSET LOWER BYTE REGISTER

Address: 0x048, Reset: 0x00, Name: CH7_OFFSET_LOWER_BYTE

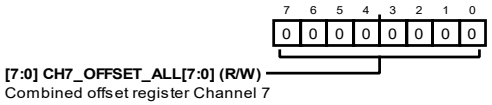

Table 116. Bit Descriptions for CH7_OFFSET_LOWER_BYTE

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	CH7_OFFSET_ALL[7:0]		Combined Offset Register Channel 7	0x0	R/W

CHANNEL 7 GAIN UPPER BYTE REGISTER

Address: 0x049, Reset: 0x00, Name: CH7_GAIN_UPPER_BYTE

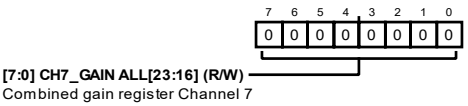

Table 117. Bit Descriptions for CH7_GAIN_UPPER_BYTE

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	CH7_GAIN ALL[23:16]		Combined Gain Register Channel 7	0x0	R/W

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CHANNEL 7 GAIN MIDDLE BYTE REGISTER

Address: 0x04A, Reset: 0x00, Name: CH7_GAIN_MID_BYTE

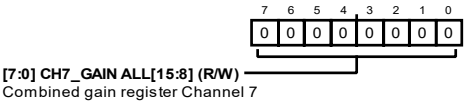

Table 118. Bit Descriptions for CH7_GAIN_MID_BYTE

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	CH7_GAIN ALL[15:8]		Combined Gain Register Channel 7	0x0	R/W

CHANNEL 7 GAIN LOWER BYTE REGISTER

Address: 0x04B, Reset: 0x00, Name: CH7_GAIN_LOWER_BYTE

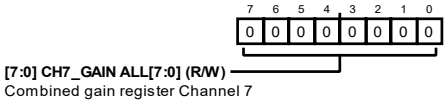

Table 119. Bit Descriptions for CH7_GAIN_LOWER_BYTE

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	CH7_GAIN ALL[7:0]		Combined Gain Register Channel 7	0x0	R/W

CHANNEL 0 STATUS REGISTER

Address: 0x04C, Reset: 0x00, Name: CH0_ERR_REG

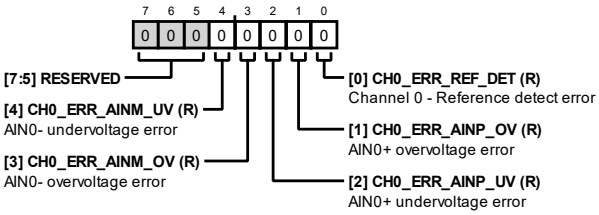

Table 120. Bit Descriptions for CH0_ERR_REG

Bits	Bit Name	Settings	Description	Reset	Access
[7:5]	RESERVED		Reserved	0x0	R/W
4	CH0_ERR_AINM_UV		Channel 0—AIN0– Undervoltage Error	0x0	R
3	CH0_ERR_AINM_OV		Channel 0—AIN0– Overvoltage Error	0x0	R
2	CH0_ERR_AINP_UV		Channel 0—AIN0+ Undervoltage Error	0x0	R
1	CH0_ERR_AINP_OV		Channel 0—AIN0+ Overvoltage Error	0x0	R
0	CH0_ERR_REF_DET		Channel 0—Reference Detect Error	0x0	R

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CHANNEL 1 STATUS REGISTER

Address: 0x04D, Reset: 0x00, Name: CH1_ERR_REG

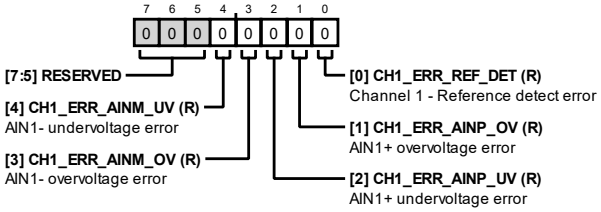

Table 121. Bit Descriptions for CH1_ERR_REG

Bits	Bit Name	Settings	Description	Reset	Access
[7:5]	RESERVED		Reserved	0x0	R/W
4	CH1_ERR_AINM_UV		Channel 1—AIN1– Undervoltage Error	0x0	R
3	CH1_ERR_AINM_OV		Channel 1—AIN1– Overvoltage Error	0x0	R
2	CH1_ERR_AINP_UV		Channel 1—AIN1+ Undervoltage Error	0x0	R
1	CH1_ERR_AINP_OV		Channel 1—AIN1+ Overvoltage Error	0x0	R
0	CH1_ERR_REF_DET		Channel 1—Reference Detect Error	0x0	R

CHANNEL 2 STATUS REGISTER

Address: 0x04E, Reset: 0x00, Name: CH2_ERR_REG

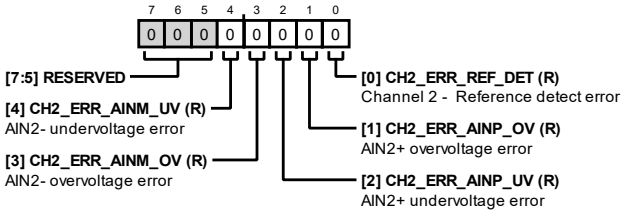

Table 122. Bit Descriptions for CH2_ERR_REG

Bits	Bit Name	Settings	Description	Reset	Access
[7:5]	RESERVED		Reserved	0x0	R/W
4	CH2_ERR_AINM_UV		Channel 2—AIN2– Undervoltage Error	0x0	R
3	CH2_ERR_AINM_OV		Channel 2—AIN2– Overvoltage Error	0x0	R
2	CH2_ERR_AINP_UV		Channel 2—AIN2+ Undervoltage Error	0x0	R
1	CH2_ERR_AINP_OV		Channel 2—AIN2+ Overvoltage Error	0x0	R
0	CH2_ERR_REF_DET		Channel 2—Reference Detect Error	0x0	R

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CHANNEL 3 STATUS REGISTER

Address: 0x04F, Reset: 0x00, Name: CH3_ERR_REG

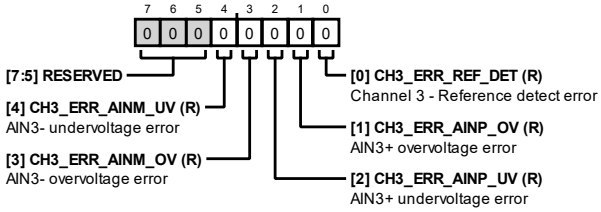

Table 123. Bit Descriptions for CH3_ERR_REG

Bits	Bit Name	Settings	Description	Reset	Access
[7:5]	RESERVED		Reserved	0x0	R/W
4	CH3_ERR_AINM_UV		Channel 3—AIN3– Undervoltage Error	0x0	R
3	CH3_ERR_AINM_OV		Channel 3—AIN3– Overvoltage Error	0x0	R
2	CH3_ERR_AINP_UV		Channel 3—AIN3+ Undervoltage Error	0x0	R
1	CH3_ERR_AINP_OV		Channel 3—AIN3+ Overvoltage Error	0x0	R
0	CH3_ERR_REF_DET		Channel 3—Reference Detect Error	0x0	R

CHANNEL 4 STATUS REGISTER

Address: 0x050, Reset: 0x00, Name: CH4_ERR_REG

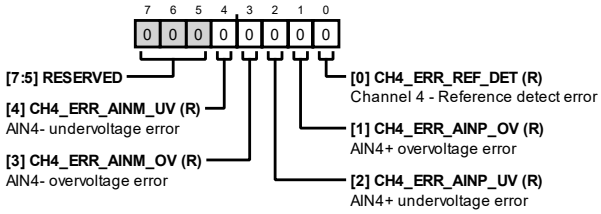

Table 124. Bit Descriptions for CH4_ERR_REG

Bits	Bit Name	Settings	Description	Reset	Access
[7:5]	RESERVED		Reserved	0x0	R/W
4	CH4_ERR_AINM_UV		Channel 4—AIN4– Undervoltage Error	0x0	R
3	CH4_ERR_AINM_OV		Channel 4—AIN4– Overvoltage Error	0x0	R
2	CH4_ERR_AINP_UV		Channel 4—AIN4+ Undervoltage Error	0x0	R
1	CH4_ERR_AINP_OV		Channel 4—AIN4+ Overvoltage Error	0x0	R
0	CH4_ERR_REF_DET		Channel 4—Reference Detect Error	0x0	R

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CHANNEL 5 STATUS REGISTER

Address: 0x051, Reset: 0x00, Name: CH5_ERR_REG

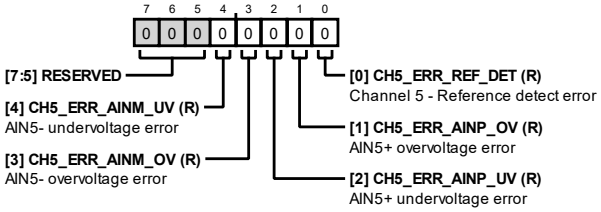

Table 125. Bit Descriptions for CH5_ERR_REG

Bits	Bit Name	Settings	Description	Reset	Access
[7:5]	RESERVED		Reserved	0x0	R/W
4	CH5_ERR_AINM_UV		Channel 5—AIN5– Undervoltage Error	0x0	R
3	CH5_ERR_AINM_OV		Channel 5—AIN5– Overvoltage Error	0x0	R
2	CH5_ERR_AINP_UV		Channel 5—AIN5+ Undervoltage Error	0x0	R
1	CH5_ERR_AINP_OV		Channel 5—AIN5+ Overvoltage Error	0x0	R
0	CH5_ERR_REF_DET		Channel 5—Reference Detect Error	0x0	R

CHANNEL 6 STATUS REGISTER

Address: 0x052, Reset: 0x00, Name: CH6_ERR_REG

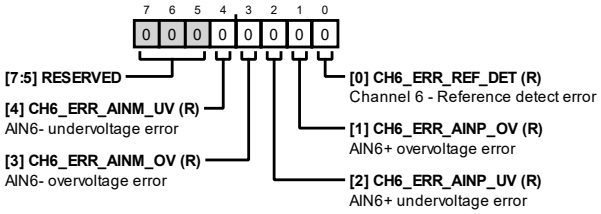

Table 126. Bit Descriptions for CH6_ERR_REG

Bits	Bit Name	Settings	Description	Reset	Access
[7:5]	RESERVED		Reserved	0x0	R/W
4	CH6_ERR_AINM_UV		Channel 6—AIN6– Undervoltage Error	0x0	R
3	CH6_ERR_AINM_OV		Channel 6—AIN6– Overvoltage Error	0x0	R
2	CH6_ERR_AINP_UV		Channel 6—AIN6+ Undervoltage Error	0x0	R
1	CH6_ERR_AINP_OV		Channel 6—AIN6+ Overvoltage Error	0x0	R
0	CH6_ERR_REF_DET		Channel 6—Reference Detect Error	0x0	R

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CHANNEL 7 STATUS REGISTER

Address: 0x053, Reset: 0x00, Name: CH7_ERR_REG

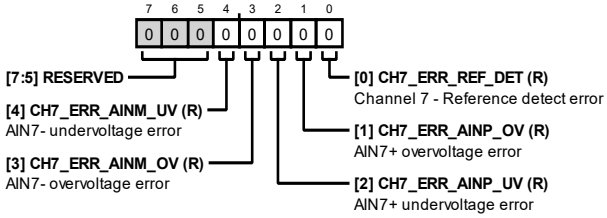

Table 127. Bit Descriptions for CH7_ERR_REG

Bits	Bit Name	Settings	Description	Reset	Access
4	CH7_ERR_AINM_UV		Channel 7—AIN7– Undervoltage Error	0x0	R
3	CH7_ERR_AINM_OV		Channel 7—AIN7– Overvoltage Error	0x0	R
2	CH7_ERR_AINP_UV		Channel 7—AIN7+ Undervoltage Error	0x0	R
1	CH7_ERR_AINP_OV		Channel 7—AIN7+ Overvoltage Error	0x0	R
0	CH7_ERR_REF_DET		Channel 7—Reference Detect Error	0x0	R

CHANNEL 0/CHANNEL 1 DSP ERRORS REGISTER

Address: 0x054, Reset: 0x00, Name: CH0_1_SAT_ERR

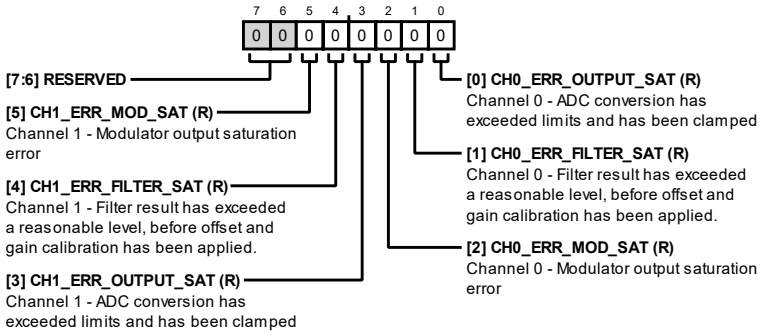

Table 128. Bit Descriptions for CH0_1_SAT_ERR

Bits	Bit Name	Settings	Description	Reset	Access
5	CH1_ERR_MOD_SAT		Channel 1—Modulator Output Saturation Error	0x0	R
4	CH1_ERR_FILTER_SAT		Channel 1—Filter result has exceeded a reasonable level, before offset and gain calibration has been applied	0x0	R
3	CH1_ERR_OUTPUT_SAT		Channel 1—ADC conversion has exceeded limits and has been clamped	0x0	R
2	CH0_ERR_MOD_SAT		Channel 0—Modulator Output Saturation Error	0x0	R
1	CH0_ERR_FILTER_SAT		Channel 0—Filter result has exceeded a reasonable level, before offset and gain calibration has been applied	0x0	R
0	CH0_ERR_OUTPUT_SAT		Channel 0—ADC conversion has exceeded limits and has been clamped	0x0	R

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CHANNEL 2/CHANNEL 3 DSP ERRORS REGISTER

Address: 0x055, Reset: 0x00, Name: CH2_3_SAT_ERR

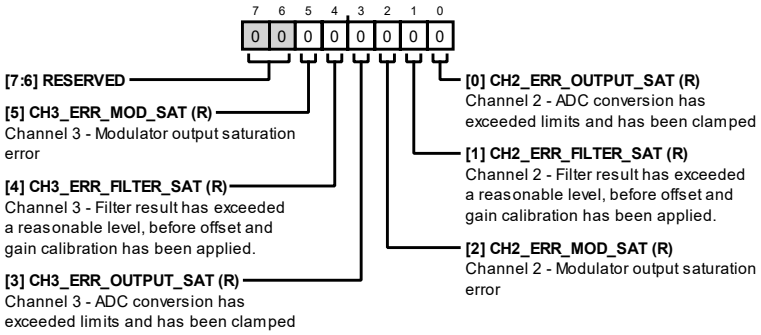

Table 129. Bit Descriptions for CH2_3_SAT_ERR

Bits	Bit Name	Settings	Description	Reset	Access
5	CH3_ERR_MOD_SAT		Channel 3—Modulator Output Saturation Error	0x0	R
4	CH3_ERR_FILTER_SAT		Channel 3—Filter result has exceeded a reasonable level, before offset and gain calibration has been applied	0x0	R
3	CH3_ERR_OUTPUT_SAT		Channel 3—ADC conversion has exceeded limits and has been clamped	0x0	R
2	CH2_ERR_MOD_SAT		Channel 2—Modulator Output Saturation Error	0x0	R
1	CH2_ERR_FILTER_SAT		Channel 2—Filter result has exceeded a reasonable level, before offset and gain calibration has been applied	0x0	R
0	CH2_ERR_OUTPUT_SAT		Channel 2—ADC conversion has exceeded limits and has been clamped	0x0	R

CHANNEL 4/CHANNEL 5 DSP ERRORS REGISTER

Address: 0x056, Reset: 0x00, Name: CH4_5_SAT_ERR

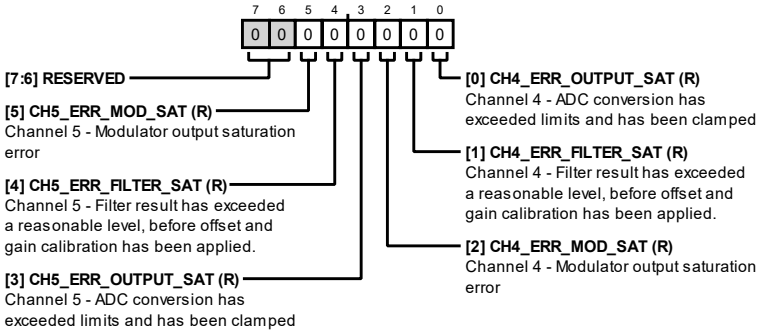

Table 130. Bit Descriptions for CH4_5_SAT_ERR

Bits	Bit Name	Settings	Description	Reset	Access
5	CH5_ERR_MOD_SAT		Channel 5—Modulator Output Saturation Error	0x0	R
4	CH5_ERR_FILTER_SAT		Channel 5—Filter result has exceeded a reasonable level, before offset and gain calibration has been applied	0x0	R
3	CH5_ERR_OUTPUT_SAT		Channel 5—ADC conversion has exceeded limits and has been clamped	0x0	R
2	CH4_ERR_MOD_SAT		Channel 4—Modulator Output Saturation Error	0x0	R
1	CH4_ERR_FILTER_SAT		Channel 4—Filter result has exceeded a reasonable level, before offset and gain calibration has been applied	0x0	R
0	CH4_ERR_OUTPUT_SAT		Channel 4—ADC conversion has exceeded limits and has been clamped	0x0	R

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CHANNEL 6/CHANNEL 7 DSP ERRORS REGISTER

Address: 0x057, Reset: 0x00, Name: CH6_7_SAT_ERR

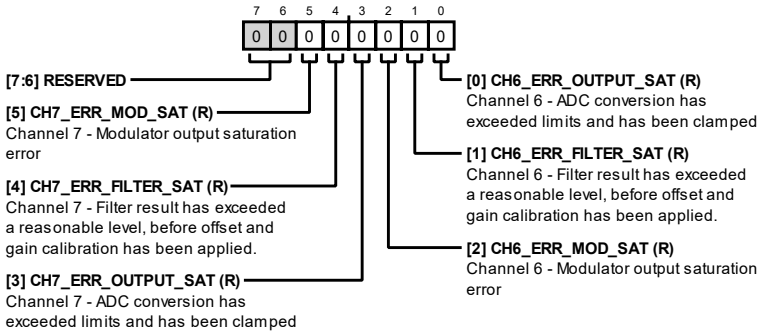

Table 131. Bit descriptions for CH6_7_SAT_ERR

Bits	Bit Name	Settings	Description	Reset	Access
5	CH7_ERR_MOD_SAT		Channel 7—Modulator Output Saturation Error	0x0	R
4	CH7_ERR_FILTER_SAT		Channel 7—Filter result has exceeded a reasonable level, before offset and gain calibration has been applied	0x0	R
3	CH7_ERR_OUTPUT_SAT		Channel 7—ADC conversion has exceeded limits and has been clamped	0x0	R
2	CH6_ERR_MOD_SAT		Channel 6—Modulator Output Saturation Error	0x0	R
1	CH6_ERR_FILTER_SAT		Channel 6—Filter result has exceeded a reasonable level, before offset and gain calibration has been applied	0x0	R
0	CH6_ERR_OUTPUT_SAT		Channel 6—ADC conversion has exceeded limits and has been clamped	0x0	R

CHANNEL 0 TO CHANNEL 7 ERROR REGISTER ENABLE REGISTER

Address: 0x058, Reset: 0xFE, Name: CHX_ERR_REG_EN

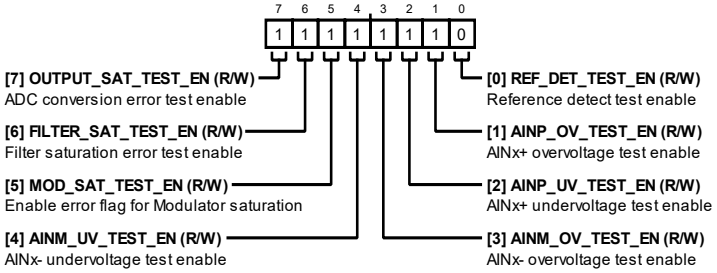

Table 132. Bit Descriptions for CHX_ERR_REG_EN

Bits	Bit Name	Settings	Description	Reset	Access
7	OUTPUT_SAT_TEST_EN		ADC Conversion Error Test Enable	0x1	R/W
6	FILTER_SAT_TEST_EN		Filter Saturation Test Enable	0x1	R/W
5	MOD_SAT_TEST_EN		Enable Error Flag for Modulator Saturation	0x1	R/W
4	AINM_UV_TEST_EN		AINx– Undervoltage Test Enable	0x1	R/W
3	AINM_OV_TEST_EN		AINx– Overvoltage Test Enable	0x1	R/W
2	AINP_UV_TEST_EN		AINx+ Undervoltage Test Enable	0x1	R/W
1	AINP_OV_TEST_EN		AINx+ Overvoltage Test Enable	0x1	R/W
0	REF_DET_TEST_EN		Reference Detect Test Enable	0x0	R/W

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GENERAL ERRORS REGISTER 1

Address: 0x059, Reset: 0x00, Name: GEN_ERR_REG_1

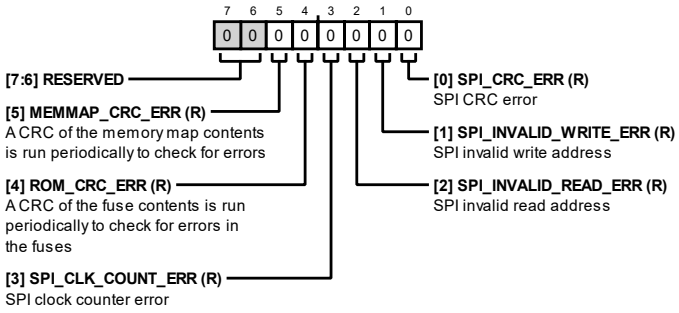

Table 133. Bit Descriptions for GEN_ERR_REG_1

Bits	Bit Name	Settings	Description	Reset	Access
5	MEMMAP_CRC_ERR		A CRC of the memory map contents is run periodically to check for errors	0x0	R
4	ROM_CRC_ERR		A CRC of the fuse contents is run periodically to check for errors in the fuses	0x0	R
3	SPI_CLK_COUNT_ERR		SPI clock counter error	0x0	R
2	SPI_INVALID_READ_ERR		SPI invalid read address	0x0	R
1	SPI_INVALID_WRITE_ERR		SPI invalid write address	0x0	R
0	SPI_CRC_ERR		SPI CRC error	0x0	R

GENERAL ERRORS REGISTER 1 ENABLE

Address: 0x05A, Reset: 0x3E, Name: GEN_ERR_REG_1_EN

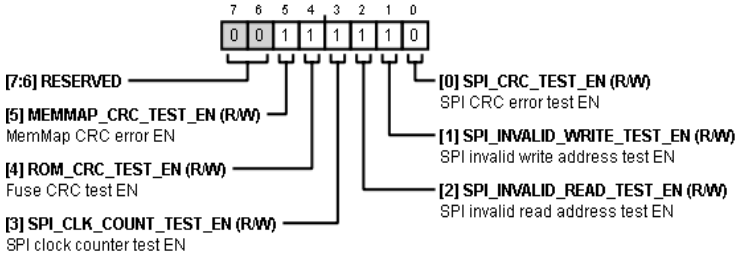

Table 134. Bit Descriptions for GEN_ERR_REG_1_EN

Bits	Bit Name	Settings	Description	Reset	Access
5	MEMMAP_CRC_TEST_EN		Memory Map CRC Test Enable	0x1	R/W
4	ROM_CRC_TEST_EN		Fuse CRC Test Enable	0x1	R/W
3	SPI_CLK_COUNT_TEST_EN		SPI Clock Counter Test Enable	0x1	R/W
2	SPI_INVALID_READ_TEST_EN		SPI Invalid Read Address Test Enable	0x1	R/W
1	SPI_INVALID_WRITE_TEST_EN		SPI Invalid Write Address Test Enable	0x1	R/W
0	SPI_CRC_TEST_EN		SPI CRC Error Test Enable	0x0	R/W

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GENERAL ERRORS REGISTER 2

Address: 0x05B, Reset: 0x00, Name: GEN_ERR_REG_2

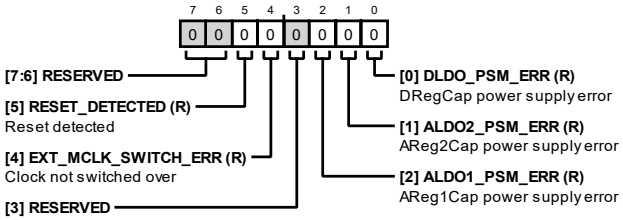

Table 135. Bit Descriptions for GEN_ERR_REG_2

Bits	Bit Name	Settings	Description	Reset	Access
5	RESET_DETECTED		Reset Detected	0x0	R
4	EXT_MCLK_SWITCH_ERR		Clock Not Switched Over	0x0	R
2	ALDO1_PSM_ERR		AREG1CAP Power Supply Error	0x0	R
1	ALDO2_PSM_ERR		AREG2CAP Power Supply Error	0x0	R
0	DLDO_PSM_ERR		DREGCAP Power Supply Error	0x0	R

GENERAL ERRORS REGISTER 2 ENABLE

Address: 0x05C, Reset: 0x3C, Name: GEN_ERR_REG_2_EN

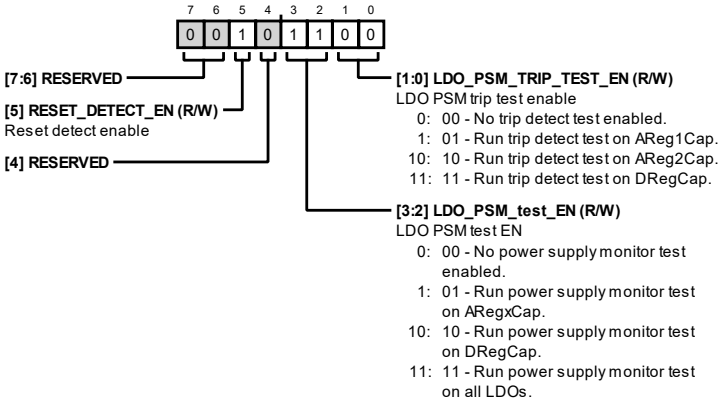

Table 136. Bit Descriptions for GEN_ERR_REG_2_EN

Bits	Bit Name	Settings	Description	Reset	Access
5	RESET_DETECT_EN		Reset Detect Enable	0x1	R/W
4	RESERVED		Reserved	0x1	R/W
[3:2]	LDO_PSM_TEST_EN		LDO PSM Test EN	0x3	R/W
		0	00—no power supply monitor test enabled.		
		1	01—run power supply monitor test on AREGxCAP		
		10	10—run power supply monitor test on DREGCAP		
		11	11—run power supply monitor test on all LDOs		
[1:0]	LDO_PSM_TRIP_TEST_EN		LDO PSM Trip Test Enable	0x0	R/W
		0	00—no trip detect test enabled		
		1	01—run trip detect test on AREG1CAP		
		10	10—run trip detect test on AREG2CAP		
		11	11—run trip detect test on DREGCAP		

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ERROR STATUS REGISTER 1

Address: 0x05D, Reset: 0x00, Name: STATUS_REG_1

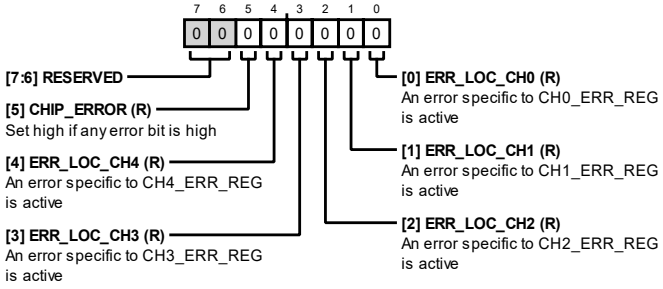

Table 137. Bit Descriptions for STATUS_REG_1

Bits	Bit Name	Settings	Description	Reset	Access
5	CHIP_ERROR		Set this bit high if any error bit is high	0x0	R
4	ERR_LOC_CH4		An error specific to CH4_ERR_REG is active	0x0	R
3	ERR_LOC_CH3		An error specific to CH3_ERR_REG is active	0x0	R
2	ERR_LOC_CH2		An error specific to CH2_ERR_REG is active	0x0	R
1	ERR_LOC_CH1		An error specific to CH1_ERR_REG is active	0x0	R
0	ERR_LOC_CH0		An error specific to CH0_ERR_REG is active	0x0	R

ERROR STATUS REGISTER 2

Address: 0x05E, Reset: 0x00, Name: STATUS_REG_2

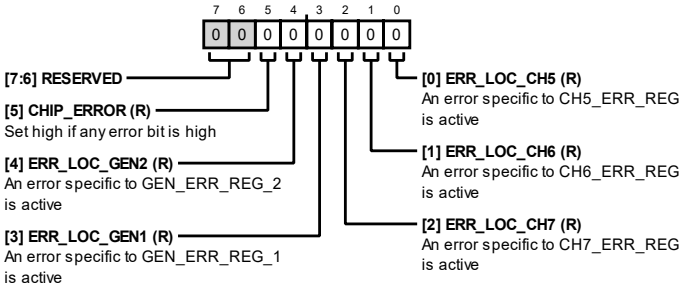

Table 138. Bit Descriptions for STATUS_REG_2

Bits	Bit Name	Settings	Description	Reset	Access
5	CHIP_ERROR		Set high if any error bit is high	0x0	R
4	ERR_LOC_GEN2		An error specific to GEN_ERR_REG_2 is active	0x0	R
3	ERR_LOC_GEN1		An error specific to GEN_ERR_REG_1 is active	0x0	R
2	ERR_LOC_CH7		An error specific to CH7_ERR_REG is active	0x0	R
1	ERR_LOC_CH6		An error specific to CH6_ERR_REG is active	0x0	R
0	ERR_LOC_CH5		An error specific to CH5_ERR_REG is active	0x0	R

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ERROR STATUS REGISTER 3

Address: 0x05F, Reset: 0x00, Name: STATUS_REG_3

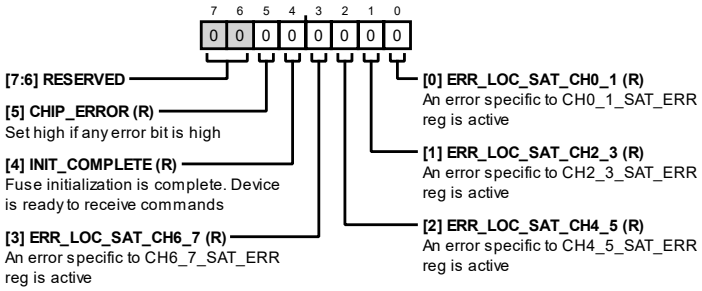

Table 139. Bit Descriptions for STATUS_REG_3

Bits	Bit Name	Settings	Description	Reset	Access
5	CHIP_ERROR		Set high if any error bit is high.	0x0	R
4	INIT_COMPLETE		Fuse initialization is complete. Device is ready to receive commands.	0x0	R
3	ERR_LOC_SAT_CH6_7		An error specific to CH6_7_SAT_ERR register is active.	0x0	R
2	ERR_LOC_SAT_CH4_5		An error specific to CH4_5_SAT_ERR register is active.	0x0	R
1	ERR_LOC_SAT_CH2_3		An error specific to CH2_3_SAT_ERR register is active.	0x0	R
0	ERR_LOC_SAT_CH0_1		An error specific to CH0_1_SAT_ERR register is active.	0x0	R

DECIMATION RATE (N) MSB REGISTER

Address: 0x060, Reset: 0x00, Name: SRC_N_MSB

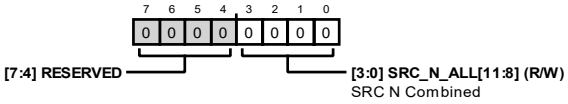

Table 140. Bit Descriptions for SRC_N_MSB

Bits	Bit Name	Settings	Description	Reset	Access
[3:0]	SRC_N_ALL[11:8]		SRC N Combined	0x0	R/W

DECIMATION RATE (N) LSB REGISTER

Address: 0x061, Reset: 0x80, Name: SRC_N_LSB

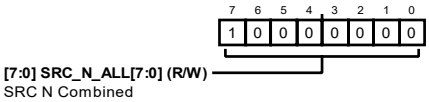

Table 141. Bit Descriptions for SRC_N_LSB

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	SRC_N_ALL[7:0]		SRC N Combined	0x0	R/W

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DECIMATION RATE (IF) MSB REGISTER

Address: 0x062, Reset: 0x00, Name: SRC_IF_MSB

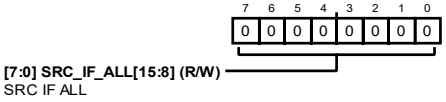

Table 142. Bit Descriptions for SRC_IF_MSB

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	SRC_IF_ALL[15:8]		SRC IF All	0x0	R/W

DECIMATION RATE (IF) LSB REGISTER

Address: 0x063, Reset: 0x00, Name: SRC_IF_LSB

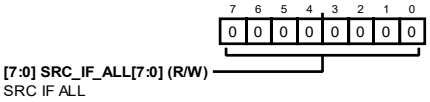

Table 143. Bit Descriptions for SRC_IF_LSB

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	SRC_IF_ALL[7:0]		SRC IF All	0x0	R/W

SRC LOAD SOURCE AND LOAD UPDATE REGISTER

Address: 0x064, Reset: 0x00, Name: SRC_UPDATE

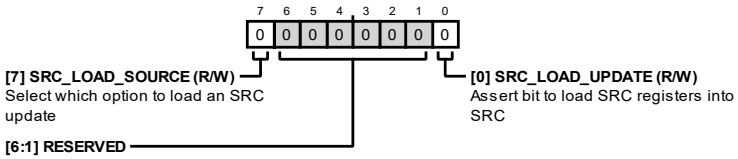

Table 144. Bit Descriptions for SRC_UPDATE

Bits	Bit Name	Settings	Description	Reset	Access
7	SRC_LOAD_SOURCE		Selects which option to load an SRC update	0x0	R/W
0	SRC_LOAD_UPDATE		Asserts bit to load SRC registers into SRC	0x0	R/W

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OUTLINE DIMENSIONS

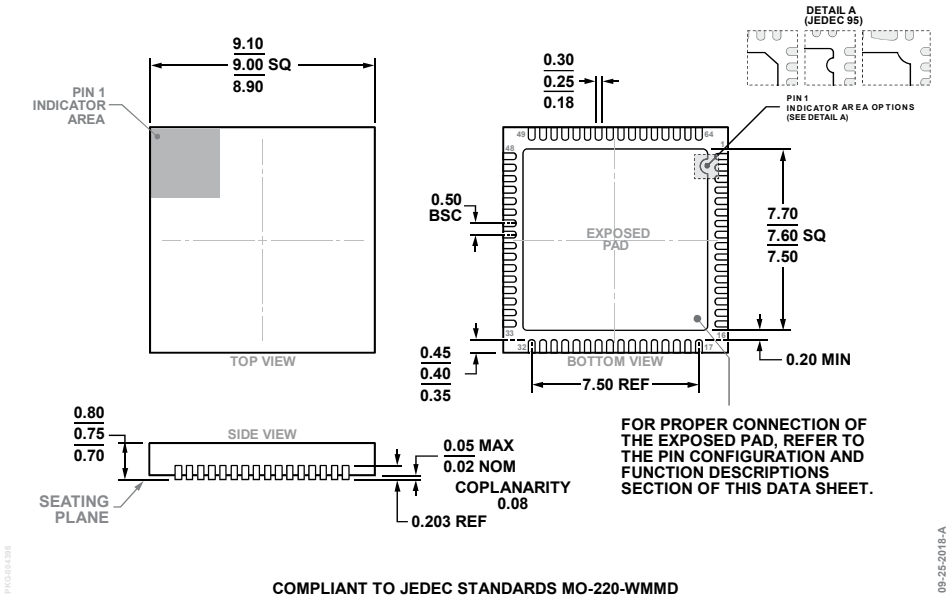

Figure 124. 64-Lead Lead Frame Chip Scale Package [LFCSP]
9 mm × 9 mm Body and 0.75 mm Package Height
(CP-64-15)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD7779ACPZ	−40°C to +125°C	64-Lead Lead Frame Chip Scale Package [LFCSP]	CP-64-15
AD7779ACPZ-RL	−40°C to +125°C	64-Lead Lead Frame Chip Scale Package [LFCSP]	CP-64-15
EVAL-AD7779FMCZ		Evaluation Board	
EVAL-SDP-CH1Z		SDP Controller Board	

[1] Z = RoHS Compliant Part.

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