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## REVISION HISTORY

**12/12—Rev. 0 to Rev. A**

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**10/06—Revision 0: Initial Version**

# SPECIFICATIONS

AVDD = DVDD = 5 V; OVDD = 2.7 V to 5.5 V; VCC = 15 V; VEE = −15 V; $V_{REF}$ = 5 V; all specifications $T_{MIN}$ to $T_{MAX}$, unless otherwise noted.

**Table 2.**

| Parameter | Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| RESOLUTION | | 16 | | | Bits |
| ANALOG INPUT | | | | | |
| Voltage Range, $V_{IN}$ | $V_{IN+} - V_{IN-}$ = 0 V to 5 V | −0.1 | | +5.1 | V |
| | $V_{IN+} - V_{IN-}$ = 0V to 10 V | −0.1 | | +10.1 | V |
| | $V_{IN+} - V_{IN-}$ = ±5 V | −5.1 | | +5.1 | V |
| | $V_{IN+} - V_{IN-}$ = ±10 V | −10.1 | | +10.1 | V |
| | $V_{IN-}$ to AGND | −0.1 | | +0.1 | V |
| Analog Input CMRR | $f_{IN}$ = 100 kHz | | 75 | | dB |
| Input Current | $V_{IN}$ = ±5 V, ±10 V @ 750 kSPS | | 220[1] | | µA |
| Input Impedance | See Analog Inputs section | | | | |
| THROUGHPUT SPEED | | | | | |
| Complete Cycle | In warp mode | | | 1.33 | µs |
| Throughput Rate | In warp mode | 1 | | 750[2] | kSPS |
| Time Between Conversions | In warp mode | | | 1 | ms |
| Complete Cycle | In normal mode | | | 1.67 | µs |
| Throughput Rate | In normal mode | 0 | | 600 | kSPS |
| Complete Cycle | In impulse mode | | | 2 | µs |
| Throughput Rate | In impulse mode | 0 | | 500 | kSPS |
| DC ACCURACY | | | | | |
| Integral Linearity Error[3] | | −1.5 | ±0.75 | +1.5 | LSB[4] |
| No Missing Codes[3] | | 16 | | | Bits |
| Differential Linearity Error[3] | | −1 | | +1.5 | LSB |
| Transition Noise | | | 0.55 | | LSB |
| Zero Error (Unipolar or Bipolar) | | −35 | | +35 | LSB |
| Zero Error Temperature Drift | | | ±1 | | ppm/°C |
| Bipolar Full-Scale Error | | −50 | | +50 | LSB |
| Unipolar Full-Scale Error | | −70 | | +70 | LSB |
| Full-Scale Error Temperature Drift | | | ±1 | | ppm/°C |
| Power Supply Sensitivity | AVDD = 5 V ± 5% | | 3 | | LSB |
| AC ACCURACY | | | | | |
| Dynamic Range | $V_{IN}$ = 0 V to 5 V, $f_{IN}$ = 2 kHz, −60 dB | 92.5 | 93.5 | | dB[5] |
| | $V_{IN}$ = 0 V to 10 V, ±5 V, $f_{IN}$ = 2 kHz, −60 dB | | 94 | | dB |
| | $V_{IN}$ = ±10 V, $f_{IN}$ = 2 kHz, −60 dB | | 94.5 | | dB |
| Signal-to-Noise Ratio | $V_{IN}$ = 0 V to 5 V, 0 V to 10 V, $f_{IN}$ = 2 kHz | 92 | 93 | | dB |
| | $V_{IN}$ = ±5 V, ±10 V, $f_{IN}$ = 2 kHz | | 94 | | dB |
| Signal-to-(Noise + Distortion) (SINAD) | $V_{IN}$ = ±5 V, $f_{IN}$ = 2 kHz | | 92.5 | | dB |
| | $V_{IN}$ = 0 V to 10 V, ±5 V, $f_{IN}$ = 2 kHz | | 93 | | dB |
| | $V_{IN}$ = ±10 V, $f_{IN}$ = 2 kHz | | 93.5 | | dB |
| Total Harmonic Distortion | $f_{IN}$ = 2 kHz | | −107 | | dB |
| Spurious-Free Dynamic Range | $f_{IN}$ = 2 kHz | | 107 | | dB |
| −3 dB Input Bandwidth | $V_{IN}$ = 0 V to 5 V | | 45 | | MHz |
| Aperture Delay | | | 2 | | ns |
| Aperture Jitter | | | 5 | | ps rms |
| Transient Response | Full-scale step | | | 500 | ns |
| INTERNAL REFERENCE | PDREF = PDBUF = low | | | | |
| Output Voltage | REF @ 25°C | 4.965 | 5.000 | 5.035 | V |
| Temperature Drift | −40°C to +85°C | | ±3 | | ppm/°C |
| Line Regulation | AVDD = 5 V ± 5% | | ±15 | | ppm/V |
| Long-Term Drift | 1000 hours | | 50 | | ppm |
| Turn-On Settling Time | $C_{REF}$ = 22 µF | | 10 | | ms |

| Parameter | Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| REFERENCE BUFFER | PDREF = high | | | | |
| REFBUFIN Input Voltage Range | | 2.4 | 2.5 | 2.6 | V |
| EXTERNAL REFERENCE | PDREF = PDBUF = high | | | | |
| Voltage Range | REF | 4.75 | 5 | AVDD + 0.1 | V |
| Current Drain | 750 kSPS throughput | | 250 | | µA |
| TEMPERATURE PIN | | | | | |
| Voltage Output | @ 25°C | | 311 | | mV |
| Temperature Sensitivity | | | 1 | | mV/°C |
| Output Resistance | | | 4.33 | | kΩ |
| DIGITAL INPUTS | | | | | |
| Logic Levels | | | | | |
| $V_{IL}$ | | −0.3 | | +0.6 | V |
| $V_{IH}$ | | 2.1 | | OVDD + 0.3 | V |
| $I_{IL}$ | | −1 | | +1 | µA |
| $I_{IH}$ | | −1 | | +1 | µA |
| DIGITAL OUTPUTS | | | | | |
| Data Format | Parallel or serial 16-bit | | | | |
| Pipeline Delay[6] | | | | | |
| $V_{OL}$ | $I_{SINK}$ = 500 µA | | | 0.4 | V |
| $V_{OH}$ | $I_{SOURCE}$ = −500 µA | OVDD − 0.6 | | | V |
| POWER SUPPLIES | | | | | |
| Specified Performance | | | | | |
| AVDD | | 4.75[7] | 5 | 5.25 | V |
| DVDD | | 4.75 | 5 | 5.25 | V |
| OVDD | | 2.7 | | 5.25 | V |
| VCC | | 7 | 15 | 15.75 | V |
| VEE | | −15.75 | −15 | 0 | V |
| Operating Current[8, 9] | @ 750 kSPS throughput | | | | |
| AVDD | | | | | |
| With Internal Reference | | | 19.5 | | mA |
| With Internal Reference Disabled | | | 18 | | mA |
| DVDD | | | 6.5 | | mA |
| OVDD | | | 0.5 | | mA |
| VCC | VCC = 15 V, with internal reference buffer | | 3 | | mA |
| | VCC = 15 V | | 2.3 | | mA |
| VEE | VEE = −15 V | | 2 | | mA |
| Power Dissipation | @ 750 kSPS throughput | | | | |
| With Internal Reference | PDREF = PDBUF = low | | 205 | 230 | mW |
| With Internal Reference Disabled | PDREF = PDBUF = high | | 190 | 210 | mW |
| In Power-Down Mode[10] | PD = high | | 10 | | µW |
| TEMPERATURE RANGE[11] | | | | | |
| Specified Performance | $T_{MIN}$ to $T_{MAX}$ | −40 | | +85 | °C |

[1] With $V_{IN}$ = 0 V to 5 V or 0 V to 10 V ranges, the input current is typically 70 µA. In all input ranges, the input current scales with throughput. See the Analog Inputs section.
[2] All specified performance is guaranteed up to 750 kSPS throughout, however throughputs up to 900 kSPS can be used with some linearity performance degradation.
[3] Linearity is tested using endpoints, not best fit. All linearity is tested with an external 5 V reference.
[4] LSB means least significant bit. All specifications in LSB do not include the error contributed by the reference.
[5] All specifications in decibels are referred to a full-scale range input, FSR. Tested with an input signal at 0.5 dB below full-scale, unless otherwise specified.
[6] Conversion results are available immediately after completed conversion.
[7] 4.75 V or $V_{REF}$ − 0.1 V, whichever is larger.
[8] Tested in parallel reading mode.
[9] With internal reference, PDREF = PDBUF = low; with internal reference disabled, PDREF = PDBUF = high. With internal reference buffer, PDBUF = low.
[10] With all digital inputs forced to OVDD.
[11] Consult sales for extended temperature range.

## TIMING SPECIFICATIONS

AVDD = DVDD = 5 V; OVDD = 2.7 V to 5.5 V; VCC = 15 V; VEE = −15 V; $V_{REF}$ = 5 V; all specifications $T_{MIN}$ to $T_{MAX}$, unless otherwise noted.

**Table 3.**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| CONVERSION AND RESET (See Figure 33 and Figure 34) | | | | | |
| Convert Pulse Width | $t_1$ | 10 | | | ns |
| Time Between Conversions | $t_2$ | | | | |
| Warp Mode/Normal Mode/Impulse Mode[1] | | 1.33/1.67/2 | | | µs |
| $\overline{CNVST}$ Low to BUSY High Delay | $t_3$ | | | 35 | ns |
| BUSY High All Modes (Except Master Serial Read After Convert) | $t_4$ | | | | |
| Warp Mode/Normal Mode/Impulse Mode | | | | 950/1250/1450 | ns |
| Aperture Delay | $t_5$ | | 2 | | ns |
| End of Conversion to BUSY Low Delay | $t_6$ | 10 | | | ns |
| Conversion Time | $t_7$ | | | | |
| Warp Mode/Normal Mode/Impulse Mode | | | | 950/1250/1450 | ns |
| Acquisition Time | $t_8$ | | | | |
| Warp Mode/Normal Mode/Impulse Mode | | 380 | | | ns |
| RESET Pulse Width | $t_9$ | 10 | | | ns |
| PARALLEL INTERFACE MODES (See Figure 35 and Figure 37) | | | | | |
| $\overline{CNVST}$ Low to DATA Valid Delay | $t_{10}$ | | | | |
| Warp Mode/Normal Mode/Impulse Mode | | | | 910/1160/1410 | ns |
| DATA Valid to BUSY Low Delay | $t_{11}$ | 20 | | | ns |
| Bus Access Request to DATA Valid | $t_{12}$ | | | 40 | ns |
| Bus Relinquish Time | $t_{13}$ | 2 | | 15 | ns |
| MASTER SERIAL INTERFACE MODES[2] (See Figure 39 and Figure 40) | | | | | |
| $\overline{CS}$ Low to SYNC Valid Delay | $t_{14}$ | | | 10 | ns |
| $\overline{CS}$ Low to Internal SDCLK Valid Delay[2] | $t_{15}$ | | | 10 | ns |
| $\overline{CS}$ Low to SDOUT Delay | $t_{16}$ | | | 10 | ns |
| $\overline{CNVST}$ Low to SYNC Delay, Read During Convert | $t_{17}$ | | | | |
| Warp Mode/Normal Mode/Impulse Mode | | | 65/315/560 | | ns |
| SYNC Asserted to SDCLK First Edge Delay | $t_{18}$ | 3 | | | ns |
| Internal SDCLK Period[3] | $t_{19}$ | 30 | | 45 | ns |
| Internal SDCLK High[3] | $t_{20}$ | 15 | | | ns |
| Internal SDCLK Low[3] | $t_{21}$ | 10 | | | ns |
| SDOUT Valid Setup Time[3] | $t_{22}$ | 4 | | | ns |
| SDOUT Valid Hold Time[3] | $t_{23}$ | 5 | | | ns |
| SDCLK Last Edge to SYNC Delay[3] | $t_{24}$ | 5 | | | ns |
| $\overline{CS}$ High to SYNC HI-Z | $t_{25}$ | | | 10 | ns |
| $\overline{CS}$ High to Internal SDCLK HI-Z | $t_{26}$ | | | 10 | ns |
| $\overline{CS}$ High to SDOUT HI-Z | $t_{27}$ | | | 10 | ns |
| BUSY High in Master Serial Read After Convert[3] | $t_{28}$ | | See Table 4 | | |
| $\overline{CNVST}$ Low to SYNC Delay, Read After Convert | | | | | |
| Warp Mode/Normal Mode/Impulse Mode | $t_{29}$ | | 830/1070/1310 | | ns |
| SYNC Deasserted to BUSY Low Delay | $t_{30}$ | | 25 | | ns |

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| SLAVE SERIAL/SERIAL CONFIGURATION INTERFACE MODES[2] (See Figure 42, Figure 43, and Figure 45) | | | | | |
| External SDCLK, SCCLK Setup Time | $t_{31}$ | 5 | | | ns |
| External SDCLK Active Edge to SDOUT Delay | $t_{32}$ | 2 | | 18 | ns |
| SDIN/SCIN Setup Time | $t_{33}$ | 5 | | | ns |
| SDIN/SCIN Hold Time | $t_{34}$ | 5 | | | ns |
| External SDCLK/SCCLK Period | $t_{35}$ | 25 | | | ns |
| External SDCLK/SCCLK High | $t_{36}$ | 10 | | | ns |
| External SDCLK/SCCLK Low | $t_{37}$ | 10 | | | ns |

[1] In warp mode only, the time between conversions is 1 ms; otherwise, there is no required maximum time.
[2] In serial interface modes, the SDSYNC, SDSCLK, and SDOUT timings are defined with a maximum load $C_L$ of 10 pF; otherwise, the load is 60 pF maximum.
[3] In serial master read during convert mode. See Table 4 for serial master read after convert mode.

**Table 4. Serial Clock Timings in Master Read After Convert Mode**

| DIVSCLK[1] | | 0 | 0 | 1 | 1 | |
|---|---|---|---|---|---|---|
| DIVSCLK[0] | Symbol | 0 | 1 | 0 | 1 | Unit |
| SYNC to SDCLK First Edge Delay Minimum | $t_{18}$ | 3 | 20 | 20 | 20 | ns |
| Internal SDCLK Period Minimum | $t_{19}$ | 30 | 60 | 120 | 240 | ns |
| Internal SDCLK Period Maximum | $t_{19}$ | 45 | 90 | 180 | 360 | ns |
| Internal SDCLK High Minimum | $t_{20}$ | 15 | 30 | 60 | 120 | ns |
| Internal SDCLK Low Minimum | $t_{21}$ | 10 | 25 | 55 | 115 | ns |
| SDOUT Valid Setup Time Minimum | $t_{22}$ | 4 | 20 | 20 | 20 | ns |
| SDOUT Valid Hold Time Minimum | $t_{23}$ | 5 | 8 | 35 | 90 | ns |
| SDCLK Last Edge to SYNC Delay Minimum | $t_{24}$ | 5 | 7 | 35 | 90 | ns |
| BUSY High Width Maximum | $t_{28}$ | | | | | |
| Warp Mode | | 1.65 | 2.35 | 3.75 | 6.53 | µs |
| Normal Mode | | 1.9 | 2.6 | 4.00 | 6.78 | µs |
| Impulse Mode | | 2.15 | 2.85 | 4.25 | 7.03 | µs |

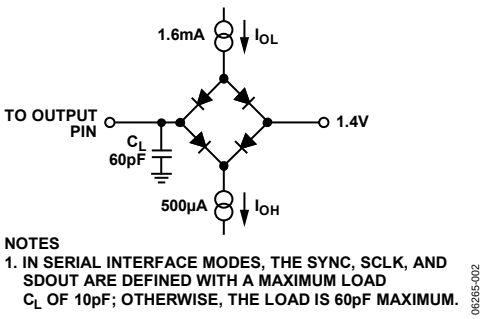



*Figure 2. Load Circuit for Digital Interface Timing, SDOUT, SYNC, and SCLK Outputs, $C_L$ = 10 pF*

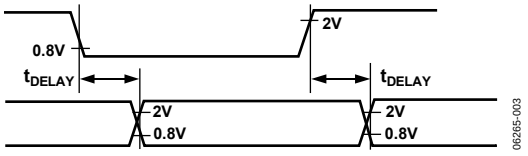



*Figure 3. Voltage Reference Levels for Timing*

# ABSOLUTE MAXIMUM RATINGS

**Table 5.**

| Parameter | Rating |
|---|---|
| Analog Inputs/Outputs | |
| IN+[1], IN−[1] to AGND | VEE − 0.3 V to VCC + 0.3 V |
| REF, REFBUFIN, TEMP, REFGND to AGND | AVDD + 0.3 V to AGND − 0.3 V |
| Ground Voltage Differences | |
| AGND, DGND, OGND | ±0.3 V |
| Supply Voltages | |
| AVDD, DVDD, OVDD | −0.3 V to +7 V |
| AVDD to DVDD, AVDD to OVDD | ±7 V |
| DVDD to OVDD | ±7 V |
| VCC to AGND, DGND | −0.3 V to +16.5 |
| VEE to GND | +0.3 V to −16.5 |
| Digital Inputs | −0.3 V to OVDD + 0 .3 V |
| PDREF, PDBUF[2] | ±20 mA |
| Internal Power Dissipation[3] | 700 mW |
| Internal Power Dissipation[4] | 2.5 W |
| Junction Temperature | 125°C |
| Storage Temperature Range | −65°C to +125°C |

[1] See the Analog Inputs section.
[2] See the Voltage Reference Input section.
[3] Specification is for the device in free air: 48-Lead LFQP; $\theta_{JA}$ = 91°C/W, $\theta_{JC}$ = 30°C/W.
[4] Specification is for the device in free air: 48-Lead LFCSP; $\theta_{JA}$ = 26°C/W.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ESD CAUTION

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

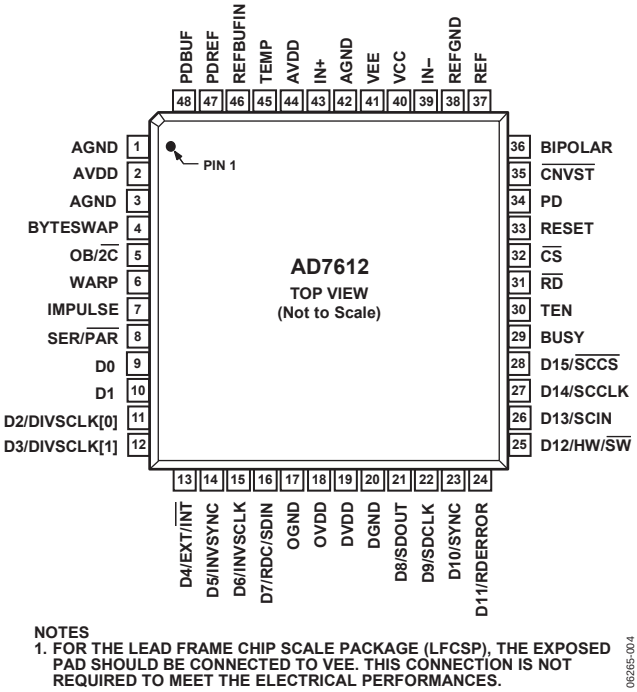



*Figure 4. Pin Configuration*

**Table 6. Pin Function Descriptions**

| Pin No. | Mnemonic | Type[1] | Description |
|---|---|---|---|
| 1, 3, 42 | AGND | P | Analog Power Ground Pins. Ground reference point for all analog I/O. All analog I/O should be referenced to AGND and should be connected to the analog ground plane of the system. In addition, the AGND, DGND, and OGND voltages should be at the same potential. |
| 2, 44 | AVDD | P | Analog Power Pins. Nominally 4.75 V to 5.25 V and decoupled with 10 µF and 100 nF capacitors. |
| 4 | BYTESWAP | DI | Parallel Mode Selection (8-Bit/16-Bit). When high, the LSB is output on D[15:8] and the MSB is output on D[7:0]; when low, the LSB is output on D[7:0] and the MSB is output on D[15:8]. |
| 5 | OB/$\overline{2C}$ | DI[2] | Straight Binary/Binary Twos Complement Output. When high, the digital output is straight binary. When low, the MSB is inverted resulting in a twos complement output from its internal shift register. |
| 6 | WARP | DI[2] | Conversion Mode Selection. Used in conjunction with the IMPULSE input per the following:<br>**Conversion Mode / WARP / IMPULSE**<br>Normal / Low / Low<br>Impulse / Low / High<br>Warp / High / Low<br>Normal / High / High<br>See the Modes of Operation section for a more detailed description. |
| 7 | IMPULSE | DI[2] | Conversion Mode Selection. See the WARP pin description in the previous row of this table. See the Modes of Operation section for a more detailed description. |
| 8 | SER/$\overline{PAR}$ | DI | Serial/Parallel Selection Input.<br>When SER/$\overline{PAR}$ = low, the parallel mode is selected.<br>When SER/$\overline{PAR}$ = high, the serial modes are selected. Some bits of the data bus are used as a serial port and the remaining data bits are high impedance outputs. |
| 9, 10 | D[0:1] | DO | Bit 0 and Bit 1 of the parallel port data output bus. These pins are always outputs regardless of the state of SER/$\overline{PAR}$. |

| Pin No. | Mnemonic | Type[1] | Description |
|---|---|---|---|
| 11, 12 | D[2:3] or DIVSCLK[0:1] | DI/O | In parallel mode, these outputs are used as Bit 2 and Bit 3 of the parallel port data output bus.<br>Serial Data Division Clock Selection. In serial master read after convert mode (SER/$\overline{PAR}$ = high, EXT/$\overline{INT}$ = low, RDC/SDIN = low) these inputs can be used to slow down the internally generated serial data clock that clocks the data output. In other serial modes, these pins are high impedance outputs. |
| 13 | D4 or EXT/$\overline{INT}$ | DI/O | In parallel mode, this output is used as Bit 4 of the parallel port data output bus.<br>Serial Data Clock Source Select. In serial mode, this input is used to select the internally generated (master) or external (slave) serial data clock for the AD7612 output data.<br>When EXT/$\overline{INT}$ = low, master mode; the internal serial data clock is selected on SDCLK output.<br>When EXT/$\overline{INT}$ = high, slave mode; the output data is synchronized to an external clock signal (gated by $\overline{CS}$) connected to the SDCLK input. |
| 14 | D5 or INVSYNC | DI/O | In parallel mode, this output is used as Bit 5 of the parallel port data output bus.<br>Serial Data Invert Sync Select. In serial master mode (SER/$\overline{PAR}$ = high, EXT/$\overline{INT}$ = low). This input is used to select the active state of the SYNC signal.<br>When INVSYNC = low, SYNC is active high.<br>When INVSYNC = high, SYNC is active low. |
| 15 | D6 or INVSCLK | DI/O | In parallel mode, this output is used as Bit 6 of the parallel port data output bus.<br>In all serial modes, invert SDCLK/SCCLK select. This input is used to invert both SDCLK and SCCLK.<br>When INVSCLK = low, the rising edge of SDCLK/SCCLK are used.<br>When INVSCLK = high, the falling edge of SDCLK/SCCLK are used. |
| 16 | D7 or RDC or | DI/O | In parallel mode, this output is used as Bit 7 of the parallel port data output bus.<br>Serial Data Read During Convert. In serial master mode (SER/$\overline{PAR}$ = high, EXT/$\overline{INT}$ = low) RDC is used to select the read mode. Refer to the Master Serial Interface section.<br>When RDC = low, the current result is read after conversion. Note the maximum throughput is not attainable in this mode.<br>When RDC = high, the previous conversion result is read during the current conversion. |
| | SDIN | | Serial Data In. In serial slave mode (SER/$\overline{PAR}$ = high EXT/$\overline{INT}$ = high) SDIN can be used as a data input to daisy-chain the conversion results from two or more ADCs onto a single SDOUT line. The digital data level on SDIN is output on SDOUT with a delay of 16 SDCLK periods after the initiation of the read sequence. |
| 17 | OGND | P | Input/Output Interface Digital Power Ground. Ground reference point for digital outputs. Should be connected to the system digital ground ideally at the same potential as AGND and DGND. |
| 18 | OVDD | P | Input/Output Interface Digital Power. Nominally at the same supply as the supply of the host interface 2.5 V, 3 V, or 5 V and decoupled with 10 µF and 100 nF capacitors. |
| 19 | DVDD | P | Digital Power. Nominally at 4.75 V to 5.25 V and decoupled with 10 µF and 100 nF capacitors. Can be supplied from AVDD. |
| 20 | DGND | P | Digital Power Ground. Ground reference point for digital outputs. Should be connected to system digital ground ideally at the same potential as AGND and OGND. |
| 21 | D8 or SDOUT | DO | In parallel mode, this output is used as Bit 8 of the parallel port data output bus.<br>Serial Data output. In all serial modes this pin is used as the serial data output synchronized to SDCLK. Conversion results are stored in an on-chip register. The AD7612 provides the conversion result, MSB first, from its internal shift register. The data format is determined by the logic level of OB/$\overline{2C}$.<br>When EXT/$\overline{INT}$ = low, (master mode) SDOUT is valid on both edges of SDCLK.<br>When EXT/$\overline{INT}$ = high, (slave mode).<br>When INVSCLK = low, SDOUT is updated on SDCLK rising edge.<br>When INVSCLK = high, SDOUT is updated on SDCLK falling edge. |
| 22 | D9 or SDCLK | DI/O | In parallel mode, this output is used as Bit 9 of the parallel port data output bus.<br>Serial Data Clock. In all serial modes, this pin is used as the serial data clock input or output, dependent on the logic state of the EXT/$\overline{INT}$ pin. The active edge where the data SDOUT is updated depends on the logic state of the INVSCLK pin. |

| Pin No. | Mnemonic | Type[1] | Description |
|---|---|---|---|
| 23 | D10 or SYNC | DO | In parallel mode, this output is used as Bit 10 of the parallel port data output bus.<br>Serial Data Frame Synchronization. In serial master mode (SER/$\overline{PAR}$ = high, EXT/$\overline{INT}$= low), this output is used as a digital output frame synchronization for use with the internal data clock.<br>When a read sequence is initiated and INVSYNC = low, SYNC is driven high and remains high while the SDOUT output is valid.<br>When a read sequence is initiated and INVSYNC = high, SYNC is driven low and remains low while the SDOUT output is valid. |
| 24 | D11 or RDERROR | DO | In parallel mode, this output is used as Bit 11 of the parallel port data output bus.<br>Serial Data Read Error. In serial slave mode (SER/$\overline{PAR}$ = high, EXT/$\overline{INT}$ = high), this output is used as an incomplete data read error flag. If a data read is started and not completed when the current conversion is complete, the current data is lost and RDERROR is pulsed high. |
| 25 | D12 or HW/$\overline{SW}$ | DI/O | In parallel mode, this output is used as Bit 12 of the parallel port data output bus.<br>Serial Configuration Hardware/Software Select. In serial mode, this input is used to configure the AD7612 by hardware or software. See the Hardware Configuration section and Software Configuration section.<br>When HW/$\overline{SW}$ = low, the AD7612 is configured through software using the serial configuration register.<br>When HW/$\overline{SW}$ = high, the AD7612 is configured through dedicated hardware input pins. |
| 26 | D13 or SCIN | DI/O | In parallel mode, this output is used as Bit 13 of the parallel port data output bus.<br>Serial Configuration Data Input. In serial software configuration mode (SER/$\overline{PAR}$ = high, HW/$\overline{SW}$ = low) this input is used to serially write in, MSB first, the configuration data into the serial configuration register. The data on this input is latched with SCCLK. See the Software Configuration section. |
| 27 | D14 or SCCLK | DI/O | In parallel mode, this output is used as Bit 14 of the parallel port data output bus.<br>Serial Configuration Clock. In serial software configuration mode (SER/$\overline{PAR}$ = high, HW/$\overline{SW}$ = low) this input is used to clock in the data on SCIN. The active edge where the data SCIN is updated depends on the logic state of the INVSCLK pin. See the Software Configuration section. |
| 28 | D15 or $\overline{SCCS}$ | DI/O | In parallel mode, this output is used as Bit 15 of the parallel port data output bus.<br>Serial Configuration Chip Select. In serial software configuration mode (SER/$\overline{PAR}$ = high, HW/$\overline{SW}$ = low) this input enables the serial configuration port. See the Software Configuration section. |
| 29 | BUSY | DO | Busy Output. Transitions high when a conversion is started, and remains high until the conversion is complete and the data is latched into the on-chip shift register. The falling edge of BUSY can be used as a data ready clock signal. Note that in master read after convert mode (SER/$\overline{PAR}$ = high, EXT/$\overline{INT}$ = low, RDC = low) the busy time changes according to Table 4. |
| 30 | TEN | DI[2] | Input Range Select. Used in conjunction with BIPOLAR per the following:<br>**Input Range / BIPOLAR / TEN**<br>0 V to 5 V / Low / Low<br>0 V to 10 V / Low / High<br>±5 V / High / Low<br>±10 V / High / High |
| 31 | $\overline{RD}$ | DI | Read Data. When $\overline{CS}$ and $\overline{RD}$ are both low, the interface parallel or serial output bus is enabled. |
| 32 | $\overline{CS}$ | DI | Chip Select. When $\overline{CS}$ and $\overline{RD}$ are both low, the interface parallel or serial output bus is enabled. $\overline{CS}$ is also used to gate the external clock in slave serial mode (not used for serial programmable port). |
| 33 | RESET | DI | Reset Input. When high, reset the AD7612. Current conversion, if any, is aborted. The falling edge of RESET resets the data outputs to all zero's (with OB/$\overline{2C}$ = high) and clears the configuration register. See the Digital Interface section. If not used, this pin can be tied to OGND. |
| 34 | PD | DI[2] | Power-Down Input. When PD = high, power down the ADC. Power consumption is reduced and conversions are inhibited after the current one is completed. The digital interface remains active during power down. |
| 35 | $\overline{CNVST}$ | DI | Conversion Start. A falling edge on $\overline{CNVST}$ puts the internal sample-and-hold into the hold state and initiates a conversion. |
| 36 | BIPOLAR | DI[2] | Input Range Select. See description for Pin 30. |

| Pin No. | Mnemonic | Type[1] | Description |
|---|---|---|---|
| 37 | REF | AI/O | Reference Input/Output.<br>When PDREF/PDBUF = low, the internal reference and buffer are enabled, producing 5 V on this pin.<br>When PDREF/PDBUF = high, the internal reference and buffer are disabled, allowing an externally supplied voltage reference up to AVDD volts. Decoupling with at least a 22 µF is required with or without the internal reference and buffer. See the Reference Decoupling section. |
| 38 | REFGND | AI | Reference Input Analog Ground. Connected to analog ground plane. |
| 39 | IN− | AI | Analog Input Ground Sense. Should be connected to the analog ground plane or to a remote sense ground. |
| 40 | VCC | P | High Voltage Positive Supply. Normally +7 V to +15 V. |
| 41 | VEE | P | High Voltage Negative Supply. Normally 0 V to −15 V (0 V in unipolar ranges). |
| 43 | IN+ | AI | Analog Input. Referenced to IN−. |
| 45 | TEMP | AO | Temperature Sensor Analog Output. |
| 46 | REFBUFIN | AI | Reference Buffer Input. When using an external reference with the internal reference buffer (PDBUF = low, PDREF = high), applying 2.5 V on this pin produces 5 V on the REF pin. See the Voltage Reference Input section. |
| 47 | PDREF | DI | Internal Reference Power-Down Input.<br>When low, the internal reference is enabled.<br>When high, the internal reference is powered down, and an external reference must be used. |
| 48 | PDBUF | DI | Internal Reference Buffer Power-Down Input.<br>When low, the buffer is enabled (must be low when using internal reference).<br>When high, the buffer is powered-down. |
| 49 | EPAD[3] | NC | Exposed Pad. The exposed pad is not connected internally. It is recommended that the pad be soldered to VEE. |

[1] AI = analog input; AI/O = bidirectional analog; AO = analog output; DI = digital input; DI/O = bidirectional digital; DO = digital output; P = power.

[2] In serial configuration mode (SER/$\overline{\text{PAR}}$ = high, HW/$\overline{\text{SW}}$ = low), this input is programmed with the serial configuration register and this pin is a don't care. See the Hardware Configuration section and Software Configuration section.

[3] LFCSP_VQ package only.

# TYPICAL PERFORMANCE CHARACTERISTICS

AVDD = DVDD = 5 V; OVDD = 5 V; VCC = 15 V; VEE = −15 V; $V_{REF}$ = 5 V; $T_A$ = 25°C.

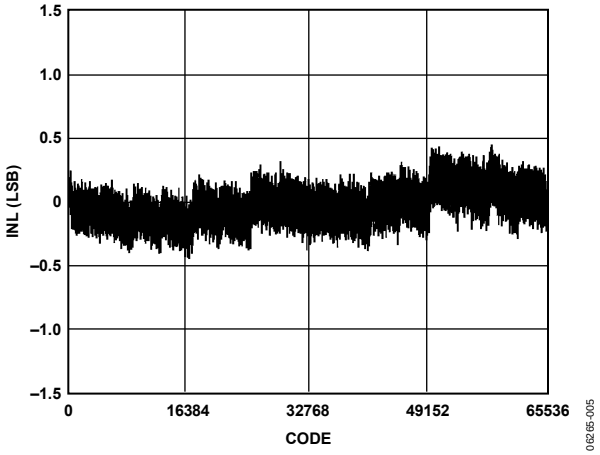



Figure 5. Integral Nonlinearity vs. Code

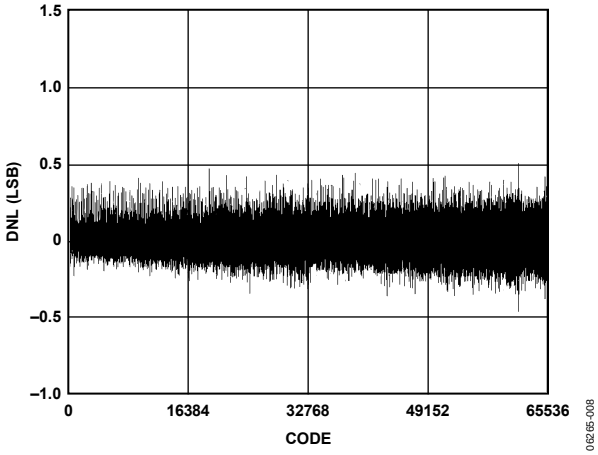



Figure 8. Differential Nonlinearity vs. Code

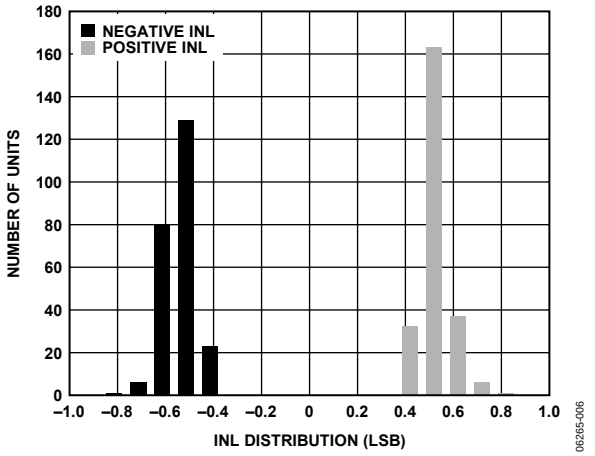



Figure 6. Integral Nonlinearity Distribution (239 Devices)

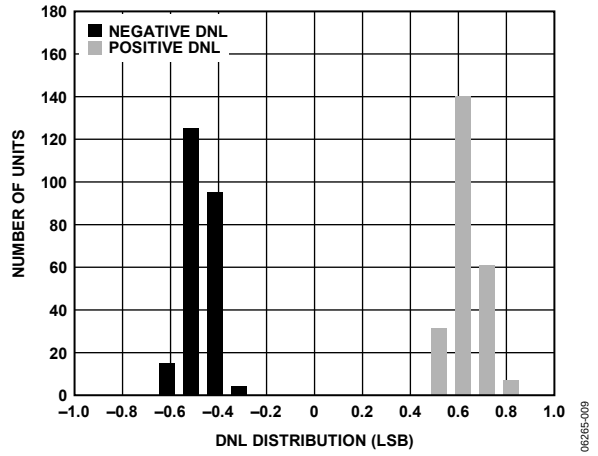



Figure 9. Differential Nonlinearity Distribution (239 Devices)

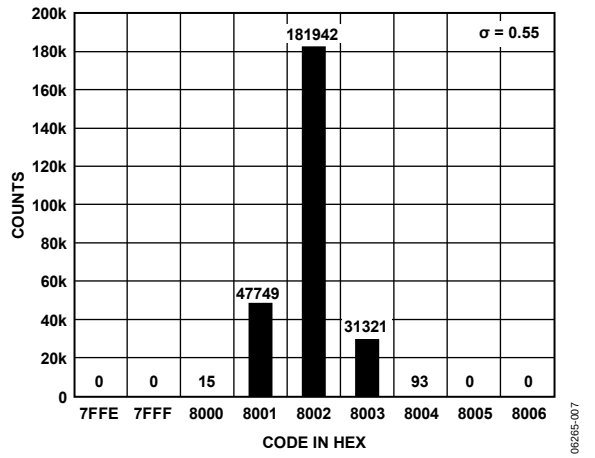



Figure 7. Histogram of 261,120 Conversions of a DC Input at the Code Center

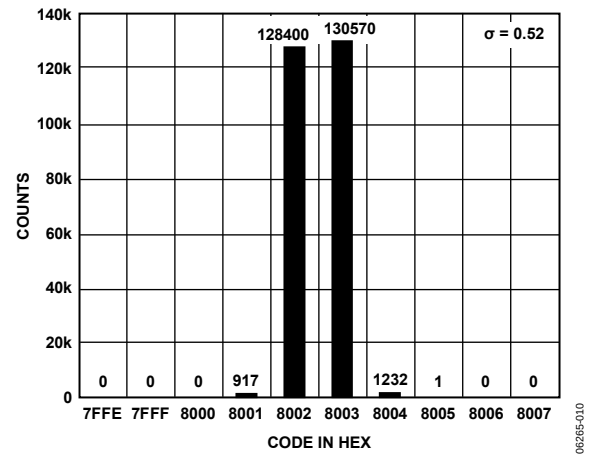



Figure 10. Histogram of 261,120 Conversions of a DC Input at the Code Transition

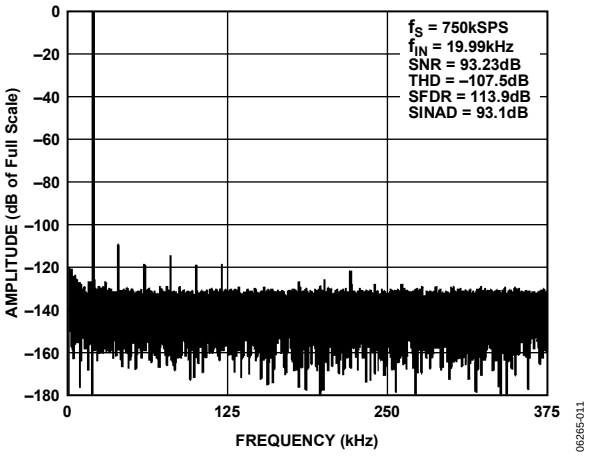



Figure 11. FFT 20 kHz

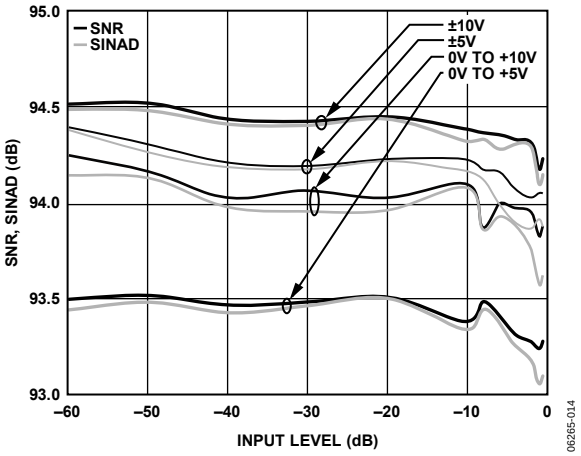



Figure 14. SNR and SINAD vs. Input Level (Referred to Full Scale)

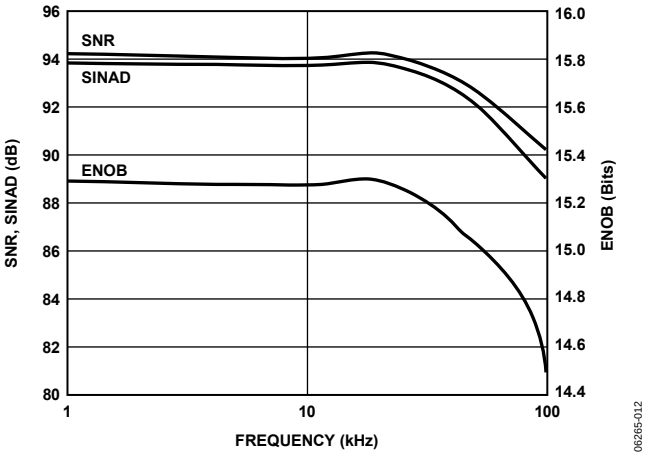



Figure 12. SNR, SINAD, and ENOB vs. Frequency

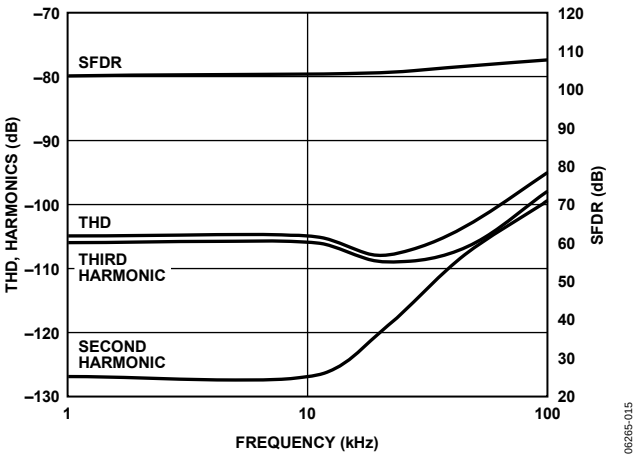



Figure 15. THD, Harmonics, and SFDR vs. Frequency

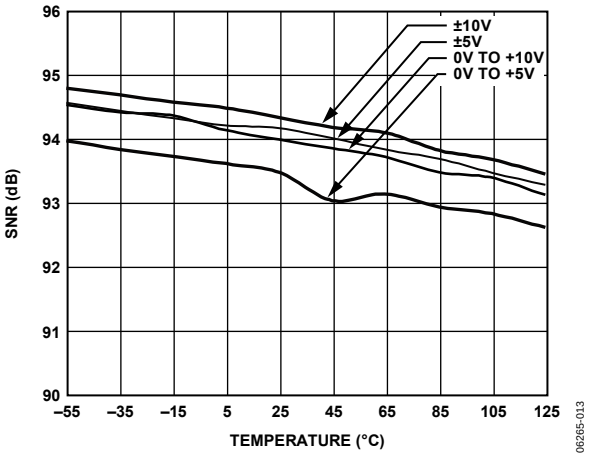



Figure 13. SNR vs. Temperature

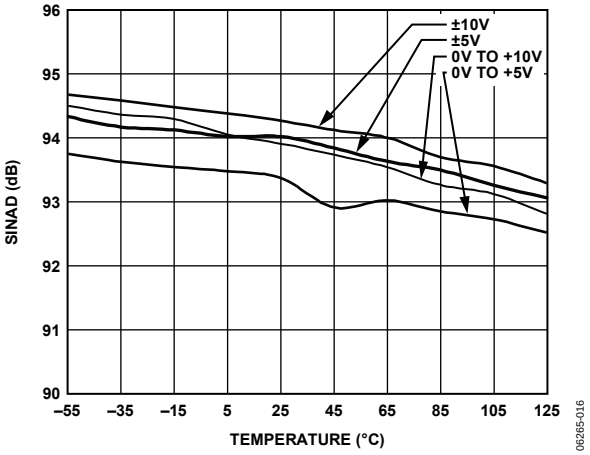



Figure 16. SINAD vs. Temperature

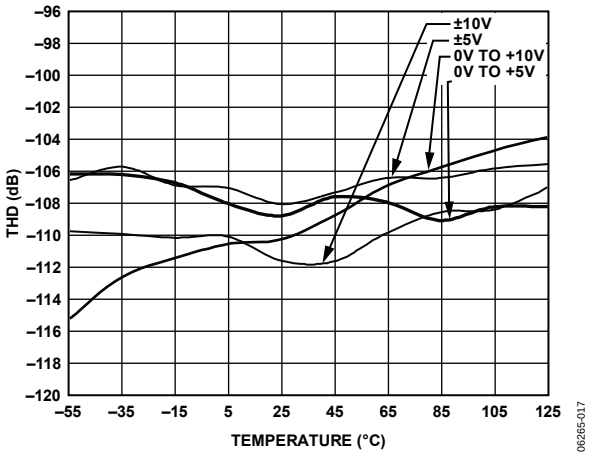



Figure 17. THD vs. Temperature

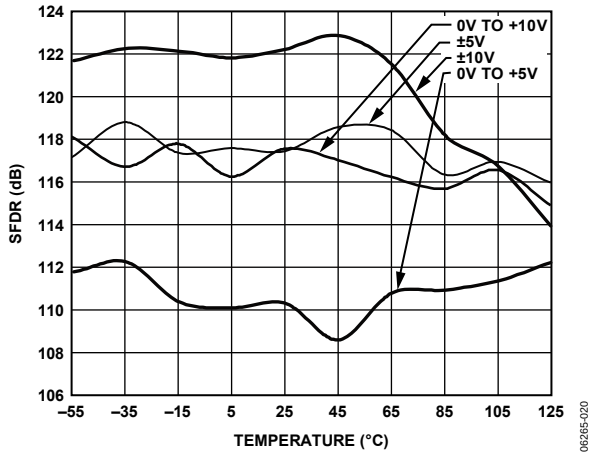



Figure 20. SFDR vs. Temperature (Excludes Harmonics)

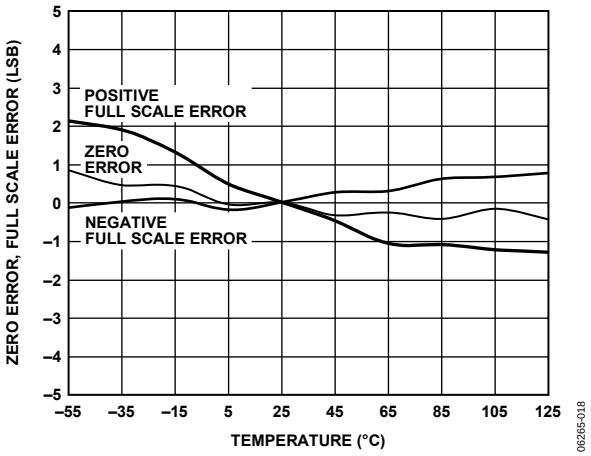



Figure 18. Zero Error, Positive and Negative Full Scale vs. Temperature

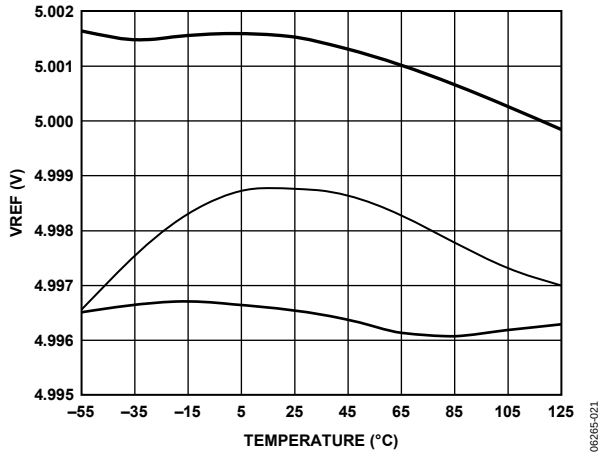



Figure 21. Typical Reference Voltage Output vs. Temperature (3 Devices)

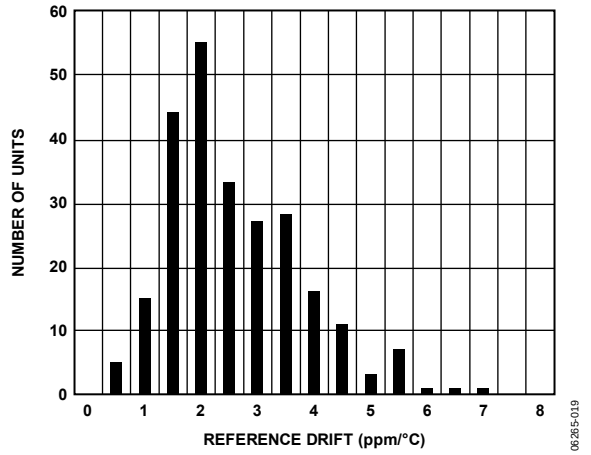



Figure 19. Reference Voltage Temperature Coefficient Distribution (247 Devices)

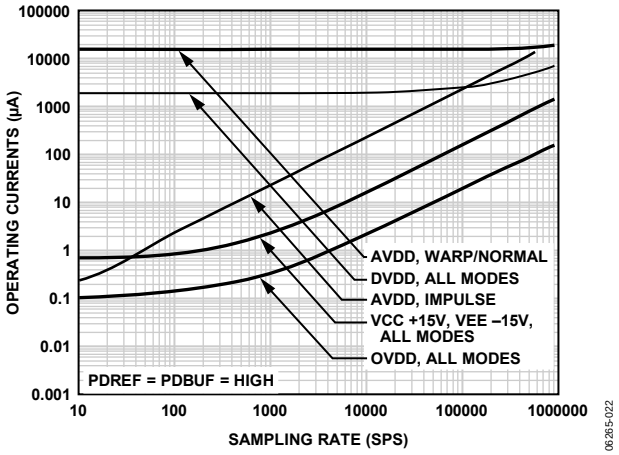



Figure 22. Operating Currents vs. Sample Rate

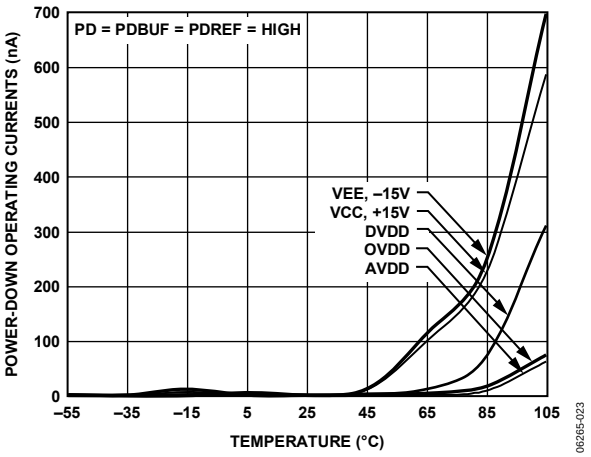



Figure 23. Power-Down Operating Currents vs. Temperature

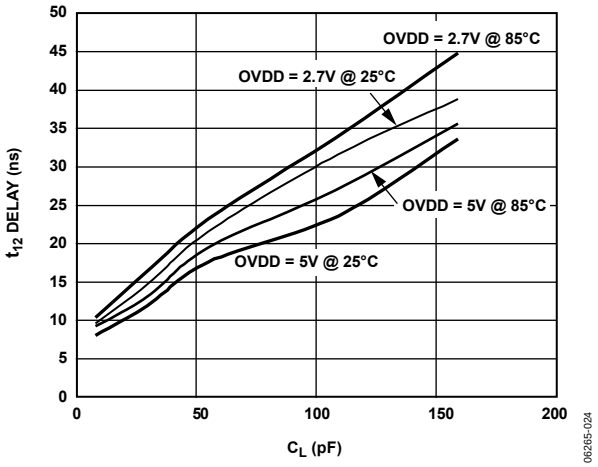



Figure 24. Typical Delay vs. Load Capacitance $C_L$

# TERMINOLOGY

**Least Significant Bit (LSB)**
The least significant bit, or LSB, is the smallest increment that can be represented by a converter. For an analog-to-digital converter with *N* bits of resolution, the LSB expressed in volts is

$$LSB(V) = \frac{V_{INp\text{-}p}}{2^N}$$

**Integral Nonlinearity Error (INL)**
Linearity error refers to the deviation of each individual code from a line drawn from negative full-scale through positive full-scale. The point used as negative full-scale occurs a ½ LSB before the first code transition. Positive full-scale is defined as a level 1½ LSBs beyond the last code transition. The deviation is measured from the middle of each code to the true straight line.

**Differential Nonlinearity Error (DNL)**
In an ideal ADC, code transitions are 1 LSB apart. Differential nonlinearity is the maximum deviation from this ideal value. It is often specified in terms of resolution for which no missing codes are guaranteed.

**Bipolar Zero Error**
The difference between the ideal midscale input voltage (0 V) and the actual voltage producing the midscale output code.

**Unipolar Offset Error**
The first transition should occur at a level ½ LSB above analog ground. The unipolar offset error is the deviation of the actual transition from that point.

**Full-Scale Error**
The last transition (from 111…10 to 111…11) should occur for an analog voltage 1½ LSB below the nominal full-scale. The full-scale error is the deviation in LSB (or % of full-scale range) of the actual level of the last transition from the ideal level and includes the effect of the offset error. Closely related is the gain error (also in LSB or % of full-scale range), which does not include the effects of the offset error.

**Dynamic Range**
Dynamic range is the ratio of the rms value of the full-scale to the rms noise measured for an input typically at −60 dB. The value for dynamic range is expressed in decibels.

**Signal-to-Noise Ratio (SNR)**
SNR is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, excluding harmonics and dc. The value for SNR is expressed in decibels.

**Total Harmonic Distortion (THD)**
THD is the ratio of the rms sum of the first five harmonic components to the rms value of a full-scale input signal and is expressed in decibels.

**Signal-to-(Noise + Distortion) Ratio (SINAD)**
SINAD is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for SINAD is expressed in decibels.

**Spurious-Free Dynamic Range (SFDR)**
The difference, in decibels (dB), between the rms amplitude of the input signal and the peak spurious signal.

**Effective Number of Bits (ENOB)**
ENOB is a measurement of the resolution with a sine wave input. It is related to SINAD and is expressed in bits by

$$ENOB = [(SINAD_{dB} - 1.76)/6.02]$$

**Aperture Delay**
Aperture delay is a measure of the acquisition performance measured from the falling edge of the $\overline{\text{CNVST}}$ input to when the input signal is held for a conversion.

**Transient Response**
The time required for the AD7612 to achieve its rated accuracy after a full-scale step function is applied to its input.

**Reference Voltage Temperature Coefficient**
Reference voltage temperature coefficient is derived from the typical shift of output voltage at 25°C on a sample of parts at the maximum and minimum reference output voltage ($V_{REF}$) measured at $T_{MIN}$, T(25°C), and $T_{MAX}$. It is expressed in ppm/°C as

$$TCV_{REF}(\text{ppm/°C}) = \frac{V_{REF}(Max) - V_{REF}(Min)}{V_{REF}(25°C) \times (T_{MAX} - T_{MIN})} \times 10^6$$

where:
$V_{REF}(Max)$ = maximum $V_{REF}$ at $T_{MIN}$, T(25°C), or $T_{MAX}$.
$V_{REF}(Min)$ = minimum $V_{REF}$ at $T_{MIN}$, T(25°C), or $T_{MAX}$.
$V_{REF}(25°C)$ = $V_{REF}$ at 25°C.
$T_{MAX}$ = +85°C.
$T_{MIN}$ = −40°C.

# THEORY OF OPERATION

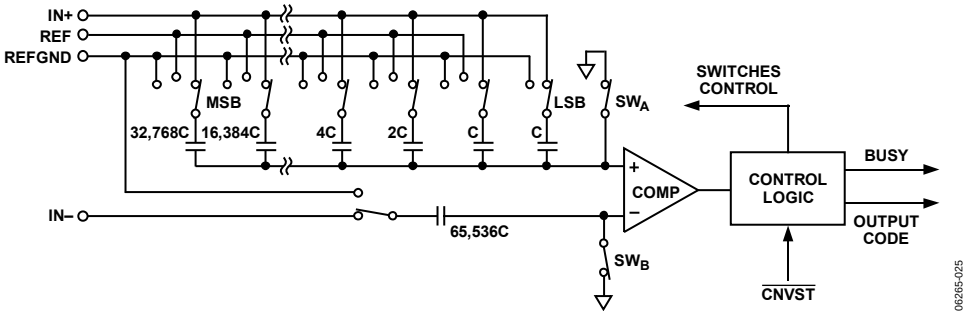



*Figure 25. ADC Simplified Schematic*

## OVERVIEW

The AD7612 is a very fast, low power, precise, 16-bit analog-to-digital converter (ADC) using successive approximation capacitive digital-to-analog (CDAC) architecture.

The AD7612 can be configured at any time for one of four input ranges and conversion mode with inputs in parallel and serial hardware modes or by a dedicated write only, SPI-compatible interface via a configuration register in serial software mode. The AD7612 uses Analog Device's patented *i*CMOS high voltage process to accommodate 0 to 5 V, 0 to 10 V, ±5 V, and ±10 V input ranges without the use of conventional thin films. Only one acquisition cycle, $t_8$, is required for the inputs to latch to the correct configuration. Resetting or power cycling is not required for reconfiguring the ADC.

The AD7612 features different modes to optimize performance according to the applications. It is capable of converting 750,000 samples per second (750 kSPS) in warp mode, 600 kSPS in normal mode, and 500 kSPS in impulse mode.

The AD7612 provides the user with an on-chip track-and-hold, successive approximation ADC that does not exhibit any pipeline or latency, making it ideal for multiple multiplexed channel applications.

For unipolar input ranges, the AD7612 typically requires three supplies; VCC, AVDD (which can supply DVDD), and OVDD which can be interfaced to either 5 V, 3.3 V, or 2.5 V digital logic. For bipolar input ranges, the AD7612 requires the use of the additional VEE supply.

The device is housed in Pb-free, 48-lead LQFP or tiny LFCSP 7 mm × 7 mm packages that combine space savings with flexibility. In addition, the AD7612 can be configured as either a parallel or serial SPI-compatible interface.

## CONVERTER OPERATION

The AD7612 is a successive approximation ADC based on a charge redistribution DAC. Figure 25 shows the simplified schematic of the ADC. The CDAC consists of two identical arrays of 16 binary weighted capacitors, which are connected to the two comparator inputs.

During the acquisition phase, terminals of the array tied to the comparator's input are connected to AGND via SW+ and SW−. All independent switches are connected to the analog inputs. Thus, the capacitor arrays are used as sampling capacitors and acquire the analog signal on IN+ and IN− inputs. A conversion phase is initiated once the acquisition phase is complete and the $\overline{\text{CNVST}}$ input goes low. When the conversion phase begins, SW+ and SW− are opened first. The two capacitor arrays are then disconnected from the inputs and connected to the REFGND input. Therefore, the differential voltage between the inputs (IN+ and IN−) captured at the end of the acquisition phase is applied to the comparator inputs, causing the comparator to become unbalanced. By switching each element of the capacitor array between REFGND and REF, the comparator input varies by binary weighted voltage steps ($V_{REF}/2$, $V_{REF}/4$ through $V_{REF}/65536$). The control logic toggles these switches, starting with the MSB first, in order to bring the comparator back into a balanced condition.

After the completion of this process, the control logic generates the ADC output code and brings the BUSY output low.

## MODES OF OPERATION

The AD7612 features three modes of operation: warp, normal, and impulse. Each of these modes is more suitable to specific applications. The mode is configured with the input pins, WARP and IMPULSE, or via the configuration register. See Table 6 for the pin details and the Hardware Configuration section and Software Configuration section for programming the mode selection with either pins or configuration register. Note that when using the configuration register, the WARP and IMPULSE inputs are don't cares and should be tied to either high or low.

### *Warp Mode*

Setting WARP = high and IMPULSE = low allow the fastest conversion rate up to 750 kSPS. However, in this mode, the full specified accuracy is guaranteed only when the time between conversions does not exceed 1 ms. If the time between two consecutive conversions is longer than 1 ms (after power-up), the first conversion result should be ignored since in warp mode, the ADC performs a background calibration during the SAR conversion process. This calibration can drift if the time between conversions exceeds 1 ms thus causing the first conversion to appear offset. This mode makes the AD7612 ideal for applications where both high accuracy and fast sample rate are required. In addition, the AD7612 can run up to 900 kSPS throughput with some performance degradation, mainly dc linearity.

### *Normal Mode*

Setting WARP = IMPULSE = low or WARP = IMPULSE = high allows the fastest mode (600 kSPS) without any limitation on time between conversions. This mode makes the AD7612 ideal for asynchronous applications such as data acquisition systems, where both high accuracy and fast sample rate are required.

### *Impulse Mode*

Setting WARP = low and IMPULSE = high uses the lowest power dissipation mode and allows power saving between conversions. The maximum throughput in this mode is 500 kSPS and in this mode, the ADC powers down circuits after conversion making the AD7612 ideal for battery-powered applications.

## TRANSFER FUNCTIONS

Using the OB/$\overline{2C}$ digital input or via the configuration register, the AD7612 offers two output codings: straight binary and twos complement. See Figure 26 and Table 7 for the ideal transfer characteristic and digital output codes for the different analog input ranges, $V_{IN}$. Note that when using the configuration register, the OB/$\overline{2C}$ input is a don't care and should be tied to either high or low.

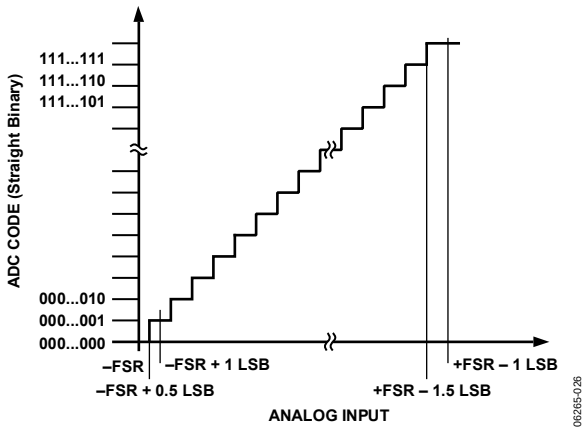



*Figure 26. ADC Ideal Transfer Function*

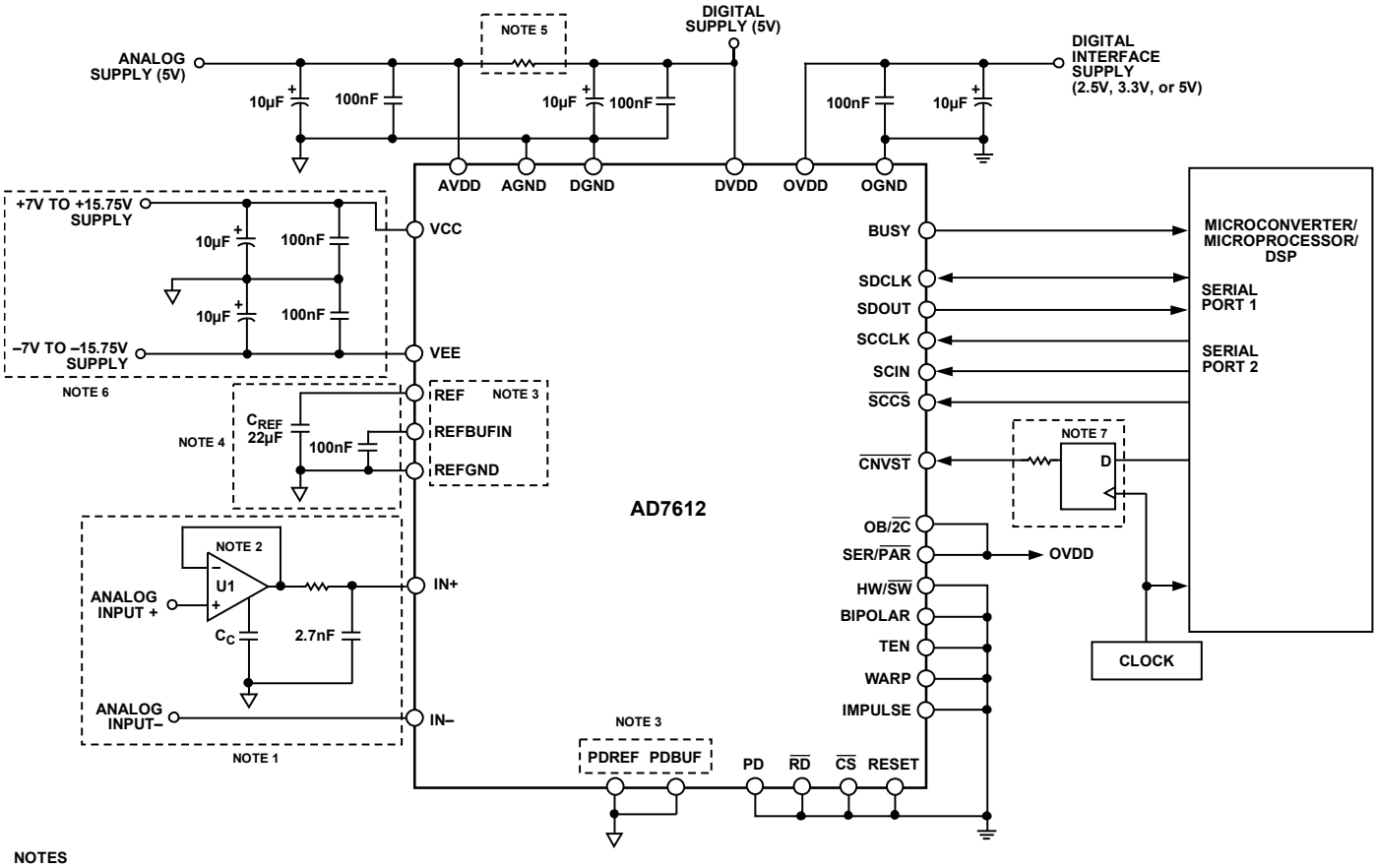
**Table 7. Output Codes and Ideal Input Voltages**

| | $V_{REF}$ = 5 V | | | | Digital Output Code | |
|---|---|---|---|---|---|---|
| **Description** | **$V_{IN}$ = 5 V** | **$V_{IN}$ = 10 V** | **$V_{IN}$ = ±5 V** | **$V_{IN}$ = ±10 V** | **Straight Binary** | **Twos Complement** |
| FSR – 1 LSB | 4.999924 V | 9.999847 V | +4.999847 V | +9.999695 V | 0xFFFF[1] | 0x7FFF[1] |
| FSR – 2 LSB | 4.999847 V | 9.999695 V | +4.999695 V | +9.999390 V | 0xFFFE | 0x7FFE |
| Midscale + 1 LSB | 2.500076 V | 5.000153 V | +152.6 µV | +305.2 µV | 0x8001 | 0x0001 |
| Midscale | 2.5 V | 5.000000 V | 0 V | 0 V | 0x8000 | 0x0000 |
| Midscale – 1 LSB | 2.499924 V | 4.999847 V | −152.6 µV | −305.2 µV | 0x7FFF | 0xFFFF |
| –FSR + 1 LSB | 76.3 µV | 152.6 µV | −4.999847 V | −9.999695 V | 0x0001 | 0x8001 |
| –FSR | 0 V | 0 V | −5 V | −10 V | 0x0000[2] | 0x8000[2] |

[1] This is also the code for overrange analog input ($V_{IN+}$ – $V_{IN-}$ above $V_{REF}$ – $V_{REFGND}$).
[2] This is also the code for overrange analog input ($V_{IN+}$ – $V_{IN-}$ below $V_{REF}$ – $V_{REFGND}$).

## TYPICAL CONNECTION DIAGRAM

Figure 27 shows a typical connection diagram for the AD7612 using the internal reference, serial data interface, and serial configuration port. Different circuitry from that shown in Figure 27 is optional and is discussed in the following sections.




NOTES
1. SEE ANALOG INPUT SECTION. ANALOG INPUT(–) IS REFERENCED TO AGND ±0.1V.
2. THE AD8021 IS RECOMMENDED. SEE DRIVER AMPLIFIER CHOICE SECTION.
3. THE CONFIGURATION SHOWN IS USING THE INTERNAL REFERENCE. SEE VOLTAGE REFERENCE INPUT SECTION.
4. A 22µF CERAMIC CAPACITOR (X5R, 1206 SIZE) IS RECOMMENDED (FOR EXAMPLE, PANASONIC ECJ4YB1A226M). SEE VOLTAGE REFERENCE INPUT SECTION.
5. OPTION, SEE POWER SUPPLY SECTION.
6. THE VCC AND VEE SUPPLIES SHOULD BE VCC = [VIN(MAX) +2V] and VEE = [VIN(MIN) –2V] FOR BIPOLAR INPUT RANGES. FOR UNIPOLAR INPUT RANGES, VEE CAN BE 0V. SEE POWER SUPPLY SECTION.
7. OPTIONAL LOW JITTER $\overline{\text{CNVST}}$, SEE CONVERSION CONTROL SECTION.

06265-027

*Figure 27. Typical Connection Diagram Shown with Serial Interface and Serial Programmable Port*

## ANALOG INPUTS

### *Input Range Selection*

In parallel mode and serial hardware mode, the input range is selected by using the BIPOLAR (bipolar) and TEN (10 Volt range) inputs. See Table 6 for pin details and the Hardware Configuration section and Software Configuration section for programming the mode selection with either pins or configuration register. Note that when using the configuration register, the BIPOLAR and TEN inputs are don't cares and should be tied to either high or low.

### *Input Structure*

Figure 28 shows an equivalent circuit for the input structure of the AD7612.

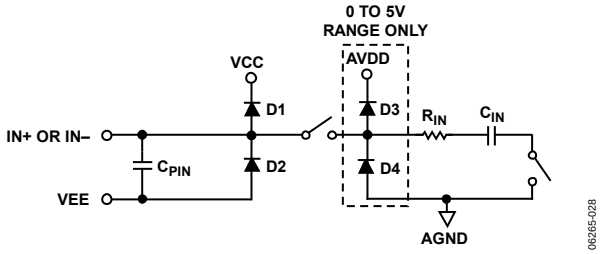



*Figure 28. AD7612 Simplified Analog Input*

The four diodes, D1 to D4, provide ESD protection for the analog inputs, IN+ and IN–. Care must be taken to ensure that the analog input signal never exceeds the supply rails by more than 0.3 V, because this causes the diodes to become forward-biased and to start conducting current. These diodes can handle a forward-biased current of 120 mA maximum. For instance, these conditions could eventually occur when the input buffer's U1 supplies are different from AVDD, VCC, and VEE. In such a case, an input buffer with a short-circuit current limitation can be used to protect the part although most op amps' short circuit current is <100 mA. Note that D3 and D4 are only used in the 0 V to 5 V range to allow for additional protection in applications that are switching from the higher voltage ranges.

This analog input structure allows the sampling of the differential signal between IN+ and IN–. By using this differential input, small signals common to both inputs are rejected as shown in Figure 29, which represents the typical CMRR over frequency.

For instance, by using IN– to sense a remote signal ground, ground potential differences between the sensor and the local ADC ground are eliminated.

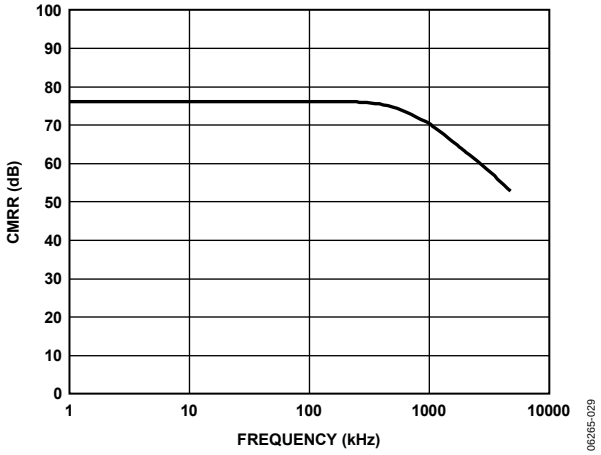



*Figure 29. Analog Input CMRR vs. Frequency*

During the acquisition phase for ac signals, the impedance of the analog inputs, IN+ and IN–, can be modeled as a parallel combination of Capacitor $C_{PIN}$ and the network formed by the series connection of $R_{IN}$ and $C_{IN}$. $C_{PIN}$ is primarily the pin capacitance. $R_{IN}$ is typically 70 Ω and is a lumped component comprised of serial resistors and the on resistance of the switches. $C_{IN}$ is primarily the ADC sampling capacitor and depending on the input range selected is typically 48 pF in the 0 V to 5 V range, typically 24 pF in the 0 V to 10 V and ±5 V ranges and typically 12 pF in the ±10 V range. During the conversion phase, when the switches are opened, the input impedance is limited to $C_{PIN}$.

Since the input impedance of the AD7612 is very high, it can be directly driven by a low impedance source without gain error. To further improve the noise filtering achieved by the AD7612 analog input circuit, an external, one-pole RC filter between the amplifier's outputs and the ADC analog inputs can be used, as shown in Figure 27. However, large source impedances significantly affect the ac performance, especially total harmonic distortion (THD). The maximum source impedance depends on the amount of THD that can be tolerated. The THD degrades as a function of the source impedance and the maximum input frequency.

## DRIVER AMPLIFIER CHOICE

Although the AD7612 is easy to drive, the driver amplifier must meet the following requirements:

- For multichannel, multiplexed applications, the driver amplifier and the AD7612 analog input circuit must be able to settle for a full-scale step of the capacitor array at a 16-bit level (0.0015%). For the amplifier, settling at 0.1% to 0.01% is more commonly specified. This differs significantly from the settling time at a 16-bit level and should be verified prior to driver selection. The AD8021 op amp combines ultra-low noise and high gain bandwidth and meets this settling time requirement even when used with gains of up to 13.
- The noise generated by the driver amplifier needs to be kept as low as possible to preserve the SNR and transition noise performance of the AD7612. The noise coming from the driver is filtered by the external 1-pole low-pass filter as shown in Figure 27. The SNR degradation due to the amplifier is

$$SNR_{LOSS} = 20\log\left(\frac{V_{NADC}}{\sqrt{V_{NADC}^2 + \frac{\pi}{2} f_{-3dB}(Ne_N)^2}}\right)$$

where:

$V_{NADC}$ is the noise of the ADC, which is:

$$V_{NADC} = \frac{\frac{V_{INp\text{-}p}}{2\sqrt{2}}}{10^{\frac{SNR}{20}}}$$

$f_{-3dB}$ is the cutoff frequency of the input filter (3.9 MHz).

$N$ is the noise factor of the amplifier (+1 in buffer configuration).

$e_N$ is the equivalent input voltage noise density of the op amp, in nV/√Hz.

- The driver needs to have a THD performance suitable to that of the AD7612. Figure 15 shows the THD vs. frequency that the driver should exceed.

The AD8021 meets these requirements and is appropriate for almost all applications. The AD8021 needs a 10 pF external compensation capacitor that should have good linearity as an NPO ceramic or mica type. Moreover, the use of a noninverting +1 gain arrangement is recommended and helps to obtain the best signal-to-noise ratio.

The AD8022 can also be used when a dual version is needed and a gain of 1 is present. The AD829 is an alternative in applications where high frequency (above 100 kHz) performance is not required. In applications with a gain of 1, an 82 pF compensation capacitor is required. The AD8610 is an option when low bias current is needed in low frequency applications.

Since the AD7612 uses a large geometry, high voltage input switch, the best linearity performance is obtained when using the amplifier at its maximum full power bandwidth. Gaining the amplifier to make use of the more dynamic range of the ADC results in increased linearity errors. For applications requiring more resolution, the use of an additional amplifier with gain should precede a unity follower driving the AD7612. See Table 8 for a list of recommended op amps.

**Table 8. Recommended Driver Amplifiers**

| Amplifier | Typical Application |
|---|---|
| ADA4841-x | 12 V supply, very low noise, low distortion, low power, low frequency |
| AD829 | ±15 V supplies, very low noise, low frequency |
| AD8021 | ±12 V supplies, very low noise, high frequency |
| AD8022 | ±12 V supplies, very low noise, high frequency, dual |
| AD8610/AD8620 | ±13 V supplies, low bias current, low frequency, single/dual |

## VOLTAGE REFERENCE INPUT/OUTPUT

The AD7612 allows the choice of either a very low temperature drift internal voltage reference, an external reference or an external buffered reference.

The internal reference of the AD7612 provides excellent performance and can be used in almost all applications. However, the linearity performance is guaranteed only with an external reference.

### *Internal Reference (REF = 5 V) (PDREF = Low, PDBUF = Low)*

To use the internal reference, the PDREF and PDBUF inputs must be low. This enables the on-chip band gap reference, buffer, and TEMP sensor resulting in a 5.00 V reference on the REF pin.

The internal reference is temperature-compensated to 5.000 V ±35 mV. The reference is trimmed to provide a typical drift of 3 ppm/°C. This typical drift characteristic is shown in Figure 19.

### *External 2.5 V Reference and Internal Buffer (REF = 5 V) (PDREF = High, PDBUF = Low)*

To use an external reference with the internal buffer, PDREF should be high and PDBUF should be low. This powers down the internal reference and allows the 2.5 V reference to be applied to REFBUFIN producing 5 V on the REF pin. The internal reference buffer is useful in multiconverter applications since a buffer is typically required in these applications.

### *External 5 V Reference (PDREF = High, PDBUF = High)*

To use an external reference directly on the REF pin, PDREF and PDBUF should both be high. PDREF and PDBUF power down the internal reference and the internal reference buffer, respectively. For improved drift performance, an external reference such as the ADR445 or ADR435 is recommended.

### *Reference Decoupling*

Whether using an internal or external reference, the AD7612 voltage reference input (REF) has a dynamic input impedance; therefore, it should be driven by a low impedance source with efficient decoupling between the REF and REFGND inputs. This decoupling depends on the choice of the voltage reference, but usually consists of a low ESR capacitor connected to REF and REFGND with minimum parasitic inductance. A 22 µF (X5R, 1206 size) ceramic chip capacitor (or 47 µF tantalum capacitor) is appropriate when using either the internal reference or the ADR445/ADR435 external reference.

The placement of the reference decoupling is also important to the performance of the AD7612. The decoupling capacitor should be mounted on the same side as the ADC right at the REF pin with a thick PCB trace. The REFGND should also connect to the reference decoupling capacitor with the shortest distance and to the analog ground plane with several vias.

For applications that use multiple AD7612 or other PulSAR devices, it is more effective to use the internal reference buffer to buffer the external 2.5 V reference voltage.

The voltage reference temperature coefficient (TC) directly impacts full scale; therefore, in applications where full-scale accuracy matters, care must be taken with the TC. For instance, a ±15 ppm/°C TC of the reference changes full-scale by ±1 LSB/°C.

### *Temperature Sensor*

The TEMP pin measures the temperature of the AD7612. To improve the calibration accuracy over the temperature range, the output of the TEMP pin is applied to one of the inputs of the analog switch (such as ADG779), and the ADC itself is used to measure its own temperature. This configuration is shown in Figure 30.

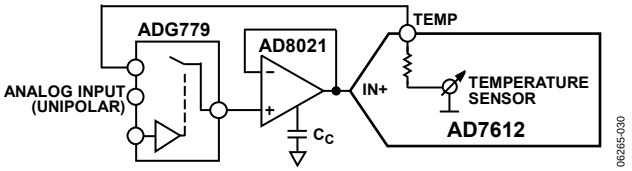



*Figure 30. Use of the Temperature Sensor*

## POWER SUPPLIES

The AD7612 uses five sets of power supply pins:

- AVDD: analog 5 V core supply
- VCC: analog high voltage positive supply
- VEE: high voltage negative supply
- DVDD: digital 5 V core supply
- OVDD: digital input/output interface supply

### *Core Supplies*

The AVDD and DVDD supply the AD7612 analog and digital cores respectively. Sufficient decoupling of these supplies is required consisting of at least a 10 µF capacitor and 100 nF on each supply. The 100 nF capacitors should be placed as close as possible to the AD7612. To reduce the number of supplies needed, the DVDD can be supplied through a simple RC filter from the analog supply, as shown in Figure 27.

### *High Voltage Supplies*

The high voltage bipolar supplies, VCC and VEE are required and must be at least 2 V larger than the maximum input, $V_{IN}$. For example, if using the bipolar 10 V range, the supplies should be ±12 V minimum. Sufficient decoupling of these supplies is also required consisting of at least a 10 µF capacitor and 100 nF on each supply. For unipolar operation, the VEE supply can be grounded with some slight THD performance degradation.

### *Digital Output Supply*

The OVDD supplies the digital outputs and allows direct interface with any logic working between 2.3 V and 5.25 V. OVDD should be set to the same level as the system interface. Sufficient decoupling is required consisting of at least a 10 µF capacitor and 100 nF with the 100 nF placed as close as possible to the AD7612.

### Power Sequencing

The AD7612 requires sequencing of the AVDD and DVDD supplies. AVDD should come up prior to or simultaneously with DVDD. This can be achieved using the configuration in Figure 27 or sequencing the supplies in that manner. The other supplies can be sequenced as desired as long as absolute maximum ratings are observed. The AD7612 is very insensitive to power supply variations on AVDD over a wide frequency range, as shown in Figure 31.

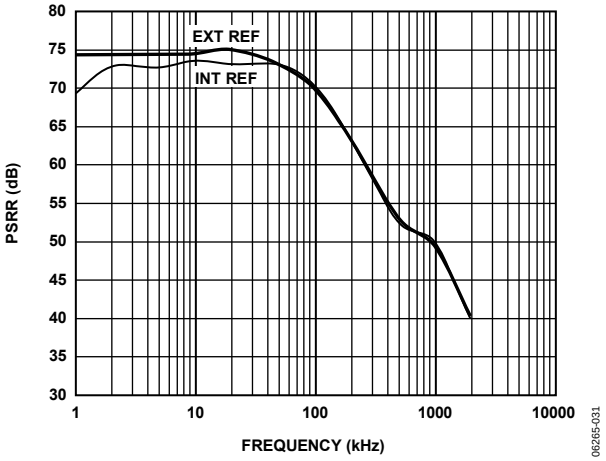



*Figure 31. AVDD PSRR vs. Frequency*

### Power Dissipation vs. Throughput

In impulse mode, the AD7612 automatically reduces its power consumption at the end of each conversion phase. During the acquisition phase, the operating currents are very low, which allows a significant power savings when the conversion rate is reduced (see Figure 32). This feature makes the AD7612 ideal for very low power, battery-operated applications.

It should be noted that the digital interface remains active even during the acquisition phase. To reduce the operating digital supply currents even further, drive the digital inputs close to the power rails (that is, OVDD and OGND).

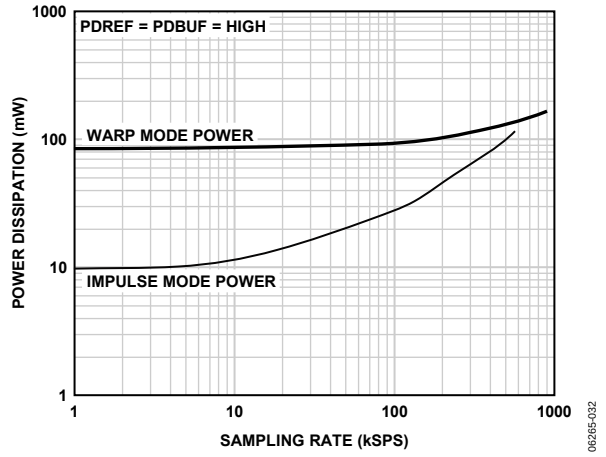



*Figure 32. Power Dissipation vs. Sample Rate*

### Power Down

Setting PD = high powers down the AD7612, thus reducing supply currents to their minimums as shown in Figure 23. When the ADC is in power down, the current conversion (if any) is completed and the digital bus remains active. To further reduce the digital supply currents, drive the inputs to OVDD or OGND.

Power down can also be programmed with the configuration register. See the Software Configuration section for details. Note that when using the configuration register, the PD input is a don't care and should be tied to either high or low.

## CONVERSION CONTROL

The AD7612 is controlled by the $\overline{\text{CNVST}}$ input. A falling edge on $\overline{\text{CNVST}}$ is all that is necessary to initiate a conversion. Detailed timing diagrams of the conversion process are shown in Figure 33. Once initiated, it cannot be restarted or aborted, even by the power-down input, PD, until the conversion is complete. The $\overline{\text{CNVST}}$ signal operates independently of $\overline{\text{CS}}$ and $\overline{\text{RD}}$ signals.

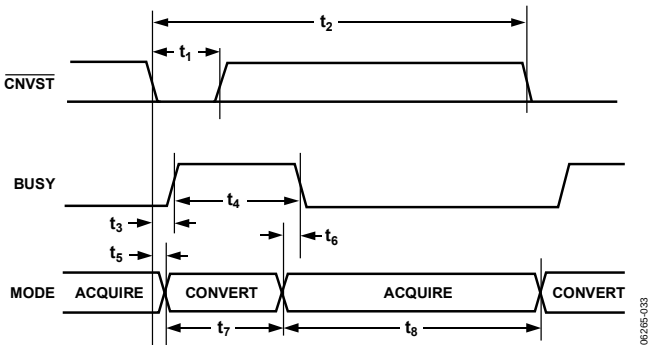



*Figure 33. Basic Conversion Timing*

Although $\overline{\text{CNVST}}$ is a digital signal, it should be designed with special care with fast, clean edges, and levels with minimum overshoot, undershoot, or ringing.

The $\overline{\text{CNVST}}$ trace should be shielded with ground and a low value (such as 50 Ω) serial resistor termination should be added close to the output of the component that drives this line.

For applications where SNR is critical, the $\overline{\text{CNVST}}$ signal should have very low jitter. This can be achieved by using a dedicated oscillator for $\overline{\text{CNVST}}$ generation, or by clocking $\overline{\text{CNVST}}$ with a high frequency, low jitter clock, as shown in Figure 27.

# INTERFACES

## DIGITAL INTERFACE

The AD7612 has a versatile digital interface that can be set up as either a serial or a parallel interface with the host system. The serial interface is multiplexed on the parallel data bus. The AD7612 digital interface also accommodates 2.5 V, 3.3 V, or 5 V logic. In most applications, the OVDD supply pin is connected to the host system interface 2.5 V to 5.25 V digital supply. Finally, by using the OB/$\overline{2C}$ input pin, both twos complement or straight binary coding can be used.

Two signals, $\overline{CS}$ and $\overline{RD}$, control the interface. When at least one of these signals is high, the interface outputs are in high impedance. Usually, $\overline{CS}$ allows the selection of each AD7612 in multi-circuit applications and is held low in a single AD7612 design. $\overline{RD}$ is generally used to enable the conversion result on the data bus.

### *RESET*

The RESET input is used to reset the AD7612. A rising edge on RESET aborts the current conversion (if any) and tristates the data bus. The falling edge of RESET resets the AD7612 and clears the data bus and configuration register. See Figure 34 for the RESET timing details.

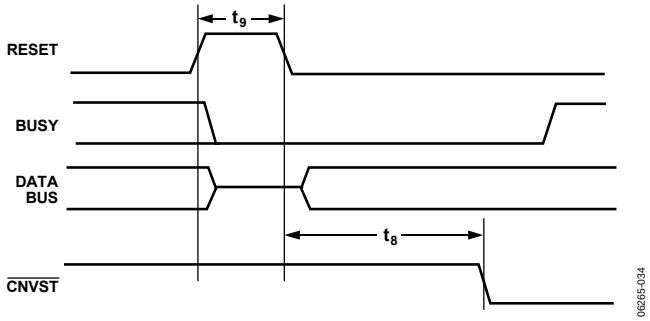



*Figure 34. RESET Timing*

## PARALLEL INTERFACE

The AD7612 is configured to use the parallel interface when SER/$\overline{PAR}$ is held low.

### *Master Parallel Interface*

Data can be continuously read by tying $\overline{CS}$ and $\overline{RD}$ low, thus requiring minimal microprocessor connections. However, in this mode, the data bus is always driven and cannot be used in shared bus applications (unless the device is held in RESET). Figure 35 details the timing for this mode.

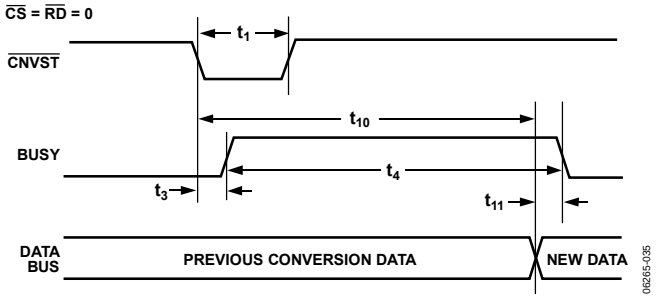



*Figure 35. Master Parallel Data Timing for Reading (Continuous Read)*

### *Slave Parallel Interface*

In slave parallel reading mode, the data can be read either after each conversion, which is during the next acquisition phase, or during the following conversion, as shown in Figure 36 and Figure 37, respectively. When the data is read during the conversion, it is recommended that it is read only during the first half of the conversion phase. This avoids any potential feedthrough between voltage transients on the digital interface and the most critical analog conversion circuitry.

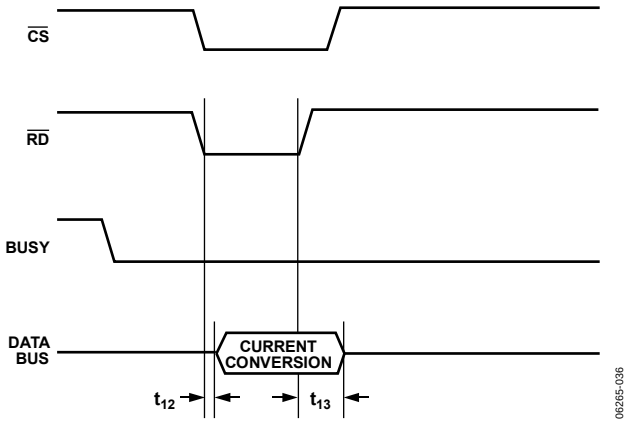



*Figure 36. Slave Parallel Data Timing for Reading (Read After Convert)*

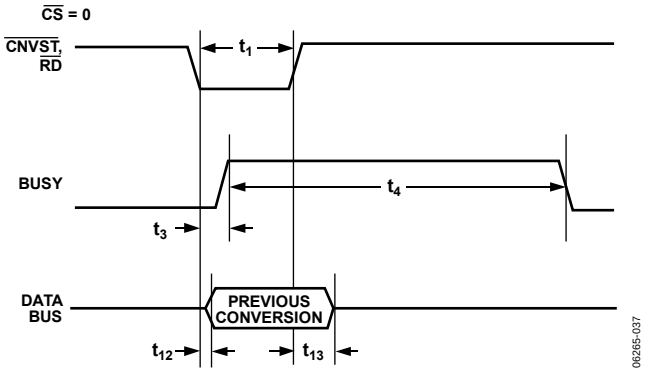



*Figure 37. Slave Parallel Data Timing for Reading (Read During Convert)*

### 8-Bit Interface (Master or Slave)

The BYTESWAP pin allows a glueless interface to an 8-bit bus. As shown in Figure 38, when BYTESWAP is low, the LSB byte is output on D[7:0] and the MSB is output on D[15:8]. When BYTESWAP is high, the LSB and MSB bytes are swapped; the LSB is output on D[15:8] and the MSB is output on D[7:0]. By connecting BYTESWAP to an address line, the 16-bit data can be read in two bytes on either D[15:8] or D[7:0]. This interface can be used in both master and slave parallel reading modes.

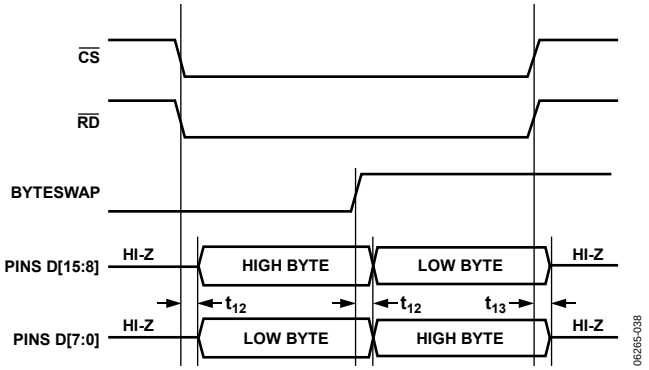



*Figure 38. 8-Bit and 16-Bit Parallel Interface*

## SERIAL INTERFACE

The AD7612 has a serial interface (SPI-compatible) multiplexed on the data pins D[15:2]. The AD7612 is configured to use the serial interface when SER/$\overline{\text{PAR}}$ is held high.

### Data Interface

The AD7612 outputs 16 bits of data, MSB first, on the SDOUT pin. This data is synchronized with the 16 clock pulses provided on the SDCLK pin. The output data is valid on both the rising and falling edge of the data clock.

### Serial Configuration Interface

The AD7612 can be configured through the serial configuration register only in serial mode as the serial configuration pins are also multiplexed on the data pins D[15:12]. Refer to the Hardware Configuration section and Software Configuration section for more information.

## MASTER SERIAL INTERFACE

The pins multiplexed on D[10:2] and used for master serial interface are DIVSCLK[0], DIVSCLK[1], EXT/$\overline{\text{INT}}$, INVSYNC, INVSCLK, RDC, SDOUT, SDCLK and SYNC.

### Internal Clock (SER/$\overline{\text{PAR}}$ = high, EXT/$\overline{\text{INT}}$ = Low)

The AD7612 is configured to generate and provide the serial data clock, SDCLK, when the EXT/$\overline{\text{INT}}$ pin is held low. The AD7612 also generates a SYNC signal to indicate to the host when the serial data is valid. The SDCLK, and the SYNC signals can be inverted, if desired using the INVSCLK and INVSYNC inputs, respectively. Depending on the input, RDC, the data can be read during the following conversion or after each conversion. Figure 39 and Figure 40 show detailed timing diagrams of these two modes.

### Read During Convert (RDC = High)

Setting RDC = high allows the master read (previous conversion result) during conversion mode. Usually, because the AD7612 is used with a fast throughput, this mode is the most recommended serial mode. In this mode, the serial clock and data toggle at appropriate instances, minimizing potential feed through between digital activity and critical conversion decisions. In this mode, the SDCLK period changes since the LSBs require more time to settle and the SDCLK is derived from the SAR conversion cycle. In this mode, the AD7612 generates a discontinuous SDCLK of two different periods and the host should use an SPI interface.

### Read During Convert (RDC = Low, DIVSCLK[1:0] = [0 to 3])

Setting RDC = low allows the read after conversion mode. Unlike the other serial modes, the BUSY signal returns low after the 16 data bits are pulsed out and not at the end of the conversion phase, resulting in a longer BUSY width (refer to Table 4 for BUSY timing specifications). The DIVSCLK[1:0] inputs control the SDCLK period and SDOUT data rate. As a result, the maximum throughput cannot be achieved in this mode. In this mode, the AD7612 also generates a discontinuous SDCLK however, a fixed period and hosts supporting both SPI and serial ports can also be used.

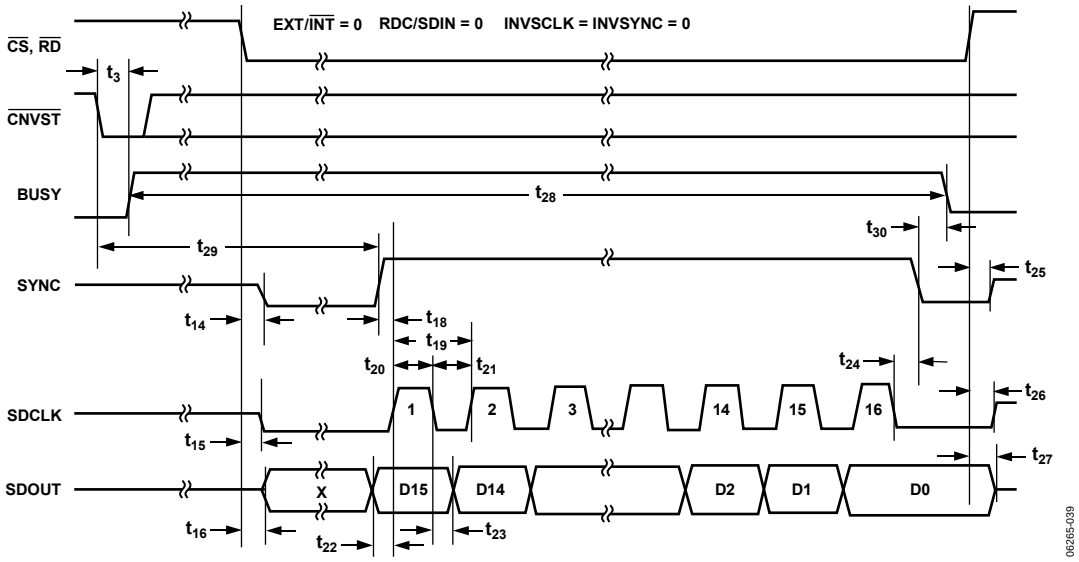



*Figure 39. Master Serial Data Timing for Reading (Read After Convert)*

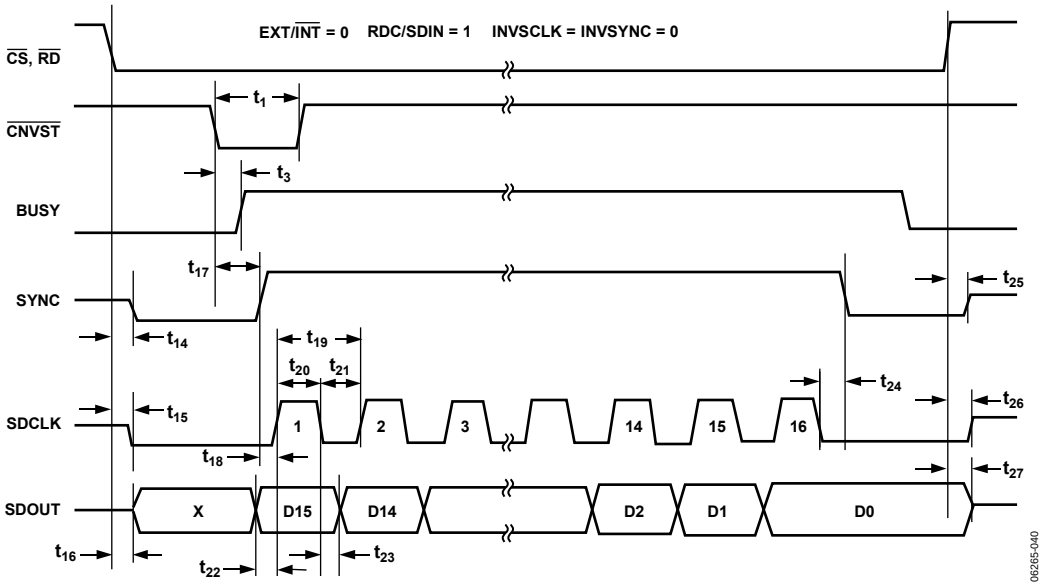



*Figure 40. Master Serial Data Timing for Reading (Read Previous Conversion During Convert)*

## SLAVE SERIAL INTERFACE

The pins multiplexed on D[11:4] used for slave serial interface are: EXT/$\overline{\text{INT}}$, INVSCLK, SDIN, SDOUT, SDCLK and RDERROR.

### *External Clock (SER/$\overline{\text{PAR}}$ = High, EXT/$\overline{\text{INT}}$ = High)*

Setting the EXT/$\overline{\text{INT}}$ = high allows the AD7612 to accept an externally supplied serial data clock on the SDCLK pin. In this mode, several methods can be used to read the data. The external serial clock is gated by $\overline{\text{CS}}$. When $\overline{\text{CS}}$ and $\overline{\text{RD}}$ are both low, the data can be read after each conversion or during the following conversion. A clock can be either normally high or normally low when inactive. For detailed timing diagrams, see Figure 42 and Figure 43.

While the AD7612 is performing a bit decision, it is important that voltage transients be avoided on digital input/output pins, or degradation of the conversion result may occur. This is particularly important during the last 475 ns of the conversion phase because the AD7612 provides error correction circuitry that can correct for an improper bit decision made during the first part of the conversion phase. For this reason, it is recommended that any external clock provided, is a discontinuous clock that transitions only when BUSY is low, or, more importantly, that it does not transition during the last 475 ns of BUSY high.

### *External Discontinuous Clock Data Read After Conversion*

Though the maximum throughput cannot be achieved using this mode, it is the most recommended of the serial slave modes. Figure 42 shows the detailed timing diagrams for this method. After a conversion is complete, indicated by BUSY returning low, the conversion result can be read while both $\overline{\text{CS}}$ and $\overline{\text{RD}}$ are low. Data is shifted out MSB first with 16 clock pulses and, depending on the SDCLK frequency, can be valid on the falling and rising edges of the clock.

One advantage of this method is that conversion performance is not degraded because there are no voltage transients on the digital interface during the conversion process. Another advantage is the ability to read the data at any speed up to 40 MHz, which accommodates both the slow digital host interface and the fastest serial reading.

### *Daisy-Chain Feature*

Also in the read after convert mode, the AD7612 provides a daisy-chain feature for cascading multiple converters together using the serial data input, SDIN, pin. This feature is useful for reducing component count and wiring connections when desired, for instance, in isolated multiconverter applications. See Figure 42 for the timing details.

An example of the concatenation of two devices is shown in Figure 41. Simultaneous sampling is possible by using a common $\overline{\text{CNVST}}$ signal. Note that the SDIN input is latched on the opposite edge of SDCLK used to shift out the data on SDOUT (SDCLK falling edge when INVSCLK = low). Therefore, the MSB of the upstream converter follows the LSB of the downstream converter on the next SDCLK cycle. In this mode, the 40 MHz SDCLK rate cannot be used since the SDIN to SDCLK setup time, $t_{33}$, is less than the minimum time specified. (SDCLK to SDOUT delay, $t_{32}$, is the same for all converters when simultaneously sampled). For proper operation, the SDCLK edge for latching SDIN (or ½ period of SDCLK) needs to be:

$$t_{1/2SDCLK} = t_{32} + t_{33}$$

Or the max SDCLK frequency needs to be:

$$f_{SDCLK} = \frac{1}{2(t_{32} + t_{33})}$$

If not using the daisy-chain feature, the SDIN input should be tied either high or low.

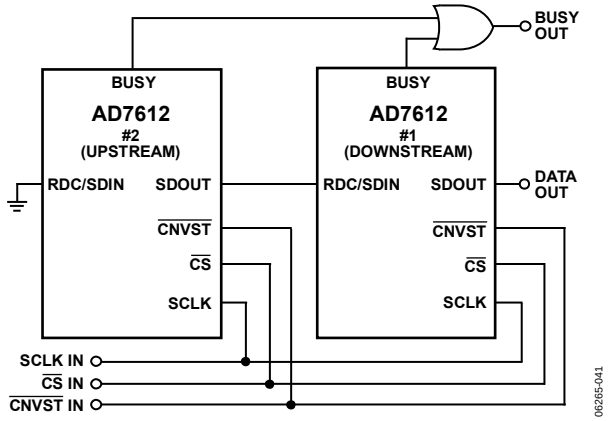



*Figure 41. Two AD7612 Devices in a Daisy-Chain Configuration*

### *External Clock Data Read During Previous Conversion*

Figure 43 shows the detailed timing diagrams for this method. During a conversion, while both $\overline{\text{CS}}$ and $\overline{\text{RD}}$ are low, the result of the previous conversion can be read. Data is shifted out MSB first with 16 clock pulses and, depending on the SDCLK frequency, can be valid on the falling and rising edges of the clock. The 16 bits have to be read before the current conversion is complete; otherwise, RDERROR is pulsed high and can be used to interrupt the host interface to prevent incomplete data reading.

To reduce performance degradation due to digital activity, a fast discontinuous clock of at least 40 MHz is recommended to ensure that all the bits are read during the first half of the SAR conversion phase.

The daisy-chain feature should not be used in this mode since digital activity occurs during the second half of the SAR conversion phase likely resulting in performance degradation.

### *External Clock Data Read After/During Conversion*

It is also possible to begin to read data after conversion and continue to read the last bits after a new conversion has been initiated. This method allows the full throughput and the use of a slower SDCLK frequency. Again, it is recommended to use a discontinuous SDCLK whenever possible to minimize potential incorrect bit decisions. For the different modes, the use of a slower SDCLK such as 20 MHz in warp mode, 15 MHz in normal mode and 13 MHz in impulse mode can be used.

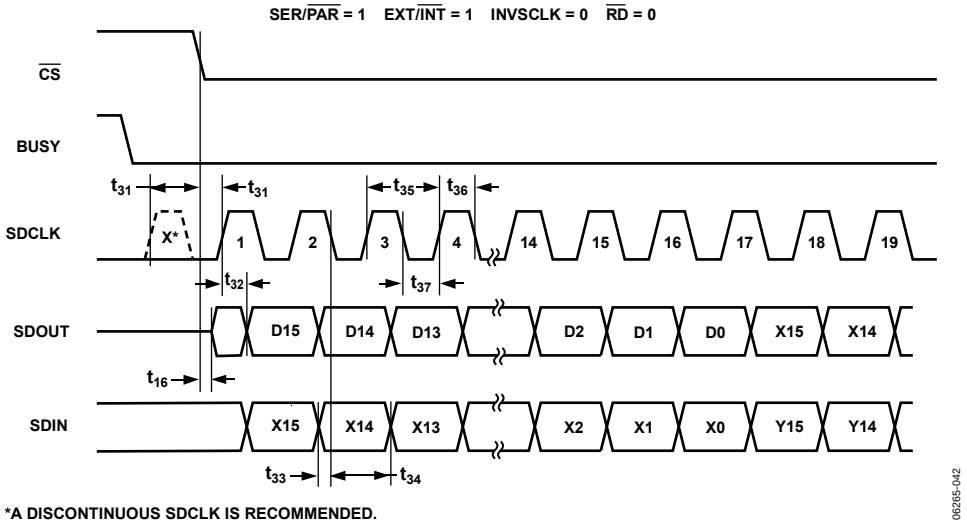



*Figure 42. Slave Serial Data Timing for Reading (Read After Convert)*

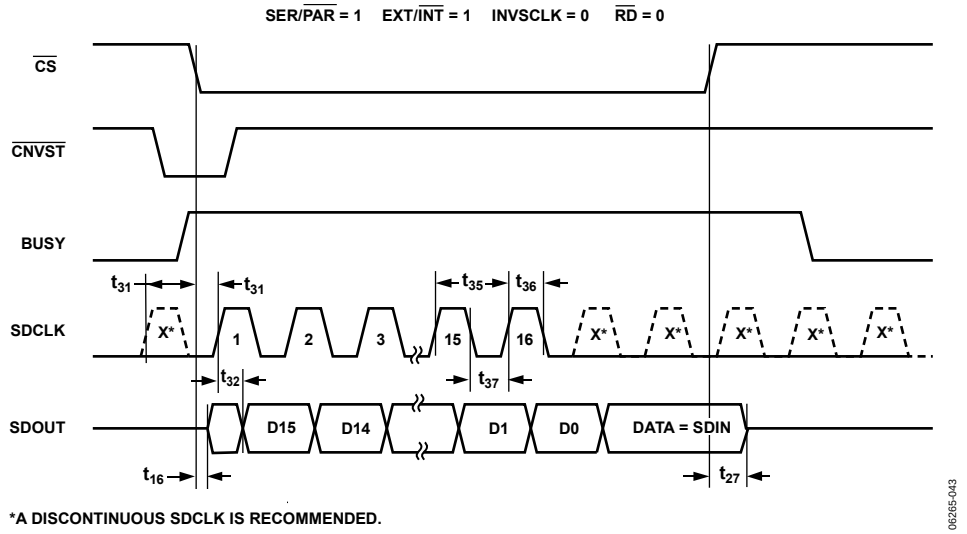



*Figure 43. Slave Serial Data Timing for Reading (Read Previous Conversion During Convert)*

## HARDWARE CONFIGURATION

The AD7612 can be configured at any time with the dedicated hardware pins WARP, IMPULSE, BIPOLAR, TEN, OB/$\overline{2C}$, and PD for parallel mode (SER/$\overline{PAR}$ = low) or serial hardware mode (SER/ $\overline{PAR}$ = high, HW/$\overline{SW}$ = high). Programming the AD7612 for mode selection and input range configuration can be done before or during conversion. Like the RESET input, the ADC requires at least one acquisition time to settle as indicated in Figure 44. See Table 6 for pin descriptions. Note that these inputs are high impedance when using the software configuration mode.

## SOFTWARE CONFIGURATION

The pins multiplexed on D[15:12] used for software configuration are: HW/$\overline{SW}$, SCIN, SCCLK, and $\overline{SCCS}$. The AD7612 is programmed using the dedicated write-only serial configurable port (SCP) for conversion mode, input range selection, output coding, and power-down using the serial configuration register. See Table 9 for details of each bit in the configuration register. The SCP can only be used in serial software mode selected with SER/$\overline{PAR}$ = high and HW/$\overline{SW}$ = low since the port is multiplexed on the parallel interface.

The SCP is accessed by asserting the port's chip select, $\overline{SCCS}$, and then writing SCIN synchronized with SCCLK, which (like SDCLK) is edge sensitive depending on the state of INVSCLK. See Figure 45 for timing details. SCIN is clocked into the configuration register MSB first. The configuration register is an internal shift register that begins with Bit 8, the start bit. The 9$^{th}$ SPPCLK edge updates the register and allows the new settings to be used. As indicated in the timing diagram, at least one acquisition time is required from the 9$^{th}$ SCCLK edge. Bits [1:0] are reserved bits and are not written to while the SCP is being updated.

The SCP can be written to at any time, up to 40 MHz, and it is recommended to write to while the AD7612 is not busy converting, as detailed in Figure 45. In this mode, the full 750 kSPS is not attainable because the time required for SCP access is ($t_{31}$ + 8 × 1/SCCLK +$t_8$) minimum. If the full throughput is required, the SCP can be written to during conversion, however it is not recommended to write to the SCP during the last 475 ns of conversion (BUSY = high) or performance degradation can result. In addition, the SCP can be accessed in both serial master and serial slave read during and read after convert modes.

Note that at power up, the configuration register is undefined. The RESET input clears the configuration register (sets all bits to 0), thus placing the configuration to 0 V to 5 V input, normal mode, and twos complemented output.

**Table 9. Configuration Register Description**

| Bit | Name | Description |
|---|---|---|
| 8 | START | START bit. With the SCP enabled ($\overline{SCCS}$ = low), when START is high, the first rising edge of SCCLK (INVSCLK = low) begins to load the register with the new configuration. |
| 7 | BIPOLAR | Input Range Select. Used in conjunction with Bit 6, TEN, per the following:<br>**Input Range / BIPOLAR / TEN**<br>0 V to 5 V / Low / Low<br>0 V to 10 V / Low / High<br>±5 V / High / Low<br>±10 V / Low / High |
| 6 | TEN | Input Range Select. See Bit 7, BIPOLAR. |
| 5 | PD | Power Down.<br>PD = Low, normal operation.<br>PD = High, power down the ADC. The SCP is accessible while in power down. To power up the ADC, write PD = low on the next configuration setting. |
| 4 | IMPULSE | Mode Select. Used in conjunction with Bit 3, WARP per the following:<br>**Mode / WARP / IMPULSE**<br>Normal / Low / Low<br>Impulse / Low / High<br>Warp / High / Low<br>Normal / High / High |
| 3 | WARP | Mode Select. See Bit 4, IMPULSE. |
| 2 | OB/$\overline{2C}$ | Output Coding<br>OB/$\overline{2C}$ = Low, use twos complement output.<br>OB/$\overline{2C}$ = High, use straight binary output. |
| 1 | RSV | Reserved. |
| 0 | RSV | Reserved. |

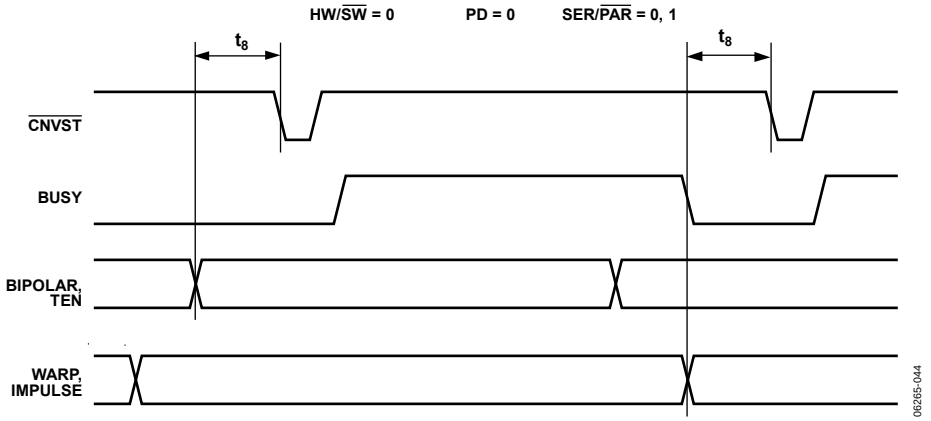



*Figure 44. Hardware Configuration Timing*

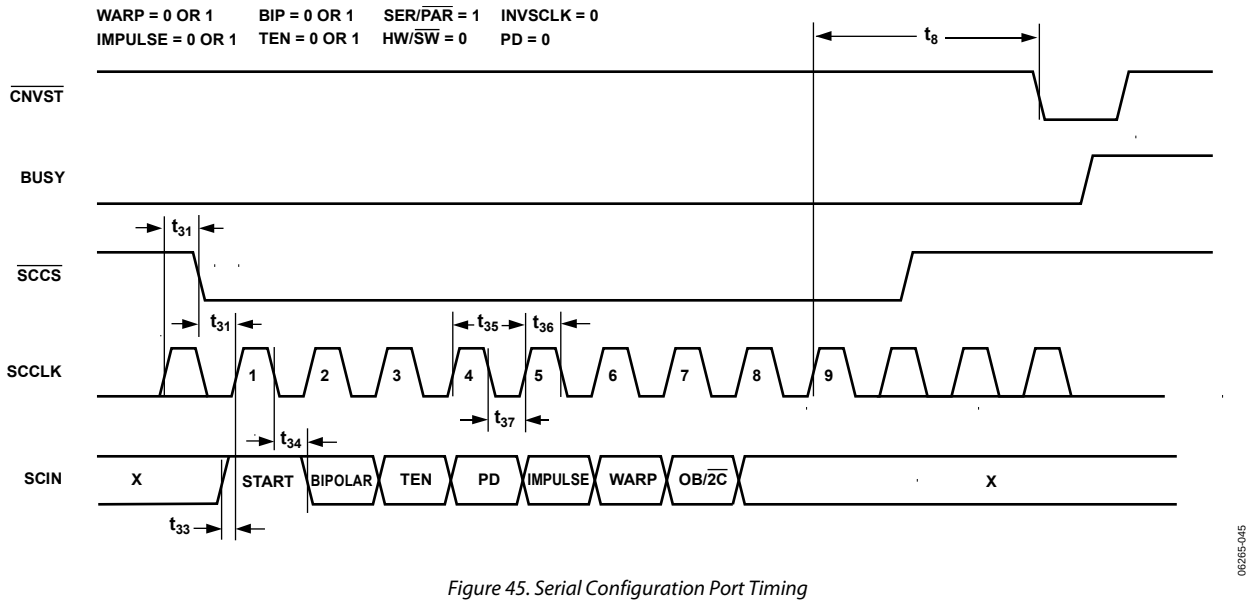



*Figure 45. Serial Configuration Port Timing*

## MICROPROCESSOR INTERFACING

The AD7612 is ideally suited for traditional dc measurement applications supporting a microprocessor, and ac signal processing applications interfacing to a digital signal processor. The AD7612 is designed to interface with a parallel 8-bit or 16-bit wide interface, or with a general-purpose serial port or I/O ports on a microcontroller. A variety of external buffers can be used with the AD7612 to prevent digital noise from coupling into the ADC.

### *SPI Interface*

The AD7612 is compatible with SPI and QSPI digital hosts and DSPs such as Blackfin® ADSP-BF53x and ADSP-218x/ADSP-219x. Figure 46 shows an interface diagram between the AD7612 and the SPI-equipped ADSP-219x. To accommodate the slower speed of the DSP, the AD7612 acts as a slave device, and data must be read after conversion. This mode also allows the daisy-chain feature. The convert command could be initiated in response to an internal timer interrupt.

The reading process can be initiated in response to the end-of-conversion signal (BUSY going low) using an interrupt line of the DSP. The serial peripheral interface (SPI) on the ADSP-219x is configured for master mode (MSTR) = 1, clock polarity bit (CPOL) = 0, clock phase bit (CPHA) = 1, and SPI interrupt enable (TIMOD) = 0 by writing to the SPI control register (SPICLTx).

It should be noted that to meet all timing requirements, the SPI clock should be limited to 17 Mbps allowing it to read an ADC result in less than 1 µs. When a higher sampling rate is desired, use one of the parallel interface modes.

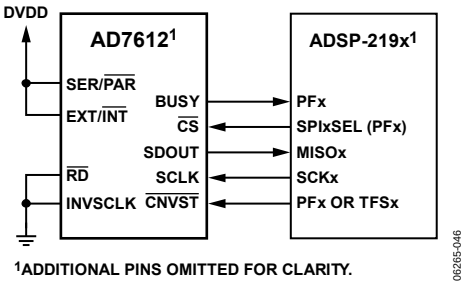



*Figure 46. Interfacing the AD7612 to SPI Interface*

# APPLICATION INFORMATION

## LAYOUT GUIDELINES

While the AD7612 has very good immunity to noise on the power supplies, exercise care with the grounding layout. To facilitate the use of ground planes that can be easily separated, design the printed circuit board that houses the AD7612 so that the analog and digital sections are separated and confined to certain areas of the board. Digital and analog ground planes should be joined in only one place, preferably underneath the AD7612, or as close as possible to the AD7612. If the AD7612 is in a system where multiple devices require analog-to-digital ground connections, the connections should still be made at one point only, a star ground point, established as close as possible to the AD7612.

To prevent coupling noise onto the die, avoid radiating noise, and to reduce feedthrough:

- Do not run digital lines under the device.
- Do run the analog ground plane under the AD7612.
- Do shield fast switching signals, like $\overline{\text{CNVST}}$ or clocks, with digital ground to avoid radiating noise to other sections of the board, and never run them near analog signal paths.
- Avoid crossover of digital and analog signals.
- Run traces on different but close layers of the board, at right angles to each other, to reduce the effect of feedthrough through the board.

The power supply lines to the AD7612 should use as large a trace as possible to provide low impedance paths and reduce the effect of glitches on the power supply lines. Good decoupling is also important to lower the impedance of the supplies presented to the AD7612, and to reduce the magnitude of the supply spikes. Decoupled ceramic capacitors, typically 100 nF, should be placed on each of the power supplies pins, AVDD, DVDD, and OVDD, VCC, and VEE. The capacitors should be placed close to, and ideally right up against, these pins and their corresponding ground pins. Additionally, low ESR 10 µF capacitors should be located in the vicinity of the ADC to further reduce low frequency ripple.

The DVDD supply of the AD7612 can be either a separate supply or come from the analog supply, AVDD, or from the digital interface supply, OVDD. When the system digital supply is noisy, or fast switching digital signals are present, and no separate supply is available, it is recommended to connect the DVDD digital supply to the analog supply AVDD through an RC filter, and to connect the system supply to the interface digital supply OVDD and the remaining digital circuitry. See Figure 27 for an example of this configuration. When DVDD is powered from the system supply, it is useful to insert a bead to further reduce high frequency spikes.

The AD7612 has four different ground pins: REFGND, AGND, DGND, and OGND.

- REFGND senses the reference voltage and, because it carries pulsed currents, should be a low impedance return to the reference.
- AGND is the ground to which most internal ADC analog signals are referenced; it must be connected with the least resistance to the analog ground plane.
- DGND must be tied to the analog or digital ground plane depending on the configuration.
- OGND is connected to the digital system ground.

The layout of the decoupling of the reference voltage is important. To minimize parasitic inductances, place the decoupling capacitor close to the ADC and connect it with short, thick traces.

## EVALUATING PERFORMANCE

A recommended layout for the AD7612 is outlined in the EVAL-AD7612EDZ evaluation board documentation. The evaluation board package includes a fully assembled and tested evaluation board, documentation, and software for controlling the board from a PC via the EVAL-CED1Z.

# OUTLINE DIMENSIONS

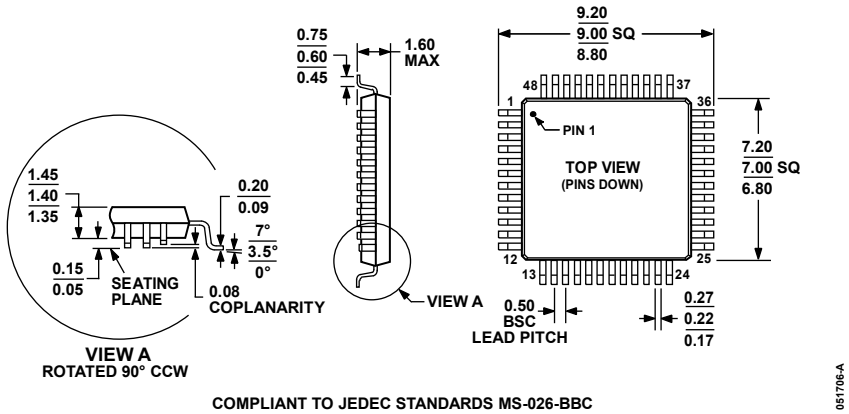



*Figure 47. 48-Lead Low Profile Quad Flat Package [LQFP]*
*(ST-48)*
*Dimensions shown in millimeters*

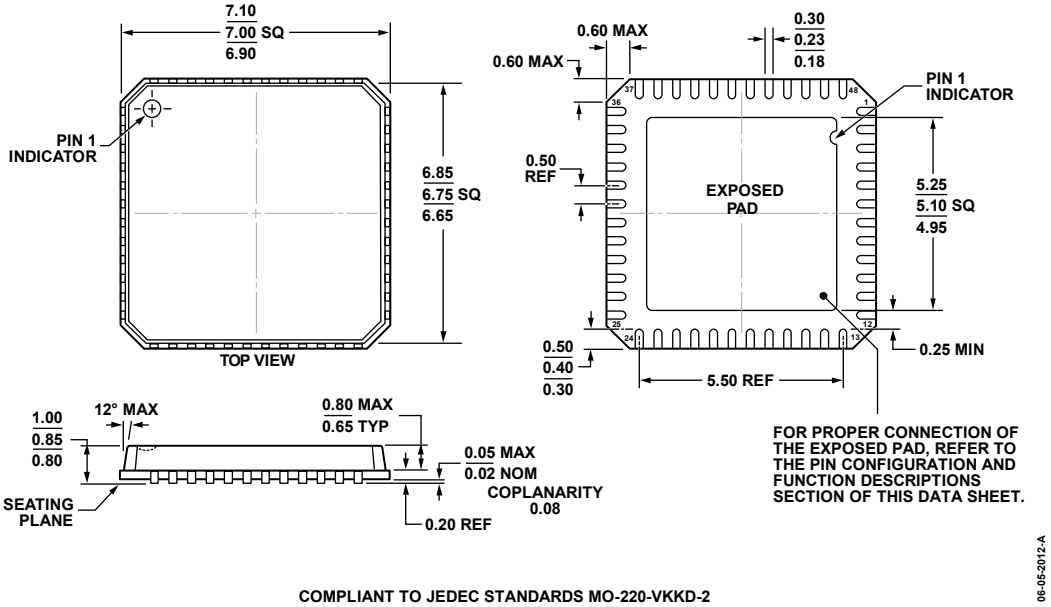



*Figure 48. 48-Lead Lead Frame Chip Scale Package [LFCSP_VQ]*
*7 mm × 7 mm Body, Very Thin Quad*
*(CP-48-1)*
*Dimensions shown in millimeters*

## ORDERING GUIDE

| Model[1] | Notes | Temperature Range | Package Description | Package Option |
|---|---|---|---|---|
| AD7612BCPZ | | −40°C to +85°C | 48-Lead Lead Frame Chip Scale Package (LFCSP_VQ) | CP-48-1 |
| AD7612BCPZ-RL | | −40°C to +85°C | 48-Lead Lead Frame Chip Scale Package (LFCSP_VQ) | CP-48-1 |
| AD7612BSTZ | | −40°C to +85°C | 48-Lead Low Profile Quad Flat Package (LQFP) | ST-48 |
| AD7612BSTZ-RL | | −40°C to +85°C | 48-Lead Low Profile Quad Flat Package (LQFP) | ST-48 |
| EVAL-AD7612EDZ | 2 | | Evaluation Board | |
| EVAL-CED1Z | 3 | | Converter Evaluation and Development Board | |

[1] Z = RoHS Compliant Part.
[2] This board can be used as a standalone evaluation board or in conjunction with the EVAL-CED1Z for evaluation/demonstration purposes.
[3] This board allows a PC to control and communicate with all Analog Devices evaluation boards ending with the ED designators.