AD7390/AD7391–SPECIFICATIONS

AD7390 ELECTRICAL CHARACTERISTICS (@ $V_{REF\ IN}$ = 2.5 V, –40°C < T_A < +85°C unless otherwise noted.)

Parameter	Symbol	Conditions	3 V ± 10%	5 V ± 10%	Unit
STATIC PERFORMANCE					
Resolution[1]	N		12	12	Bits
Relative Accuracy[2]	INL	T_A = 25°C	±1.6	±1.6	LSB max
	INL	T_A = −40°C, +85°C	±2.0	±2	LSB max
Differential Nonlinearity[2]	DNL	T_A = 25°C, Monotonic	±0.9	±0.9	LSB max
	DNL	Monotonic	±1	±1	LSB max
Zero-Scale Error	V_{ZSE}	Data = 000_H	4.0	4.0	mV max
Full-Scale Voltage Error	V_{FSE}	T_A = 25°C, 85°C, Data = FFF_H	±8	±8	mV max
	V_{FSE}	T_A = −40°C, Data = FFF_H	±20	±20	mV max
Full-Scale Tempco[3]	TCV_{FS}		16	16	ppm/°C typ
REFERENCE INPUT					
$V_{REF\ IN}$ Range	V_{REF}		0/V_{DD}	0/V_{DD}	V min/max
Input Resistance	R_{REF}		2.5	2.5	MΩ typ[4]
Input Capacitance[3]	C_{REF}		5	5	pF typ
ANALOG OUTPUT					
Output Current (Source)	I_{OUT}	Data = 800_H, ΔV_{OUT} = 5 LSB	1	1	mA typ
Output Current (Sink)	I_{OUT}	Data = 800_H, ΔV_{OUT} = 5 LSB	3	3	mA typ
Capacitive Load[3]	C_L	No Oscillation	100	100	pF typ
LOGIC INPUTS					
Logic Input Low Voltage	V_{IL}		0.5	0.8	V max
Logic Input High Voltage	V_{IH}		V_{DD} − 0.6	V_{DD} − 0.6	V min
Input Leakage Current	I_{IL}		10	10	µA max
Input Capacitance[3]	C_{IL}		10	10	pF max
INTERFACE TIMING[3, 5]					
Clock Width High	t_{CH}		50	30	ns min
Clock Width Low	t_{CL}		50	30	ns min
Load Pulsewidth	t_{LDW}		30	20	ns min
Data Setup	t_{DS}		10	10	ns min
Data Hold	t_{DH}		30	15	ns min
Clear Pulsewidth	t_{CLRW}		15	15	ns min
Load Setup	t_{LD1}		30	15	ns min
Load Hold	t_{LD2}		40	20	ns min
AC CHARACTERISTICS[6]					
Output Slew Rate	SR	Data = 000_H to FFF_H to 000_H	0.05	0.05	V/µs typ
Settling Time	t_S	To ±0.1% of Full Scale	70	60	µs typ
DAC Glitch	Q	Code $7FF_H$ to 800_H to $7FF_H$	65	65	nVs typ
Digital Feedthrough	Q		15	15	nVs typ
Feedthrough	V_{OUT}/V_{REF}	V_{REF} = 1.5 V_{DC} + 1 V p-p, Data = 000_H, f = 100 kHz	−63	−63	dB typ
SUPPLY CHARACTERISTICS					
Power Supply Range	$V_{DD\ RANGE}$	DNL < ±1 LSB	2.7/5.5	2.7/5.5	V min/max
Positive Supply Current	I_{DD}	V_{IL} = 0 V, No Load, T_A = 25°C	55	55	µA typ
	I_{DD}	V_{IL} = 0 V, No Load	100	100	µA max
Power Dissipation	P_{DISS}	V_{IL} = 0 V, No Load	300	500	µW max
Power Supply Sensitivity	PSS	ΔV_{DD} = ±5%	0.006	0.006	%/% max

NOTES

[1]One LSB = V_{REF}/4096 V for the 12-bit AD7390.

[2]The first two codes (000_H, 001_H) are excluded from the linearity error measurement.

[3]These parameters are guaranteed by design and not subject to production testing.

[4]Typicals represent average readings measured at 25°C.

[5]All input control signals are specified with t_R = t_F = 2 ns (10% to 90% of 3 V) and timed from a voltage level of 1.6 V.

[6]The settling time specification does not apply for negative going transitions within the last 3 LSBs of ground.

Specifications subject to change without notice.

AD7391 ELECTRICAL CHARACTERISTICS (@ $V_{REF\ IN}$ = 2.5 V, −40°C < T_A < +85°C unless otherwise noted.)

Parameter	Symbol	Conditions	3 V ± 10%	5 V ± 10%	Unit
STATIC PERFORMANCE					
Resolution[1]	N		10	10	Bits
Relative Accuracy[2]	INL	T_A = 25°C	±1.75	±1.75	LSB max
	INL	T_A = −40°C, +85°C, +125°C	±2.0	±2.0	LSB max
	INL	T_A = −55°C, S Grade		±3	LSB max
Differential Nonlinearity[2]	DNL	Monotonic	±0.9	±0.9	LSB max
	DNL	T_A = −55°C, S Grade		±2	LSB max
Zero-Scale Error	V_{ZSE}	Data = 000_H	9.0	9.0	mV max
	V_{ZSE}	T_A = −55°C, S Grade		20	mV max
Full-Scale Error	V_{FSE}	T_A = 25°C, 85°C, 125°C, Data = $3FF_H$	±32	±32	mV max
	V_{FSE}	T_A = −55°C, S Grade		±55	mV max
Full-Scale Tempco[3]	TCV_{FS}		16	16	ppm/°C typ
	TCV_{FS}	T_A = −55°C, S Grade		32	ppm/°C typ
REFERENCE INPUT					
$V_{REF\ IN}$ Range	V_{REF}		0/V_{DD}	0/V_{DD}	V min/max
Input Resistance	R_{REF}		2.5	2.5	MΩ typ[4]
Input Capacitance[3]	C_{REF}		5	5	pF typ
ANALOG OUTPUT					
Output Current (Source)	I_{OUT}	Data = 800_H, ΔV_{OUT} = 5 LSB	1	1	mA typ
Output Current (Sink)	I_{OUT}	Data = 800_H, ΔV_{OUT} = 5 LSB	3	3	mA typ
Capacitive Load[3]	C_L	No Oscillation	100	100	pF typ
LOGIC INPUTS					
Logic Input Low Voltage	V_{IL}		0.5	0.8	V max
Logic Input High Voltage	V_{IH}		V_{DD} − 0.6	V_{DD} − 0.6	V min
Input Leakage Current	I_{IL}		10	10	µA max
Input Capacitance[3]	C_{IL}		10	10	pF max
INTERFACE TIMING[3, 5]					
Clock Width High	t_{CH}		50	30	ns
Clock Width Low	t_{CL}		50	30	ns
Load Pulsewidth	t_{LDW}		30	20	ns
Data Setup	t_{DS}		10	10	ns
Data Hold	t_{DH}		30	15	ns
Clear Pulsewidth	t_{CLRW}		15	15	ns
Load Setup	t_{LD1}		30	15	ns
Load Hold	t_{LD2}		40	20	ns
AC CHARACTERISTICS[6]					
Output Slew Rate	SR	Data = 000_H to $3FF_H$ to 000_H	0.05	0.05	V/µs typ
Settling Time	t_S	To ±0.1% of Full Scale	70	60	µs typ
	t_S	T_A = –55°C, S Grade		100	µs typ
DAC Glitch	Q	Code $7FF_H$ to 800_H to $7FF_H$	65	65	nVs typ
Digital Feedthrough	Q		15	15	nVs typ
Feedthrough	V_{OUT}/V_{REF}	V_{REF} = 1.5 V_{DC} +1 V p-p, Data = 000_H, f = 100 kHz	−63	−63	dB typ
SUPPLY CHARACTERISTICS					
Power Supply Range	$V_{DD\ RANGE}$	DNL < ±1 LSB	2.7/5.5	2.7/5.5	V min/max
Positive Supply Current	I_{DD}	V_{IL} = 0 V, No Load, T_A = 25°C	55	55	µA typ
	I_{DD}	V_{IL} = 0 V, No Load	100	100	µA max
Power Dissipation	P_{DISS}	V_{IL} = 0 V, No Load	300	500	µW max
Power Supply Sensitivity	PSS	ΔV_{DD} = ±5%	0.006	0.006	%/% max

NOTES
[1]One LSB = V_{REF}/1024 V for the 10-bit AD7391.
[2]The first two codes (000_H, 001_H) are excluded from the linearity error measurement.
[3]These parameters are guaranteed by design and not subject to production testing.
[4]Typicals represent average readings measured at 25°C.
[5]All input control signals are specified with t_R = t_F = 2 ns (10% to 90% of +3 V) and timed from a voltage level of 1.6 V.
[6]The settling time specification does not apply for negative going transitions within the last 3 LSBs of ground.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

V_{DD} to GND ..... −0.3 V, +8 V
V_{REF} to GND ..... +0.3 V, V_{DD} + 0.3 V
Logic Inputs to GND ..... −0.3 V, +8 V
V_{OUT} to GND ..... −0.3 V, V_{DD} + 0.3 V
I_{OUT} Short Circuit to GND ..... 50 mA
Package Power Dissipation ..... $(T_{J\,MAX} - T_A)/\theta_{JA}$
Thermal Resistance θ_{JA}
8-Lead Plastic DIP Package (N-8) ..... 103°C/W
8-Lead SOIC Package (SO-8) ..... 158°C/W
TSSOP-8 Package (RU-8) ..... 240°C/W
Maximum Junction Temperature ($T_{J\,MAX}$) ..... 150°C
Operating Temperature Range ..... −40°C to +85°C
AD7391AR ..... −40°C to +125°C
Storage Temperature Range ..... −65°C to +150°C
Lead Temperature (Soldering, 10 secs) ..... 300°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational specification is not implied. Exposure to the above maximum rating conditions for extended periods may affect device reliability.

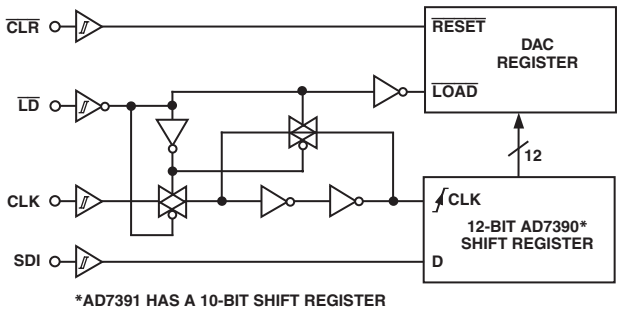
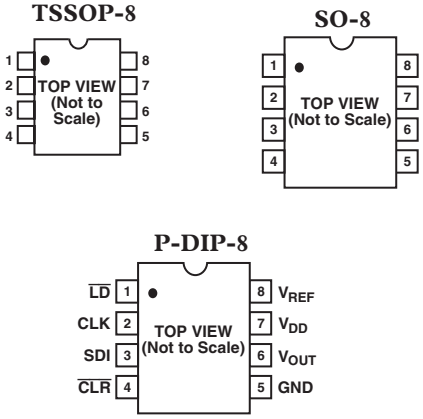


Figure 3. Digital Control Logic

PIN CONFIGURATIONS



PIN DESCRIPTIONS

Pin No.	Name	Function
1	$\overline{LD}$	Load Strobe. Transfers shift register data to DAC register while active low. See truth table for operation.
2	CLK	Clock Input. Positive edge clocks data into shift register.
3	SDI	Serial Data Input. Data loads directly into the shift register.
4	$\overline{CLR}$	Resets DAC register to zero condition. Active low input.
5	GND	Analog and Digital Ground.
6	V_{OUT}	DAC Voltage Output. Full-scale output 1 LSB less than reference input voltage REF.
7	V_{DD}	Positive Power Supply Input. Specified range of operation 2.7 V to 5.5 V.
8	V_{REF}	DAC Reference Input Pin. Establishes DAC full-scale voltage.

ORDERING GUIDE[1]

Model	Resolution	Temperature Range	Package Description	Package Option	Top Mark[2]	Number of Devices Per Container
AD7390AN	12	−40°C to +85°C	8-Lead P-DIP	N-8	AD7390[2]	50
AD7390AR	12	−40°C to +85°C	8-Lead SOIC	SO-8	AD7390[3]	196
AD7390AR-REEL7	12	−40°C to +85°C	8-Lead SOIC	SO-8	AD7390[3]	1000
AD7391AN	10	−40°C to +85°C	8-Lead P-DIP	N-8	AD7391[2]	50
AD7391AR	10	−40°C to +125°C	8-Lead SOIC	SO-8	AD7391[3]	196
AD7391SR	10	−55°C to +125°C	8-Lead SOIC	SO-8	AD7391[3]	39
AD7391ARU-REEL	10	−40°C to +85°C	TSSOP-8	RU-8	AD7391A[4]	2500

NOTES
[1]The AD7390 contains 588 transistors. The die size measures 70 mm × 68 mm.
[2]Line 1 contains ADI logo symbol and part number. Line 2 contains grade and date code YWW. Line 3 contains the letter G plus the 4-digit lot number.
[3]Line 1 contains part number. Line 2 contains grade and date code YWW. Line 3 contains the letter G plus the 4-digit lot number and the ADI logo symbol.
[4]Line 1 contains the date code YWW. Line 2 contains the 4-digit part number plus grade.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7390/AD7391 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

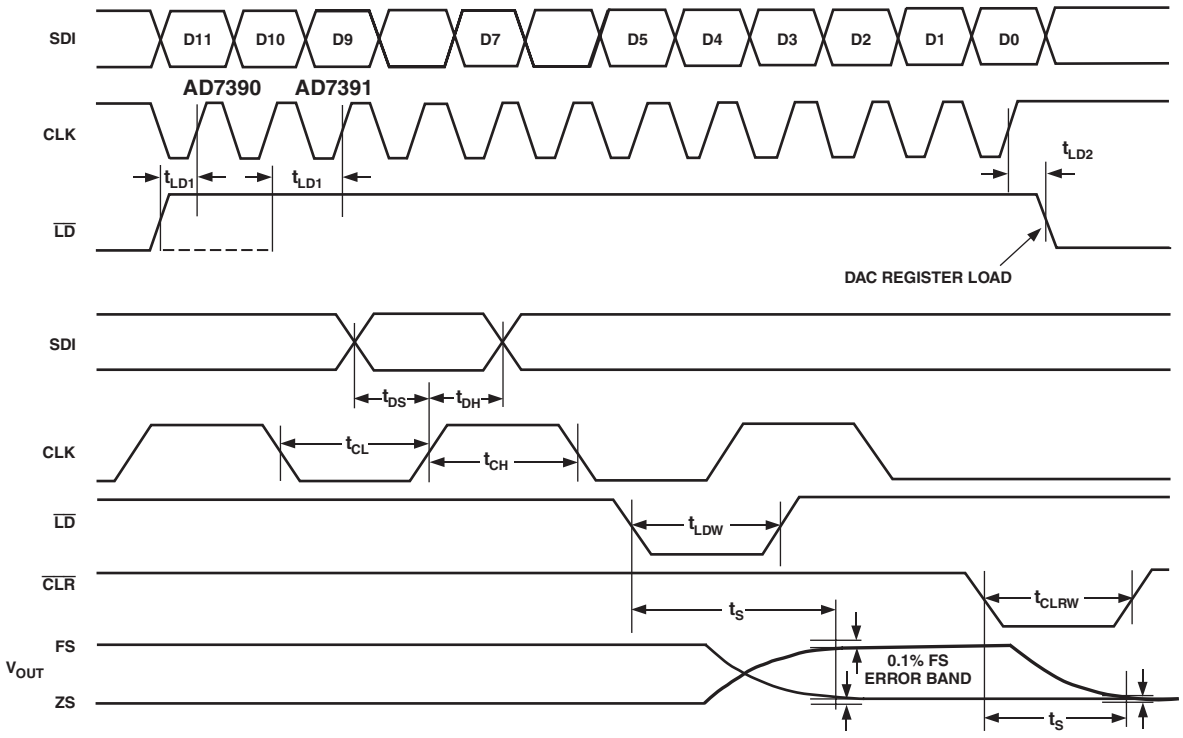


Figure 4. Timing Diagram

Table I. Control-Logic Truth Table

CLK	$\overline{CLR}$	$\overline{LD}$	Serial Shift Register Function	DAC Register Function
↑	H	H	Shift-Register-Data Advanced One-Bit	Latched
X	H	L	Disables	Updated with Current Shift Register Contents
X	L	X	No Effect	Loaded with all Zeros
X	↑	H	No Effect	Latched with all Zeros
X	↑	L	Disabled	Previous SR Contents Loaded (Avoid usage of $\overline{CLR}$ when $\overline{LD}$ is logic low, since SR data could be corrupted if a clock edge takes place, while $\overline{CLR}$ returns high.)

↑ = Positive logic transition.
X = Don't care.

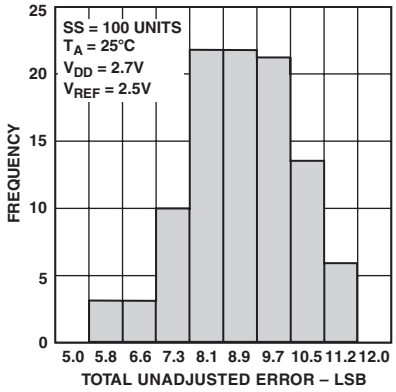
Table II. AD7390 Serial Input Register Data Format, Data is Loaded in the MSB-First Format

	MSB											LSB
	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
AD7390	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

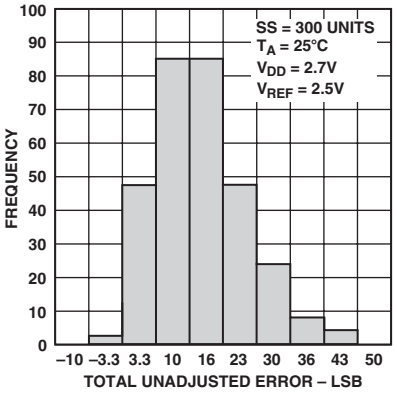
Table III. AD7391 Serial Input Register Data Format, Data is Loaded in the MSB-First Format

	MSB									LSB
	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
AD7391	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

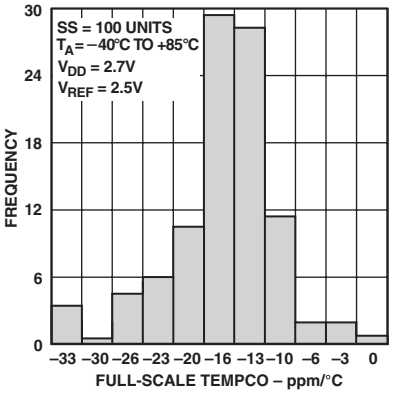
AD7390/AD7391–Typical Performance Characteristics



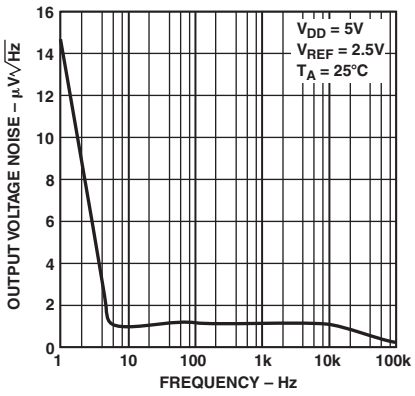
TPC 1. AD7390 Total Unadjusted Error Histogram



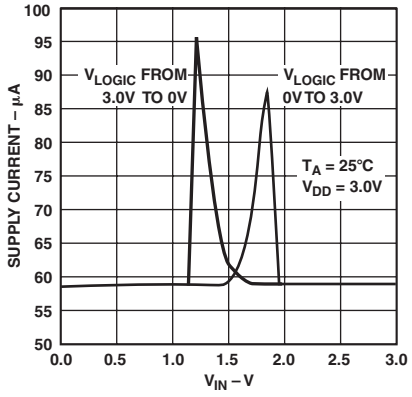
TPC 2. AD7391 Total Unadjusted Error Histogram



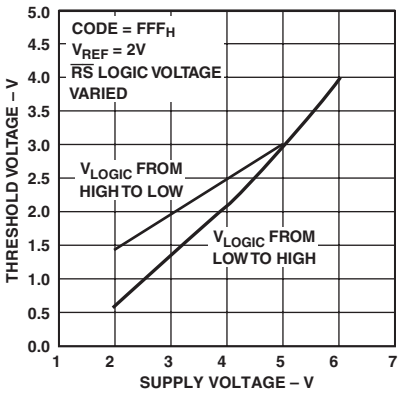
TPC 3. AD7391 Full-Scale Output Tempco Histogram



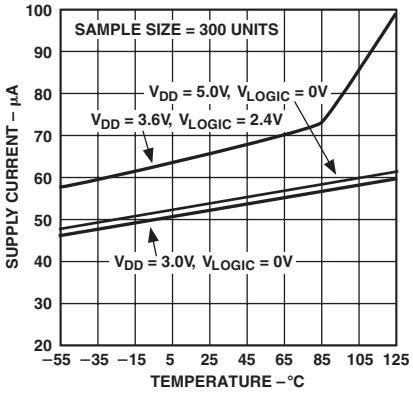
TPC 4. AD7390 Voltage Noise Density vs. Frequency



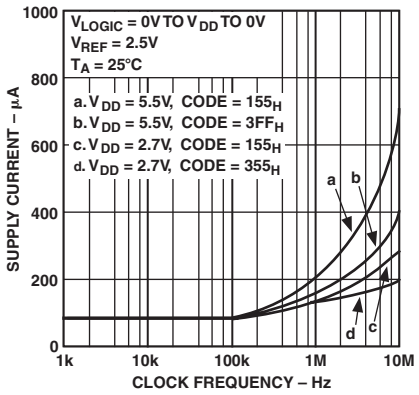
TPC 5. AD7390 Supply Current vs. Logic Input Voltage



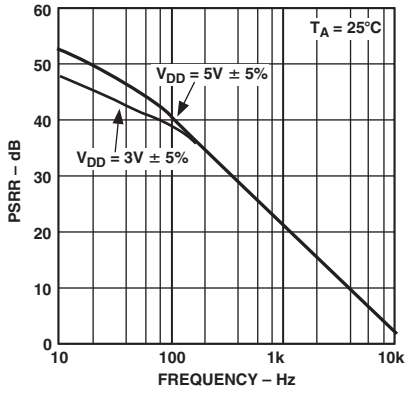
TPC 6. AD7390 Logic Threshold vs. Supply Voltage



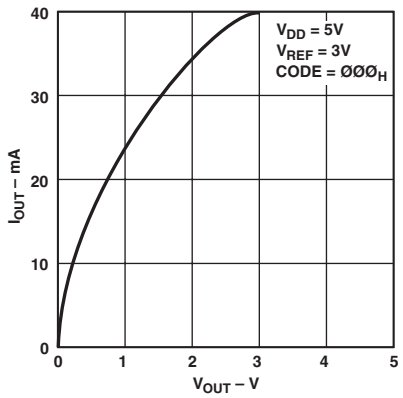
TPC 7. AD7390 Supply Current vs. Temperature



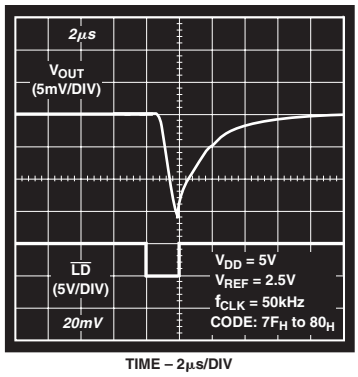
TPC 8. AD7391 Supply Current vs. Clock Frequency



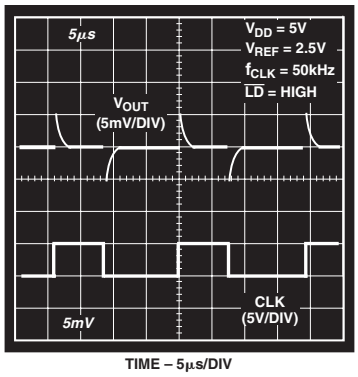
TPC 9. Power Supply Rejection vs. Frequency



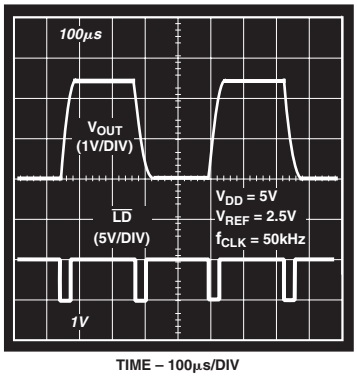
TPC 10. I_{OUT} at Zero Scale vs. V_{OUT}



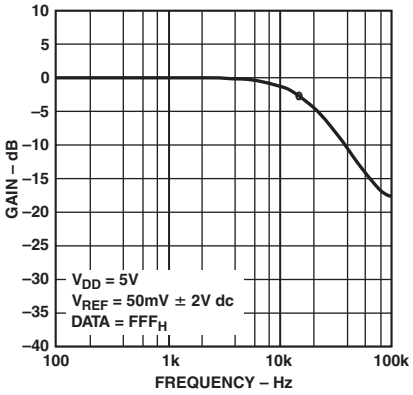
TPC 11. AD7390 Midscale Transition Performance



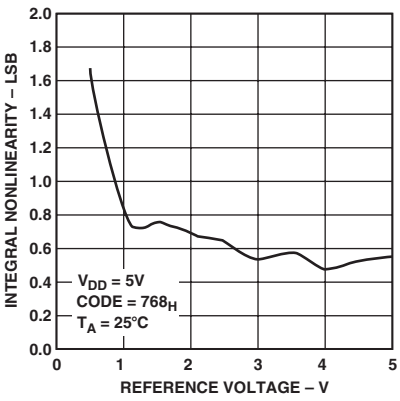
TPC 12. Digital Feedthrough



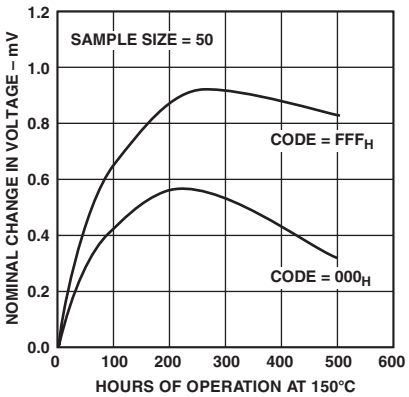
TPC 13. AD7390 Large Signal Settling Time



TPC 14. AD7390 Gain vs. Frequency



TPC 15. AD7390 INL Error vs. Reference Voltage



TPC 16. AD7390 Long-Term Drift Accelerated by Burn-In

OPERATION

The AD7390 and AD7391 are a set of pin compatible, 12-bit/10-bit digital-to-analog converters. These single-supply operation devices consume less than 100 microamps of current while operating from power supplies in the 2.7 V to 5.5 V range making them ideal for battery operated applications. They contain a voltage-switched, 12-bit/10-bit, laser-trimmed digital-to-analog converter, rail-to-rail output op amps, serial-input register, and a DAC register. The external reference input has constant input resistance independent of the digital code setting of the DAC. In addition, the reference input can be tied to the same supply voltage as V_{DD} resulting in a maximum output voltage span of 0 to V_{DD}. The SPI compatible, serial-data interface consists of a serial data input (SDI), clock (CLK), and load ($\overline{LD}$) pins. A $\overline{CLR}$ pin is available to reset the DAC register to zero-scale. This function is useful for power-on reset or system failure recovery to a known state.

D/A CONVERTER SECTION

The voltage switched R-2R DAC generates an output voltage dependent on the external reference voltage connected to the V_{REF} pin according to the following equation:

$$V_{OUT} = V_{REF} \times \frac{D}{2^N} \quad (1)$$

where D is the decimal data word loaded into the DAC register, and N is the number of bits of DAC resolution. In the case of the 10-bit AD7391 using a 2.5 V reference, Equation 1 simplifies to:

$$V_{OUT} = 2.5 \times \frac{D}{1024} \quad (2)$$

Using Equation 2 the nominal midscale voltage at V_{OUT} is 1.25 V for D = 512; full-scale voltage is 2.497 V. The LSB step size is = 2.5 × 1/1024 = 0.0024 V.

For the 12-bit AD7390 operating from a 5.0 V reference Equation 1 becomes:

$$V_{OUT} = 5.0 \times \frac{D}{4096} \quad (3)$$

Using Equation 3 the AD7390 provides a nominal midscale voltage of 2.5 V for D = 2048, and a full-scale output of 4.998 V. The LSB step size is = 5.0 × 1/4096 = 0.0012 V.

AMPLIFIER SECTION

The internal DAC's output is buffered by a low power consumption precision amplifier. The op amp has a 60 µs typical settling time to 0.1% of full scale. There are slight differences in settling time for negative slewing signals versus positive. Also, negative transition settling time to within the last 6 LSBs of zero volts has an extended settling time. The rail-to-rail output stage of this amplifier has been designed to provide precision performance while operating near either power supply. Figure 5 shows an equivalent output schematic of the rail-to-rail amplifier with its N-channel pull-down FETs that will pull an output load directly to GND. The output sourcing current is provided by a P-channel pull-up device that can source current to GND terminated loads.

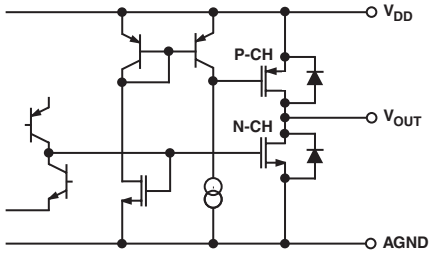


Figure 5. Equivalent Analog Output Circuit

The rail-to-rail output stage provides ±1 mA of output current. The N-channel output pull-down MOSFET shown in Figure 5 has a 35 Ω ON resistance, which sets the sink current capability near ground. In addition to resistive load driving capability, the amplifier has also been carefully designed and characterized for up to 100 pF capacitive load driving capability.

REFERENCE INPUT

The reference input terminal has a constant input-resistance independent of digital code which results in reduced glitches on the external reference voltage source. The high 2 MΩ input-resistance minimizes power dissipation within the AD7390/AD7391 D/A converters. The V_{REF} input accepts input voltages ranging from ground to the positive-supply voltage V_{DD}. One of the simplest applications which saves an external reference voltage source is connection of the V_{REF} terminal to the positive V_{DD} supply. This connection results in a rail-to-rail voltage output span maximizing the programmed range. The reference input will accept ac signals as long as they are kept within the supply voltage range, $0 < V_{REF\,IN} < V_{DD}$. The reference bandwidth and integral nonlinearity error performance are plotted in the typical performance section (see TPCs 14 and 15). The ratiometric reference feature makes the AD7390/AD7391 an ideal companion to ratiometric analog-to-digital converters such as the AD7896.

POWER SUPPLY

The very low power consumption of the AD7390/AD7391 is a direct result of a circuit design optimizing the use of a CBCMOS process. By using the low power characteristics of CMOS for the logic, and the low noise, tight-matching of the complementary bipolar transistors, excellent analog accuracy is achieved. One advantage of the rail-to-rail output amplifiers used in the AD7390/AD7391 is the wide range of usable supply voltage. The part is fully specified and tested for operation from 2.7 V to 5.5 V.

POWER SUPPLY BYPASSING AND GROUNDING

Precision analog products, such as the AD7390/AD7391, require a well filtered power source. Since the AD7390/AD7391 operates from a single 3 V to 5 V supply, it seems convenient to simply tap into the digital logic power supply. Unfortunately, the logic supply is often a switch-mode design, which generates noise in the 20 kHz to 1 MHz range. In addition, fast logic gates can generate glitches hundred of millivolts in amplitude due to wiring resistance and inductance. The power supply noise generated thereby means that special care must be taken to assure that the inherent precision of the DAC is maintained. Good engineering judgment should be exercised when addressing the power supply grounding and bypassing of the AD7390.

The AD7390 should be powered directly from the system power supply. This arrangement, shown in Figure 6, employs an LC filter and separate power and ground connections to isolate the analog section from the logic switching transients.

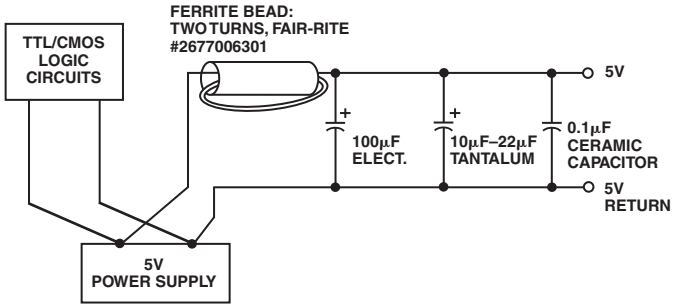


Figure 6. Use Separate Traces to Reduce Power Supply Noise

Whether or not a separate power supply trace is available, however, generous supply bypassing will reduce supply-line induced errors. Local supply bypassing consisting of a 10 µF tantalum electrolytic in parallel with a 0.1 µF ceramic capacitor is recommended in all applications (Figure 7).

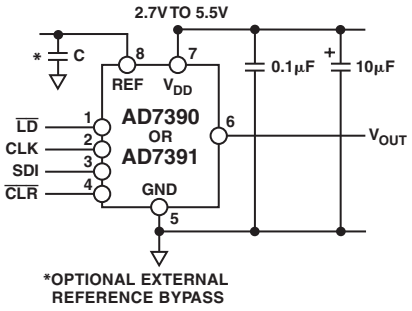


Figure 7. Recommended Supply Bypassing

INPUT LOGIC LEVELS

All digital inputs are protected with a Zener-type ESD protection structure (Figure 8) that allows logic input voltages to exceed the V_{DD} supply voltage. This feature can be useful if the user is driving one or more of the digital inputs with a 5 V CMOS logic input-voltage level while operating the AD7390/AD7391 on a 3 V power supply. If this mode of interface is used, make sure that the V_{OL} of the 5 V CMOS meets the V_{IL} input requirement of the AD7390/AD7391 operating at 3 V. See TPC 6 for a graph for digital logic input threshold versus operating V_{DD} supply voltage.

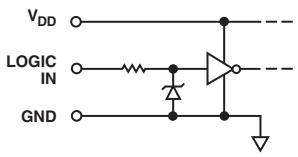


Figure 8. Equivalent Digital Input ESD Protection

In order to minimize power dissipation from input-logic levels that are near the V_{IH} and V_{IL} logic input voltage specifications, a Schmitt trigger design was used that minimizes the input-buffer current consumption compared to traditional CMOS input stages. TPC 5 shows a plot of incremental input voltage versus supply current showing that negligible current consumption takes place when logic levels are in their quiescent state. The normal crossover current still occurs during logic transitions. A secondary advantage of this Schmitt trigger is the prevention of false triggers that would occur with slow moving logic transitions when a standard CMOS logic interface or opto isolators are used. The logic inputs SDI, CLK, $\overline{LD}$, $\overline{CLR}$ all contain the Schmitt trigger circuits.

DIGITAL INTERFACE

The AD7390/AD7391 have a double-buffered serial data input. The serial-input register is separate from the DAC register, which allows preloading of a new data value into the serial register without disturbing the present DAC values. A functional block diagram of the digital section is shown in Figure 4, while Table I contains the truth table for the control logic inputs. Three pins control the serial data input. Data at the Serial Data Input (SDI) is clocked into the shift register on the rising edge of CLK. Data is entered in MSB-first format. Twelve clock pulses are required to load the 12-bit AD7390 DAC value. If additional bits are clocked into the shift register, for example when a microcontroller sends two 8-bit bytes, the MSBs are ignored (Figure 9). The CLK pin is only enabled when Load ($\overline{LD}$) is high. The lower resolution 10-bit AD7391 contains a 10-bit shift register. The AD7391 is also loaded MSB first with 10 bits of data. Again if additional bits are clocked into the shift register, only the last 10 bits clocked in are used.

The Load pin ($\overline{LD}$) controls the flow of data from the shift register to the DAC register. After a new value is clocked into the serial-input register, it will be transferred to the DAC register by the negative transition of the Load pin ($\overline{LD}$).

BYTE 1								BYTE 0							
MSB							LSB	MSB							LSB
B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
X	X	X	X	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

D11–D0: 12-BIT AD7390 DAC VALUE; D9–D0: 10-BIT AD7391 DAC VALUE
X = DON'T CARE
THE MSB OF BYTE 1 IS THE FIRST BIT THAT IS LOADED INTO THE DAC

Figure 9. Typical AD7390-Microprocessor Serial Data Input Forms

RESET ($\overline{CLR}$) PIN

Forcing the $\overline{CLR}$ pin low will set the DAC register to all zeros and the DAC output voltage will be zero volts. The reset function is useful for setting the DAC outputs to zero at power-up or after a power supply interruption. Test systems and motor controllers are two of many applications which benefit from powering up to a known state. The external reset pulse can be generated by the microprocessor's power-on RESET signal, by an output from the microprocessor, or by an external resistor and capacitor. $\overline{CLR}$ has a Schmitt trigger input which results in a clean reset function when using external resistor/capacitor generated pulses. The $\overline{CLR}$ input overrides other logic inputs, specifically $\overline{LD}$. However, $\overline{LD}$ should be set high before $\overline{CLR}$ goes high. If $\overline{CLR}$ is kept low, then the contents of the shift register will be transferred to the DAC register as soon as $\overline{CLR}$ returns high. See the Control-Logic Truth Table I.

UNIPOLAR OUTPUT OPERATION

This is the basic mode of operation for the AD7390. As shown in Figure 10, the AD7390 has been designed to drive loads as low as 5 kΩ in parallel with 100 pF. The code table for this operation is shown in Table IV.

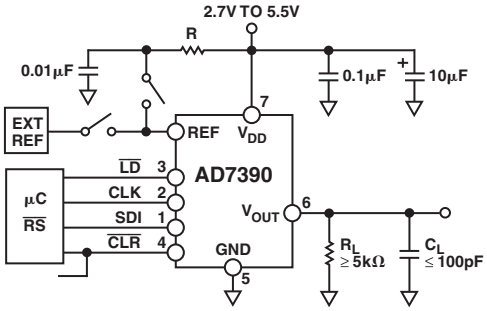


Figure 10. AD7390 Unipolar Output Operation

Table IV. AD7390 Unipolar Code Table

Hexadecimal Number in DAC Register	Decimal Number in DAC Register	Output Voltage (V) V_{REF} = 2.5 V
FFF	4095	2.4994
801	2049	1.2506
800	2048	1.2500
7FF	2047	1.2494
000	0	0

The circuit can be configured with an external reference plus power supply, or powered from a single dedicated regulator or reference, depending on the application performance requirements.

BIPOLAR OUTPUT OPERATION

Although the AD7391 has been designed for single-supply operation, the output can be easily configured for bipolar operation. A typical circuit is shown in Figure 11. This circuit uses a clean regulated 5 V supply for power, which also provides the circuit's reference voltage. Since the AD7391 output span swings from ground to very near 5 V, it is necessary to choose an external amplifier with a common-mode input voltage range that extends to its positive supply rail. The micropower consumption OP196 has been designed just for this purpose and results in only 50 microamps of maximum current consumption. Connection of the equally valued 470 kΩ resistors results in a differential amplifier mode of operation with a voltage gain of two, which results in a circuit output span of ten volts, that is, 25 V to 15 V. As the DAC is programmed with zero-code 000_H to midscale 200_H to full-scale $3FF_H$, the circuit output voltage V_O is set at 25 V, 0 V and 15 V (minus 1 LSB). The output voltage V_O is coded in offset binary according to Equation 4.

$$V_O = \left[\left(\frac{D}{512}\right) - 1\right] \times 5 \qquad (4)$$

where *D* is the decimal code loaded in the AD7391 DAC register. Note that the LSB step size is 10/1024 = 10 mV. This circuit has been optimized for micropower consumption including the 470 kΩ gain setting resistors, which should have low temperature coefficients to maintain accuracy and matching (preferably the same material, such as metal film). If better stability is required, the power supply could be substituted with a precision reference voltage such as the low dropout REF195, which can easily supply the circuit's 162 µA of current, and still provide additional power for the load connected to V_O. The micropower REF195 is guaranteed to source 10 mA output drive current, but only consumes 50 µA internally. If higher resolution is required, the AD7390 can be used with the addition of two more bits of data inserted into the software coding, which would result in a 2.5 mV LSB step size. Table V shows examples of nominal output voltages V_O provided by the Bipolar Operation circuit application.

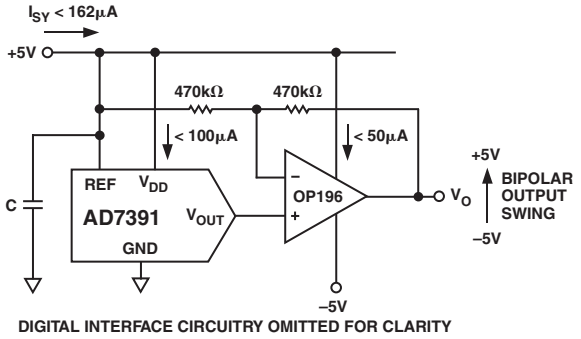


Figure 11. Bipolar Output Operation

Table V. Bipolar Code Table

Hexadecimal Number in DAC Register	Decimal Number in DAC Register	Analog Output Voltage (V)
3FF	1023	4.9902
201	513	0.0097
200	512	0.0000
1FF	511	–0.0097
000	0	–5.0000

MICROCOMPUTER INTERFACES

The AD7390 serial data input provides an easy interface to a variety of single-chip microcomputers (µCs). Many µCs have a built-in serial data capability which can be used for communicating with the DAC. In cases where no serial port is provided, or it is being used for some other purpose (such as an RS-232 communications interface), the AD7390/AD7391 can easily be addressed in software.

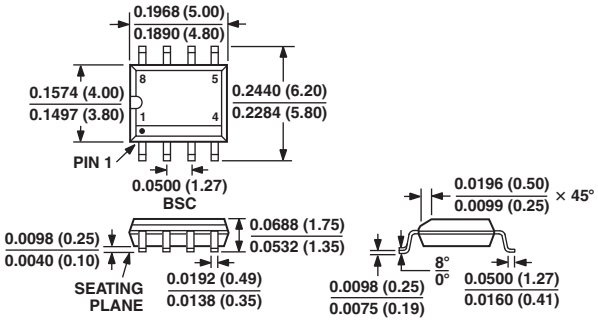
Twelve data bits are required to load a value into the AD7390. If more than 12 bits are transmitted before the load $\overline{LD}$ input goes high, the extra (i.e., the most-significant) bits are ignored. This feature is valuable because most µCs only transmit data in 8-bit increments. Thus, the µC sends 16 bits to the DAC instead of 12 bits. The AD7390 will only respond to the last 12 bits clocked into the SDI input, however, so the serial-data interface is not affected.

Ten data bits are required to load a value into the AD7391. If more than 10 bits are transmitted before load $\overline{LD}$ returns high, the extra bits are ignored.

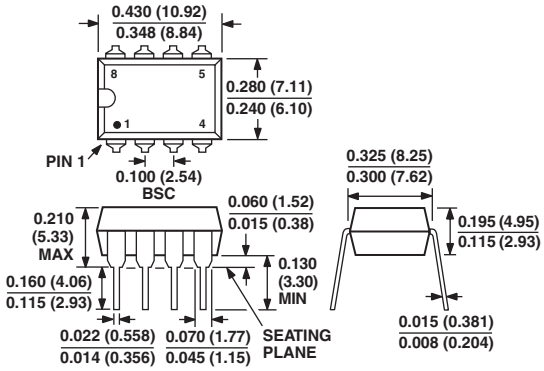
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

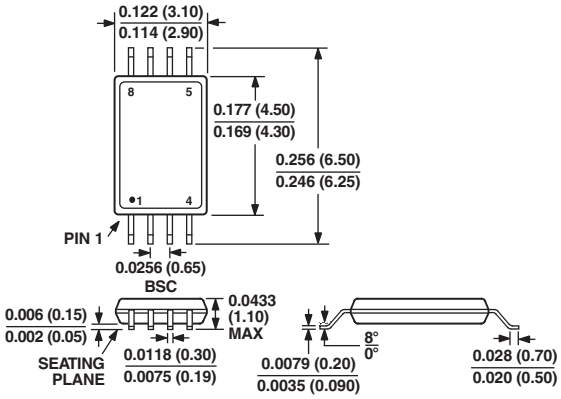
8-Lead SOIC
(R-8)



8-Lead Plastic DIP
(N-8)



8-Lead TSSOP
(RU-8)



Revision History

Location	Page
Data Sheet changed from REV. 0 to REV. A.	
Edits to SPECIFICATIONS	2
Edits to ABSOLUTE MAXIMUM RATINGS	3
Edits to ORDERING GUIDE	3
Edit to Figure 4	4
Edit to TPC 14	7

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