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REVISION HISTORY

1/2018—Rev. B to Rev. C

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10/2017—Rev. A to Rev. B

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4/2017—Rev. 0 to Rev. A

Added 40-Lead LFCSP Package ..... Universal
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1/2017—Revision 0: Initial Version

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SPECIFICATIONS

AV_{CC} = 2.97 V to 3.6 V, V_{LOGIC} = 1.7 V to 5.5 V, AV_{DD} = 2.97 V to 16 V, AV_{SS} = −22 V to −7 V, AGND = DGND = 0 V, V_{REF} = 2.5 V, output range = ±5 V, $V_{OUT}x$ unloaded, all specifications T_{MIN} to T_{MAX}, typical specifications at T_A = 25°C, dither powered on, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
STATIC PERFORMANCE					
Resolution	16			Bits	AD5766
	12			Bits	AD5767
Relative Accuracy (INL)					
AD5766	−16		+16	LSB	
AD5767	−1		+1	LSB	
Differential Nonlinearity	−1		+1	LSB	Guaranteed monotonic by design
Bipolar Zero Error	−85	±12	+85	mV	±5 V range
	−110	±13	+110	mV	−10 V to +6 V range
	−120	±15	+120	mV	±10 V range
	−145	±16	+145	mV	−12 V to +14 V range
	−145	±16	+145	mV	−16 V to +10 V range
Bipolar Zero Error Temperature Coefficient (TC)		±2		ppm FSR/°C	
Zero-Scale Error					All 0s loaded to DAC register
	−80	±25	+80	mV	−10 V to 0 V range
	−80	±25	+80	mV	±5 V range
	−110	±35	+110	mV	−16 V to 0 V range
	−110	±35	+110	mV	−10 V to +6 V range
	−130	±35	+130	mV	−20 V to 0 V range
	−130	±35	+130	mV	±10 V range
	−140	±45	+140	mV	−12 V to +14 V range
	−140	±45	+140	mV	−16 V to +10 V range
Zero-Scale Error Temperature Coefficient (TC)		±2		ppm FSR/°C	
Full-Scale Error					All 1s loaded to DAC register.
	−0.9	±0.23	+0.9	% FSR	−10 V to 0 V range
	−0.9	±0.23	+0.9	% FSR	±5 V range
	−0.8	±0.2	+0.8	% FSR	−16 V to 0 V range
	−0.8	±0.2	+0.8	% FSR	−10 V to +6 V range
	−0.7	±0.18	+0.7	% FSR	−20 V to 0 V range
	−0.7	±0.18	+0.7	% FSR	±10 V range
	−0.6	±0.15	+0.6	% FSR	−12 V to +14 V range
	−0.6	±0.15	+0.6	% FSR	−16 V to +10 V range
Full-Scale Error Drift		±3		ppm FSR/°C	
Gain Error	−0.4	±0.07	+0.4	% FSR	
Gain Error Temperature Coefficient (TC)		±2		ppm FSR/°C	
Offset Error	−80	±25	+80	mV	−10 V to 0 V range
	−80	±25	+80	mV	±5 V range
	−110	±35	+110	mV	−16 V to 0 V range
	−110	±35	+110	mV	−10 V to +6 V range
	−130	±35	+130	mV	−20 V to 0 V range
	−130	±35	+130	mV	±10 V range
	−140	±45	+140	mV	−12 V to +14 V range
	−140	±45	+140	mV	−16 V to +10 V range
Offset Error Drift		±2		µV/°C	

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Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Total Unadjusted Error	−0.9	±0.18	+0.9	%FSR	−10 V to 0 V range
	−0.9	±0.18	+0.9	%FSR	±5 V range
	−0.8	±0.15	+0.8	%FSR	−16 V to 0 V range
	−0.8	±0.15	+0.8	%FSR	−10 V to +6 V range
	−0.7	±0.13	+0.7	%FSR	−20 V to 0 V range
	−0.7	±0.13	+0.7	%FSR	±10 V range
	−0.6	±0.12	+0.6	%FSR	−12 V to +14 V range
	−0.6	±0.12	+0.6	%FSR	−16 V to +10 V range
DC Crosstalk		30		µV	Due to output voltage change
		35		µV/mA	Due to load current change (1 LSB)
OUTPUT CHARACTERISTICS					
Output Voltage Ranges[1]	−20		0	V	
	−16		0	V	
	−10		0	V	
	−10		+6	V	
	−12		+14	V	
	−16		+10	V	
	−5		+5	V	
	−10		+10	V	
Output Current	−20		+20	mA	Refer to the Thermal Considerations section
Capacitive Load Stability			1	nF	
DC Output Impedance		0.2		Ω	
Short-Circuit Current		±60		mA	Single channel only
Output Amplifier Bandwidth		108		kHz	
REFERENCE INPUT					
Reference Input Voltage		2.5		V	±1% for specified performance
Reference Range	2.375		2.625	V	Functional performance only
DC Input Impedance	2.5			MΩ	
Input Current			1	µA	
DITHER INPUTS					For dither input to DAC output attenuation, see Figure 62 to Figure 65 for typical performance
Dither Frequency		10		kHz	Lower −3 dB point
		100		kHz	Upper −3 dB point
Amplitude			0.25	V p-p	Peak-to-peak ac voltage
	0		AV_{CC}	V	Peak-to-peak ac and dc voltage
DC Shift					See the Terminology section
AD5766	−2	±1	+2	LSB	
AD5767	−1	±0.063	+1	LSB	
Dither Transient					Dither enabled/disabled, N0 and N1 floating
Dither Selected Channel		5		nV-sec	AV_{CC} = 2.97 V and AV_{CC} = 3.6 V
Dither Nonselected Channels		2		nV-sec	AV_{CC} =2.97 V and AV_{CC} = 3.6 V
Dither Crosstalk[1]		−70		dB	10 kHz dither frequency
		−55		dB	100 kHz dither frequency
LOGIC INPUTS					
Input High Voltage, V_{IH}	0.7 × V_{LOGIC}			V	
Input Low Voltage, V_{IL}			0.3 × V_{LOGIC}	V	
Input Current	−2		+2	µA	Per pin
	−6		+6	µA	$\overline{\text{RESET}}$ pin pulled high
	−57		+57	µA	$\overline{\text{RESET}}$ pin pulled low
Input Capacitance		2		pF	Per pin

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Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LOGIC OUTPUT					
Output Low Voltage			0.4	V	Sinking 200 µA
Output High Voltage	V_{LOGIC} − 0.4			V	Sourcing 200 µA
High Impedance Leakage Current	−1		+1	µA	
High Impedance Output Capacitance		5		pF	
VOLTAGE MONITOR PIN (MUX_OUT)					
Impedance		1.3		kΩ	
Three-State Leakage Current	−1	0.006	+1	µA	
Continuous Current	−1		+1	mA	Die temperature below 105°C
Glitch Impulse		0.2		nV-sec	V_{OUT}x glitch due to mux enable
Voltage Settling Time		12		µs	¼ to ¾ scale settling to ±0.5 LSB, ±5 V range and −10 V to 0 V range
POWER SUPPLIES					
AV_{DD}	2.97		16	V	AV_{DD} − AV_{SS} must be less than or equal to 30 V
AV_{SS}	−22		−7	V	AV_{DD} − AV_{SS} must be less than or equal to 30 V
AV_{CC}	2.97		3.6	V	
V_{LOGIC}	1.7		5.5	V	
Headroom/Footroom		±0.7		V	Output voltage offset to ±2 LSB for 20 mA output load; applies to AV_{DD} and AV_{SS}
		±2		V	Output voltage offset to ±1 LSB for 20 mA output load; applies to AV_{DD} and AV_{SS}
Normal Mode					
AI_{DD}		6	9	mA	All output ranges, −40°C to +105°C
AI_{SS}	−11	−9		mA	All output ranges, −40°C to +105°C
AI_{CC}		8.3	10	mA	All output ranges, −40°C to +105°C
I_{LOGIC}		0.02	1	µA	All output ranges, −40°C to +105°C, $V_{IH} = V_{LOGIC}$, V_{IL} = DGND
DC Power Supply Rejection Ratio (PSRR)		50		µV/V	AV_{DD} power supply
		50		µV/V	AV_{SS} power supply
		3		mV/V	AV_{CC} power supply
AC Power Supply Rejection Ratio (PSRR)		−80		dB	AV_{DD} power supply, at 50 Hz
		−80		dB	AV_{SS} power supply, at 50 Hz
		−50		dB	AV_{CC} power supply, at 50 Hz

[1] Output amplifier headroom requirement is 2 V minimum.

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AV_{CC} = 2.97 V to 3.6 V, V_{LOGIC} = 1.7 V to 5.5 V, AV_{DD} = 2.97 V to 16 V, AV_{SS} = −22 V to −7 V, AGND = DGND = 0 V, V_{REF} = 2.5 V, output range = ±5 V, V_{OUT}x unloaded, all specifications T_{MIN} to T_{MAX}, typical specifications at T_A = 25°C, dither powered off, unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
BIPOLAR ZERO ERROR	−50	±11	+50	mV	±5 V range
	−75	±12	+75	mV	−10 V to +6 V range
	−90	±12	+90	mV	±10 V range
	−110	±13	+110	mV	−12 V to +14 V range
	−110	±13	+110	mV	−16 V to +10 V range
ZERO-SCALE ERROR					All 0s loaded to DAC register
	−50	±15	+50	mV	−10 V to 0 V range
	−50	±15	+50	mV	±5 V range
	−75	±20	+75	mV	−16 V to 0 V range
	−75	±20	+75	mV	−10 V to +6 V range
	−90	±25	+90	mV	−20 V to 0 V range
	−90	±25	+90	mV	±10 V range
	−110	±35	+110	mV	−12 V to +14 V range
	−110	±35	+110	mV	−16 V to +10 V range
FULL-SCALE ERROR	−0.5	±0.15	+0.5	% FSR	All 1s loaded to DAC register; all output ranges
GAIN ERROR	−0.3	±0.07	+0.3	% FSR	All output ranges
OFFSET ERROR	−50	±15	+50	mV	−10 V to 0 V range
	−50	±15	+50	mV	±5 V range
	−75	±20	+75	mV	−16 V to 0 V range
	−75	±20	+75	mV	−10 V to +6 V range
	−90	±25	+90	mV	−20 V to 0 V range
	−90	±25	+90	mV	±10 V range
	−110	±35	+110	mV	−12 V to +14 V range
	−110	±35	+110	mV	−16 V to +10 V range
TOTAL UNADJUSTED ERROR	−0.5	±0.12	+0.5	%FSR	All output ranges

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AC PERFORMANCE CHARACTERISTICS

AV_{CC} = 2.97 V to 3.6 V, V_{LOGIC} = 1.7 V to 5.5 V, AV_{DD} = 2.97 V to 15 V, AV_{SS} = −22 V to −7 V, AGND = DGND = 0 V, V_{REF} = 2.5 V, output range = −10 V to 0 V, $V_{OUT}x$ unloaded, all specifications T_{MIN} to T_{MAX}, typical specifications at T_A = 25°C, dither powered on, analog dither signals not applied, unless otherwise noted.

Table 3.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE[1]					
Output Voltage Settling Time					
AD5766		16		µs	¼ to ¾ scale settling to ±0.5 LSB, ±5 V range, and −10 V to 0 V range
		14		µs	256 LSB step to ±0.5 LSB
AD5767		10		µs	¼ to ¾ scale settling to ±0.5 LSB, ±5 V range, and −10 V to 0 V range
		4		µs	32 LSB step to ±0.5 LSB
Slew Rate		1		V/µs	
Digital-to-Analog Glitch Energy		10		nV-sec	1 LSB change around major carry for 10 V span
Glitch Impulse Peak Amplitude		8		mV	
Digital Feedthrough		1		nV-sec	
Digital Crosstalk		2		nV-sec	
Analog Crosstalk		15		nV-sec	
DAC-to-DAC Crosstalk		15		nV-sec	
Total Harmonic Distortion		−80		dB	V_{REF} = 2.5 V ± 0.1 V p-p, frequency = 10 kHz, AV_{CC} = 2.97 V and 3.6 V
		−75		dB	V_{REF} = 2.5 V ± 0.1 V p-p, frequency = 10 kHz, AV_{CC} = 3.6 V
Output Noise Spectral Density[1]		375		nV/√Hz	−10 V to 0 V and ±5 V ranges, frequency = 1 kHz
		605		nV/√Hz	−16 V to 0 V and −10 V to +6 V ranges, frequency = 1 kHz
		750		nV/√Hz	−20 V to 0 V and ±10 V ranges, frequency = 1 kHz
		835		nV/√Hz	−12 V to 14 V and −16 V to +10 V ranges, frequency = 1 kHz
		280		nV/√Hz	−10 V to 0 V and ±5 V ranges, frequency = 10 kHz
		440		nV/√Hz	−16 V to 0 V and −10 V to +6 V ranges, frequency = 10 kHz
		470		nV/√Hz	−20 V to 0 V and ±10 V ranges, frequency = 10 kHz
		610		nV/√Hz	−12 V to 14 V and −16 V to +10 V ranges, frequency = 10 kHz
Output Noise[2]					Dither disabled
		20		µV rms	±5 V range
		23		µV rms	−10 V to 0 V range
		33		µV rms	−10 V to +6 V range
		38		µV rms	−16 V to 0 V range
		36		µV rms	±10 V range
		45		µV rms	−20 V to 0 V range
		45		µV rms	−16 V to 10 V range
		45		µV rms	−12 V to 14 V range

[1] DAC code = midscale. $AV_{DD} = V_{OUT_MAX} + 2$ V. $AV_{SS} = V_{OUT_MIN} - 2$ V.
[2] 0.1 Hz to 10 Hz. $AV_{DD} = V_{OUT_MAX} + 2$ V. $AV_{SS} = V_{OUT_MIN} - 2$ V.

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TIMING CHARACTERISTICS

All input signals are specified with $t_R = t_F = 1$ ns/V (10% to 90% of AV_{DD}) and timed from a voltage level of $(V_{IL} + V_{IH})/2$. See Figure 2, Figure 3, and Figure 4. AV_{CC} = 2.97 V to 3.6 V, V_{LOGIC} = 1.7 V to 5.5 V, V_{REF} = 2.5 V, all specifications −40°C to +105°C, dither powered on, unless otherwise noted.

Table 4.

Parameter	Limit at T_{MIN}, T_{MAX}	Unit	Description
t_1[1]	20	ns min	SCLK cycle time
t_2	10	ns min	SCLK high time
t_3	10	ns min	SCLK low time
t_4	15	ns min	$\overline{SYNC}$ falling edge to SCLK falling edge setup time
t_5	15	ns min	SCLK falling edge to $\overline{SYNC}$ rising edge time
t_6	20	ns min	Minimum $\overline{SYNC}$ high time (write mode)
t_7	5	ns min	Data setup time
t_8	5	ns min	Data hold time
t_9	4	µs typ	DAC output settling time, 32 code step to ±0.5 LSB at 12-bit resolution (see Table 3)
t_{10}	100	ns typ	$\overline{RESET}$[2] pulse width low
t_{11}	100	ns typ	$\overline{RESET}$[2] pulse activation time
t_{12}	10	ns min	$\overline{SYNC}$ rising edge to SCLK falling edge
t_{13}	40	ns max	SCLK rising edge to SDO valid (C_{L_SDO}[3] = 15 pF)
t_{14}	80	ns min	Minimum $\overline{SYNC}$ high time (readback/daisy-chain mode)
t_{15}	5	µs typ	$\overline{SYNC}$ rising edge to $\overline{SYNC}$ rising edge (DAC register updates)

[1] Maximum SCLK frequency is 50 MHz for write mode and 10 MHz for readback mode.
[2] Minimum time between a reset and the subsequent successful write is typically 25 ns.
[3] C_{L_SDO} is the capacitive load on the SDO output.

Timing Diagrams

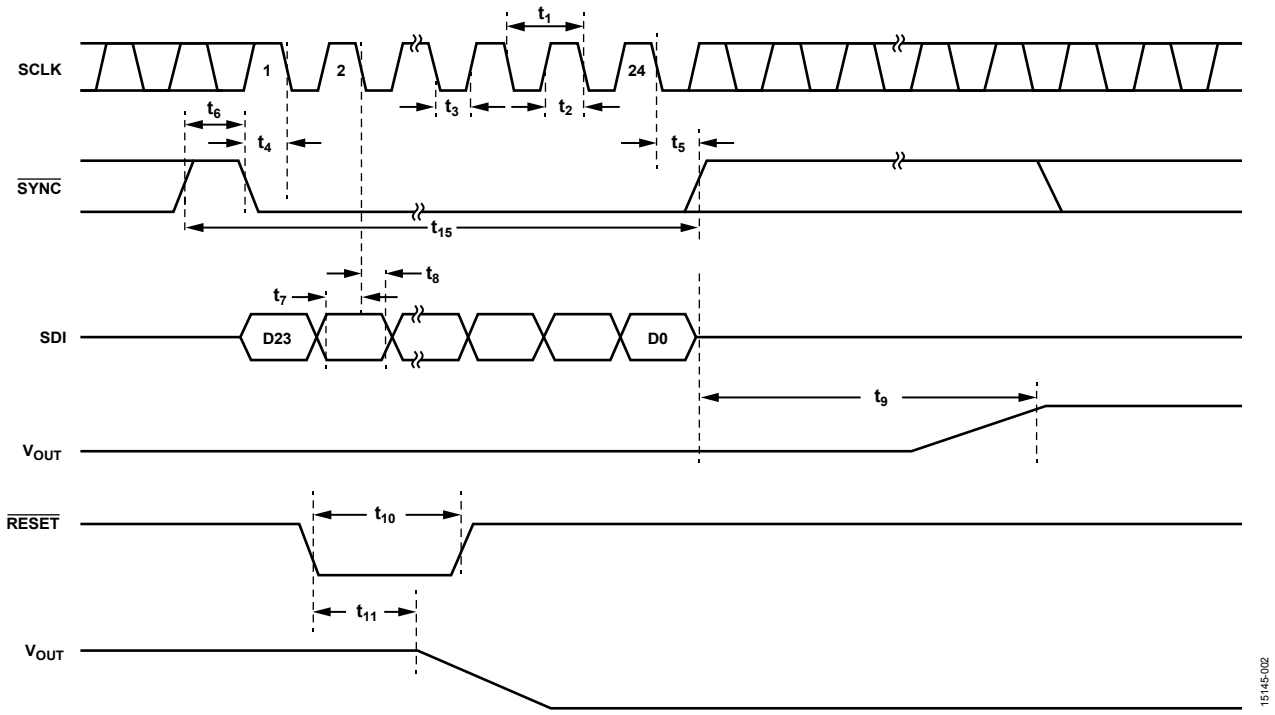

Figure 2. Serial Interface Timing Diagram

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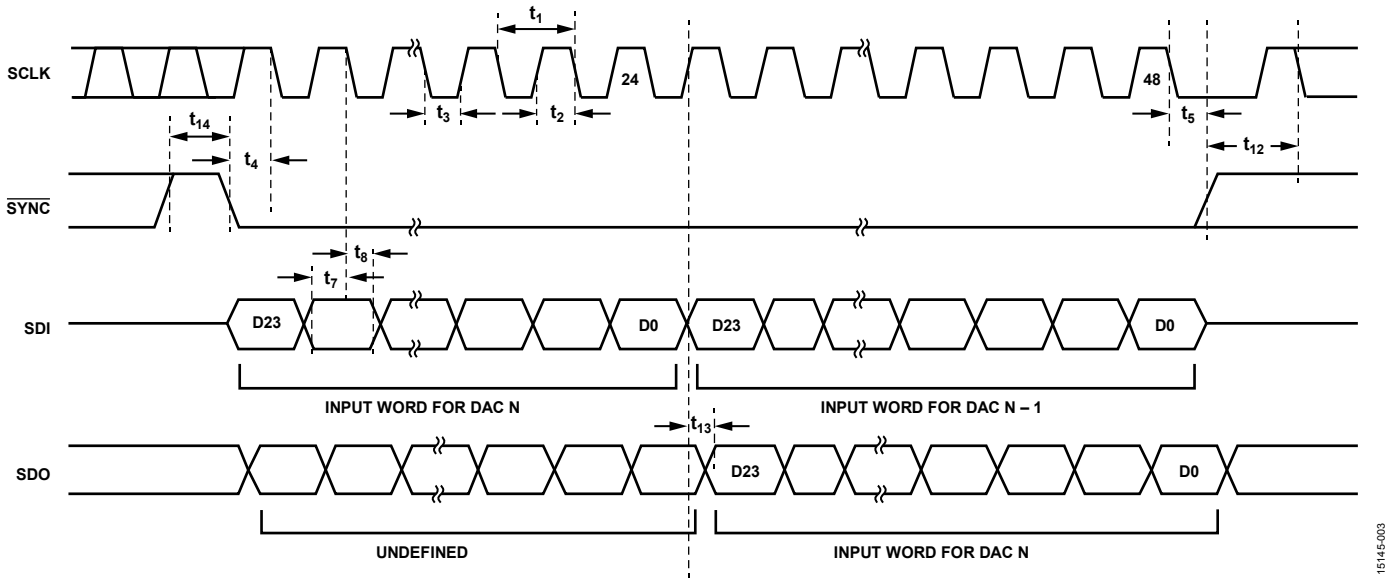

Figure 3. Daisy-Chain Timing Diagram

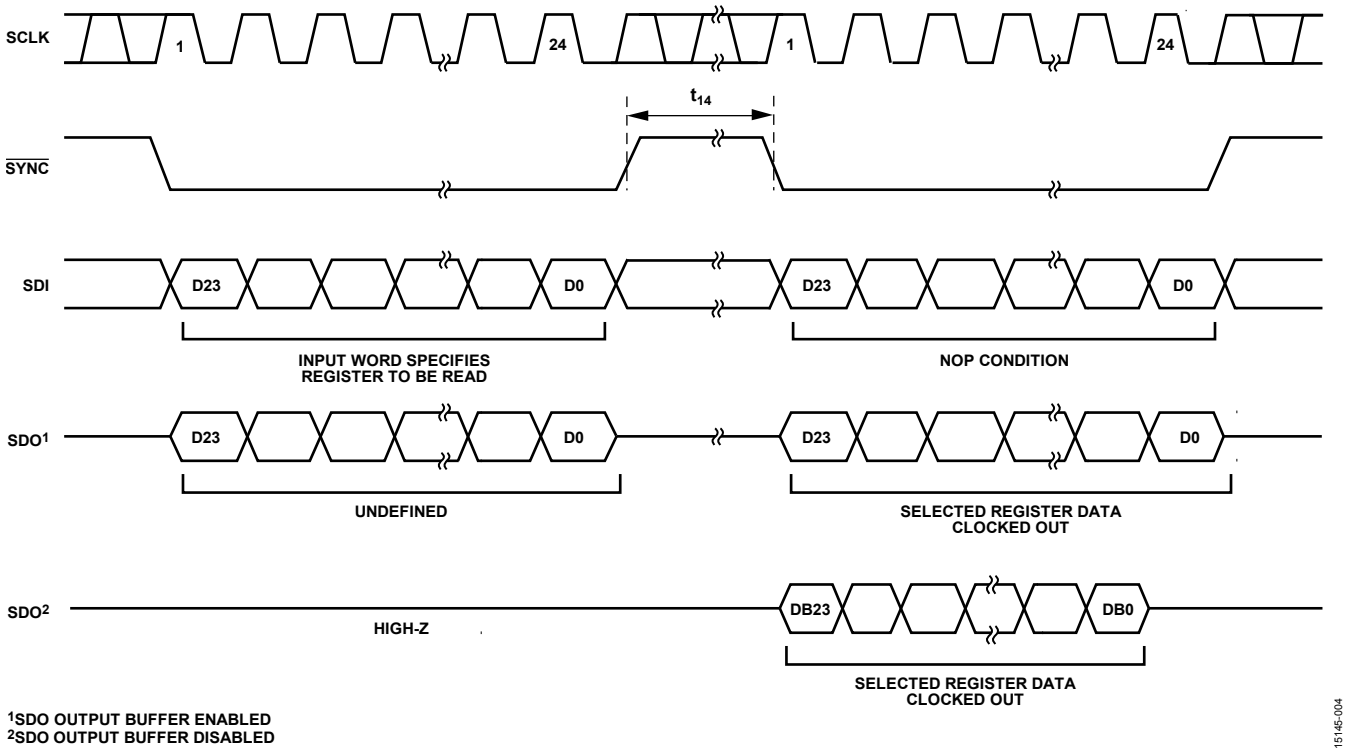

Figure 4. Readback Timing Diagram

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ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted. Transient currents of up to 100 mA do not cause silicon controlled rectifier (SCR) latch-up.

Table 5.

Parameter	Rating
AV_{DD} to AGND	−0.3 V to +34 V
AV_{SS} to AGND	+0.3 V to −34 V
AV_{DD} to AV_{SS}	−0.3 V to +34 V
AV_{CC} to AGND	−0.3 V to +7 V
AV_{CC} to AGND	−0.3 V to AV_{DD} + 0.3 V
V_{LOGIC} to DGND	−0.3 V to +7 V
Digital Inputs[1] to DGND	−0.3 V to V_{LOGIC} + 0.3 V
Digital Output (SDO) to DGND	−0.3 V to V_{LOGIC} + 0.3 V
N0, N1 to AGND	−0.3 V to AV_{CC} + 0.3 V
V_{REF} to AGND	−0.3 V to AV_{CC} + 0.3 V
V_{OUT}x to AGND	AV_{SS} − 0.3 V to AV_{DD} + 0.3 V
AGND to DGND	−0.3 V to +0.3 V
Operating Temperature Range, T_A Industrial	−40°C to +105°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature, $T_{J\,MAX}$	150°C
Power Dissipation	$(T_{J\,MAX} - T_A)/\theta_{JA}$
Lead Temperature	
Soldering Reflow	260°C, as per JEDEC J-STD-020

[1] The digital inputs include $\overline{RESET}$, SCLK, $\overline{SYNC}$, and SDI.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the natural convection junction to ambient thermal resistance measured in a one cubic foot sealed enclosure.

Table 6. Thermal Resistance

Package Type	θ_{JA}	Unit
CB-49-4[1]	53	°C/W
CP-40-7[1]	31.71	°C/W

[1] Thermal impedance simulated values are based on JEDEC 2S2P thermal test board with 16 thermal vias. See JEDEC JESD51.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

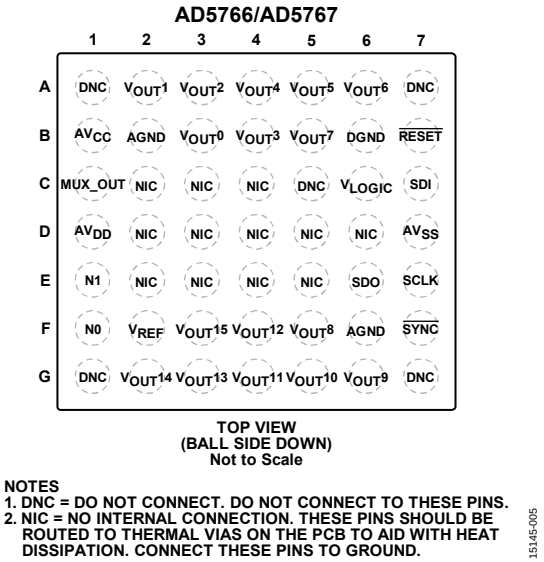

Figure 5. WLCSP Package Pin Configuration

Table 7. 49-Ball WLCSP Pin Function Descriptions

Pin No.	Mnemonic	Description
Dither		
F1	N0	Dither Signal Input Pin 0. A signal connected to this pin can be added to the DAC outputs via register commands. If unused, connect this pin to ground. Refer to the Dither section for more information.
E1	N1	Dither Signal Input Pin 1. A signal connected to this pin can be added to the DAC outputs via register commands. If unused, connect this pin to ground. Refer to the Dither section for more information.
Logic Inputs and Outputs		
E7	SCLK	Serial Clock Input. Data is clocked into the input shift register on the falling edge of the serial clock input. Data can be transferred at rates of up to 50 MHz for write mode and 10 MHz for readback and daisy-chain mode.
F7	$\overline{\text{SYNC}}$	Active Low Control Input. $\overline{\text{SYNC}}$ is the frame synchronization signal for the input data. When $\overline{\text{SYNC}}$ goes low, it powers on the SCLK and SDI buffers and enables the input shift register. Data is transferred in on the falling edges of the next 24 clocks. If $\overline{\text{SYNC}}$ is taken high before the 24th falling edge, the rising edge of $\overline{\text{SYNC}}$ acts as an interrupt, and the write sequence is ignored by the device.
C7	SDI	Serial Data Input. This device has a 24-bit shift register. Data is clocked into the register on the falling edge of the serial clock input.
E6	SDO	Serial Data Output. This pin clocks data from the serial register in daisy-chain or readback mode. Data is clocked out on the rising edge of SCLK and is valid on the falling edge of SCLK.
B7	$\overline{\text{RESET}}$	Active Low Reset Input. Asserting this pin logic low returns the AD5766/AD5767 to the default power-on state. After this pin returns to logic high, the device comes out of the reset mode and is ready to accept a new SPI command. This pin can be left floating, because there is a weak internal pull-up resistor.
Analog Outputs		
B3	$V_{OUT}0$	Analog Output Voltage from DAC 0.
A2	$V_{OUT}1$	Analog Output Voltage from DAC 1.
A3	$V_{OUT}2$	Analog Output Voltage from DAC 2.
B4	$V_{OUT}3$	Analog Output Voltage from DAC 3.
A4	$V_{OUT}4$	Analog Output Voltage from DAC 4.
A5	$V_{OUT}5$	Analog Output Voltage from DAC 5.
A6	$V_{OUT}6$	Analog Output Voltage from DAC 6.

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Pin No.	Mnemonic	Description
B5	$V_{OUT}7$	Analog Output Voltage from DAC 7.
F5	$V_{OUT}8$	Analog Output Voltage from DAC 8.
G6	$V_{OUT}9$	Analog Output Voltage from DAC 9.
G5	$V_{OUT}10$	Analog Output Voltage from DAC 10.
G4	$V_{OUT}11$	Analog Output Voltage from DAC 11.
F4	$V_{OUT}12$	Analog Output Voltage from DAC 12.
G3	$V_{OUT}13$	Analog Output Voltage from DAC 13.
G2	$V_{OUT}14$	Analog Output Voltage from DAC 14.
F3	$V_{OUT}15$	Analog Output Voltage from DAC 15.
Power Supplies and Reference Input		
F2	V_{REF}	Reference Input Voltage. For specified performance, V_{REFIN} = 2.5 V.
C6	V_{LOGIC}	Digital Power Supply.
B1	AV_{CC}	Power Supply Input. The AD5766/AD5767 operates from 2.97 V to 3.6 V. Decouple AV_{CC} with a 10 µF capacitor in parallel with a 0.1 µF capacitor to analog ground.
D1	AV_{DD}	Output Amplifier Positive Analog Supply.
D7	AV_{SS}	Output Amplifier Negative Analog Supply.
B2, F6	AGND	Analog Ground.
B6	DGND	Digital Ground Pin.
Channel Monitoring		
C1	MUX_OUT	Monitor Output. This pin acts as the output of a 16-to-1 channel multiplexer that can be programmed to multiplex one of 16 channels, Channel 0 to Channel 15, to the MUX_OUT pin.
Do Not Connect		
A1, A7, C5, G1, G7	DNC	Do Not Connect. Do not connect to these pins.
No Internal Connection		
C2 to C4, D2 to D6, E2 to E5	NIC	No Internal Connection. Route these pins to thermal vias on the PCB to aid with heat dissipation. Connect these pins to ground.

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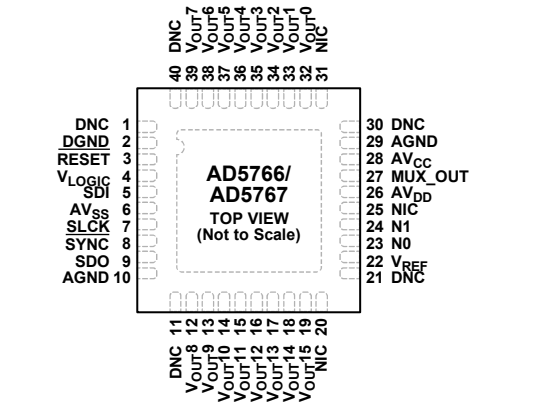

NOTES
1. DNC = DO NOT CONNECT. DO NOT CONNECT TO THESE PINS.
2. NIC = NO INTERNAL CONNECTION. THESE PINS SHOULD BE ROUTED TO THERMAL VIAS ON THE PCB TO AID WITH HEAT DISSIPATION. THESE SHOULD BE CONNECTED TO GROUND.
3. EXPOSED PAD (LFCSP PACKAGE ONLY). CONNECT THIS EXPOSED PAD TO THE POTENTIAL OF THE AV_{SS} PIN, OR, ALTERNATIVELY, LEAVE IT ELECTRICALLY UNCONNECTED. IT IS RECOMMENDED THAT THE PAD BE THERMALLY CONNECTED TO A COPPER PLANE FOR ENHANCED THERMAL PERFORMANCE.

15145-006

Figure 6. LFCSP Package Pin Configuration

Table 8. 40-Lead LFCSP Pin Function Descriptions

Pin No.	Mnemonic	Description
Dither		
23	N0	Dither Signal Input Pin 0. A signal connected to this pin can be added to the DAC outputs via register commands. If unused, connect this pin to ground. Refer to the Dither section for more information.
24	N1	Dither Signal Input Pin 1. A signal connected to this pin can be added to the DAC outputs via register commands. If unused, connect this pin to ground. Refer to the Dither section for more information.
Logic Inputs and Outputs		
7	SCLK	Serial Clock Input. Data is clocked into the input shift register on the falling edge of the serial clock input. Data can be transferred at rates of up to 50 MHz for write mode and 10 MHz for readback and daisy-chain mode.
8	$\overline{\text{SYNC}}$	Active Low Control Input. $\overline{\text{SYNC}}$ is the frame synchronization signal for the input data. When $\overline{\text{SYNC}}$ goes low, it powers on the SCLK and SDI buffers and enables the input shift register. Data is transferred in on the falling edges of the next 24 clocks. If $\overline{\text{SYNC}}$ is taken high before the 24th falling edge, the rising edge of $\overline{\text{SYNC}}$ acts as an interrupt, and the write sequence is ignored by the device.
5	SDI	Serial Data Input. This device has a 24-bit shift register. Data is clocked into the register on the falling edge of the serial clock input.
9	SDO	Serial Data Output. This pin clocks data from the serial register in daisy-chain or readback mode. Data is clocked out on the rising edge of SCLK and is valid on the falling edge of SCLK.
3	$\overline{\text{RESET}}$	Active Low Reset Input. Asserting this pin logic low returns the AD5766/AD5767 to the default power-on state. After this pin returns to logic high, the device comes out of the reset mode and is ready to accept a new SPI command. This pin can be left floating, because there is a weak internal pull-up resistor.
Analog Outputs		
32	$V_{OUT}0$	Analog Output Voltage from DAC 0.
33	$V_{OUT}1$	Analog Output Voltage from DAC 1.
34	$V_{OUT}2$	Analog Output Voltage from DAC 2.
35	$V_{OUT}3$	Analog Output Voltage from DAC 3.
36	$V_{OUT}4$	Analog Output Voltage from DAC 4.
37	$V_{OUT}5$	Analog Output Voltage from DAC 5.

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Pin No.	Mnemonic	Description
38	$V_{OUT}6$	Analog Output Voltage from DAC 6.
39	$V_{OUT}7$	Analog Output Voltage from DAC 7.
12	$V_{OUT}8$	Analog Output Voltage from DAC 8.
13	$V_{OUT}9$	Analog Output Voltage from DAC 9.
14	$V_{OUT}10$	Analog Output Voltage from DAC 10.
15	$V_{OUT}11$	Analog Output Voltage from DAC 11.
16	$V_{OUT}12$	Analog Output Voltage from DAC 12.
17	$V_{OUT}13$	Analog Output Voltage from DAC 13.
18	$V_{OUT}14$	Analog Output Voltage from DAC 14.
19	$V_{OUT}15$	Analog Output Voltage from DAC 15.
Power Supplies and Reference Input		
22	V_{REF}	Reference Input Voltage. For specified performance, V_{REFIN} = 2.5 V.
4	V_{LOGIC}	Digital Power Supply.
28	AV_{CC}	Power Supply Input. The AD5766/AD5767 operates from 2.97 V to 3.6 V. Decouple AV_{CC} with a 10 µF capacitor in parallel with a 0.1 µF capacitor to analog ground.
26	AV_{DD}	Output Amplifier Positive Analog Supply.
6	AV_{SS}	Output Amplifier Negative Analog Supply.
10, 29	AGND	Analog Ground.
2	DGND	Digital Ground Pin.
Channel Monitoring		
27	MUX_OUT	Monitor Output. This pin acts as the output of a 16-to-1 channel multiplexer that can be programmed to multiplex one of 16 channels, Channel 0 to Channel 15, to the MUX_OUT pin.
Do Not Connect		
1, 11, 21, 30, 40	DNC	Do Not Connect. Do not connect to these pins.
No Internal Connection		
20, 25, 31	NIC	No Internal Connection. Route these pins to thermal vias on the PCB to aid with heat dissipation. Connect these pins to ground.
Not Applicable	EPAD	Exposed Pad. Connect this exposed pad to the potential of the AV_{SS} pin, or, alternatively, leave it electrically unconnected. It is recommended that the exposed pad be thermally connected to a copper plane for enhanced thermal performance.

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TYPICAL PERFORMANCE CHARACTERISTICS

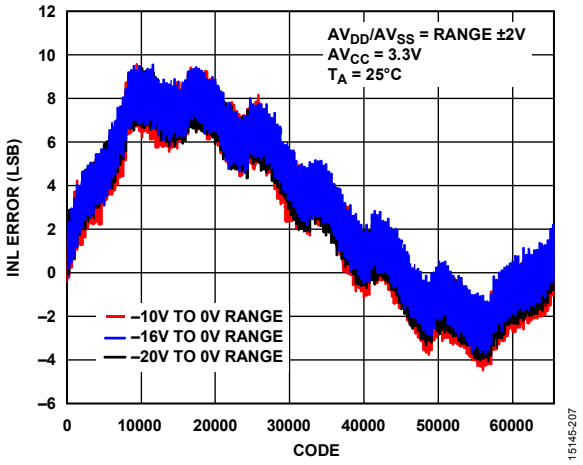

Figure 7. AD5766 INL Error vs. DAC Code (Unipolar Output)

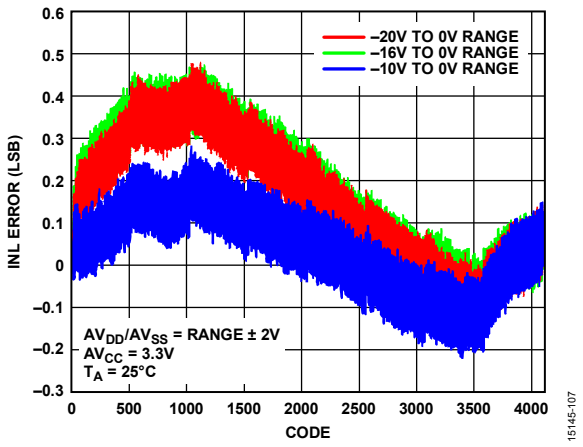

Figure 8. AD5767 INL Error vs. DAC Code (Unipolar Output)

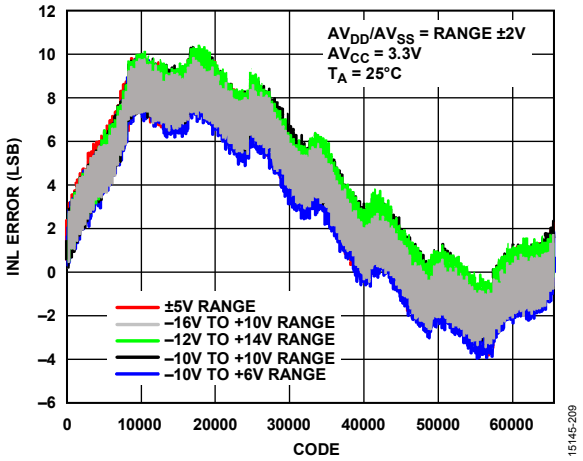

Figure 9. AD5766 INL Error vs. DAC Code (Bipolar Outputs)

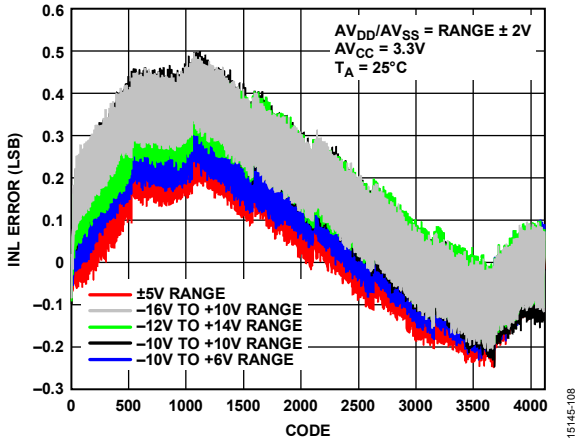

Figure 10. AD5767 INL Error vs. DAC Code (Bipolar Outputs)

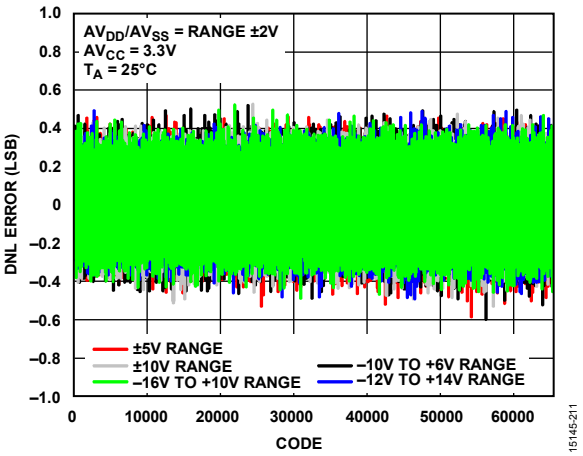

Figure 11. AD5766 DNL Error vs. DAC Code (Bipolar Outputs)

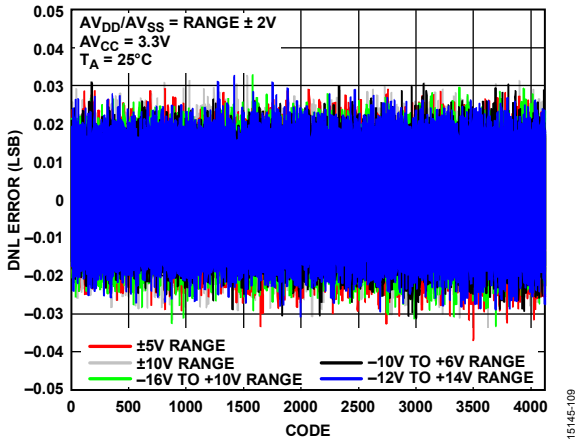

Figure 12. AD5767 DNL Error vs. DAC Code (Bipolar Outputs)

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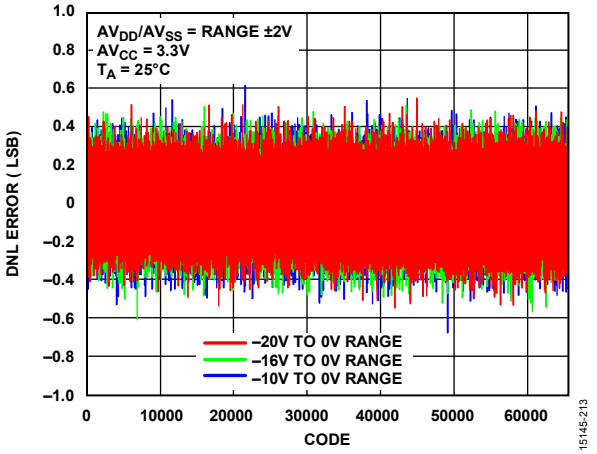

Figure 13. AD5766 DNL Error vs. DAC Code (Unipolar Outputs)

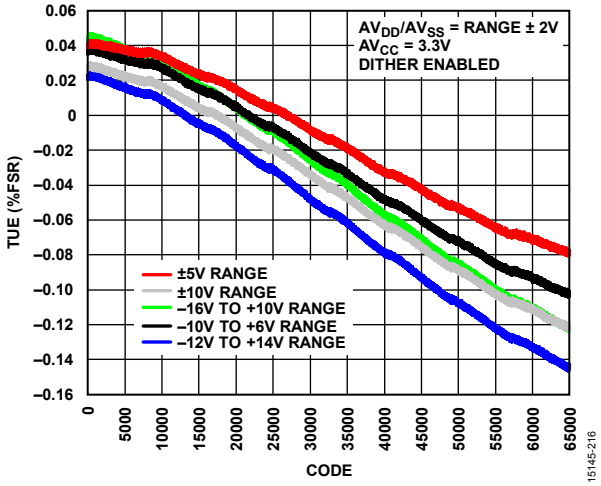

Figure 16. Total Unadjusted Error (TUE) vs. DAC Code (Bipolar Outputs)

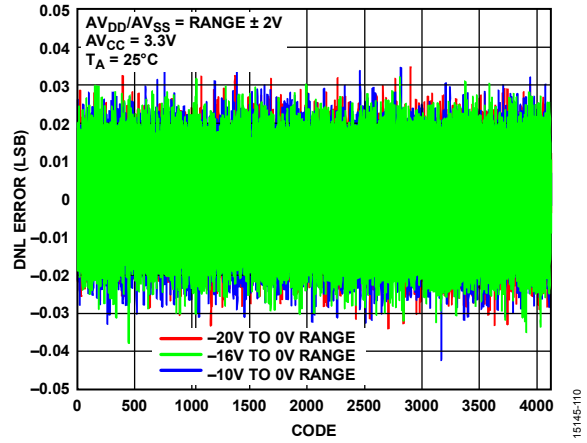

Figure 14. AD5767 DNL Error vs. DAC Code (Unipolar Outputs)

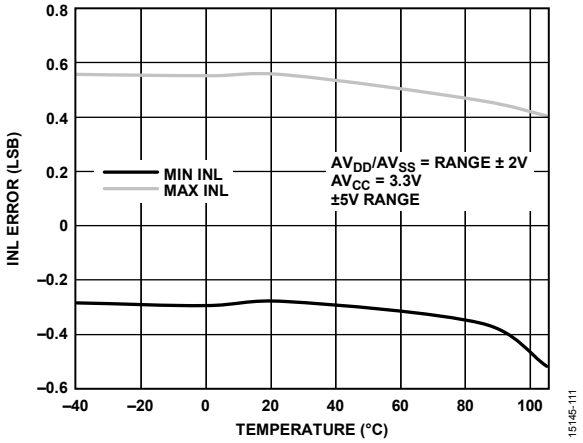

Figure 17. INL Error vs. Temperature

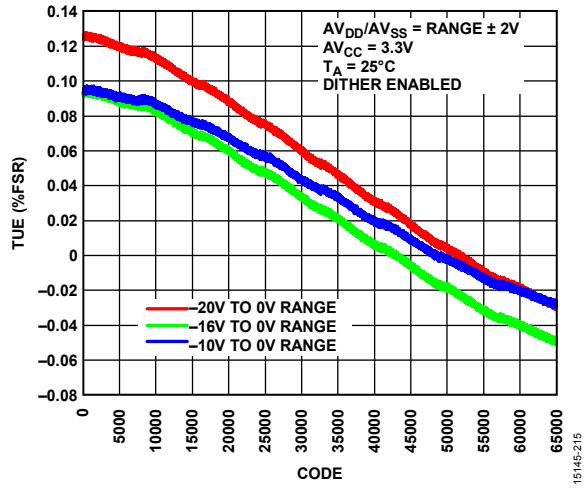

Figure 15. Total Unadjusted Error (TUE) vs. DAC Code (Unipolar Outputs)

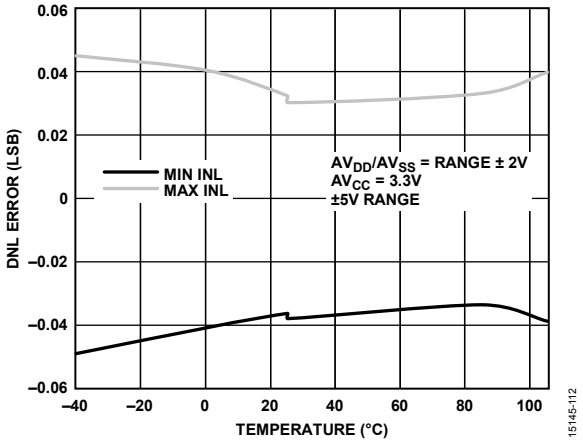

Figure 18. DNL Error vs. Temperature

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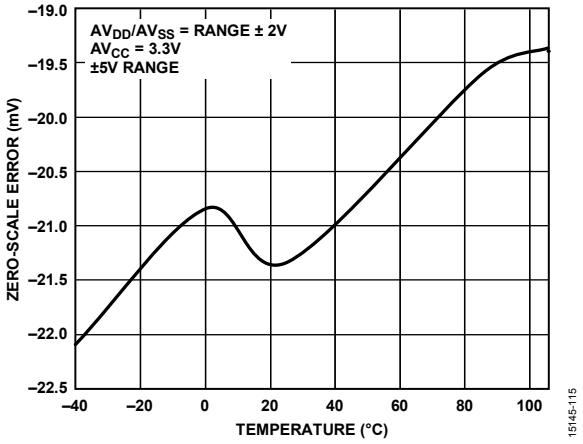

Figure 19. Zero-Scale Error vs. Temperature

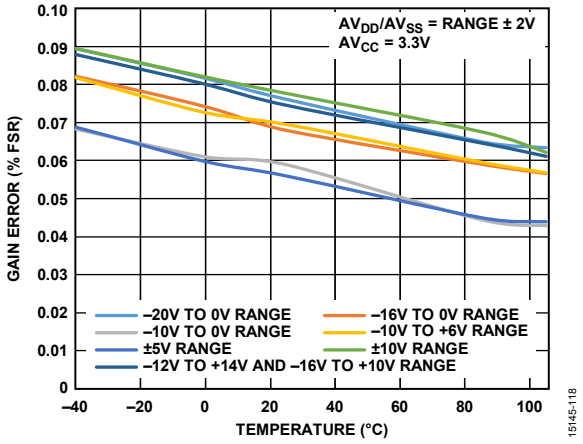

Figure 22. Gain Error vs. Temperature

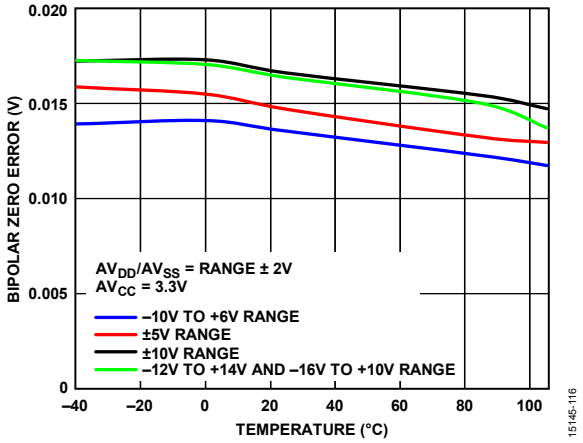

Figure 20. Bipolar Zero Error vs. Temperature

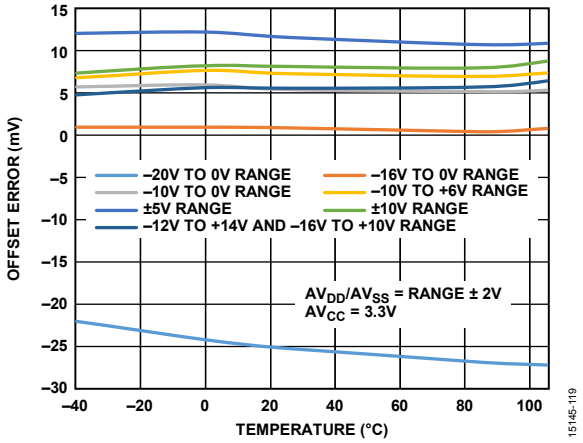

Figure 23. Offset Error vs. Temperature

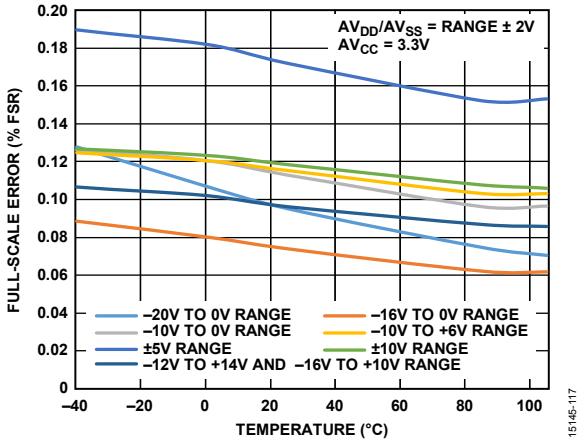

Figure 21. Full-Scale Error vs. Temperature

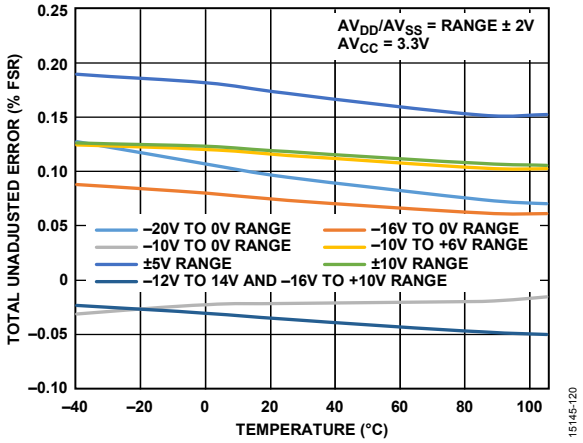

Figure 24. Total Unadjusted Error vs. Temperature

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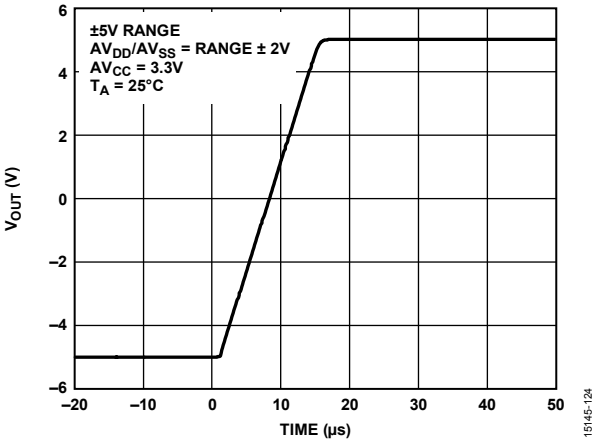

Figure 25. Full-Scale Settling Time (Rising Voltage Step)

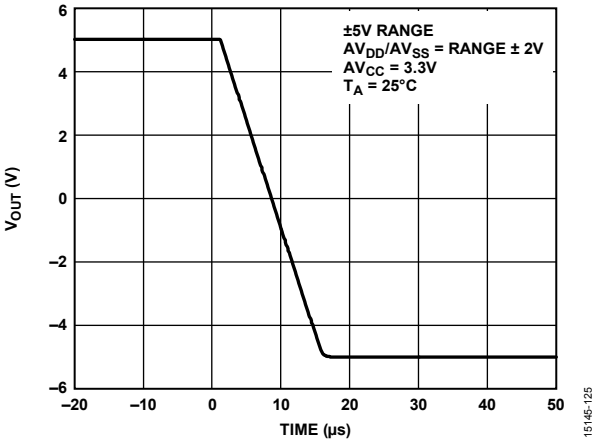

Figure 26. Full-Scale Settling Time (Falling Voltage Step)

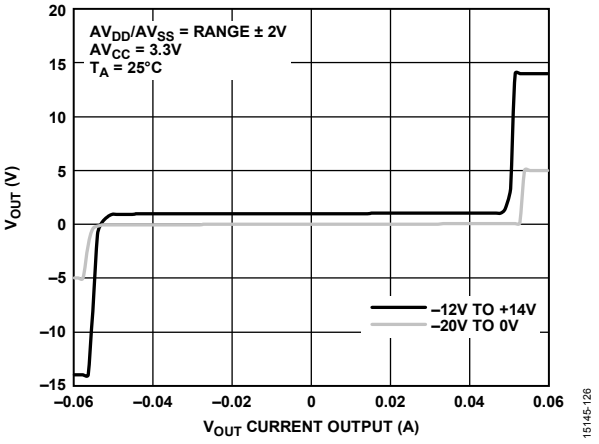

Figure 27. Source and Sink Capability of Output Amplifier

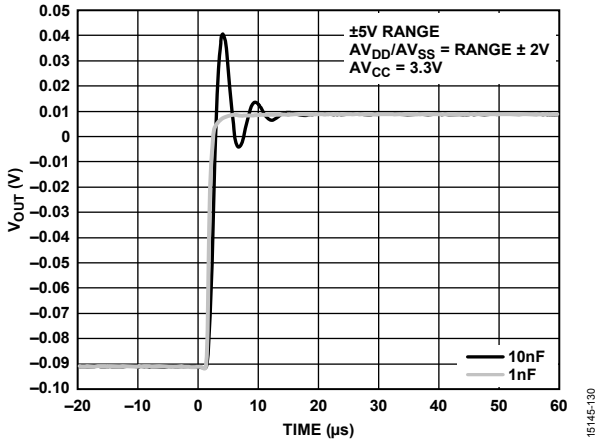

Figure 28. Output Voltage (V_{OUT}) vs. Settling Time at Various Capacitive Loads

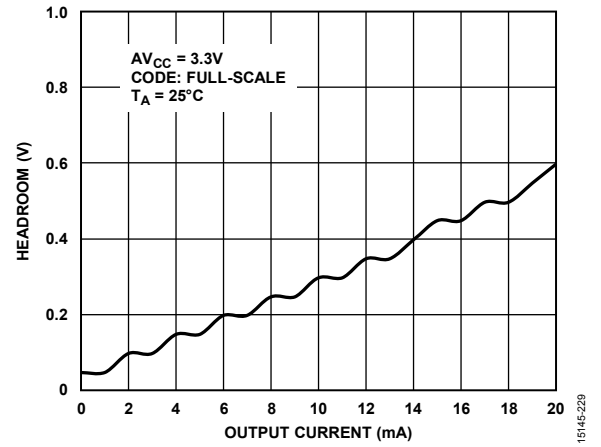

Figure 29. Headroom vs. Output Current

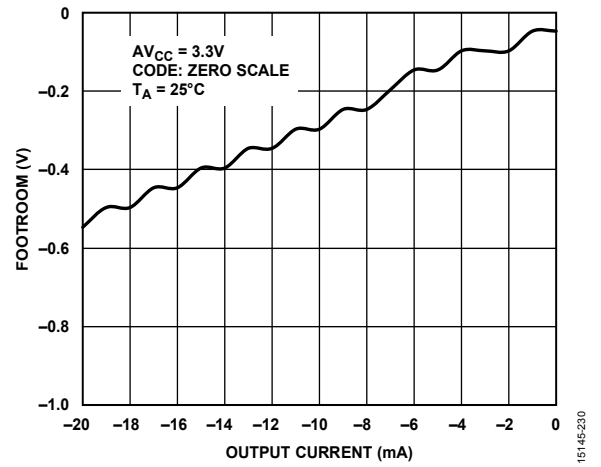

Figure 30. Footroom vs. Output Current

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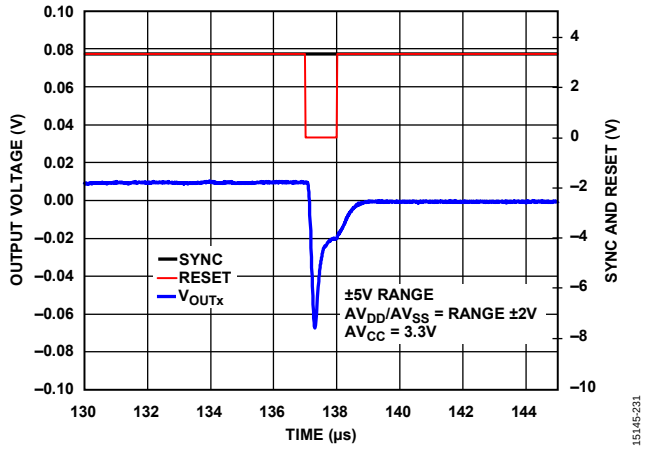

Figure 31. Hardware Reset Glitch

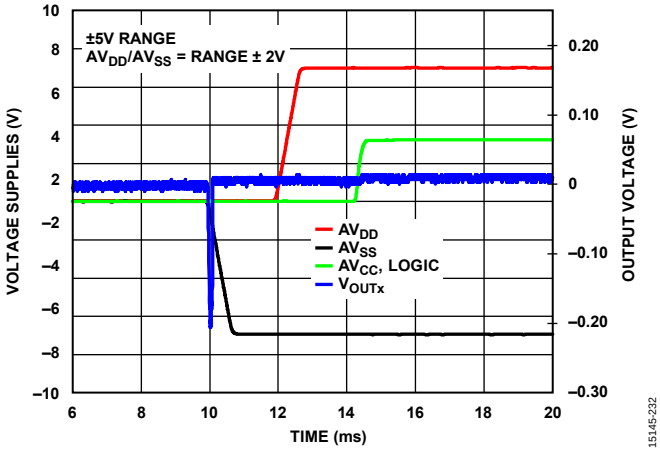

Figure 32. Power-Up Glitch

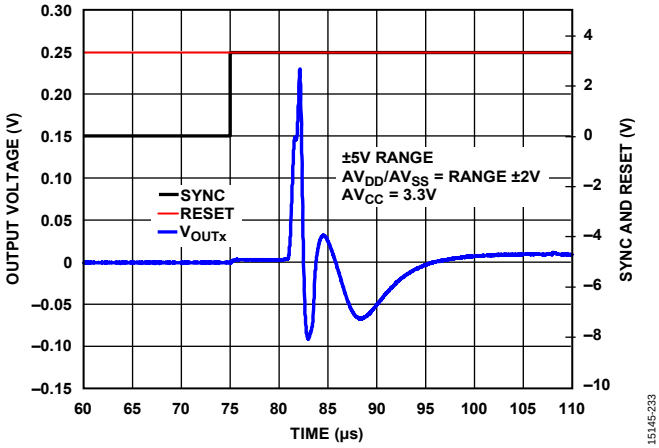

Figure 33. Output Span Enable Glitch

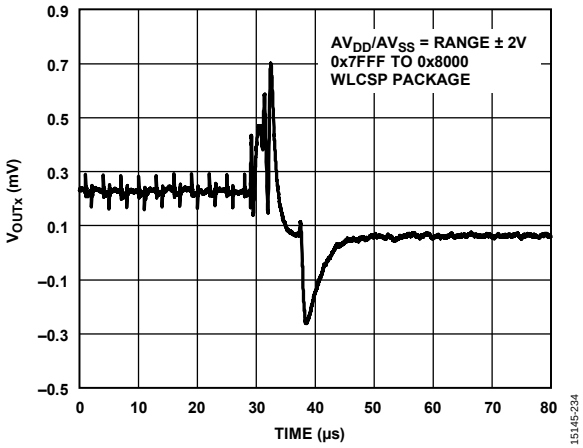

Figure 34. Digital-to-Analog Glitch Impulse for WLCSP Package

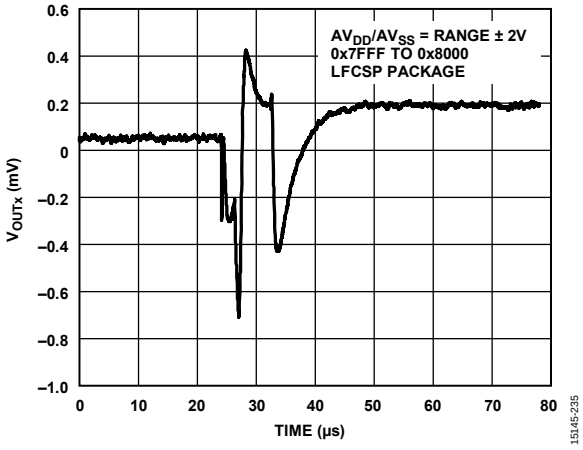

Figure 35. Digital-to-Analog Glitch Impulse for LFCSP Package

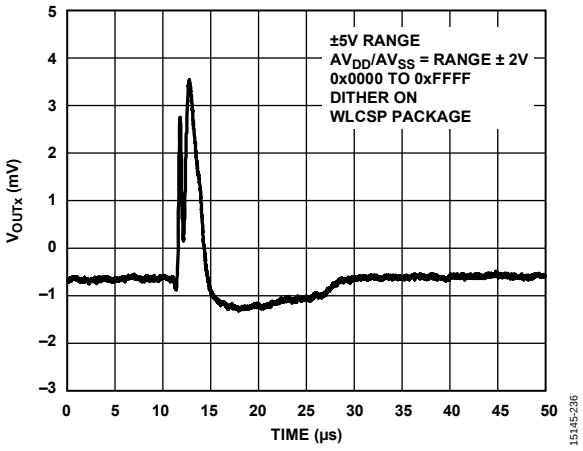

Figure 36. Analog Crosstalk for WLCSP Package (Dither Enabled)

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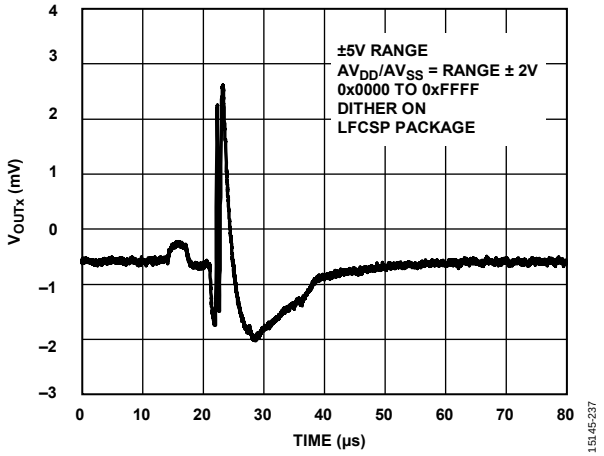

Figure 37. Analog Crosstalk for LFCSP Package (Dither Enabled)

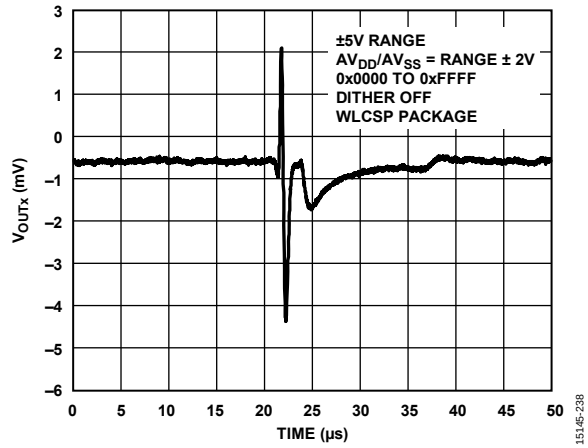

Figure 38. Analog Crosstalk for WLCSP Package (Dither Disabled)

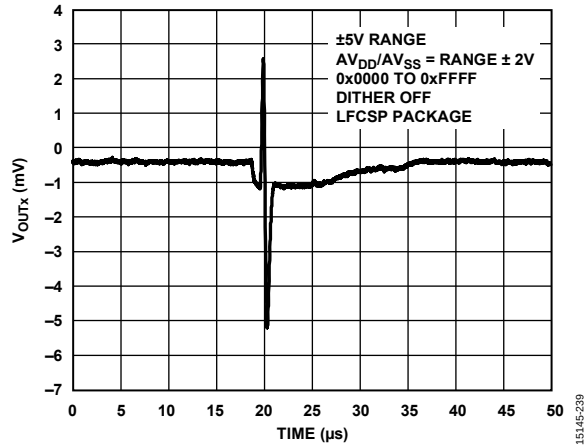

Figure 39. Analog Crosstalk for LFCSP Package (Dither Disabled)

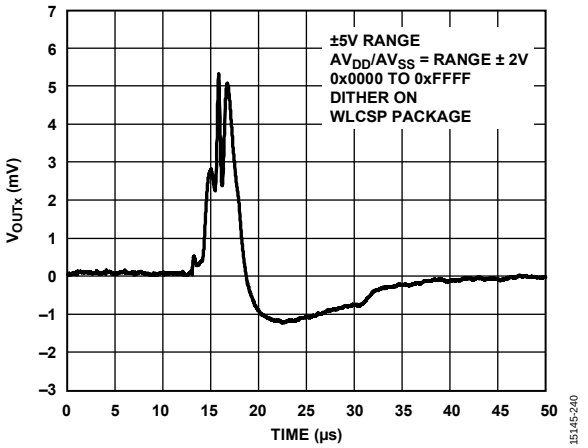

Figure 40. DAC-to-DAC Crosstalk for WLCSP Package (Dither Enabled)

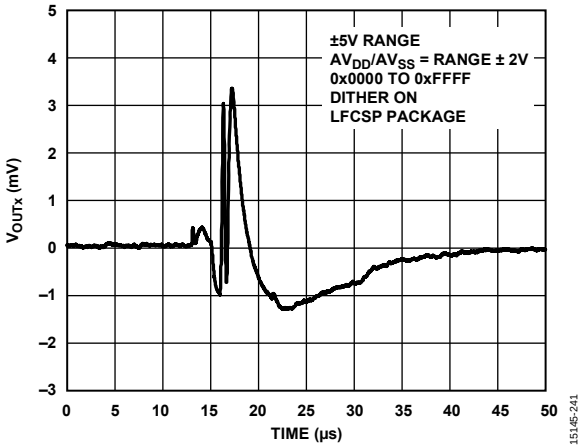

Figure 41. DAC-to-DAC Crosstalk for LFCSP Package (Dither Enabled)

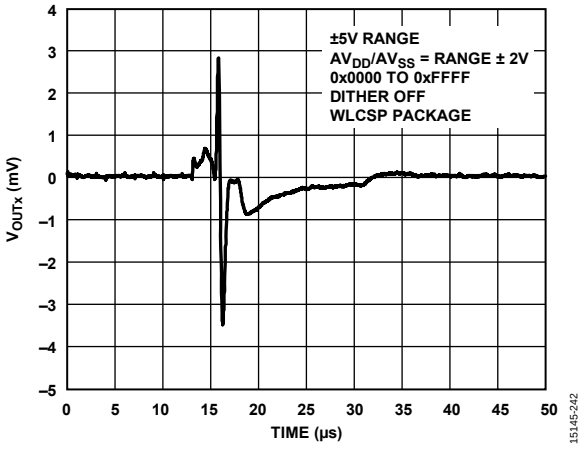

Figure 42. DAC-to-DAC Crosstalk for WLCSP Package (Dither Disabled)

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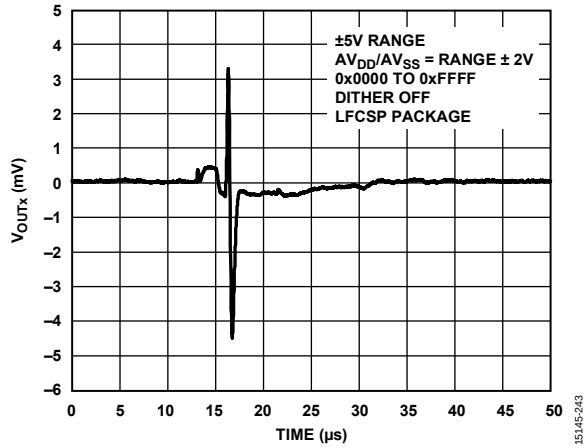

Figure 43. DAC-to-DAC Crosstalk for LFCSP Package (Dither Disabled)

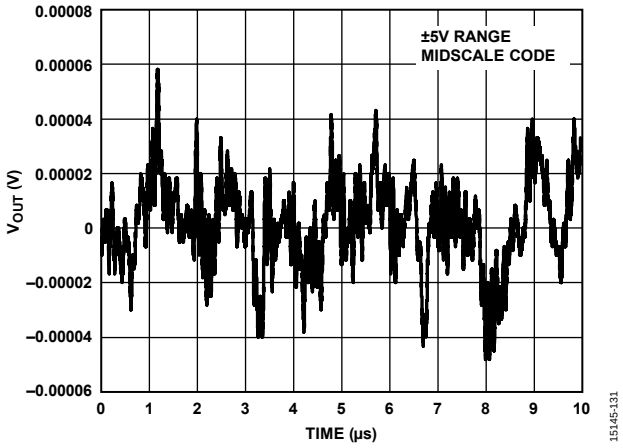

Figure 44. Peak-to-Peak Noise (0.1 Hz to 10 Hz Bandwidth) with Dither Disabled

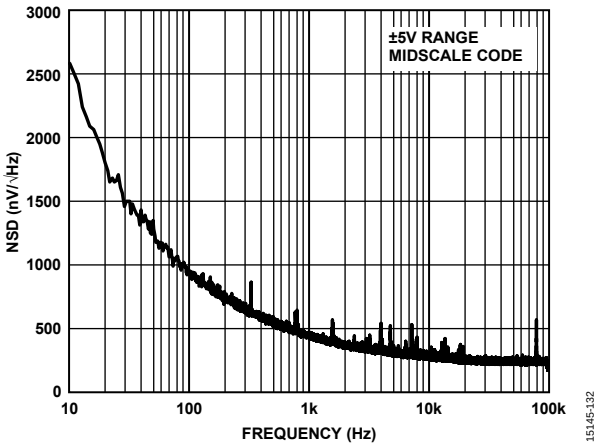

Figure 45. Noise Spectral Density (NSD) vs. Frequency

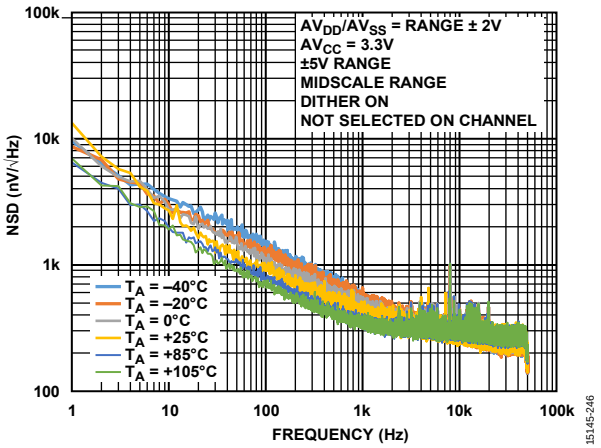

Figure 46. Output Noise (NSD) vs. Frequency over Temperature

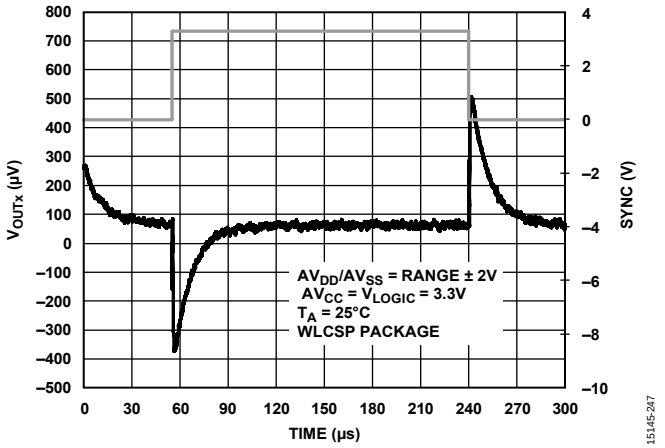

Figure 47. Digital Feedthrough for WLCSP Package

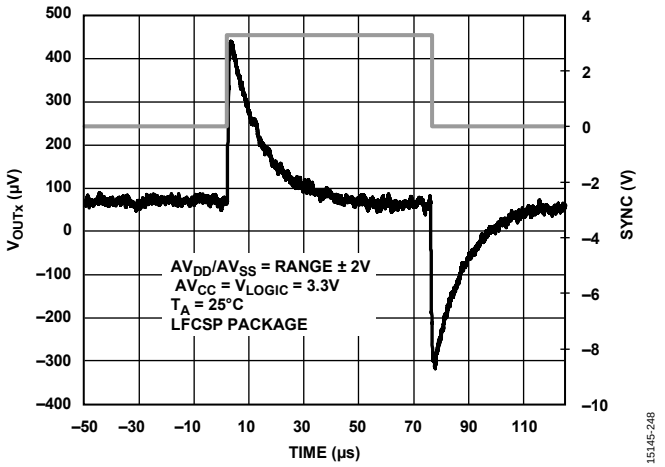

Figure 48. Digital Feedthrough for LFCSP Package

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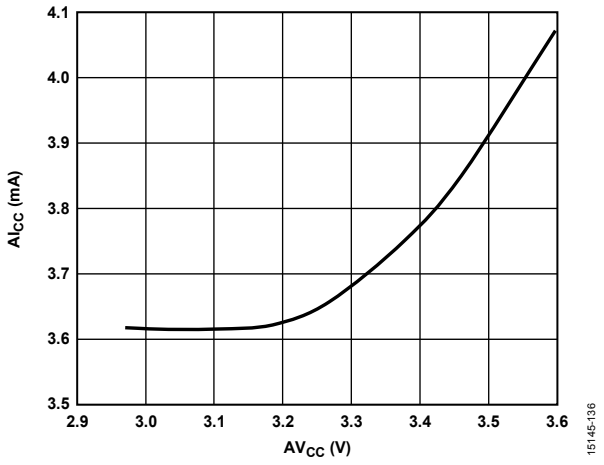

Figure 49. Supply Current (AI_{CC}) vs. Supply Voltage (AV_{CC})

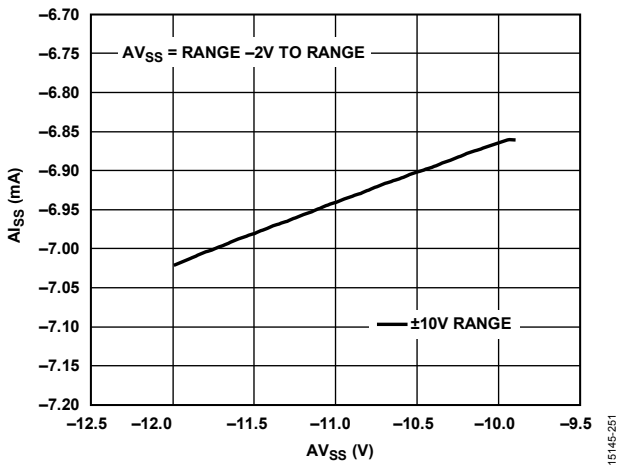

Figure 51. Supply Current (AI_{SS}) vs. Supply Voltage (AV_{SS})

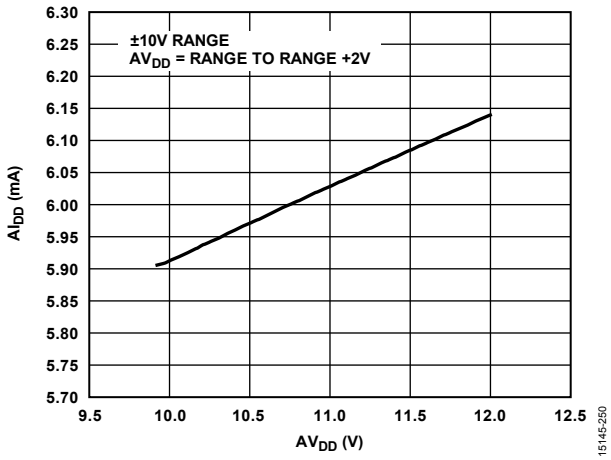

Figure 50. Supply Current (AI_{DD}) vs. Supply Voltage (AV_{DD})

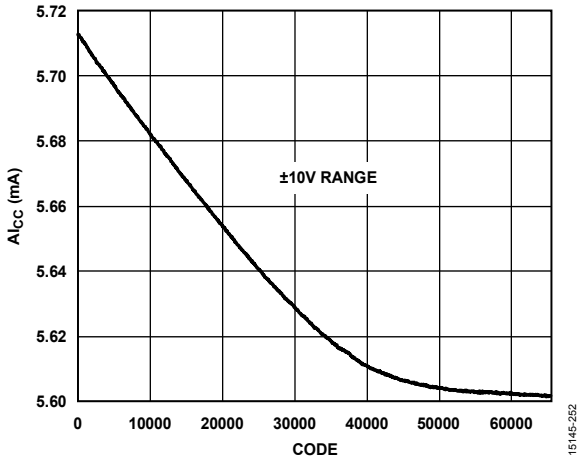

Figure 52. Supply Current (AI_{CC}) vs. Code

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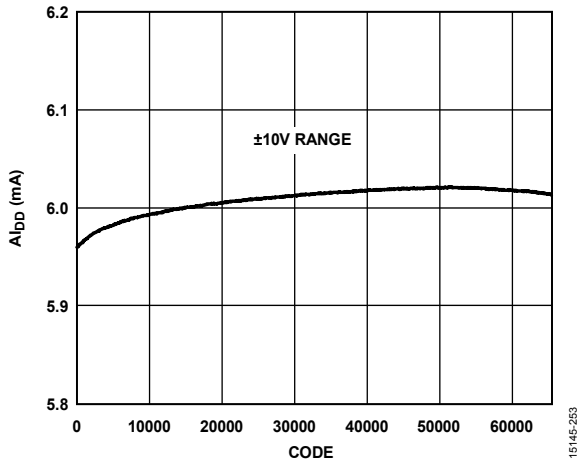

Figure 53. Supply Current (AI_{DD}) vs. Code

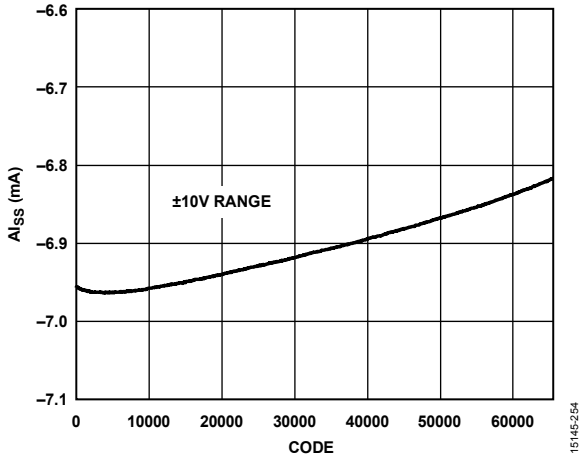

Figure 54. Supply Current (AI_{SS}) vs. Code

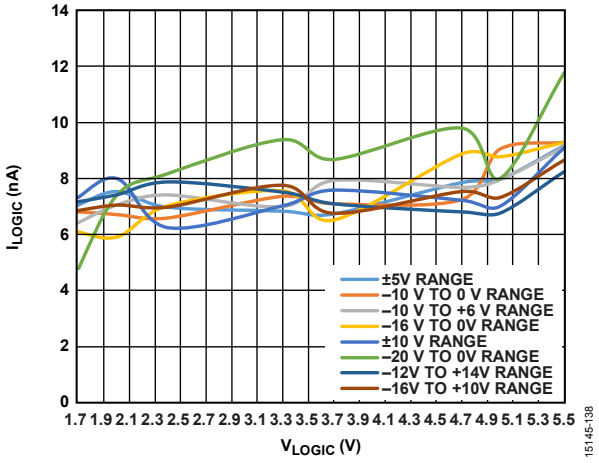

Figure 55. Logic Current (I_{LOGIC}) vs. Logic Input Voltage (V_{LOGIC})

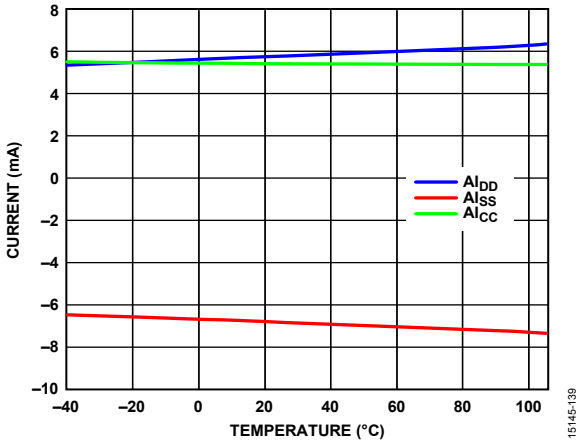

Figure 56. Supply Current vs. Temperature

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DITHER CHARACTERISTICS

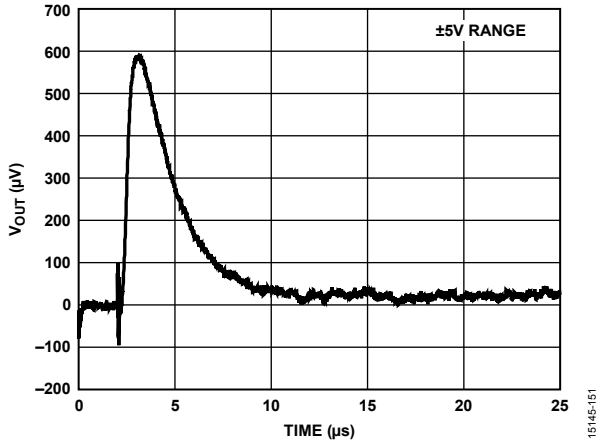

Figure 57. Transient on Dither Selected Channel (Dither Enabled)

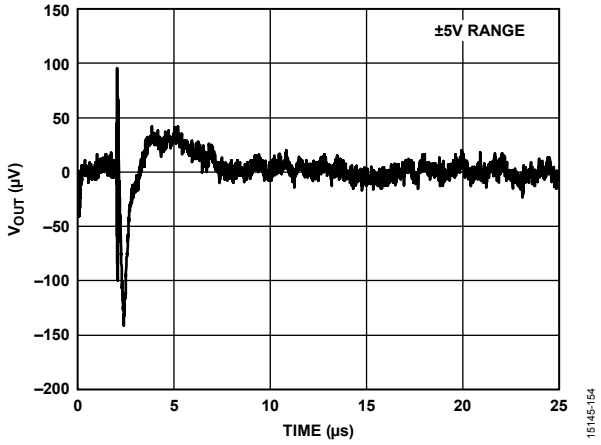

Figure 60. Transient on Nondither Selected Channel (Dither Disabled)

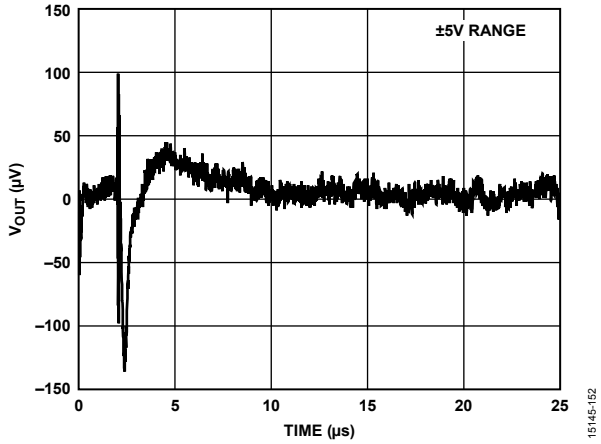

Figure 58. Transient on Nondither Selected Channel (Dither Enabled)

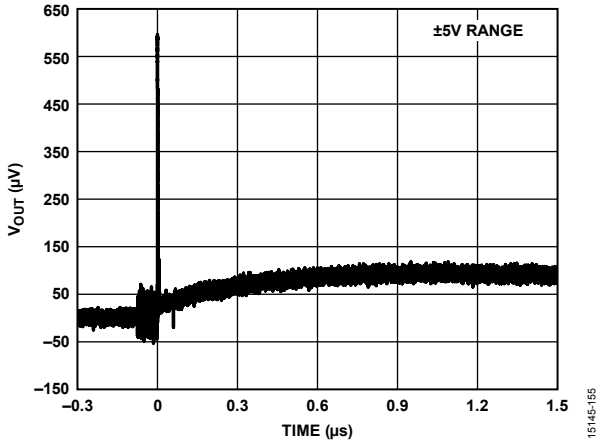

Figure 61. Dither DC Shift

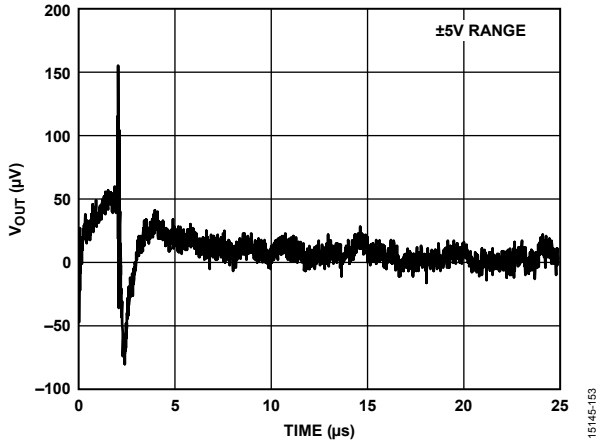

Figure 59. Transient on Dither Selected Channel (Dither Disabled)

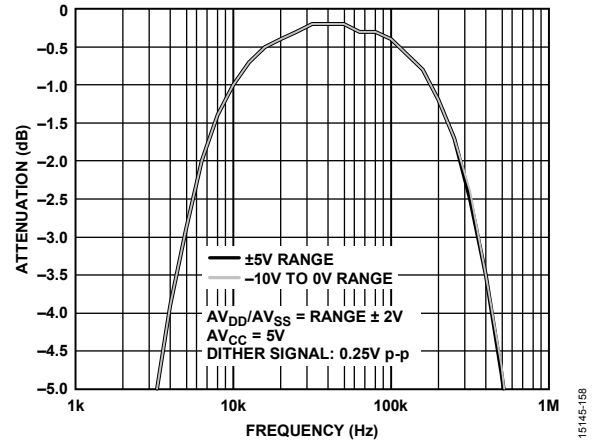

Figure 62. Dither Input to DAC Output Attenuation vs. Frequency (±5 V Range and –10 V to 0 V Range)

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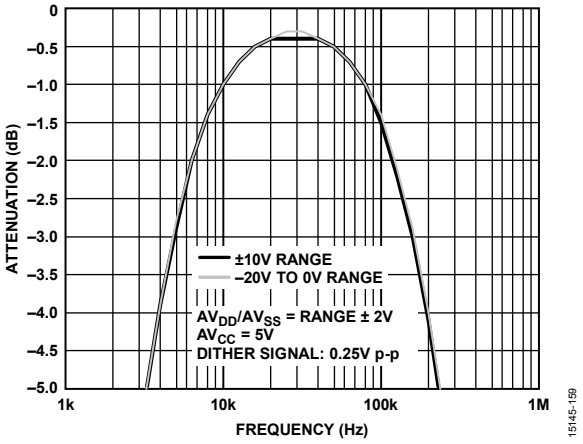

Figure 63. Dither Input to DAC Output Attenuation vs. Frequency (±10 V Range and −20 V to 0 V Range)

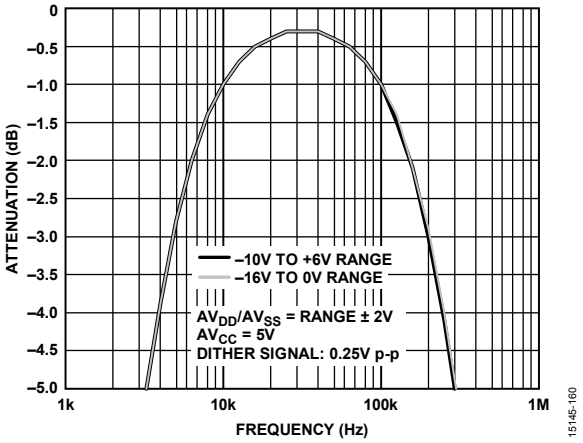

Figure 64. Dither Input to DAC Output Attenuation vs. Frequency (−10 V to +6 V Range and −16 V to 0 V Range)

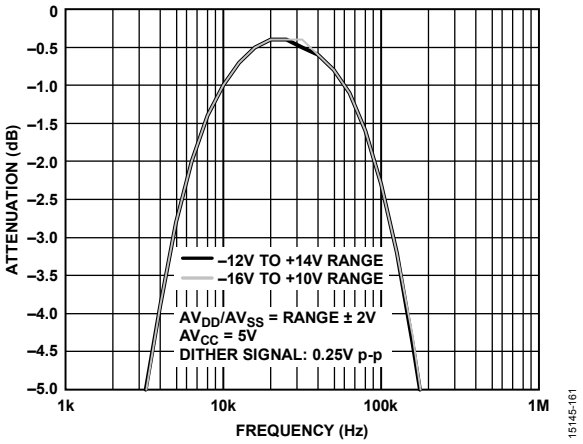

Figure 65. Dither Input to DAC Output Attenuation vs. Frequency (−12 V to +14 V Range and −16 V to +10 V Range)

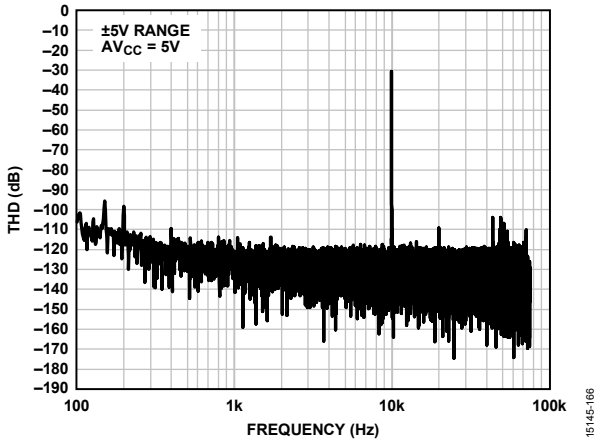

Figure 66. Total Harmonic Distortion (THD) vs. Frequency

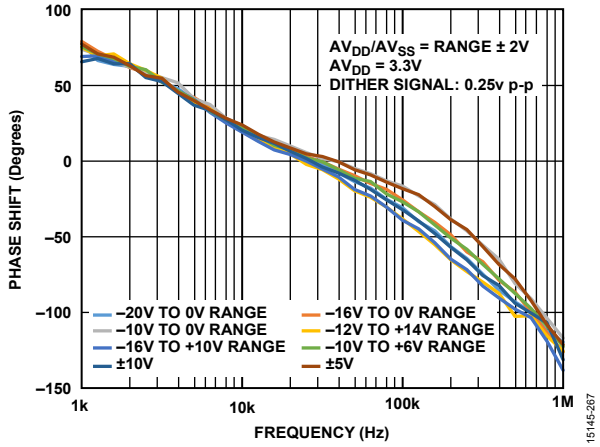

Figure 67. Dither Input to DAC Output Phase Shift vs. Frequency

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TERMINOLOGY

Total Unadjusted Error (TUE)
Total unadjusted error is a measure of the output error taking all the various errors into account, namely INL error, offset error, gain error, and output drift over supplies, temperature, and time. TUE is expressed in % FSR.

Relative Accuracy or Integral Nonlinearity (INL)
Relative accuracy or integral nonlinearity is a measurement of the maximum deviation, in LSBs, from a straight line passing through the endpoints of the DAC transfer function. Typical INL error vs. DAC code plots are shown in Figure 7 and Figure 10.

Differential Nonlinearity (DNL)
Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB maximum ensures monotonicity. This DAC is guaranteed monotonic by design. Typical DNL error vs. DAC code plots are shown in Figure 12 and Figure 14.

Zero-Scale Error
Zero-scale error is a measurement of the output error when zero code (0x0000) is loaded to the DAC register. Zero code error is expressed in mV.

Zero-Scale Error Temperature Coefficient
Zero code error drift is a measure of the change in zero code error with a change in temperature. It is expressed in µV/°C.

Bipolar Zero Error
Bipolar zero error is the deviation of the analog output from the ideal half-scale output of 0 V when the DAC register is loaded with 0x2000.

Bipolar Zero Error Temperature Coefficient
Bipolar zero drift is a measure of the change in the bipolar zero error with a change in temperature. It is expressed in µV/°C.

Gain Error
Gain error is a measure of the span error of the DAC. It is the deviation in slope of the DAC transfer characteristic from the ideal expressed as % FSR.

Gain Error Temperature Coefficient
Gain temperature coefficient is a measurement of the change in gain error with changes in temperature. It is expressed in ppm of FSR/°C.

Offset Error
Offset error is a measurement of the difference between $V_{OUT}x$ (actual) and $V_{OUT}x$ (ideal), expressed in mV, in the linear region of the transfer function. Offset error can be negative or positive.

Offset Error Drift
Offset error drift is a measurement of the change in offset error with a change in temperature. It is expressed in µV/°C.

Dither DC Shift
Dither dc shift is a measurement of the dc voltage difference between $V_{OUT}x$ (actual) and $V_{OUT}x$ (ideal) due to the coupling of a dither tone to the analog output. It is expressed in LSB.

Dither Transient
Dither transient is the amplitude of the impulse injected into the analog outputs due to the enabling or disabling of the dither functionality on an output channel. The transients are measured the selected output channel and the other nonselected channels. It is specified in nV-sec.

DC Power Supply Rejection Ratio (PSRR)
PSRR indicates how the output of the DAC is affected by changes in the supply voltage. PSRR is the ratio of the change in $V_{OUT}x$ to a change in AV_{DD} for a full-scale output of the DAC. It is measured in V/V.

Output Voltage Settling Time
Output voltage settling time is the amount of time it takes for the output of a DAC to settle to a specified level for a ¼ to ¾ full-scale input change and is measured from the rising edge of $\overline{SYNC}$.

Digital-to-Analog Glitch Impulse
Digital-to-analog glitch impulse is the impulse injected into the analog output when the input code in the DAC register changes state. It is normally specified as the area of the glitch in nV-sec, and is measured when the digital input code is changed by 1 LSB at the major carry transition (0x7FFF to 0x800 for the AD5767 and 0x7FFF to 0x8000 for the AD5766).

Digital Feedthrough
Digital feedthrough is a measure of the impulse injected into the analog output of the DAC from the digital inputs of the DAC, but is measured when the DAC output is not updated. It is specified in nV-sec, and measured with a full-scale code change on the data bus, that is, from all 0s to all 1s and vice versa.

DC Crosstalk
DC crosstalk is the dc change in the output level of one DAC in response to a change in the output of another DAC. It is measured with a full-scale output change on one DAC (or power-down and power-up) while monitoring another DAC maintained at midscale. It is expressed in µV.

DC crosstalk due to load current change is a measure of the impact that a change in load current on one DAC has to another DAC kept at midscale. It is expressed in µV/mA.

Digital Crosstalk
Digital crosstalk is the glitch impulse transferred to the output of one DAC at midscale in response to a full-scale code change (all 0s to all 1s and vice versa) in the input register of another DAC. It is measured in standalone mode and is expressed in nV-sec.

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Analog Crosstalk
Analog crosstalk is the glitch impulse transferred to the output of one DAC due to a change in the output of another DAC. It is measured by loading one of the input registers with a full-scale code change (all 0s to all 1s and vice versa), then executing a software LDAC command (see Table 21), and monitoring the output of the DAC whose digital code was not changed. The area of the glitch is expressed in nV-sec.

DAC-to-DAC Crosstalk
DAC-to-DAC crosstalk is the glitch impulse transferred to the output of one DAC due to a digital code change and subsequent analog output change of another DAC. It is measured by loading the attack channel with a full-scale code change (all 0s to all 1s and vice versa), using the write to and update commands while monitoring the output of the victim channel that is at midscale. The energy of the glitch is expressed in nV-sec.

Output Noise Spectral Density
Output noise spectral density is a measurement of the internally generated random noise. Random noise is characterized as a spectral density (nV/√Hz). It is measured by loading the DAC to midscale and measuring noise at the output. It is measured in nV/√Hz.

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THEORY OF OPERATION

DIGITAL-TO-ANALOG CONVERTER

The AD5766/AD5767 are 16-channel, 16-bit/12-bit, serial input, voltage output DACs capable of providing multiple output ranges with ±20 mA output current capability. The available output voltage ranges are as follows:

- −20 V to 0 V
- −16 V to 0 V
- −10 V to 0 V
- −10 V to +6 V
- −12 V to +14 V
- −16 V to +10 V
- ±5 V
- ±10 V

The devices operate from four supply voltages: AV_{CC}, AV_{DD}, AV_{SS}, and V_{LOGIC}. AV_{CC} is the power supply input voltage for the DACs and other low voltage circuitry, whereas AV_{DD} and AV_{SS} are the positive and negative analog supplies for the output amplifiers. The output amplifiers require +2 V of headroom and −2 V of footroom to drive 20 mA with a minimum output voltage error of less than 1 LSB. Table 9 shows the power supply requirements for the selected output range. V_{LOGIC} defines the logic levels for the digital input and output signals.

Table 9. Power Supply Requirements for the Selected Output Range

Range (V)	AV_{SS} Maximum (V)	AV_{DD} Minimum (V)
−20 to 0	−22	2.97
−16 to 0	−18	2.97
−10 to 0	−12	2.97
−10 to +6	−12	8
−12 to +14	−14	16
−16 to +10	−18	12
−5 to +5	−7	7
−10 to +10	−12	12

DAC ARCHITECTURE

The architecture of one DAC channel consists of a resistor string DAC followed by an output buffer amplifier. The voltage at the V_{REF} pin provides the reference voltage for the all DAC channels. Figure 68 shows a block diagram of the DAC architecture.

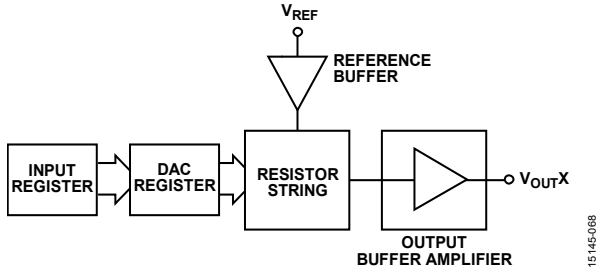

Figure 68. DAC Architecture

The input coding to the DAC is straight binary, the ideal output voltage is given by

$$V_{OUT} = \left(Span \times \frac{D}{N} \right) + V_{MIN}$$

where:
Span is the full extent of the DAC output voltage range from the minimum to the maximum limit.
D is the decimal equivalent of the binary code that is loaded to the DAC register.
N is 4096 for the AD5767 (12-bit version), and 65536 for the AD5766 (16-bit version).
V_{MIN} is the lowest voltage of the span.

RESISTOR STRING

The resistor string section is shown in Figure 69. It is a simplified resistor string structure, each of Value R. The digital code loaded to the DAC register determines at which node on the string the voltage is connected to be fed into the output amplifier. The voltage is tapped off by closing one of the switches connecting the string to the amplifier. Because a string of resistors is used, the DAC is guaranteed to be monotonic.

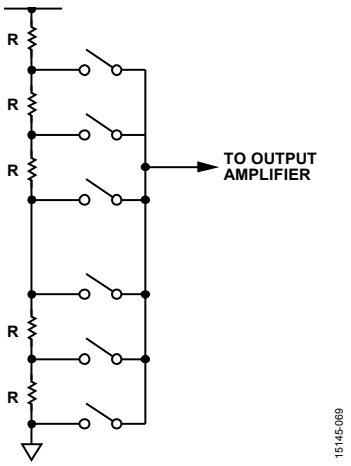

Figure 69. Resistor String

POWER-ON RESET (POR)

The AD5766/AD5767 contain a POR circuit that controls the output voltage during power-up. The AD5766/AD5767 outputs are clamped to ground at power-up and remain powered up at this level until a valid write sequence is made to the span register to configure the output range of the DAC. At power-on, the dither functionality is also enabled.

A software executable reset function resets the DAC to the power-up state. Command 0111 is reserved for this reset function (see Table 30). A minimum time is required between a reset and a successful write (see the timing characteristics in Table 4). Figure 70 shows the programming sequence to follow to configure the AD5766/AD5767 upon power-on.

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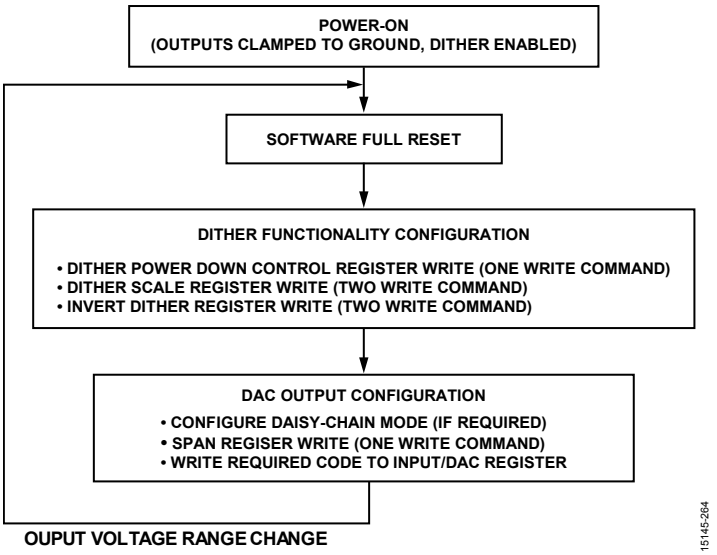

Figure 70. Programming Sequence to Write/Enable the AD5766/AD5767 Outputs

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DITHER

External dither signals can be coupled onto any DAC output by writing the appropriate value to the dither registers. The dither signals are applied to the N0 and N1 input pins (see Figure 71). If dither is not required, connect these pins to AGND. The dither signals amplitude have a maximum peak-to-peak voltage (ac voltage) of 0.25 V p-p, and the absolute input voltage (ac and dc voltage) must not exceed the range of 0 V to AV_{CC}. The dither signals can be attenuated and/or inverted internally on a per channel basis if required. Dither signals in the range of 10 kHz to 100 kHz can be applied to the dither input pins. Due to the nature of the internal dither circuitry, the dc value of the output can shift (see Table 1) and the shift can be compensated for. For the recommended configuration of the dither functionality, see the Applications Information section.

DITHER POWER-DOWN MODE

The AD5766/AD5767 contain a dither block power-down mode per channel. Command 0101 is reserved for the power-down function (see Table 10). The power-down mode is software-programmable by setting four bits, Bit D19 to Bit D16, in the power control register. To address the dither block power-down per channel function, D19 to D16 must be set to 0001 (see Table 26). Table 27 shows how the state of the Bit D16 corresponds to the mode of operation of the device. The dither functionality of any or all DACs can be powered down to the selected mode by setting the corresponding 16 bits (D15 to D0) to 1.

Ensure that all channels are powered up before writing to the span register.

MONITOR MUX

The AD5766/AD5767 contain a channel monitor function that consists of an analog multiplexer addressed via the serial interface, allowing any channel output to be routed to the common MUX_OUT pin for external monitoring.

Because the MUX_OUT pin is not buffered, the amount of current drawn from this pin creates a voltage drop across the switches, which in turn leads to an error in the voltage being monitored. Therefore, the MUX_OUT pin must be connected to only high impedance inputs or externally buffered.

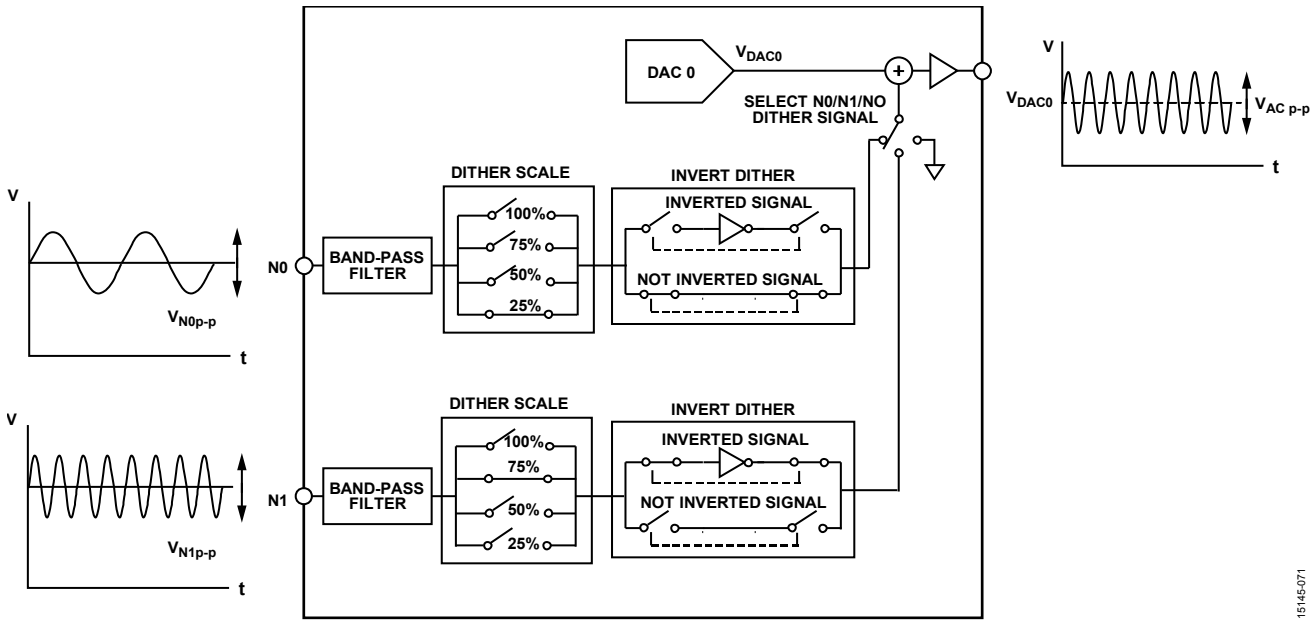

Figure 71. Dither Signal Generation

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SERIAL INTERFACE

The AD5766/AD5767 4-wire ($\overline{\text{SYNC}}$, SCLK, SDI, and SDO) interface is compatible with SPI, QSPI, and MICROWIRE interface standards as well as most digital signal processors (DSPs). The write sequence begins after bringing the $\overline{\text{SYNC}}$ line low, maintaining this line low until the complete data-word is loaded from the SDI pin. Data is loaded into the AD5766/AD5767 at the SCLK falling edge transition (see Figure 2). When a rising edge is detected on $\overline{\text{SYNC}}$, the serial data-word is decoded according to the instructions in Table 10. The command must be a multiple of 24; otherwise, the device ignores the command. The AD5766/AD5767 contain an SDO pin to allow the user to daisy-chain multiple devices together or to read back the contents of the status register.

Readback Operation

The contents of the status registers can be read back via the SDO pin. Figure 4 shows how the registers are decoded. After a register has been addressed for a read, the next 24 clock cycles clock the data out on the SDO pin. The clocks must be applied while SYNC is low. For a read of a single register, the no operation (NOP) function clocks out the data. Alternatively, if more than one register is to be read, the data of the first register to be addressed clocks out at the same time that the second register to be read is being addressed.

Daisy-Chain Operation

Daisy chaining minimizes the number of port pins required from the controlling IC. As shown in Figure 72, the SDO pin of one package must be tied to the SDI pin of the next package. To enable daisy-chain mode, the DC_EN bit in Table 15 must be high. When two AD5766/AD5767 devices are daisy-chained, 48 bits of data are required. The first 24 bits are assigned to U2, and the second 24 bits are assigned to U1, as shown in Figure 72. Keep the $\overline{\text{SYNC}}$ pin low until all 48 bits are clocked into their respective serial registers.

The $\overline{\text{SYNC}}$ pin is then pulled high to complete the operation.

To prevent data from mislocking (for example, due to noise) the device includes an internal counter; if the SCLK falling edges count is not a multiple of 24, the device ignores the command. A valid clock count is 24, 48, 72, and so on. The counter resets when $\overline{\text{SYNC}}$ returns high.

Daisy-chain mode is disabled by default and is enabled using the daisy-chain control register (see Table 15).

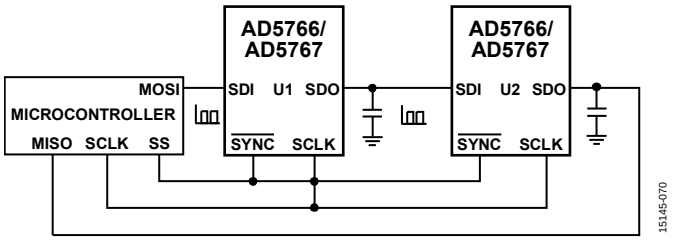

Figure 72. Daisy-Chain Block Diagram

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REGISTER DETAILS

INPUT SHIFT REGISTER

The input shift register of the AD5766/AD5767 are 24 bits wide. Data is loaded MSB first (D23). The first four bits are the command bits, C3 to C0 (see Figure 73), followed by the 4-bit DAC address bits (see Table 11), and finally the data bits. The 24-bit data-word is transferred to the input register on the 24 falling edges of SCLK and are updated on the rising edge of SYNC.

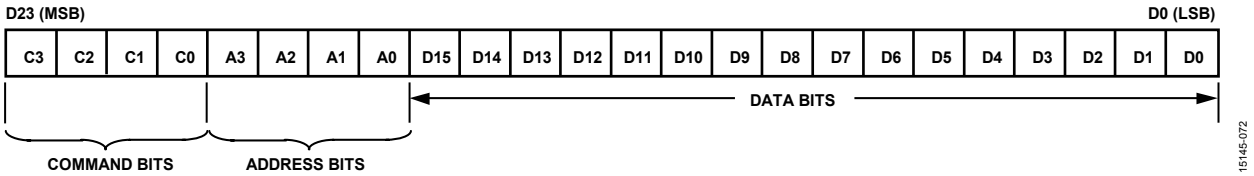

Figure 73. Input Shift Register Content

Table 10. Command Definitions[1]

C3	C2	C1	C0	A3	A2	A1	A0	Name	Description
0	0	0	0	0	0	0	0	NOP/monitor mux control	No operation (all zeros register). Monitor mux control register (D4 = 1) determines whether a DAC output or no output is switched out on the MUX_OUT pin.
0	0	0	0	0	0	0	1	Daisy-chain mode	Enables/disables the SDO output buffer for daisy-chain mode.
0	0	0	1	A3[2]	A2[2]	A1[2]	A0[2]	Write to DACx input register	Writes data to the input register for the selected DAC channel.
0	0	1	0	A3[2]	A2[2]	A1[2]	A0[2]	Write to input register and DAC register	Writes data to the input register and DAC register for the selected DAC channel.
0	0	1	1	X	X	X	X	Software load DAC (LDAC)	Updates the selected DAC register with data from the corresponding input register.
0	1	0	0	X	X	X	X	Span	Selects the output span of the AD5766/AD5767.
0	1	0	1	X	X	X	0	Reserved	Not applicable.
0	1	0	1	0	0	0	1	Dither power control	Powers up/down dither functionality of individual DAC channels.
0	1	1	0	X	X	X	X	Write input data to all DAC registers	Writes data to input registers and DAC registers for all DAC channels.
0	1	1	1	0	0	0	0	Software full reset	Writing 0x1234 to this register resets the AD5766/AD5767.
1	0	0	0	A3[2]	A2[2]	A1[2]	A0[2]	Select register for readback	Selects the register to read back for a selected DAC channel.
1	0	0	1	X	X	X	X	Apply N0 or N1 dither signal to DACs (DAC 7 to DAC 0)	Selects whether dither on N0, dither on N1, or no dither is applied to each DAC output.
1	0	1	0	X	X	X	X	Apply N0 or N1 dither signal to DACs (DAC 15 to DAC 8)	Selects whether dither on N0, dither on N1, or no dither is applied to each DAC output.
1	1	0	0	X	X	X	X	Dither scale (DAC 7 to DAC 0)	Scales the dither signal applied to the selected DAC outputs.
1	1	0	1	X	X	X	X	Dither scale (DAC 15 to DAC 8)	Scales the dither signal applied to the selected DAC outputs.
1	0	1	1	X	X	X	X	Invert dither	Inverts the dither signal applied to the selected DAC outputs.
1	1	1	0	X	X	X	X	Reserved	Not applicable.
1	1	1	1	X	X	X	X	Reserved	Not applicable.

[1] X means don't care.
[2] See Table 11 for the address bit setting.

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Table 11 shows the DAC x address commands. For applications using the WLCSP package that do not require all 16 channels, do not use Channel 8 because it is more sensitive to crosstalk and digital feedthrough.

Table 11. DAC x Address Commands

Address				
A3	**A2**	**A1**	**A0**	**Selected DAC**
0	0	0	0	DAC 0
0	0	0	1	DAC 1
0	0	1	0	DAC 2
0	0	1	1	DAC 3
0	1	0	0	DAC 4
0	1	0	1	DAC 5
0	1	1	0	DAC 6
0	1	1	1	DAC 7
1	0	0	0	DAC 8
1	0	0	1	DAC 9
1	0	1	0	DAC 10
1	0	1	1	DAC 11
1	1	0	0	DAC 12
1	1	0	1	DAC 13
1	1	1	0	DAC 14
1	1	1	1	DAC 15

MONITOR MUX CONTROL

The monitor mux control command determines whether one of the DAC outputs or none is switched out on the MUX_OUT pin depending on the desired D[4:0] value. To assert the no operation command, write all zeros to the D15 to D0 bits.

Table 12. Monitor Mux Control Register

D23	D22	D21	D20	D19	D18	D17	D16	D15 to D5	D4 to D0
0	0	0	0	0	0	0	0	Don't care	VOUT_SEL

Table 13. Output Voltage Selection from Mux

VOUT_SEL, Bits[4:0][1]					Mux Output
0	X	X	X	X	No output is switched out
1	0	0	0	0	$V_{OUT}0$
1	0	0	0	1	$V_{OUT}1$
1	0	0	1	0	$V_{OUT}2$
1	0	0	1	1	$V_{OUT}3$
1	0	1	0	0	$V_{OUT}4$
1	0	1	0	1	$V_{OUT}5$
1	0	1	1	0	$V_{OUT}6$
1	0	1	1	1	$V_{OUT}7$
1	1	0	0	0	$V_{OUT}8$
1	1	0	0	1	$V_{OUT}9$
1	1	0	1	0	$V_{OUT}10$
1	1	0	1	1	$V_{OUT}11$
1	1	1	0	0	$V_{OUT}12$
1	1	1	0	1	$V_{OUT}13$
1	1	1	1	0	$V_{OUT}14$
1	1	1	1	1	$V_{OUT}15$

[1] X means don't care.

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NO OPERATION

Writing all zeros does not vary the state of the device.

Table 14. No Operation Register

D23	D22	D21	D20	D19	D18	D17	D16	D15 to D0
0	0	0	0	0	0	0	0	0000 0000 0000 0000

DAISY-CHAIN MODE

To use the daisy-chain mode, enable the DC_EN bit in the daisy-chain control register. This bit is linked to the internal SDO buffer. If the functionality is not required, set the DC_EN bit to 0 to save the power consumed by the SDO buffer.

Table 15. Daisy-Chain Control Register

D23	D22	D21	D20	D19	D18	D17	D16	D15 to D1	D0
0	0	0	0	0	0	0	1	Don't care	DC_EN

Table 16. Daisy-Chain Enable/Disable Bit Description

DC_EN	Description
0	Daisy chain disabled (default)
1	Daisy chain enabled

WRITE AND UPDATE COMMANDS

Write to DAC x Input Register

This command allows the user to write to the dedicated input register of each DAC individually. The output of the DAC does not change its value until a write to the software LDAC register occurs with the appropriate bit set to include the addressed channel in the update.

Table 17. AD5766 Write to DAC x Input Register

D23	D22	D21	D20	D19 to D16	D15 to D0
0	0	0	1	DAC x address (see Table 11)	Input register data

Table 18. AD5767 Write to DAC x Input Register

D23	D22	D21	D20	D19 to D16	D15 to D4	D3 to D0
0	0	0	1	DAC x address (see Table 11)	Input register data	Don't care

Write to Input Register and DAC Register

This command writes directly to the selected DAC register and updates the output accordingly.

Table 19. AD5766 Write to DACx Input and DAC Register

D23	D22	D21	D20	D19 to D16	D15 to D0
0	0	1	0	DAC x address (see Table 11)	Input register data

Table 20. AD5767 Write to DACx Input and DAC Register

D23	D22	D21	D20	D19 to D16	D15 to D4	D3 to D0
0	0	1	0	DAC x address (see Table 11)	Input register data	Don't care

Software LDAC Register

This command copies data from the selected input registers to the corresponding DAC registers and the outputs update accordingly.

Table 21. Software LDAC Register

D23	D22	D21	D20	D19 to D16	D15 to D0
0	0	1	1	Don't care	LDAC (bit for each channel)

Table 22. LDAC Bit Description

LDAC	Description
0	Do not update channel
1	Update channel

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SPAN REGISTER

This register selects the output span of the AD5766/AD5767. See Table 24 and Table 25. Always issue a software reset before writing to the span register.

Table 23. Span Register

D23	D22	D21	D20	D19 to D5	D4 to D3	D2 to D0
0	1	0	0	Don't care	P[1:0] (power-up condition)	S[2:0] (span)

Table 24. Span Selection

S2	S1	S0	Output Voltage Range
0	0	0	−20 V to 0 V
0	0	1	−16 V to 0 V
0	1	0	−10 V to 0 V
0	1	1	−12 V to +14 V
1	0	0	−16 V to +10 V
1	0	1	−10 V to +6 V
1	1	0	−5 V to +5 V
1	1	1	−10 V to +10 V

Table 25. Power-Up Condition Selection

P1	P0	Power-Up Condition
0	0	Zero scale
0	1	Midscale
1	Don't care	Full scale

DITHER POWER CONTROL REGISTER

The dither power control register with D[19:16] = 0001 powers up or powers down the dither functionality of the individual DACs. It is recommended to power down the selected channel dither block during the first write to the AD5766/AD5767 if no dither tone is input on to the dither inputs N0 or N1.

Table 26. Dither Power Control Register

D23	D22	D21	D20	D19	D18	D17	D16	D15 to D0
0	1	0	1	0	0	0	1	Power-down bit for each channel dither block (for example, D15 = DAC 15, D8 = DAC 8, and D0 = DAC 0)

Table 27. Dither Power Control

D16	Operating Mode
0	Normal operation (default)
1	Powered down

WRITE INPUT DATA TO ALL DAC REGISTERS

This command writes the data in D[15:0] to the DAC register of all DACs and sets all DAC outputs to the same value. For the AD5766/AD5767, the data is written in D[15:0] for the 16-bit resolution DAC and in D[15:4] for the 12-bit resolution version.

Table 28. AD5766 Write Input Data to All DAC Registers

D23	D22	D21	D20	D19 to D16	D15 to D0
0	1	1	0	Don't care	DAC register data

Table 29. AD5767 Write Input Data to All DAC Registers

D23	D22	D21	D20	D19 to D16	D15 to D4	D3 to D0
0	1	1	0	Don't care	DAC register data	Don't care

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SOFTWARE FULL RESET

Writing 0x1234 initiates a reset routine, which returns the AD5766/AD5767 to the power-on state.

Table 30. Software Full Reset Register

D23	D22	D21	D20	D19 to D16	D15 to D12	D11 to D8	D7 to D4	D3 to D0
0	1	1	1	0000	0001	0010	0011	0100

SELECT REGISTER FOR READBACK

This command selects which registers to read back (see Table 31). After issuing this command, the contents of the selected registers are clocked out on the SDO on the next 24-bit frame (see Table 32).

Table 31. Initiate Readback Register

D23	D22	D21	D20	D19 to D16	D15 to D0
1	0	0	0	DAC x address (see Table 11)	Don't care

Table 32. Readback Data Register

D23	D22	D21	D20	D19 to D16	D15 to D10	D9	D8 to D7	D6 to D5	D4	D3	D2 to D0
1	0	0	0	DAC x address (see Table 11)	000000	Invert dither	Dither scale	Dither signal	Reserved	Reserved	Span S[2:0]

Table 33. Readback Register Data Functions

Bit Name	Description			
Span S[2:0]	Span register			
	D2	**D1**	**D0**	**Output Voltage Range**
	0	0	0	−20 V to 0 V
	0	0	1	−16 V to 0 V
	0	1	0	−10 V to 0 V
	0	1	1	−12 V to +14 V
	1	0	0	−16 V to +10 V
	1	0	1	−10 V to +6 V
	1	1	0	−5 V to +5 V
	1	1	1	−10 V to +10 V
Reserved	This is a reserved bit; ignore its contents			
Dither Signal	Apply N0 or N1 dither signal to DACs register			
	D6	**D5**	**Dither Setting**	
	0	0	No dither applied	
	0	1	N0 dither applied	
	1	0	N1 dither applied	
	1	1	No dither applied	
Dither Scale	Dither scale register			
	D8	**D7**	**Scaling Factor**	
	0	0	No scaling	
	0	1	75% scaling	
	1	0	50% scaling	
	1	1	25% scaling	
Invert Dither	Invert dither register			
	D9	**Dither Mode**		
	0	Dither signal is not inverted		
	1	Dither signal is inverted		

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APPLY N0 OR N1 DITHER SIGNAL TO DACs REGISTER

These commands determine which dither signal, N0 or N1, is applied to the selected DACs. Couple the dither signals to the AD5766/AD5767 outputs after the dither signals are configured and the clamp to ground is removed by writing to the span register. Refer to the Applications Information section for a more information.

Table 34. Apply N0 or N1 Dither Signal to DACs Register (DAC 7 to DAC 0)

D23 to D20	D19 to D16	D15 to D14	D13 to D12	D11 to D10	D9 to D8	D7 to D6	D5 to D4	D3 to D2	D1 to D0
1001	Don't care	DAC 7	DAC 6	DAC 5	DAC 4	DAC 3	DAC 2	DAC 1	DAC 0

Table 35. Apply N0 or N1 Dither Signal to DACs Register (DAC 15 to DAC 8)

D23 to D20	D19 to D16	D15 to D14	D13 to D12	D11 to D10	D9 to D8	D7 to D6	D5 to D4	D3 to D2	D1 to D0
1010	Don't care	DAC 15	DAC 14	DAC 13	DAC 12	DAC 11	DAC 10	DAC 9	DAC 8

Table 36 shows the dither scaling setting using Bits[D15:D14] as an example. To apply the N0 dither to DAC 7 (see Table 34), set D15 to 0 and D14 to 1. The same dither selection settings apply to the other bits, Bits[D13:D12], Bits[D11:D10], Bits[D9:D8], Bits[D7:D6], Bits[D5:D4], Bits[D3:D2], and Bits[D1:D0] in Table 34 and Table 35.

Table 36. Dither Selection for DAC x (DAC 0 to DAC 15)

D15	D14	Dither Setting
0	0	No dither applied
0	1	N0 dither signal applied
1	0	N1 dither signal applied
1	1	No dither applied

DITHER SCALE

This command scales the dither before it is applied to the selected channel.

Table 37. Dither Scaling Register (DAC 7 to DAC 0)

D23 to D20	D19 to D16	D15 to D14	D13 to D12	D11 to D10	D9 to D8	D7 to D6	D5 to D4	D3 to D2	D1 to D0
1100	Don't care	DAC 7	DAC 6	DAC 5	DAC 4	DAC 3	DAC 2	DAC 1	DAC 0

Table 38. Dither Scaling Register (DAC 15 to DAC 8)

D23 to D20	D19 to D16	D15 to D14	D13 to D12	D11 to D10	D9 to D8	D7 to D6	D5 to D4	D3 to D2	D1 to D0
1101	Don't care	DAC 15	DAC 14	DAC 13	DAC 12	DAC 11	DAC 10	DAC 9	DAC 8

Table 39 shows the dither scaling setting using Bits[D15:D14] as an example. To apply 25% scaling to DAC 7 (see Table 37), set D15 to 1 and D14 to 1. The same dither scaling settings apply to the other bits, Bits[D13:D12], Bits[D11:D10], Bits[D9:D8], Bits[D7:D6], Bits[D5:D4], Bits[D3:D2], and Bits[D1:D0] in Table 34 and Table 35.

Table 39. Apply Dither Signal to DAC x (DAC 0 to DAC 15)

D15	D14	Scaling Factor
0	0	No scaling
0	1	75% scaling
1	0	50% scaling
1	1	25% scaling

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INVERT DITHER REGISTER

This command inverts the dither applied to the selected DACs when the appropriate bit is set to 0.

Table 40. Invert Dither Register

D23	D22	D21	D20	D19 to D16	D15 to D0
1	0	1	1	Don't care	Dx (invert dither bit for each channel)

Table 41. Invert Dither

Dx	Dither Mode
0	Dither signal is not inverted (default)
1	Dither signal is inverted

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APPLICATIONS INFORMATION

DITHER CONFIGURATION

The AD5766/AD5767 contain two dither input pins to allow dither tone signals to be coupled to any of the 16 DAC output channels.

Operate the AD5766/AD5767 using the dither functionality to minimize the transient amplitude seen on the DAC outputs when the dither functionality is enabled or disabled. The recommended configuration of the dither functionality is as follows:

1. After the AD5766/AD5767 power up, the input dither signals must be configured by writing to the dither scale register and the invert dither register if required.
2. Configure the AD5766/AD5767 in normal operating mode before applying dither by programming the span register.
3. Write to the apply N0 or N1 dither signal to DACs register to couple the N0/N1 input dither signals to any DAC output, $V_{OUT}x$.

Enabling the dither feature on a channel can increase its sensitivity to digital feedthrough.

THERMAL CONSIDERATIONS

Up to ±20 mA can be sourced from each channel on the AD5766/AD5767; thus, it is important to understand the effects of power dissipation on the package and its effects on junction temperature. The internal junction temperature must not exceed 150°C. The AD5766/AD5767 are packaged in a 49-ball, 4 mm × 4mm WLCSP and a 40-lead 6 mm × 6 mm LFCSP package. The thermal impedance, θ_{JA}, is specified in the Absolute Maximum Ratings section. It is important that the device is not operated under conditions that cause the junction temperature to exceed the maximum temperature specified in the Absolute Maximum Ratings section.

The Thermal Calculation Example (WLCSP) section details how to calculate the die temperature and maximum permitted ambient temperature. The quiescent current of the AV_{DD}, AV_{SS}, AV_{CC}, and V_{LOGIC} pins must also be included in the calculation of the junction temperature. These calculations use the typical supply currents specified in Table 1.

Thermal Calculation Example (WLCSP)

For this thermal calculation example, all 16 channels are enabled with the ±10 V output voltage range used. Each channel is drawing 2 mA for a +1V output voltage.

$$AV_{DD} = Span + 2\text{ V} = 12\text{ V}$$

$$AV_{SS} = Span - 2\text{ V} = -12\text{ V}$$

$$AV_{CC} = V_{LOGIC} = 3.3\text{ V}$$

where *Span* is the output voltage range, ±10 V.

The current required to supply 16 channels (output power) is

$$2\text{ mA} \times 16 = 32\text{ mA}$$

The power required on the AV_{DD} rail for the AD5766/AD5767 to supply the 16 channels and 6 mA typical supply current is

$$12\text{ V} \times (32\text{ mA} + 6\text{ mA}) = 0.456\text{ W}$$

Next, add power dissipated by the AV_{SS}, AV_{CC}, and V_{LOGIC} rails (input power) as follows:

$$0.456\text{ W} + (-12\text{ V} \times -9\text{ mA}) + (3.3\text{ V} \times 8.3\text{ mA}) + (3.3\text{ V} \times 0.02\ \mu\text{A}) = 0.59\text{ W}$$

To calculate the power dissipated by the AD5766/AD5767, use the following equation:

$$P_{DISS} = Input\ Power - Output\ Power$$

For example,

$$0.59\text{ W} - (32\text{ mA} \times 1\text{ V}) = 0.558\text{ W}$$

Then, calculate the die temperature,

$$0.558\text{ W} \times 53°\text{C/W} = 29.57°\text{C}$$

Using the following equation to calculate the maximum permitted ambient temperature:

$$T_{A\,MAX} = T_{J\,MAX} - Die\ Temperature$$

For example,

$$150°\text{C} - 29.57° = 120°\text{C}$$

The θ_{JA} specification assumes that proper layout and grounding techniques are followed to minimize power dissipation, as outlined in the Layout Guidelines section

MICROPROCESSOR INTERFACING

Microprocessor interfacing to the AD5766/AD5767 is via a serial bus that uses a standard protocol compatible with DSPs and microcontrollers. The communications channel requires a 4-wire serial interface consisting of a clock signal, a data input signal, a data output signal, and a synchronization signal. The device requires a 24-bit data-word with data valid on the falling edge of SCLK.

AD5766/AD5767 TO SPI INTERFACE

The SPI interface of the AD5766/AD5767 is designed to be easily connected to industry-standard DSPs and microcontrollers. Figure 74 shows the AD5766/AD5767 connected to the Analog Devices, Inc., ADSP-BF531 Blackfin® DSP. The Blackfin has an integrated SPI port that can be connected directly to the SPI pins of the AD5766/AD5767.

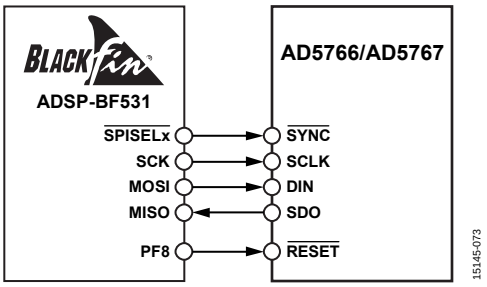

Figure 74. ADSP-BF531 SPI Interface

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LAYOUT GUIDELINES

In any circuit where accuracy is important, careful consideration of the power supply and ground return layout helps to ensure the rated performance. The PCB on which the AD5766/AD5767 are mounted must be designed so that the AD5766/AD5767 lay on the analog plane. Ensure that the board has separate analog and digital sections. If the AD5766/AD5767 are in a system where other devices require an AGND to DGND connection, make the connection at one point only. Keep this ground point as close as possible to the AD5766/AD5767.

The AD5766/AD5767 must have ample supply bypassing of 10 µF in parallel with 0.1 µF on each supply, located as close to the package as possible, ideally right up against the device. The 10 µF capacitors are the tantalum bead type. The 0.1 µF capacitor must have low effective series resistance (ESR) and low effective series inductance (ESI). Ceramic capacitors, for example, provide a low impedance path to ground at high frequencies to handle transient currents due to internal logic switching.

Ensure that the power supply line has as large a trace as possible to provide a low impedance path and reduce glitch effects on the supply line. Shield clocks and other fast switching digital signals from other parts of the board by using a digital ground. Avoid crossover of digital and analog signals if possible. When traces cross on opposite sides of the board, ensure that they run at right angles to each other to reduce feedthrough effects through the board. The best board layout technique is the microstrip technique, where the component side of the board is dedicated to the ground plane only, and the signal traces are placed on the solder side. However, this technique is not always possible with a 2-layer board.

It is often useful to provide some heat sinking capability to allow the power to dissipate easily.

For the WLCSP package, heat is transferred through the solder balls to the PCB board. θ_{JA} thermal impedance is dependent on board construction. More copper layers enable heat to be removed more effectively.

The LFCSP package of the AD5766/AD5767 have an exposed pad beneath the device. Connect this pad to the AV_{SS} supply of the device. For optimum performance, use special consideration when designing the motherboard and mounting the package. For enhanced thermal, electrical, and board level performance, solder the exposed pad on the bottom of the package to the corresponding thermal land pad on the PCB. Design thermal vias into the PCB land pad area to improve heat dissipation further.

The AV_{SS} plane on the device can be increased (as shown in Figure 75) to provide a natural heat sinking effect.

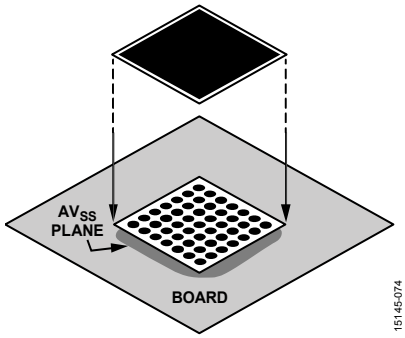

Figure 75. Exposed Pad Connection to Board

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OUTLINE DIMENSIONS

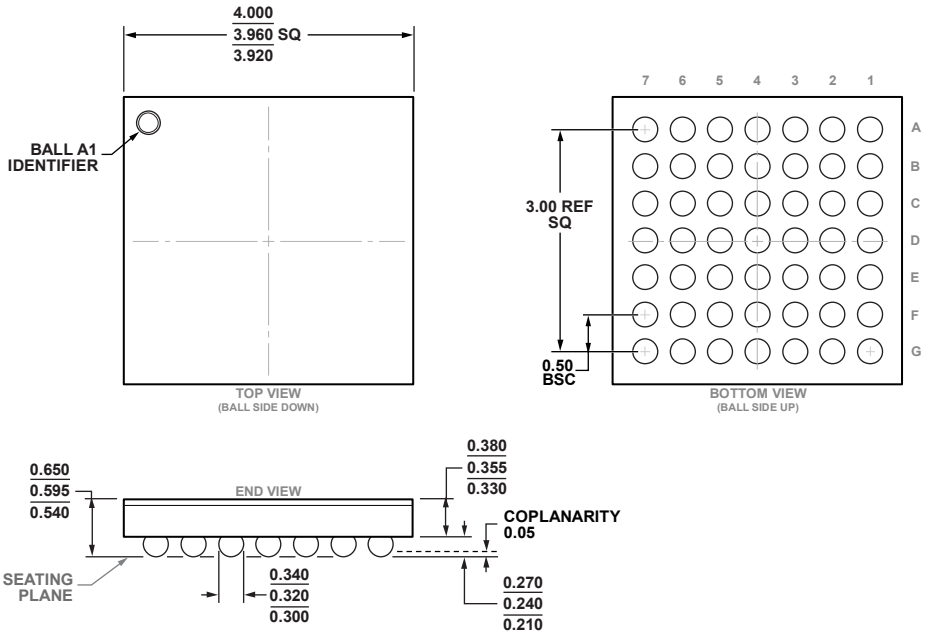
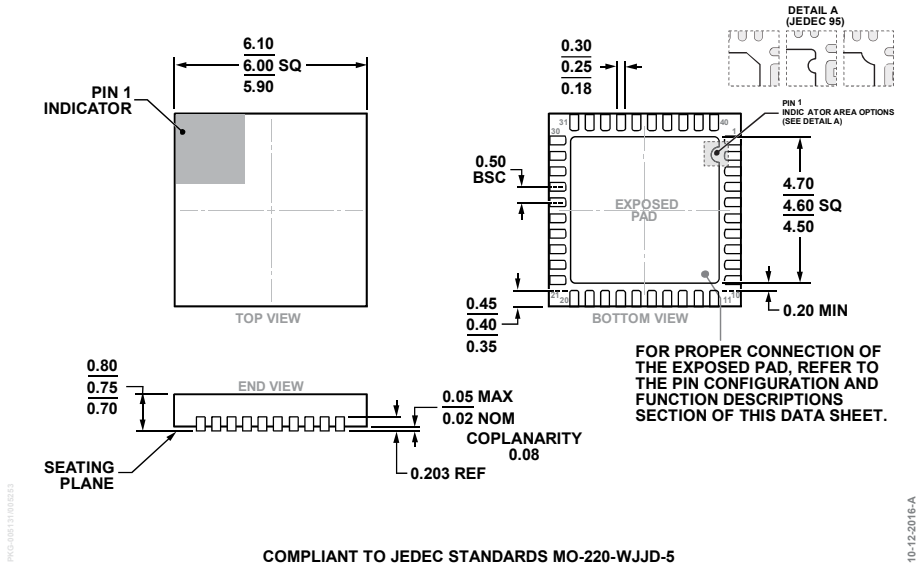


Figure 76. 49-Ball Wafer Level Chip Scale Package [WLCSP]
(CB-49-4)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-220-WJJD-5

Figure 77. 40-Lead Lead Frame Chip Scale Package [LFCSP]
6 mm × 6 mm and 0.75 mm Package Height
(CP-40-7)
Dimensions shown in millimeters

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Model[1, 2]	Resolution (Bits)	Temperature Range	Package Description	Package Option
AD5766BCBZ-RL7	16	−40°C to +105°C	49-Ball Wafer Level Chip Scale Package [WLCSP]	CB-49-4
AD5766BCPZ-RL7	16	−40°C to +105°C	40-Lead Lead Frame Chip Scale Package [LFCSP]	CP-40-7
AD5767BCBZ-RL7	12	−40°C to +105°C	49-Ball Wafer Level Chip Scale Package [WLCSP]	CB-49-4
AD5767BCPZ-RL7	12	−40°C to +105°C	40-Lead Lead Frame Chip Scale Package [LFCSP]	CP-40-7
EVAL-AD5766SD2Z			Evaluation Board	
EVAL-AD5767SD2Z			Evaluation Board	
EVAL-SDP-CB1Z			Controller Board	

[1] Z = RoHS Compliant Part.
[2] To interface with the EVAL-AD5767SD2Z an EVAL-SDP-CB1Z is also required.

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