

Figure 1 Functional Diagram

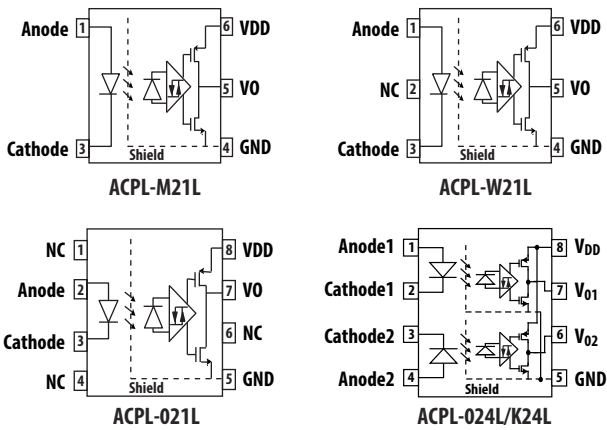


Table 1 Truth Table

| LED | VO |
|-----|------|
| ON | HIGH |
| OFF | LOW |

NOTE A 0.1 μ F bypass capacitor must be connected between pins Vdd and GND.

Ordering Information

ACPL-M21L, ACPL-024L, and ACPL-021L are UL Recognized with 3750 V_{RMS} for 1 minute per UL1577.

ACPL-W21L and ACPL-K24L are UL Recognized with 5000 V_{RMS} for 1 minute per UL1577.

Table 2 Ordering Information

| Part Number | Option | Package | Surface Mount | Tape and Reel | UL1577 5000 V _{RMS} /1 Minute Rating | IEC/EN 60747-5-5 | Quantity |
|-------------|-------------------|---------------|---------------|---------------|---|---------------------|---------------|
| | RoHS Compliant | | | | | | |
| ACPL-M21L | -000E | SO-5 | X | | | | 100 per tube |
| | -060E | | X | | | X | 100 per tube |
| | -500E | | X | X | | | 1500 per reel |
| | -560E | | X | X | | X | 1500 per reel |
| ACPL-024L | -000E | SO-8 | X | | | | 100 per tube |
| | -060E | | X | | | X | 100 per tube |
| | -500E | | X | X | | | 1500 per reel |
| | -560E | | X | X | | X | 1500 per reel |
| ACPL-021L | -000E | SO-8 | X | | | | 100 per tube |
| | -060E | | X | | | X | 100 per tube |
| | -500E | | X | X | | | 1500 per reel |
| | -560E | | X | X | | X | 1500 per reel |
| ACPL-W21L | -000E | Stretched SO6 | X | | X | | 100 per tube |
| | -060E | | X | | X | X | 100 per tube |
| | -500E | | X | X | X | | 1000 per reel |
| | -560E | | X | X | X | X | 1000 per reel |
| ACPL-K24L | -000E | Stretched SO8 | X | | X | | 80 per tube |
| | -060E | | X | | X | X | 80 per tube |
| | -500E | | X | X | X | | 1000 per reel |
| | -560E | | X | X | X | X | 1000 per reel |

To order, choose a part number from the part number column and combine with the desired option from the option column to form an order entry.

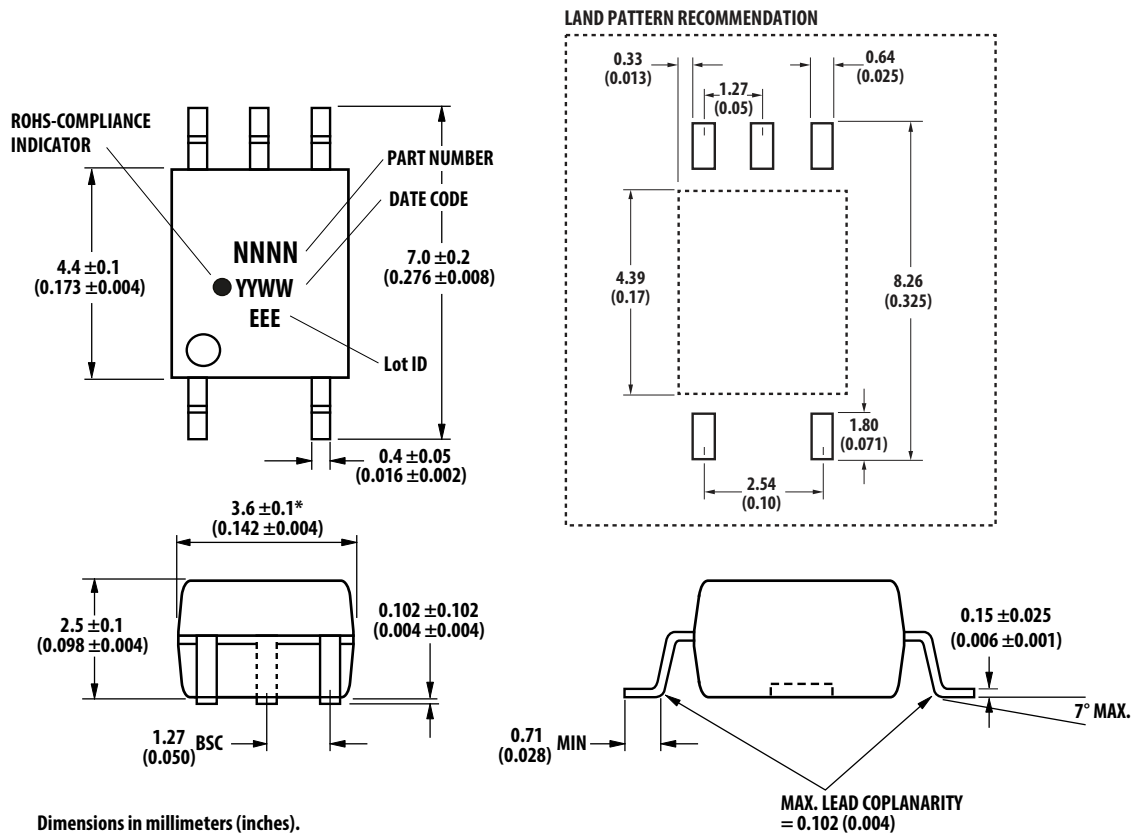
Example 1:

ACPL-M21L-500E to order product of SO-5 package in Tape and Reel packaging with RoHS compliant.

Option data sheets are available. Contact your Broadcom sales representative or authorized distributor for information.

Package Outline Drawings

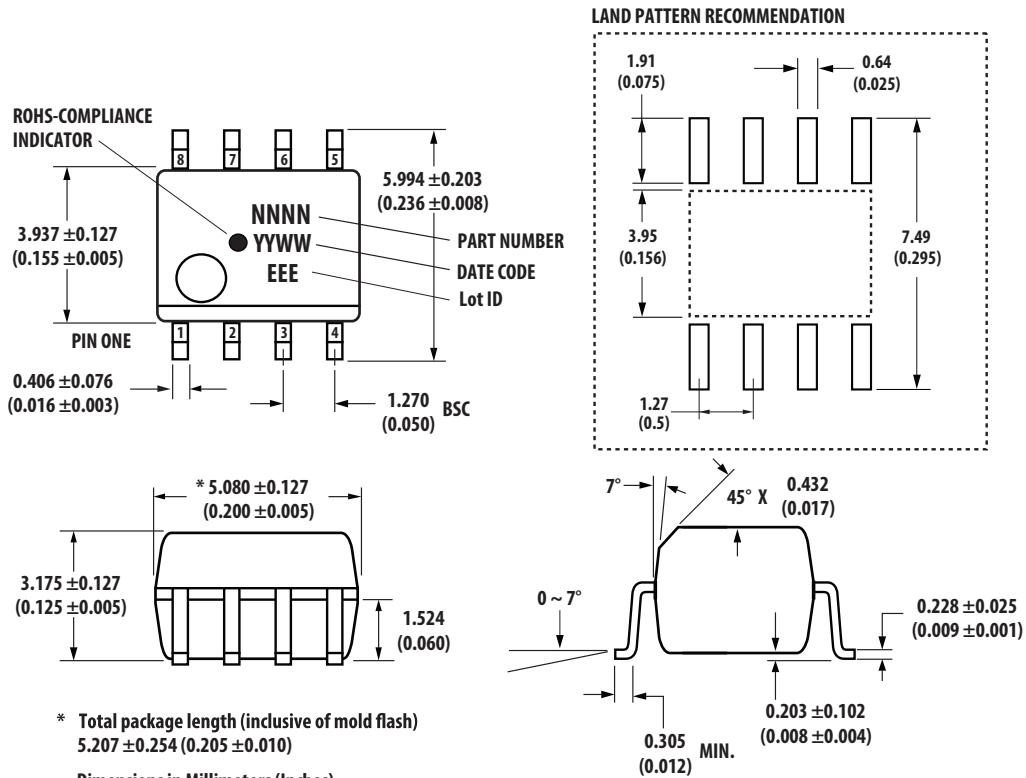
Figure 2 ACPL-M21L SO-5 Package



Dimensions in millimeters (inches).

Note: Floating Lead Protrusion is 0.15 mm (6 mils) max.

* Maximum Mold flash on each side is 0.15 mm (0.006).

Figure 3 ACPL-024L/021L SO-8 Package

* Total package length (inclusive of mold flash)
5.207 ± 0.254 (0.205 ± 0.010)

Dimensions in Millimeters (Inches).

Note: Floating lead protrusion is 0.15 mm (6 mils) max.

Lead coplanarity = 0.10 mm (0.004 inches) max.

Option number 500 not marked.

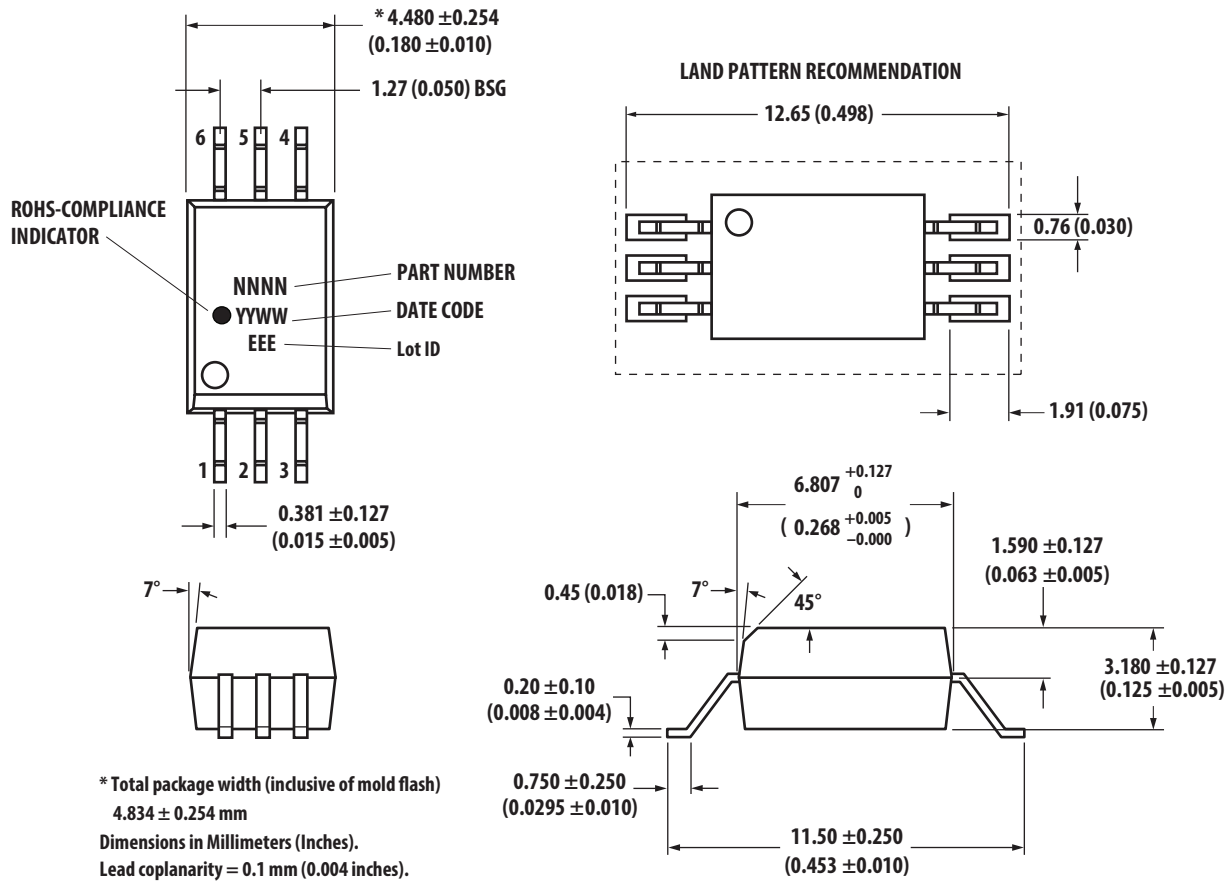
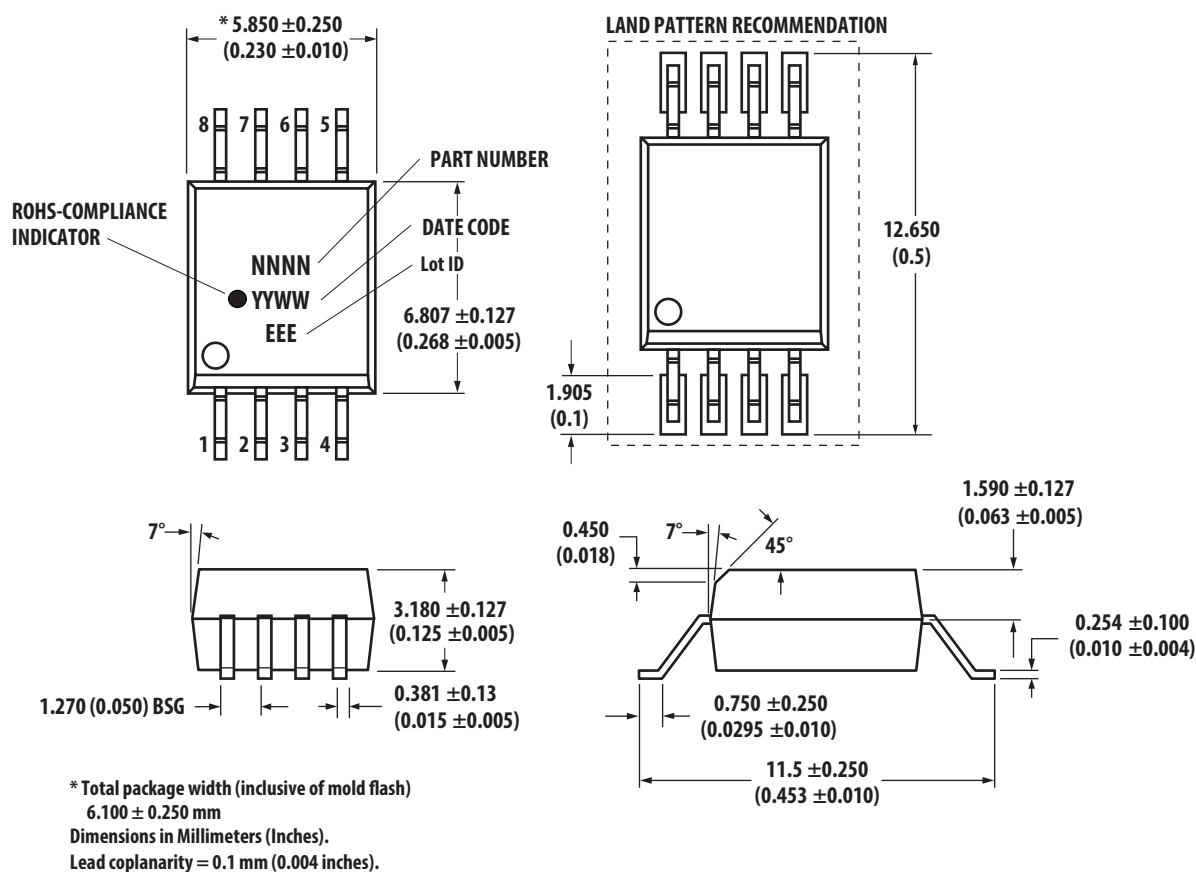
Figure 4 ACPL-W21L Stretched SO-6 Package

Figure 5 ACPL-K24L Stretched SO-8 Package Width

Solder Reflow Profile

Recommended reflow condition as per JEDEC Standard, J-STD-020 (latest revision). Non-halide flux should be used.

Regulatory Information

The ACPL-M21L/024L/021L/W21L/K24L is approved by the following organizations.

| | |
|-------------------------|---|
| UL | Approval under UL 1577, component recognition program up to $V_{ISO} = 3750 V_{RMS}$ for ACPL-M21L/024L/021L and $V_{ISO} = 5000 V_{RMS}$ for ACPL-W21L/K24L. |
| CSA | Approval under CSA Component Acceptance Notice #5. |
| IEC/EN 60747-5-5 | (Option 060 and 560 only). |

Table 3 Insulation and Safety Related Specifications

| Parameter | Symbol | ACPL-M21L | ACPL-024L ACPL-021L | ACPL-W21 ACPL-K24L | Units | Conditions |
|---|--------|-----------|------------------------|-----------------------|-------|--|
| Minimum External Air Gap (Clearance) | L(101) | 5 | 4.9 | 8 | mm | Measured from input terminals to output terminals, shortest distance through air. |
| Minimum External Tracking (Creepage) | L(102) | 5 | 4.8 | 8 | mm | Measured from input terminals to output terminals, shortest distance path along body. |
| Minimum Internal Plastic Gap (Internal Clearance) | | 0.08 | 0.08 | 0.08 | mm | Through insulation distance conductor to conductor, usually the straight line distance thickness between the emitter and detector. |
| Tracking Resistance (Comparative Tracking Index) | CTI | 175 | 175 | 175 | V | DIN IEC 112/VDE 0303 Part 1 |
| Isolation Group | | IIIa | IIIa | IIIa | | Material Group (DIN VDE 0110, 1/89, Table 1) |

Table 4 IEC/EN60747-5-5 Insulation Characteristics^a (Option 060 and 560 Only)

| Description | Symbol | Characteristic | | Units |
|---|--|-----------------------------|--|-------------------------|
| | | ACPL-M21L/ 024L/021L | ACPL-W21L/ K24L | |
| Installation classification per DIN VDE 0110/39, Table 1 for rated mains voltage $\leq 150 V_{rms}$ for rated mains voltage $\leq 300 V_{rms}$ for rated mains voltage $\leq 600 V_{rms}$ for rated mains voltage $\leq 1000 V_{rms}$ | | I – IV I – III I – II | I – IV I – IV I – III I – III | |
| Climatic Classification | | 55/105/21 | 55/105/21 | |
| Pollution Degree (DIN VDE 0110/39) | | 2 | 2 | |
| Maximum Working Insulation Voltage | V_{IORM} | 567 | 1140 | V_{peak} |
| Input to Output Test Voltage, Method b ^a $V_{IORM} \times 1.875 = V_{PR}$, 100% Production Test with $t_m = 1s$, Partial discharge $< 5 pC$ | V_{PR} | 1063 | 2137 | V_{peak} |
| Input to Output Test Voltage, Method a ^a $V_{IORM} \times 1.6 = V_{PR}$, Type and Sample Test, $t_m = 10s$, Partial discharge $< 5 pC$ | V_{PR} | 896 | 1824 | V_{peak} |
| Highest Allowable Overvoltage (Transient Overvoltage $t_{ini} = 60s$) | V_{IOTM} | 6000 | 8000 | V_{peak} |
| Safety-limiting values – maximum values allowed in the event of a failure. Case Temperature Input Current ^b Output Power ^b | T_S $I_{S, INPUT}$ $P_{S, OUTPUT}$ | 150 150 600 | 175 230 600 | $^{\circ}C$ mA mW |
| Insulation Resistance at T_S , $V_{IO} = 500V$ | R_S | $>10^9$ | $>10^9$ | Ω |

a. Refer to the optocoupler section of the Isolation and Control Components Designer's Catalog, under Product Safety Regulations section, (IEC/EN 60747-5-5) for a detailed description of Method a and Method b partial discharge test profiles.

b. Refer to the following figure for dependence of P_S and I_S on ambient temperature.

NOTE These optocouplers are suitable for "safe electrical isolation" only within the safety limit data. Maintenance of the safety limit data shall be ensured by means of protective circuits.

Table 5 Absolute Maximum Ratings

| Parameter | Symbol | Min. | Max. | Units | Condition |
|-----------------------------------|--|------|--|-------|---|
| Storage Temperature | T _S | −55 | 125 | °C | |
| Operating Temperature | T _A | −40 | 105 | °C | |
| Reverse Input Voltage | V _R | — | 5 | V | |
| Supply Voltage | V _{DD} | — | 6.5 | V | |
| Average Forward Input Current | I _F | — | 8 | mA | |
| Peak Forward Input Current | I _{F(TRAN)} | — | 1 | A | ≤1-μs pulse width, <300 pulses per second |
| Output Current | I _O | — | 10 | mA | At max V _{DD} |
| Output Voltage | V _O | −0.5 | V _{DD} +0.5 | V | |
| Lead Solder Temperature | T _{LS} | — | 260°C for 10s., 1.6 mm below seating plane | | |
| Solder Reflow Temperature Profile | See Package Outline Drawings | | | | |

Table 6 Recommended Operating Conditions

| Parameter | Symbol | Min. | Max. | Units |
|---------------------------|--------------|------------------|------|---------------|
| Operating Temperature | T_A | -40 | 105 | °C |
| Input Current, Low Level | I_{FL} | 0 | 250 | μA |
| Input Current, High Level | I_{FH} | 1.6 ^a | 6 | mA |
| Power Supply Voltage | V_{DD} | 2.7 | 5.5 | V |
| Forward Input Voltage | $V_{F(OFF)}$ | — | 0.8 | V |

- a. The initial switching threshold is 1.6 mA or less. It is recommended that 2.2 mA be used to permit at least a 20% LED degradation guardband.

Electrical Specifications (DC)

Over recommended temperature ($T_A = -40^{\circ}\text{C}$ to $+105^{\circ}\text{C}$) and supply voltage ($2.7\text{V} \leq V_{DD} \leq 5.5\text{V}$). All typical specifications are at $V_{DD} = 2.7\text{V}$, $T_A = 25^{\circ}\text{C}$, unless otherwise specified.

Table 7 Electrical Specifications (DC)

| Parameter | Symbol | Channel | Min. | Typ. | Max. | Units | Test Conditions |
|-------------------------------------|---------------------------|---------|----------------|-------|------|------------------------|--|
| Input Forward Voltage | V_F | | — | 1.5 | 2.0 | V | $I_F = 2.2\text{ mA}$ (Figure 6 and Figure 7) |
| Input Reverse Breakdown Voltage | BV_R | | 8 | 11 | — | V | $I_R = 10\text{ }\mu\text{A}$ |
| Logic High Output Voltage | V_{OH} | | $V_{DD} - 0.1$ | — | — | V | $I_F = 2.2\text{ mA}$, $I_O = -20\text{ }\mu\text{A}$ |
| | | | $V_{DD} - 1.0$ | — | — | V | $I_F = 2.2\text{ mA}$, $I_O = -3.2\text{ mA}$ (Figure 8) |
| Logic Low Output Voltage | V_{OL} | | — | 0.001 | 0.1 | V | $I_F = 0\text{ mA}$, $I_O = 20\text{ }\mu\text{A}$ |
| | | | — | 0.15 | 0.4 | V | $I_F = 0\text{ mA}$, $I_O = 3.2\text{ mA}$ (Figure 9) |
| Input Threshold Current | I_{TH} | | — | 0.5 | 1.4 | mA | Figure 10 |
| Logic Low Output Supply Current | I_{DDL} | Single | — | 0.6 | 1.1 | mA | $V_F = 0\text{V}$, $V_{DD} = 5.5\text{V}$, $I_O = \text{Open}$ (Figure 11) |
| | | Dual | — | 1.2 | 2.2 | | |
| Logic High Output Supply Current | I_{DDH} | Single | — | 0.5 | 1.1 | mA | $I_F = 2.2\text{ mA}$, $V_{DD} = 5.5\text{V}$, $I_O = \text{Open}$ (Figure 12) |
| | | Dual | — | 1.0 | 2.2 | | |
| Input Capacitance | C_{IN} | | — | 77 | — | pF | $f = 1\text{ MHz}$, $V_F = 0\text{V}$ |
| Input Diode Temperature Coefficient | $\Delta V_F / \Delta T_A$ | | — | -1.9 | — | mV/ $^{\circ}\text{C}$ | $I_F = 2.2\text{ mA}$ |

Switching Specifications (AC)

Over recommended temperature ($T_A = -40^{\circ}\text{C}$ to $+105^{\circ}\text{C}$), supply voltage ($2.7\text{V} \leq V_{DD} \leq 5.5\text{V}$). All typical specifications are at $V_{DD} = 2.7\text{V}$, $T_A = 25^{\circ}\text{C}$.

Table 8 Switching Specifications (AC)

| Parameter | Symbol | Min. | Typ. | Max. | Units | Test Conditions |
|---|-----------|------|------|------|-------------------|--|
| Propagation Delay Time to Logic Low Output ^a | t_{PHL} | — | 130 | 250 | ns | $I_F = 2.2\text{ mA}$, $C_L = 15\text{ pF}$ (Figure 13, Figure 17), CMOS Signal Levels |
| Propagation Delay Time to Logic High Output ^a | t_{PLH} | — | 115 | 250 | ns | $I_F = 2.2\text{ mA}$, $C_L = 15\text{ pF}$ (Figure 14, Figure 17), CMOS Signal Levels |
| Pulse Width Distortion ^b | PWD | — | — | 200 | ns | CMOS Signal Levels |
| Propagation Delay Skew ^c | t_{PSK} | — | — | 220 | ns | |
| Output Rise Time (10% to 90%) | t_R | — | 11 | — | ns | $I_F = 2.2\text{ mA}$, $C_L = 15\text{ pF}$, CMOS Signal Levels. |
| Output Fall Time (90% to 10%) | t_F | — | 11 | — | ns | $I_F = 2.2\text{ mA}$, $C_L = 15\text{ pF}$, CMOS Signal Levels. |
| Static Common Mode Transient Immunity at Logic High Output ^d | $ CM_H $ | 25 | 40 | — | kV/ μs | $V_{CM} = 1000\text{V}$, $T_A = 25^{\circ}\text{C}$, $I_F = 2.2\text{ mA}$, $C_L = 15\text{ pF}$, $V_I = 5\text{V}$, ($R_T = 1.6\text{ k}\Omega$) or $V_I = 3.3\text{V}$, ($R_T = 840\text{ }\Omega$), CMOS Signal Levels, Figure 18 |
| Static Common Mode Transient Immunity at Logic Low Output ^e | $ CM_L $ | 25 | 40 | — | kV/ μs | $V_{CM} = 1000\text{V}$, $T_A = 25^{\circ}\text{C}$, $I_F = 0\text{ mA}$, $C_L = 15\text{ pF}$, $V_I = 0\text{V}$, ($R_T = 1.6\text{ k}\Omega$) or ($R_T = 840\text{ }\Omega$), CMOS Signal Levels, Figure 18 |

- t_{PHL} propagation delay is measured from the 50% (V_{in} or I_F) on the falling edge of the input pulse to the 50% V_{DD} of the falling edge of the V_O signal. t_{PLH} propagation delay is measured from the 50% (V_{in} or I_F) on the rising edge of the input pulse to the 50% level of the rising edge of the V_O signal.
- PWD is defined as $|t_{PHL} - t_{PLH}|$.
- t_{PSK} is equal to the magnitude of the worst case difference in t_{PHL} and/or t_{PLH} that will be seen between units at any given temperature within the recommended operating conditions.
- CM_H is the maximum tolerable rate of rise of the common mode voltage to assure that the output will remain in a high logic state.
- CM_L is the maximum tolerable rate of rise of the common mode voltage to assure that the output will remain in a low logic state.

NOTE Use of a 0.1 μF bypass capacitor connected between V_{DD} and ground is recommended.

Package Characteristics

All typical at $T_A = 25^{\circ}\text{C}$.

Table 9 Package Characteristics

| Parameter | Symbol | Part Number | Min. | Typ. | Max. | Units | Test Conditions |
|--------------------------|-----------|---------------------|------|-----------|------|-----------|--|
| Input-Output Insulation | V_{ISO} | ACPL-M21L/024L/021L | 3750 | — | — | V_{rms} | $RH < 50\%$ for 1 min., $T_A = 25^{\circ}\text{C}$ |
| | | ACPL-W21L/K24L | 5000 | — | — | | |
| Input-Output Resistance | R_{I-O} | | — | 10^{12} | — | Ω | $V_{I-O} = 500\text{V}$ |
| Input-Output Capacitance | C_{I-O} | | — | 0.6 | — | pF | $f = 1\text{ MHz}$, $T_A = 25^{\circ}\text{C}$ |

Figure 6 Forward Voltage vs. Temperature

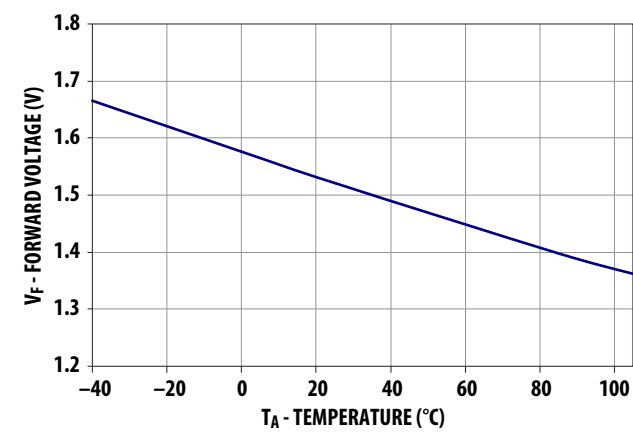


Figure 7 Forward Current vs. Forward Voltage

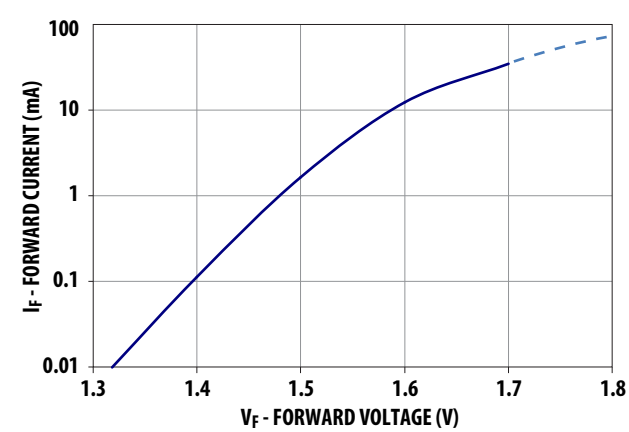


Figure 8 Logic High Output Voltage vs. Supply Voltage

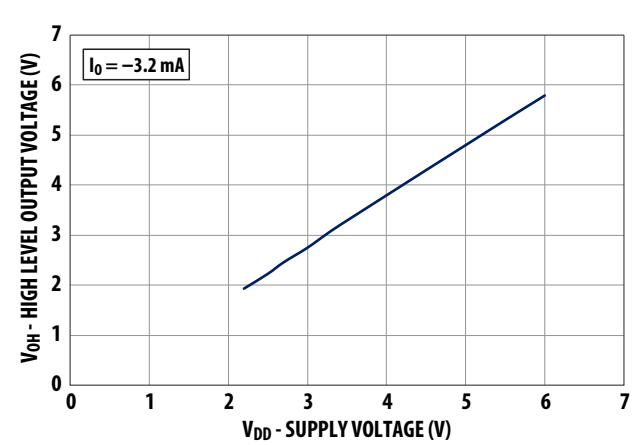


Figure 9 Logic Low Output Voltage vs. Temperature

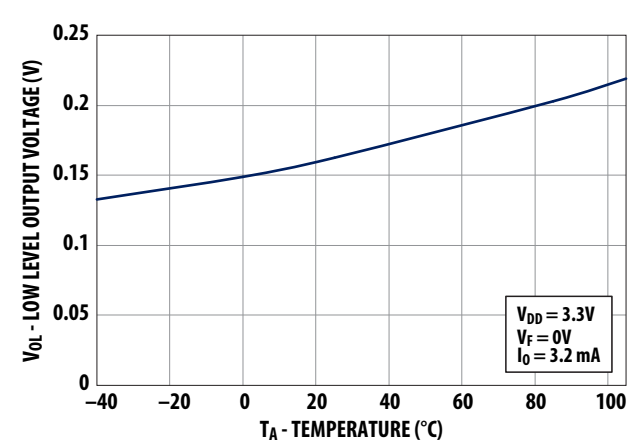


Figure 10 Input Threshold Current vs. Temperature

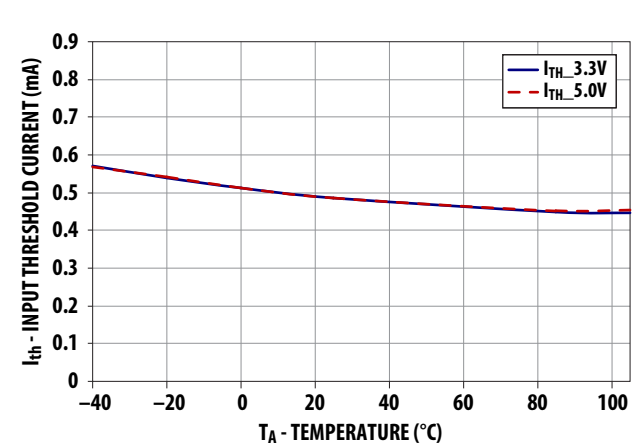


Figure 11 Logic Low Output Supply Current vs. Temperature

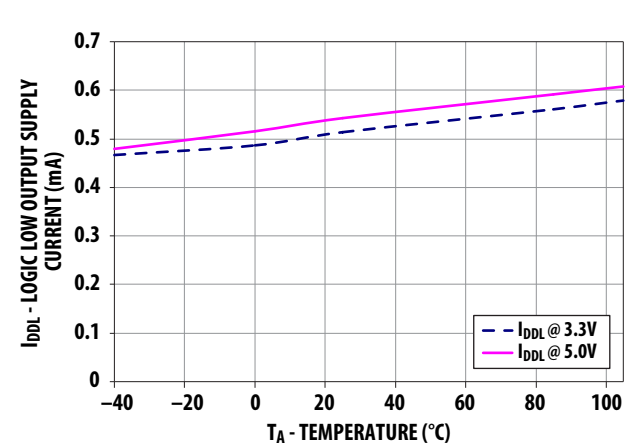


Figure 12 Logic High Output Supply Current vs. Temperature

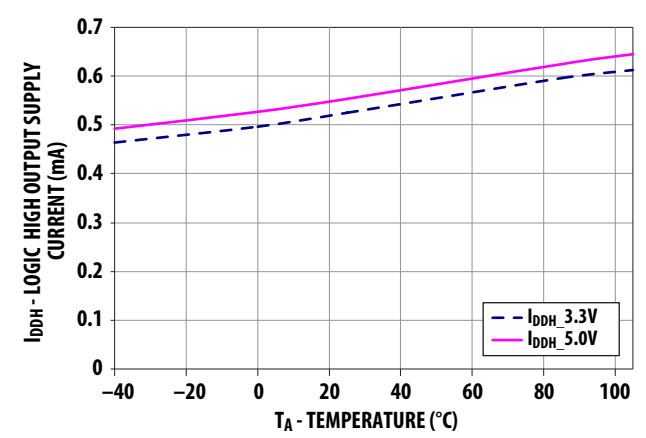


Figure 13 Propagation Delay, t_{pHL} vs. Temperature

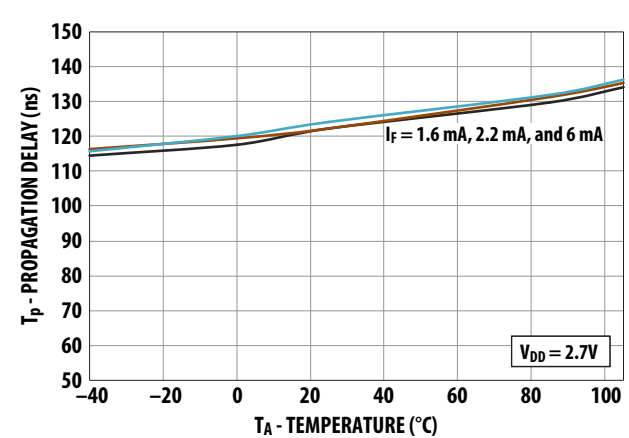


Figure 14 Propagation Delay, t_{pLH} vs. Temperature

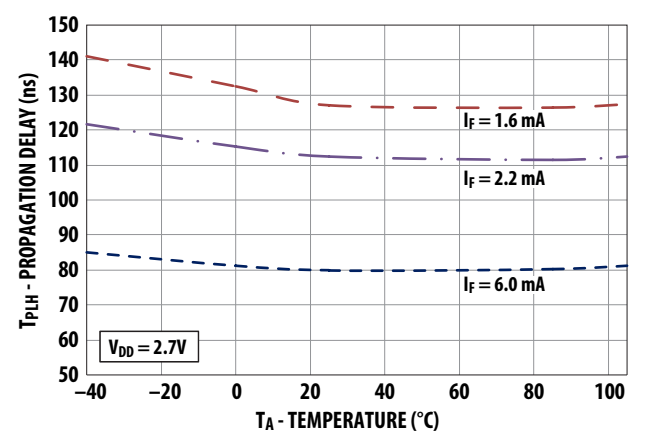


Figure 15 Output Voltage vs. Input Current @ V_{DD} = 3.3V

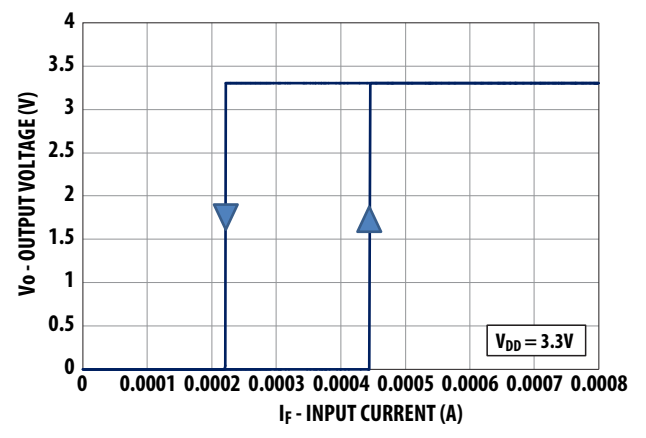


Figure 16 Output Voltage vs. Input Current @ V_{DD} = 5V

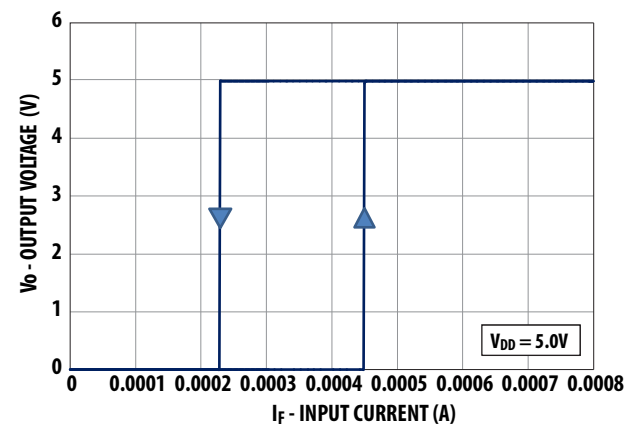
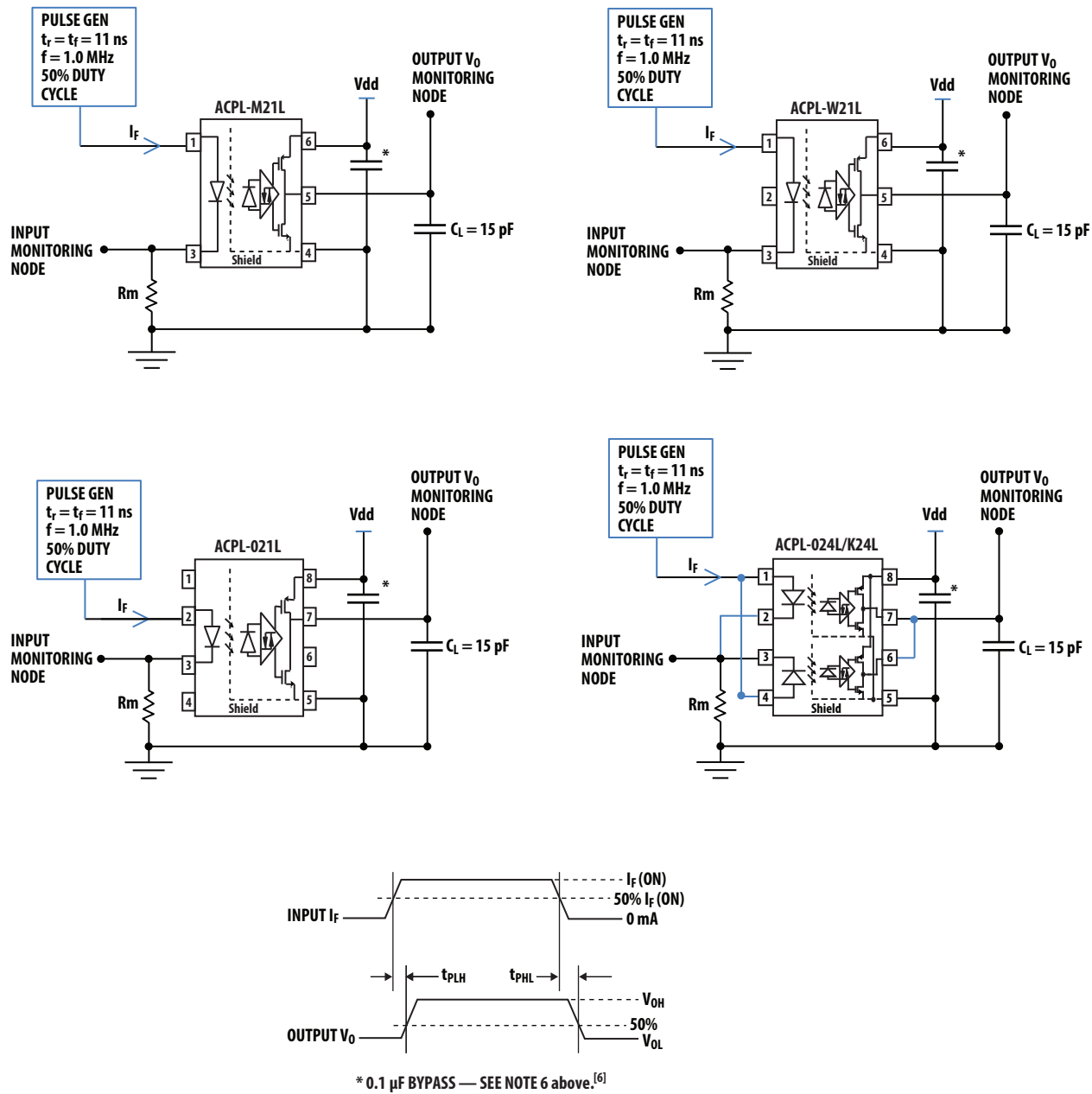


Figure 17 Circuit for t_{PLH} , t_{PHL} , t_r , t_f 

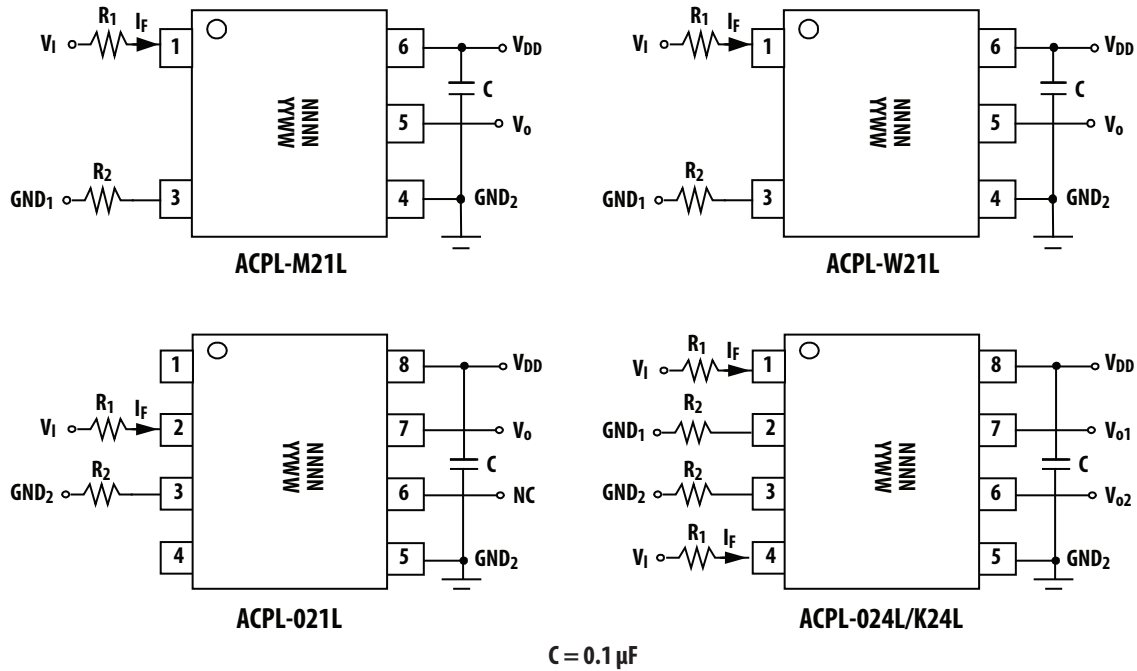
ACPL-M21L, ACPL-021L, ACPL-024L, ACPL-W21L, ACPL-K24L:

$$V_I = 3.3V: R_1 = 510\Omega \pm 1\%, R_2 = 330\Omega \pm 1\%$$

$$V_I = 5.0V: R_1 = 1\text{ k}\Omega \pm 1\%, R_2 = 600\Omega \pm 1\%$$

$$R_T = R_1 + R_2 \approx R_1 / R_2 \approx 1.5$$

Figure 18 Recommended Printed Circuit Board Layout and Input Current Limiting Resistor Selection



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