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# 1 Block diagram and pin configurations

Figure 1. Block diagram

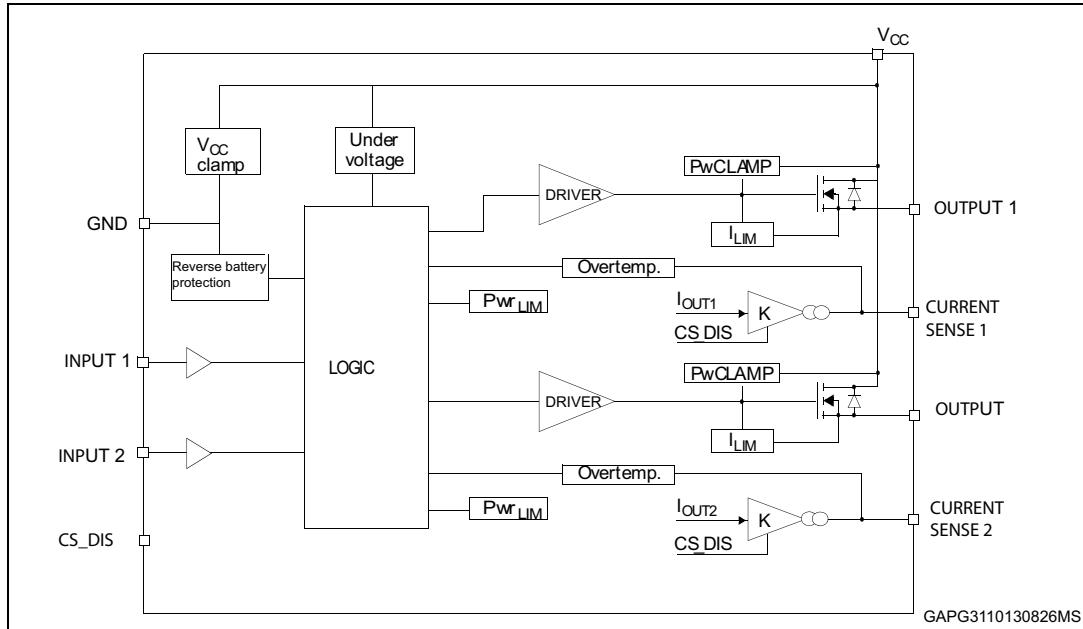


Table 2. Pin functions

| Name             | Function  |
|------------------|---|
| VCC              | Battery connection  |
| OUTPUT1,2        | Power output  |
| GND              | Ground connection   |
| INPUT1,2         | Voltage controlled input pin with hysteresis, CMOS compatible. Controls output switch state |
| CURRENT SENSE1,2 | Analog current sense pin, delivers a current proportional to the load current               |
| CS_DIS           | Active high CMOS compatible pin, to disable the current sense pins                          |

Figure 2. Configuration diagram (not to scale)

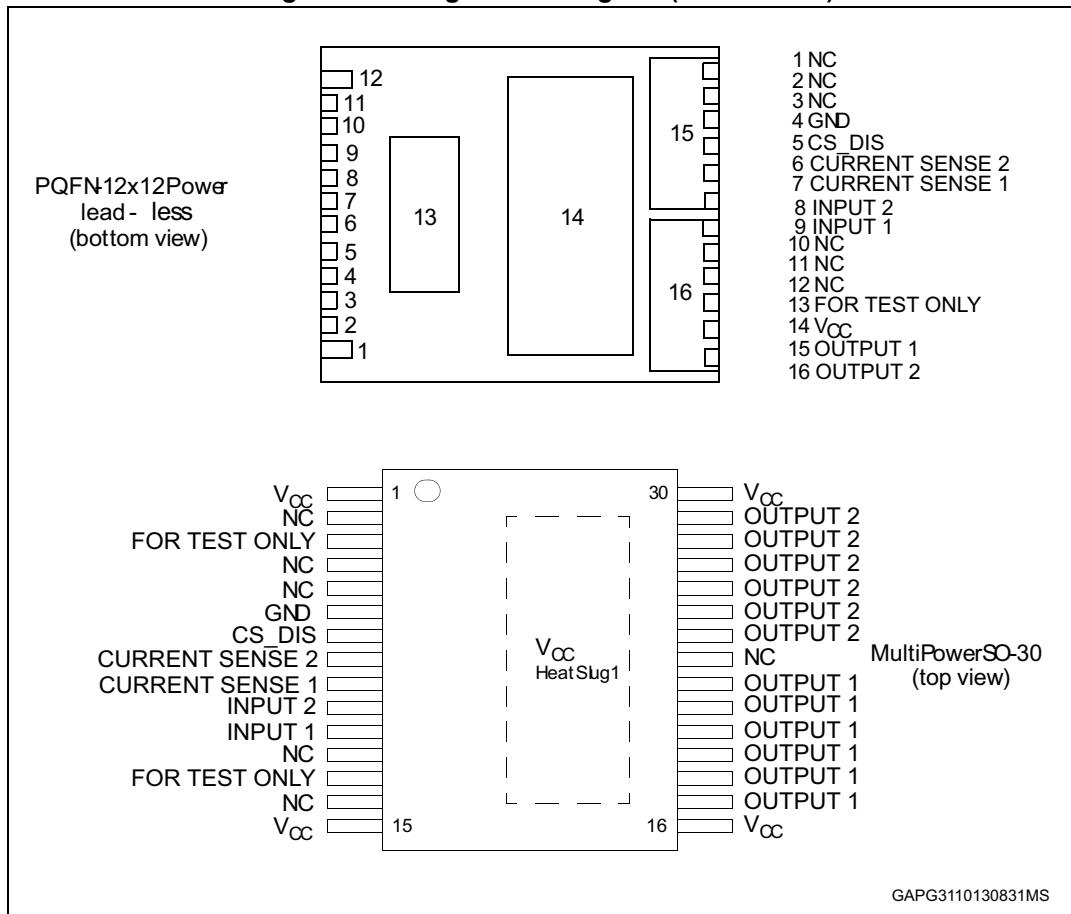


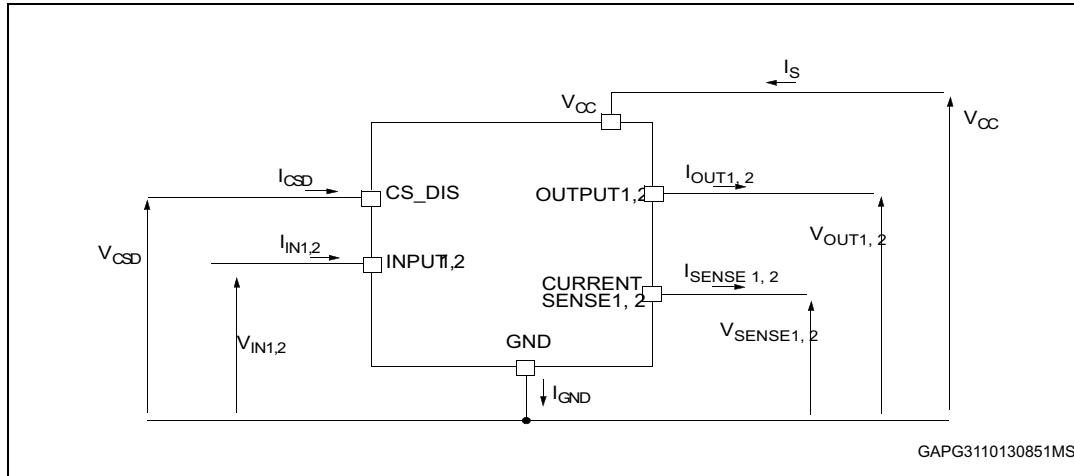
Table 3. Suggested connections for unused and n.c. pins

| Connection / Pin | Current Sense        | N.C. | Output | Input                 | CS_DIS                | For test only |
|------------------|----------------------|------|--------|-----------------------|-----------------------|---------------|
| Floating         | N.R. <sup>(1)</sup>  | X    | X      | X                     | X                     | X             |
| To ground        | Through 1kΩ resistor | X    | N.R.   | Through 10kΩ resistor | Through 10kΩ resistor | N.R.          |

1. Not recommended.

## 2 Electrical specifications

Figure 3. Current and voltage conventions



### 2.1 Absolute maximum ratings

Stressing the device above the ratings listed in the “Absolute maximum ratings” tables may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to the conditions in this section for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 4. Absolute maximum ratings

| Symbol       | Parameter  | Value                    | Unit   |
|--------------|--|--------------------------|--------|
| $V_{CC}$     | DC supply voltage  | 27                       | V      |
| $V_{CCPK}$   | Transient supply voltage ( $T < 400\text{ms}$ , $R_{load} > 0.5\Omega$ )   | 41                       | V      |
| $-V_{CC}$    | Reverse DC supply voltage  | 16                       | V      |
| $I_{OUT}$    | DC output current  | Internally limited       | A      |
| $-I_{OUT}$   | Reverse DC output current  | 70                       | A      |
| $I_{IN}$     | DC input current   | -1 to 10                 | mA     |
| $I_{CS}$     | DC current sense disable input current   | -1 to 10                 | mA     |
| $V_{CSENSE}$ | Current sense maximum voltage ( $V_{cc} > 0\text{V}$ )   | $V_{cc}-41$<br>$+V_{cc}$ | V<br>V |
| $E_{MAX}$    | Maximum switching energy (single pulse)<br>( $L=0.3\text{mH}$ ; $R_L=0\Omega$ ; $V_{bat}=13.5\text{V}$ ; $T_{jstart}=150^\circ\text{C}$ ; $I_{OUT} = I_{limL}(Typ.)$ ) | 342                      | mJ     |
| $V_{ESD}$    | Electrostatic discharge (Human Body Model: $R=1.5\text{k}\Omega$ ;<br>$C=100\text{pF}$ )   | 2000                     | V      |
| $V_{ESD}$    | Charge device model (CDM-AEC-Q100-011)   | 750                      | V      |

**Table 4. Absolute maximum ratings (continued)**

| Symbol           | Parameter                      | Value      | Unit |
|------------------|--------------------------------|------------|------|
| T <sub>j</sub>   | Junction operating temperature | -40 to 150 | °C   |
| T <sub>STG</sub> | Storage temperature            | -55 to 150 | °C   |

## 2.2 Thermal data

**Table 5. Thermal data**

| Symbol                | Parameter   | Value             |                   | Unit |
|-----------------------|---|-------------------|-------------------|------|
|                       |   | MultiPowerSO-30   | 12x12 PLLP        |      |
| R <sub>thj-case</sub> | Thermal resistance junction-case (MAX)<br>(with one channel ON) | 0.35              | 0.35              | °C/W |
| R <sub>thj-amb</sub>  | Thermal resistance junction-ambient (MAX)                       | 58 <sup>(1)</sup> | 39 <sup>(2)</sup> | °C/W |

1. PCB FR4 area 58mmX58mm, PCB thickness 2mm, Cu thickness 35 µm, minimum pad layout.

2. PCB FR4 area 78mmX78mm, PCB thickness 2mm, Cu thickness 35 µm, minimum pad layout.

## 2.3 Electrical characteristics

Values specified in this section are for  $8 \text{ V} < V_{CC} < 24 \text{ V}$ ,  $-40^\circ\text{C} < T_j < 150^\circ\text{C}$ , unless otherwise stated.

**Table 6. Power section**

| Symbol        | Parameter                               | Test conditions  | Min.   | Typ.                    | Max.                  | Unit   |
|---------------|---|--|--------|-------------------------|-----------------------|--|
| $V_{CC}$      | Operating supply voltage                |  | 4.5    | 13                      | 27                    | V  |
| $V_{USD}$     | Undervoltage shutdown                   |  |        | 3.5                     | 4.5                   | V  |
| $V_{USDhyst}$ | Undervoltage shut-down hysteresis       |  |        | 0.5                     |                       | V  |
| $R_{ON}$      | On-state resistance <sup>(1)</sup>      | $I_{OUT}=15\text{A}; T_j=25^\circ\text{C}$<br>$I_{OUT}=15\text{A}; T_j=150^\circ\text{C}$<br>$I_{OUT}=15\text{A}; V_{CC}=5\text{V}; T_j=25^\circ\text{C}$                    |        |                         | 4<br>8<br>6           | $\text{m}\Omega$<br>$\text{m}\Omega$<br>$\text{m}\Omega$ |
| $R_{ON\ REV}$ | $R_{dson}$ in reverse battery condition | $V_{CC}=-13\text{V}; I_{OUT}=-15\text{A}; T_j=25^\circ\text{C}$  |        |                         | 4                     | $\text{m}\Omega$   |
| $V_{clamp}$   | $V_{CC}$ clamp voltage                  | $I_{CC}=20\text{ mA}; I_{OUT1,2}=0\text{A}$  | 41     | 46                      | 52                    | V  |
| $I_S$         | Supply current                          | Off state; $V_{CC}=13\text{V}; T_j=25^\circ\text{C}$ ;<br>$V_{IN}=V_{OUT}=V_{SENSE}=V_{CSD}=0\text{V}$<br>On state; $V_{CC}=13\text{V}; V_{IN}=5\text{V}; I_{OUT}=0\text{A}$ |        | 2 <sup>(2)</sup><br>3.5 | 5 <sup>(2)</sup><br>6 | $\mu\text{A}$<br>mA                                      |
| $I_{L(off)}$  | Off-state output current <sup>(1)</sup> | $V_{IN}=V_{OUT}=0\text{V}; V_{CC}=13\text{V}; T_j=25^\circ\text{C}$<br>$V_{IN}=V_{OUT}=0\text{V}; V_{CC}=13\text{V}; T_j=125^\circ\text{C}$                                  | 0<br>0 | 0.01                    | 3<br>5                | $\mu\text{A}$  |

1. For each channel.
2. PowerMOS leakage included.

**Table 7. Switching ( $V_{CC} = 13\text{V}; T_j = 25^\circ\text{C}$ )**

| Symbol                | Parameter                                 | Test conditions                                   | Min. | Typ.                           | Max. | Unit                   |
|-----------------------|---|---|------|--------------------------------|------|------------------------|
| $t_{d(on)}$           | Turn-on delay time                        | $R_L=0.87\Omega$ (see <a href="#">Figure 5.</a> ) |      | 25                             |      | $\mu\text{s}$          |
| $t_{d(off)}$          | Turn-on delay time                        | $R_L=0.87\Omega$ (see <a href="#">Figure 5.</a> ) |      | 35                             |      | $\mu\text{s}$          |
| $(dV_{OUT}/dt)_{on}$  | Turn-on voltage slope                     | $R_L=0.87\Omega$                                  |      | See <a href="#">Figure 16.</a> |      | $\text{V}/\mu\text{s}$ |
| $(dV_{OUT}/dt)_{off}$ | Turn-off voltage slope                    | $R_L=0.87\Omega$                                  |      | See <a href="#">Figure 18.</a> |      | $\text{V}/\mu\text{s}$ |
| $W_{ON}$              | Switching energy losses during $t_{won}$  | $R_L=0.87\Omega$ (see <a href="#">Figure 5.</a> ) |      | 5.4                            |      | mJ                     |
| $W_{OFF}$             | Switching energy losses during $t_{woff}$ | $R_L=0.87\Omega$ (see <a href="#">Figure 5.</a> ) |      | 2.3                            |      | mJ                     |

**Table 8. Logic input**

| Symbol           | Parameter                 | Test conditions                 | Min. | Typ. | Max. | Unit    |
|------------------|---------------------------|---------------------------------|------|------|------|---------|
| $V_{IL1,2}$      | Input low level voltage   |                                 |      |      | 0.9  | V       |
| $I_{IL1,2}$      | Low level input current   | $V_{IN}=0.9V$                   | 1    |      |      | $\mu A$ |
| $V_{IH1,2}$      | Input high level voltage  |                                 | 2.1  |      |      | V       |
| $I_{IH1,2}$      | High level input current  | $V_{IN}=2.1V$                   |      |      | 10   | $\mu A$ |
| $V_{I(hyst)1,2}$ | Input hysteresis voltage  |                                 | 0.25 |      |      | V       |
| $V_{ICL1,2}$     | Input clamp voltage       | $I_{IN}=1mA$<br>$I_{IN}=-1mA$   | 5.5  | -0.7 | 7    | V<br>V  |
| $V_{CSDL}$       | CS_DIS low level voltage  |                                 |      |      | 0.9  | V       |
| $I_{CSDL}$       | Low level CS_DIS current  | $V_{CSD}=0.9V$                  | 1    |      |      | $\mu A$ |
| $V_{CSDH}$       | CS_DIS high level voltage |                                 | 2.1  |      |      | V       |
| $I_{CSDH}$       | High level CS_DIS current | $V_{CSD}=2.1V$                  |      |      | 10   | $\mu A$ |
| $V_{CSD(hyst)}$  | CS_DIS hysteresis voltage |                                 | 0.25 |      |      | V       |
| $V_{CSCL}$       | CS_DIS clamp voltage      | $I_{CSD}=1mA$<br>$I_{CSD}=-1mA$ | 5.5  | -0.7 | 7    | V<br>V  |

**Table 9. Protection and diagnostics<sup>(1)</sup>**

| Symbol      | Parameter                                    | Test conditions                      | Min.        | Typ.        | Max.        | Unit |
|-------------|--|--------------------------------------|-------------|-------------|-------------|------|
| $I_{limH}$  | Short circuit current                        | $V_{CC}=13V$<br>$5V < V_{CC} < 24V$  | 70          | 100         | 140         | A    |
| $I_{limL}$  | Short circuit current during thermal cycling | $V_{CC}=13V$ ; $T_R < T_j < T_{TSD}$ |             | 40          |             | A    |
| $T_{TSD}$   | Shutdown temperature                         |                                      | 150         | 175         | 200         | °C   |
| $T_R$       | Reset temperature                            |                                      | $T_{RS}+1$  | $T_{RS}+5$  |             | °C   |
| $T_{RS}$    | Thermal reset of STATUS                      |                                      | 135         |             |             | °C   |
| $T_{HYST}$  | Thermal hysteresis ( $T_{TSD}-T_R$ )         |                                      |             | 7           |             | °C   |
| $V_{DEMAG}$ | Turn-off output voltage clamp                | $I_{OUT}=2A$ ; $V_{IN}=0$ ; $L=6mH$  | $V_{CC}-27$ | $V_{CC}-30$ | $V_{CC}-33$ | V    |

- To ensure long term reliability under heavy overload or short-circuit conditions, protection and related diagnostic signals must be used together with a proper software strategy. If the device is subjected to abnormal conditions, this software must limit the duration and number of activation cycles.

Table 10. Current sense (8 V&lt;VCC&lt;16 V)

| Symbol         | Parameter  | Test conditions   | Min.   | Typ.  | Max.     | Unit               |
|----------------|--|---|--------|-------|----------|--------------------|
| $K_1$          | $I_{OUT}/I_{SENSE}$                                      | $I_{OUT}=15A; V_{SENSE}=4V; V_{CSD}=0V;$<br>$T_j=-40^{\circ}C$<br>$T_j=25^{\circ}C...150^{\circ}C$  | 11530  | 16000 | 19340    |                    |
|                |  |   | 12730  | 16000 | 19270    |                    |
| $K_2$          | $I_{OUT}/I_{SENSE}$                                      | $I_{OUT}=30A; V_{SENSE}=4V; V_{CSD}=0V;$<br>$T_j=-40^{\circ}C$<br>$T_j=25^{\circ}C...150^{\circ}C$  | 13430  | 16150 | 17880    |                    |
|                |  |   | 14500  | 16150 | 17880    |                    |
| $I_{SENSE0}$   | Analog sense current                                     | $I_{OUT}=0A; V_{SENSE}=0V;$<br>$V_{CSD}=5V; V_{IN}=0V; T_j=-40^{\circ}C \text{ to } 150^{\circ}C$<br>$V_{CSD}=0V; V_{IN}=5V; T_j=-40^{\circ}C \text{ to } 150^{\circ}C$ | 0<br>0 |       | 5<br>400 | $\mu A$<br>$\mu A$ |
| $V_{SENSE}$    | Max analog sense output voltage                          | $I_{OUT}=45A; V_{CSD}=0V; R_{SENSE}=3.9k\Omega$   | 5      |       |          | V                  |
| $V_{SENSEH}$   | Analog sense output voltage in overtemperature condition | $V_{CC}=13V; R_{SENSE}=3.9k\Omega$  |        | 9     |          | V                  |
| $I_{SENSEH}$   | Analog sense output current in overtemperature condition | $V_{CC}=13V; V_{SENSE}=5V$  |        | 8     |          | mA                 |
| $t_{DSENSE1H}$ | Delay response time from falling edge of CS_DIS pin      | $V_{SENSE}<4V, 5A < I_{out} < 30A$<br>$I_{SENSE}=90\% \text{ of } I_{SENSE \text{ max}}$<br>(see Figure 4.)   |        | 50    | 100      | $\mu s$            |
| $t_{DSENSE1L}$ | Delay response time from rising edge of CS_DIS pin       | $V_{SENSE}<4V, 5A < I_{out} < 30A$<br>$I_{SENSE}=10\% \text{ of } I_{SENSE \text{ max}}$<br>(see Figure 4.)   |        | 5     | 20       | $\mu s$            |
| $t_{DSENSE2H}$ | Delay response time from rising edge of INPUT pin        | $V_{SENSE}<4V, 5A < I_{out} < 30A$<br>$I_{SENSE}=90\% \text{ of } I_{SENSE \text{ max}}$<br>(see Figure 4.)   |        | 270   | 600      | $\mu s$            |
| $t_{DSENSE2L}$ | Delay response time from falling edge of INPUT pin       | $V_{SENSE}<4V, 5A < I_{out} < 30A$<br>$I_{SENSE}=10\% \text{ of } I_{SENSE \text{ max}}$<br>(see Figure 4.)   |        | 100   | 250      | $\mu s$            |

Figure 4. Current sense delay characteristics

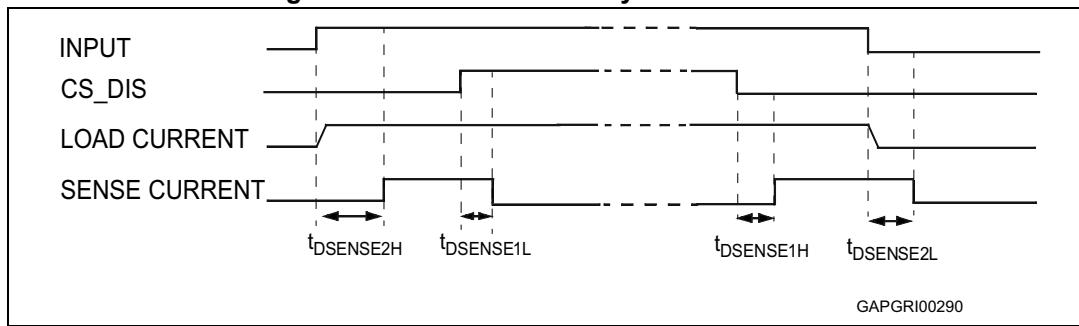
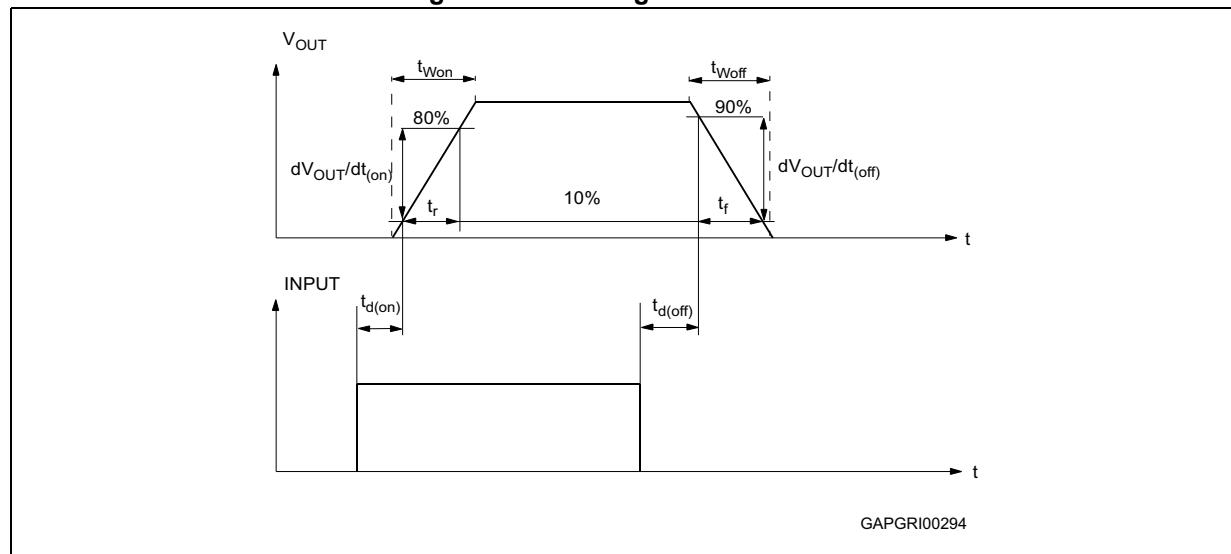


Table 11. Truth table

| Conditions   | INPUTn | OUTPUTn | SENSEn ( $V_{CSD}=0V$ ) <sup>(1)</sup><br>(see Figure 3.) |
|--|--------|---------|---|
| Normal operation   | L      | L       | 0   |
|  | H      | H       | Nominal   |
| Overtemperature  | L      | L       | 0   |
|  | H      | L       | $V_{SENSEH}$  |
| Undervoltage   | L      | L       | 0   |
|  | H      | L       | 0   |
| Short circuit to GND<br>( $R_{sc} \leq 10 \text{ m}\Omega$ ) | L      | L       | 0   |
|  | H      | L       | 0 if $T_j < T_{TSD}$                                      |
|  | H      | L       | $V_{SENSEH}$ if $T_j > T_{TSD}$                           |
| Short circuit to $V_{CC}$                                    | L      | H       | 0   |
|  | H      | H       | < Nominal   |
| Negative output voltage clamp                                | L      | L       | 0   |

1. If  $V_{CSD}$  is high, the SENSE output is at a high impedance. Its potential depends on leakage currents and the external circuit.

Figure 5. Switching characteristics



**Table 12. Electrical transient requirements (part 1)**

| ISO 7637-2:<br>2004(E)<br>Test pulse | Test levels <sup>(1)</sup> |        | Number of<br>pulses or<br>test times | Burst cycle/pulse<br>repetition time |        | Delays and<br>Impedance |
|--------------------------------------|----------------------------|--------|--------------------------------------|--------------------------------------|--------|-------------------------|
|                                      | III                        | IV     |                                      | 0.5 s                                | 5 s    |                         |
| 1                                    | -75 V                      | -100 V | 5000<br>pulses                       | 0.5 s                                | 5 s    | 2 ms, 10 Ω              |
| 2a                                   | +37 V                      | +50 V  | 5000<br>pulses                       | 0.2 s                                | 5 s    | 50 μs, 2 Ω              |
| 3a                                   | -100 V                     | -150 V | 1h                                   | 90 ms                                | 100 ms | 0.1 μs, 50 Ω            |
| 3b                                   | +75 V                      | +100 V | 1h                                   | 90 ms                                | 100 ms | 0.1 μs, 50 Ω            |
| 4                                    | -6 V                       | -7 V   | 1 pulse                              |                                      |        | 100 ms, 0.01 Ω          |
| 5b <sup>(2)</sup>                    | +65 V                      | +87 V  | 1 pulse                              |                                      |        | 400 ms, 2 Ω             |

1. The above test levels must be considered referred to  $V_{CC} = 13.5V$  except for pulse 5b.
2. Valid in case of external load dump clamp: 40V maximum referred to ground. The protection strategy allows PowerMOS to be cyclically switched on during load dump, so distributing the load dump energy along the time and to transfer a part of it to the load.

**Table 13. Electrical transient requirements (part 2)**

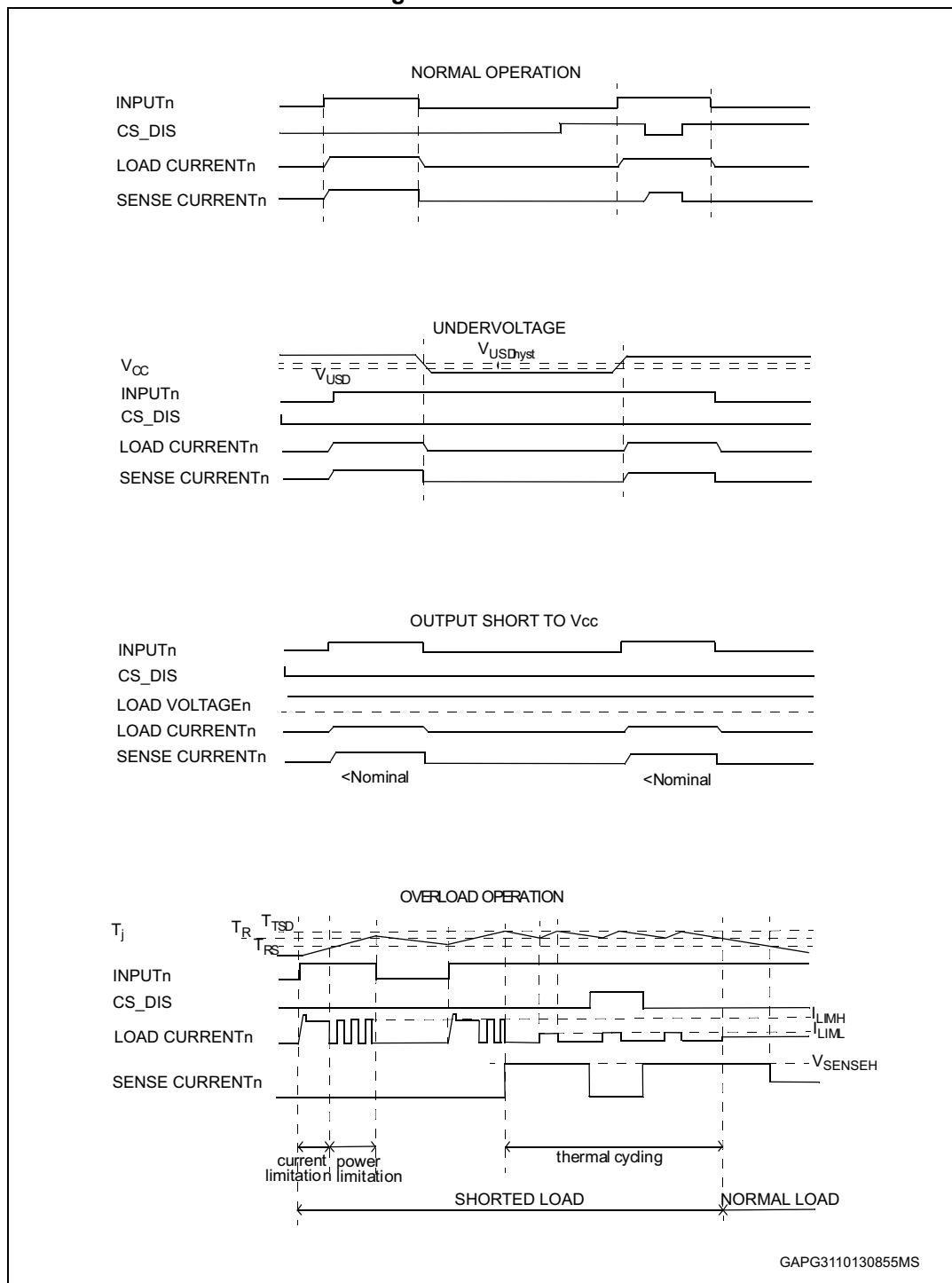
| ISO 7637-2:<br>2004(E)<br>Test pulse | Test level results <sup>(1)</sup> |    |
|--------------------------------------|-----------------------------------|----|
|                                      | III                               | IV |
| 1                                    | C                                 | C  |
| 2a                                   | C                                 | C  |
| 3a                                   | C                                 | C  |
| 3b                                   | C                                 | C  |
| 4                                    | C                                 | C  |
| 5b <sup>(2) (3)</sup>                | C                                 | C  |

1. The above test levels must be considered referred to  $V_{CC} = 13.5V$  except for pulse 5b
2. Valid in case of external load dump clamp: 40V maximum referred to ground. The protection strategy allows PowerMOS to be cyclically switched on during load dump, so distributing the load dump energy along the time and to transfer a part of it to the load.
3. Suppressed load dump (pulse 5b) is withstood with a minimum load connected as specified in [Table 4.: Absolute maximum ratings](#).

**Table 14. Electrical transient requirements (part 3)**

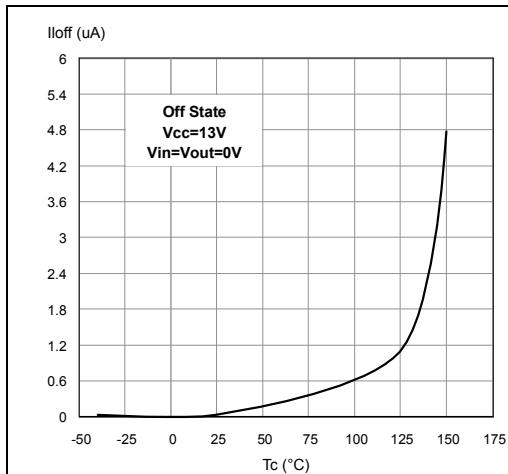
| Class | Contents   |
|-------|--|
| C     | All functions of the device are performed as designed after exposure to disturbance.   |
| E     | One or more functions of the device are not performed as designed after exposure to disturbance and cannot be returned to proper operation without replacing the device. |

Figure 6. Waveforms

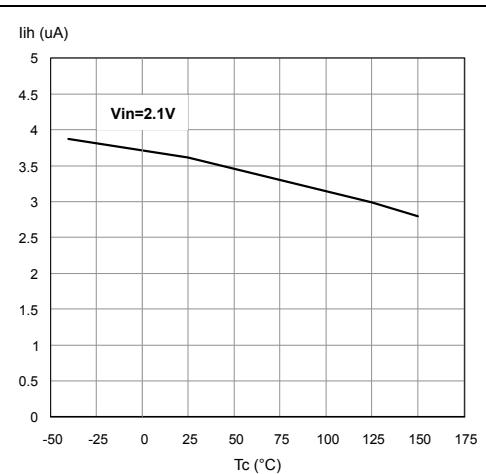


## 2.4 Electrical characteristics curves

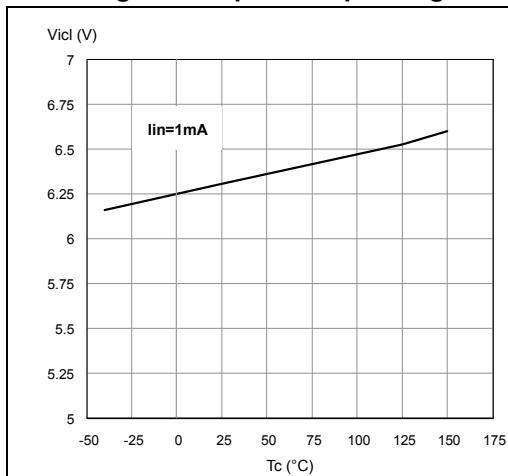
**Figure 7. Off state output current**



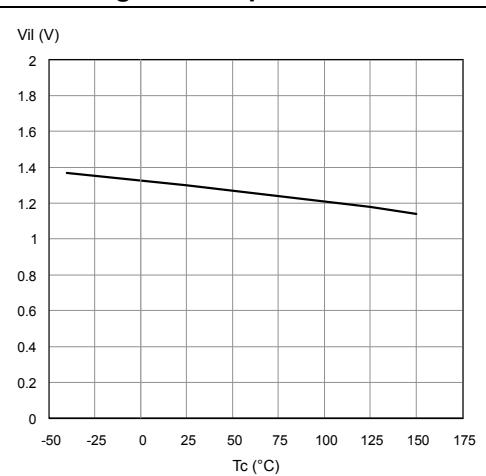
**Figure 8. High level input current**



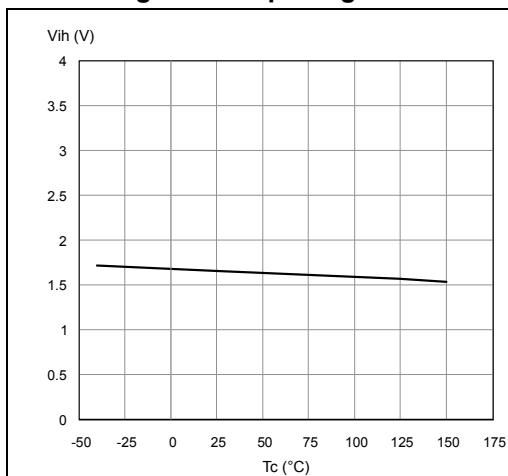
**Figure 9. Input clamp voltage**



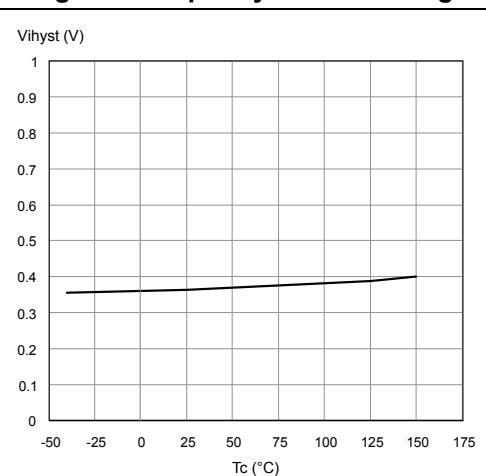
**Figure 10. Input low level**

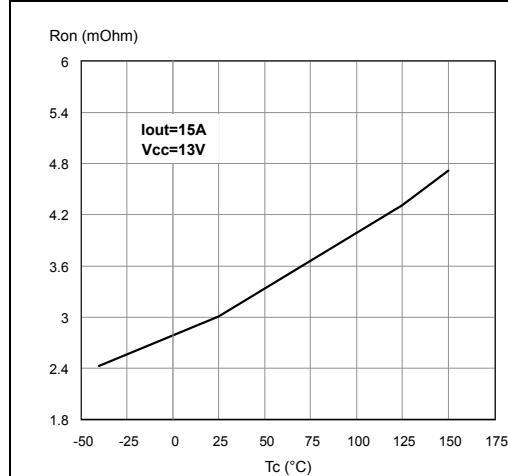
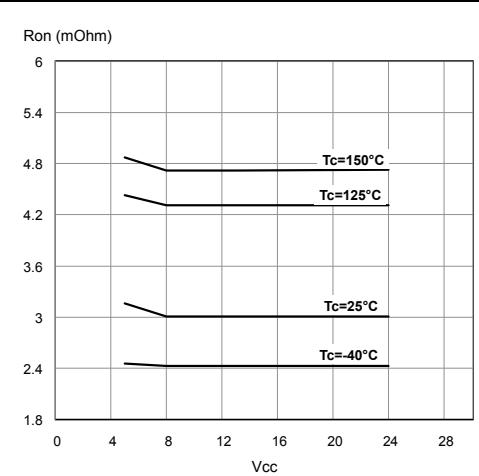
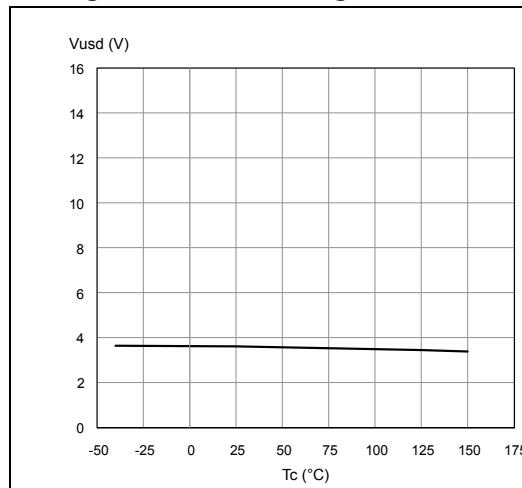
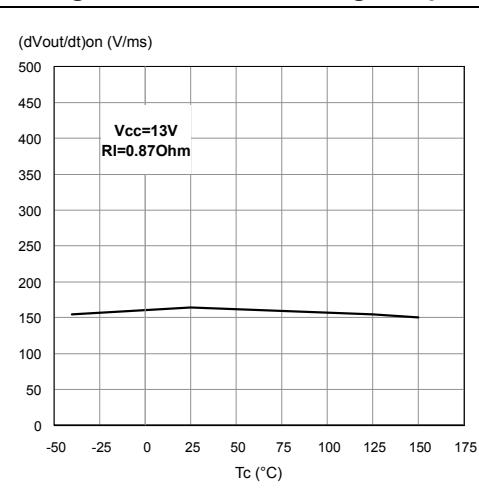
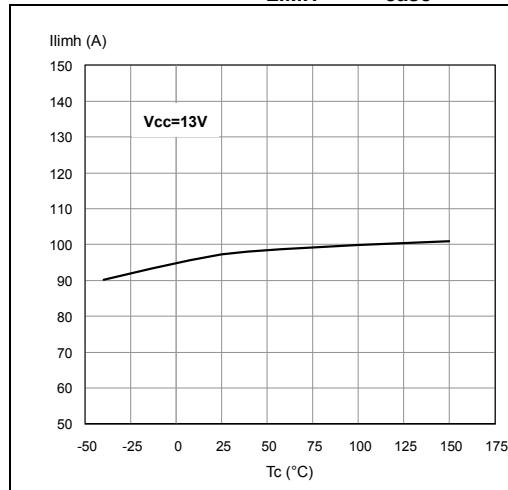
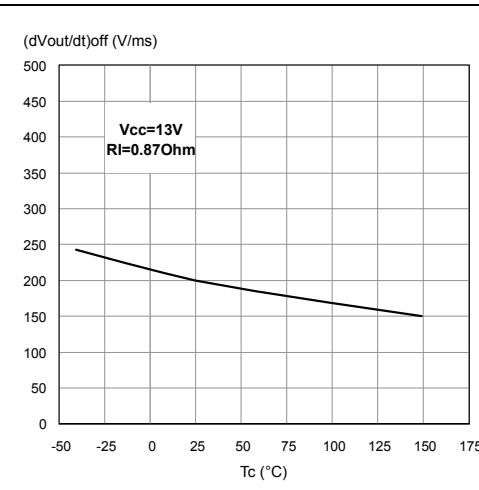


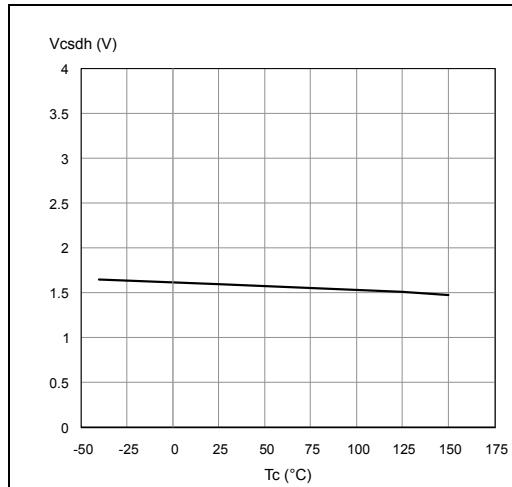
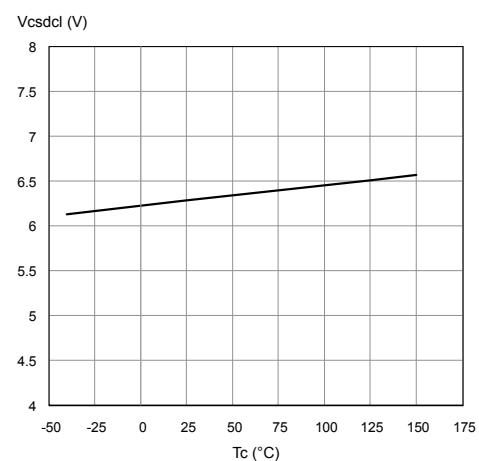
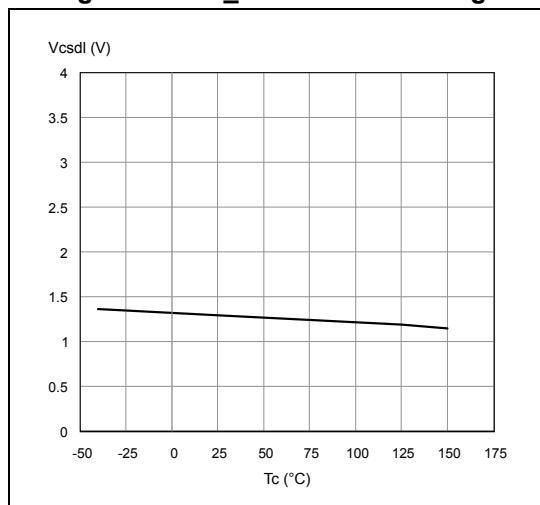
**Figure 11. Input high level**



**Figure 12. Input hysteresis voltage**

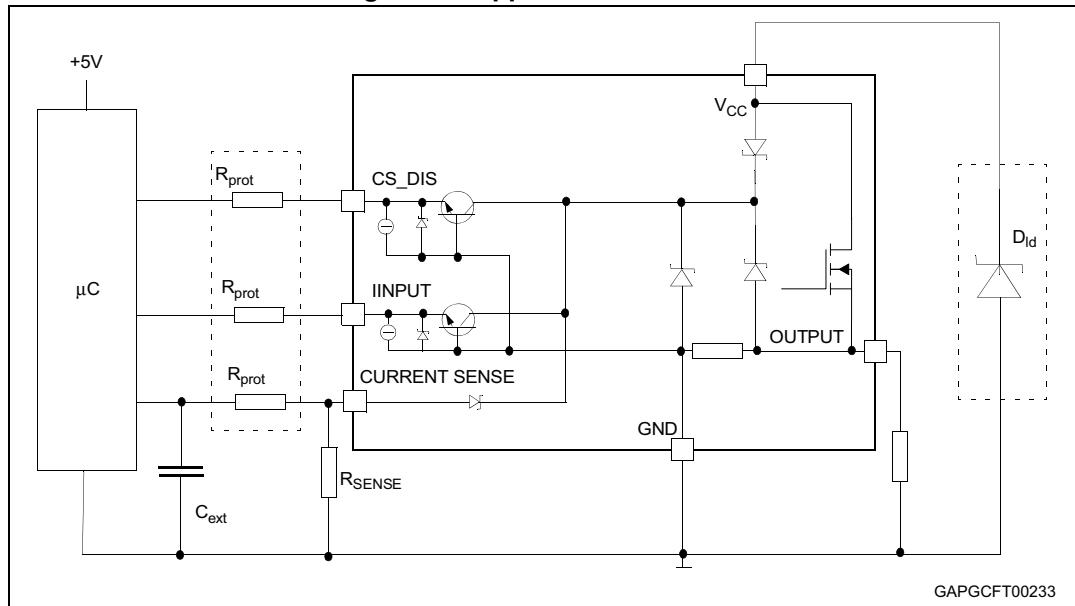


**Figure 13. On state resistance vs.  $T_{case}$** **Figure 14. On state resistance vs.  $V_{cc}$** **Figure 15. Undervoltage shutdown****Figure 16. Turn-On voltage slope****Figure 17.  $I_{LIMH}$  vs.  $T_{case}$** **Figure 18. Turn-Off voltage slope**

**Figure 19. CS\_DIS high level voltage****Figure 20. CS\_DIS clamp voltage****Figure 21. CS\_DIS low level voltage**

### 3 Application information

Figure 22. Application schematic



#### 3.1 MCU I/Os protection

When negative transients are present on the  $V_{CC}$  line, the control pins will be pulled negative to approximately -1.5 V.

ST suggests the insertion of resistors ( $R_{prot}$ ) in the lines to prevent the  $\mu$ C I/Os pins from latching up.

The values of these resistors provide a compromise between the leakage current of the  $\mu$ C, the current required by the HSD I/Os (input levels compatibility) and the latch-up limit of the  $\mu$ C I/Os.

$$-V_{CCpeak}/I_{latchup} \leq R_{prot} \leq (V_{OH\mu C} - V_{IH}) / I_{IHmax}$$

Calculation example:

For  $V_{CCpeak} = -1.5V$  and  $I_{latchup} \geq 20mA$ ;  $V_{OH\mu C} \geq 4.5V$

$$75\Omega \leq R_{prot} \leq 240k\Omega$$

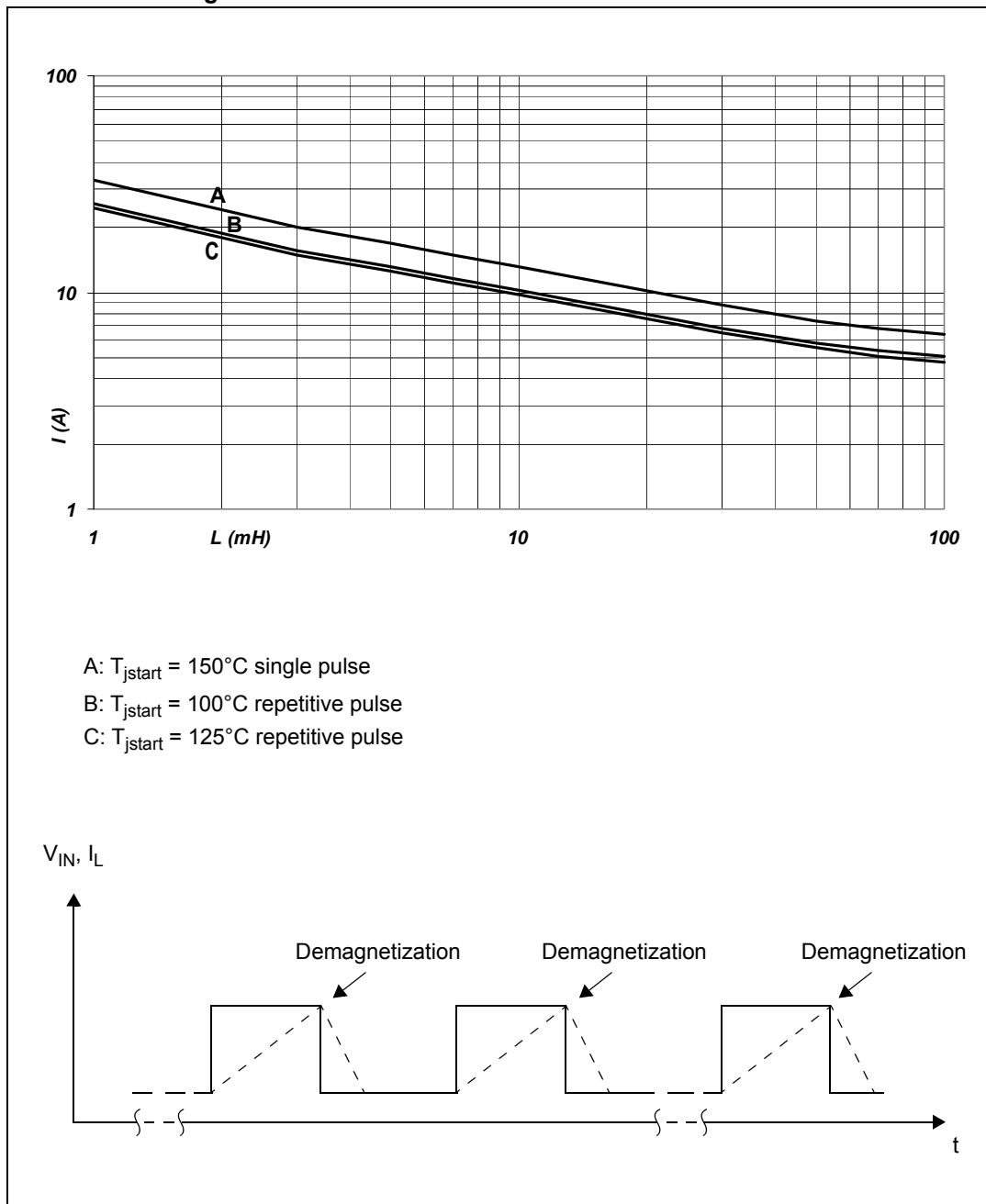
Recommended values:  $R_{prot} = 10k\Omega$ ,  $C_{EXT} = 10nF$

#### 3.2 Load dump protection

$D_{Id}$  is necessary (Voltage Transient Suppressor) if the load dump peak voltage exceeds the  $V_{CCPK}$  max rating. The same applies if the device is subject to transients on the  $V_{CC}$  line that are greater than the ones shown in [Table 12](#).

### 3.3 Maximum demagnetization energy ( $V_{CC} = 13.5$ V)

Figure 23. Maximum turn off current versus inductance



Note:

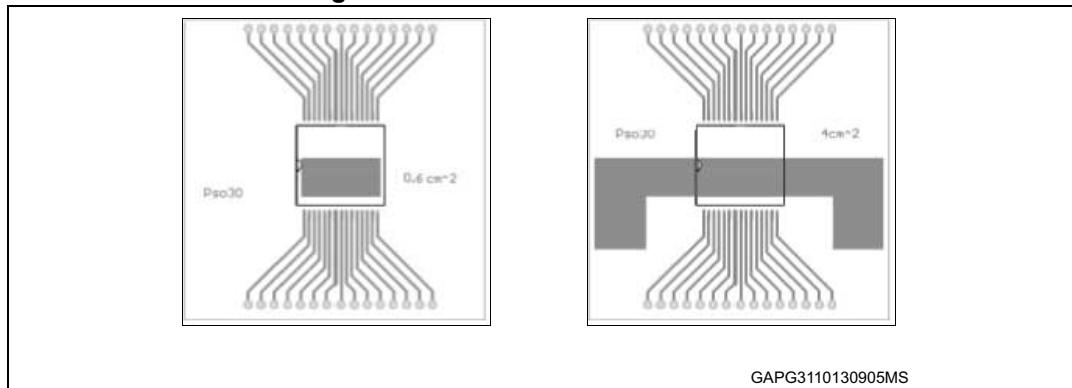
Values are generated with  $R_L = 0 \Omega$ .

In case of repetitive pulses,  $T_{jstart}$  (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves A and B.

## 4 Package and PC board thermal data

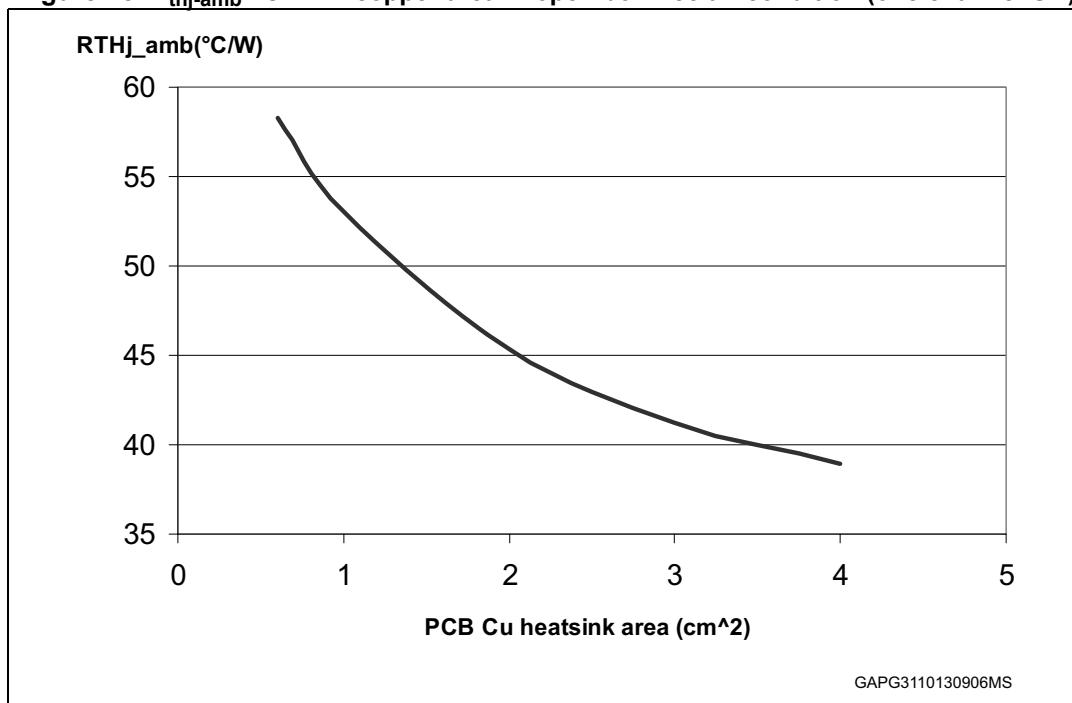
### 4.1 MultiPowerSO-30 thermal data

Figure 24. MultiPowerSO-30 PC board

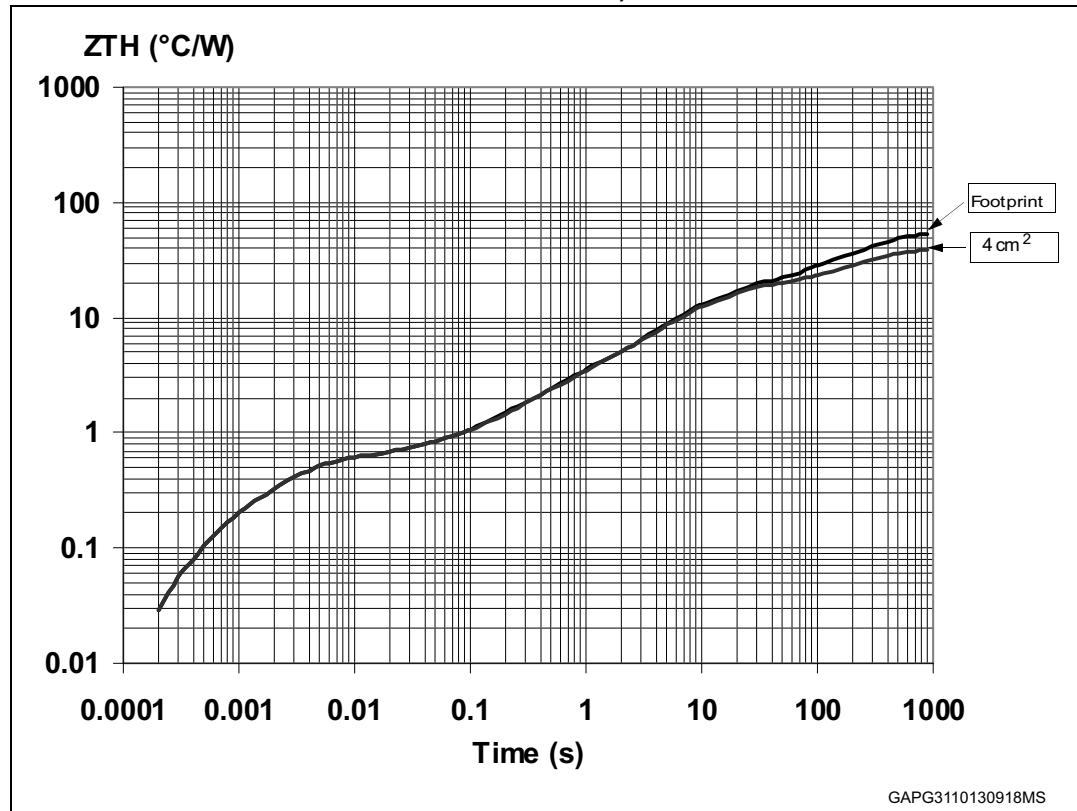


Note: Layout condition of  $R_{th}$  and  $Z_{th}$  measurements (PCB: Double layer, Thermal Vias, FR4 area= 58 mm x 58 mm, PCB thickness=2 mm, Cu thickness=35  $\mu$ m (front and back side), Copper areas: from minimum pad layout to 16  $\text{cm}^2$ ).

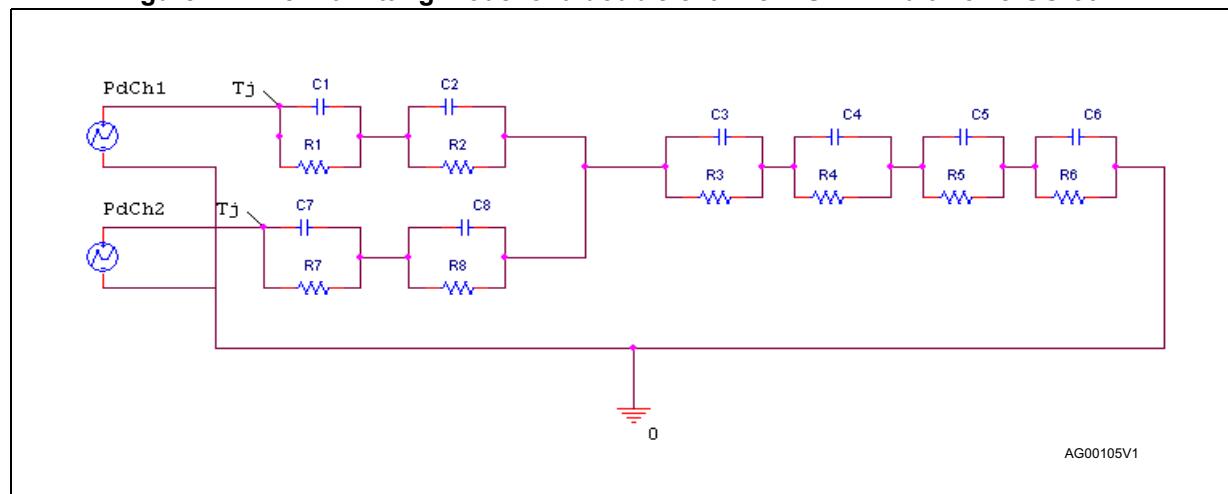
Figure 25.  $R_{thj\text{-amb}}$  Vs. PCB copper area in open box free air condition (one channel ON)



**Figure 26. MultiPowerSO-30 thermal impedance junction ambient single pulse (one channel ON)**



**Figure 27. Thermal fitting model of a double channel HSD in MultiPowerSO-30<sup>(a)</sup>**



- a. The fitting model is a simplified thermal tool and is valid for transient evolutions where the embedded protections (power limitation or thermal cycling during thermal shutdown) are not triggered.

**Equation 1: pulse calculation formula**

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

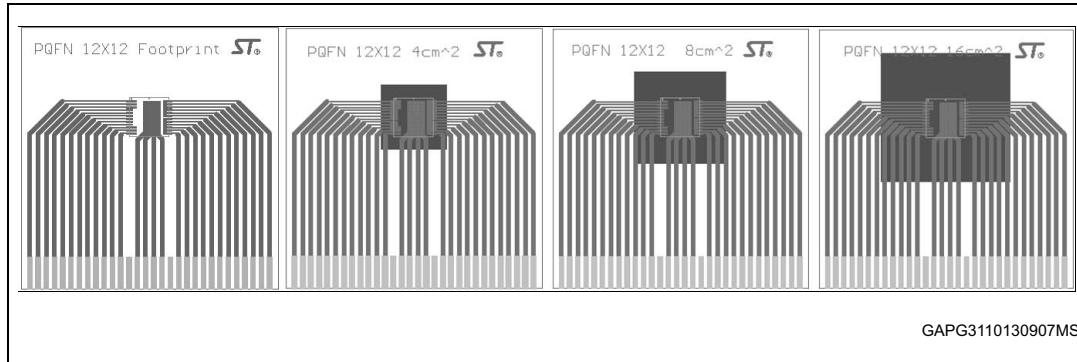
where  $\delta = t_p/T$

**Table 15. Thermal parameters for MultiPowerSO-30**

| Area/island (cm <sup>2</sup> ) | Footprint | 4    |
|--------------------------------|-----------|------|
| R1 (°C/W)                      | 0.05      |      |
| R2 (°C/W)                      | 0.3       |      |
| R3 (°C/W)                      | 0.5       |      |
| R4 (°C/W)                      | 1.3       |      |
| R5 (°C/W)                      | 14        |      |
| R6 (°C/W)                      | 44.7      | 23.7 |
| R7 (°C/W)                      | 0.05      |      |
| R8 (°C/W)                      | 0.3       |      |
| C1 (W.s/°C)                    | 0.005     |      |
| C2 (W.s/°C)                    | 0.008     |      |
| C3 (W.s/°C)                    | 0.01      |      |
| C4 (W.s/°C)                    | 0.3       |      |
| C5 (W.s/°C)                    | 0.6       |      |
| C6 (W.s/°C)                    | 5         | 11   |
| C7 (W.s/°C)                    | 0.005     |      |
| C8 (W.s/°C)                    | 0.008     |      |

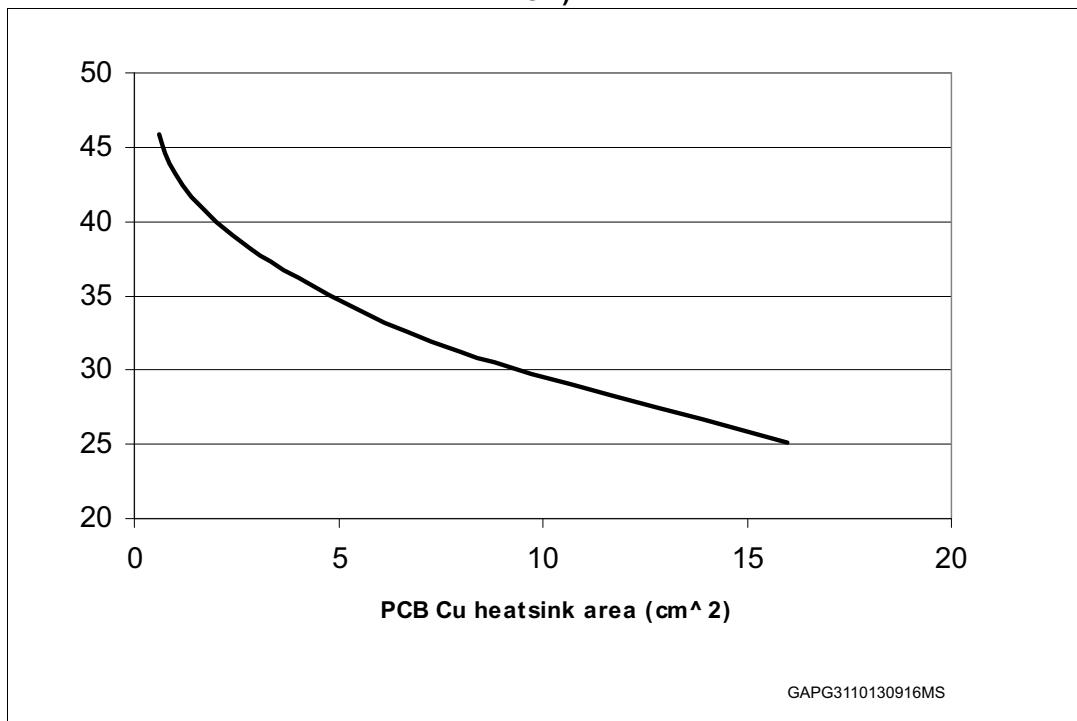
## 4.2 PQFN - 12x12 Power lead-less thermal data

Figure 28. 12x12 Power lead-less package PC board

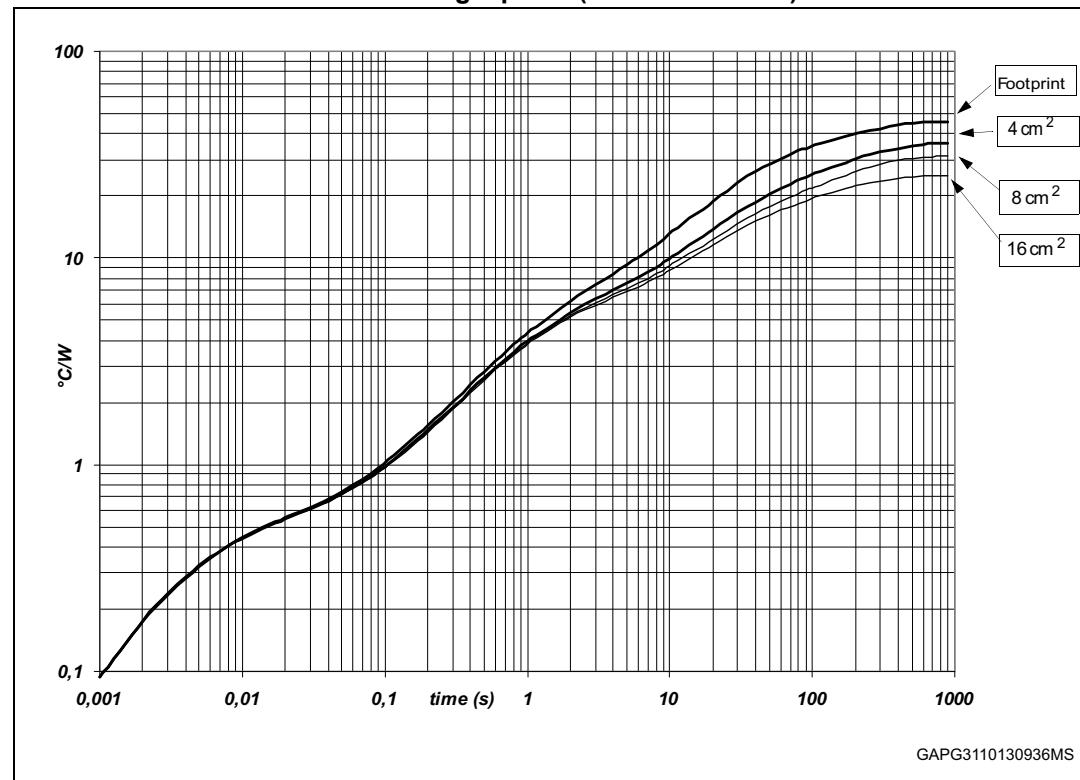


Note: Layout condition of  $R_{th}$  and  $Z_{th}$  measurements (PCB: Double layer, Thermal Vias, FR4 area= 78 mm x 78 mm, PCB thickness=2 mm, Cu thickness=35  $\mu$ m (front and back side), Copper areas: minimum pad layout).

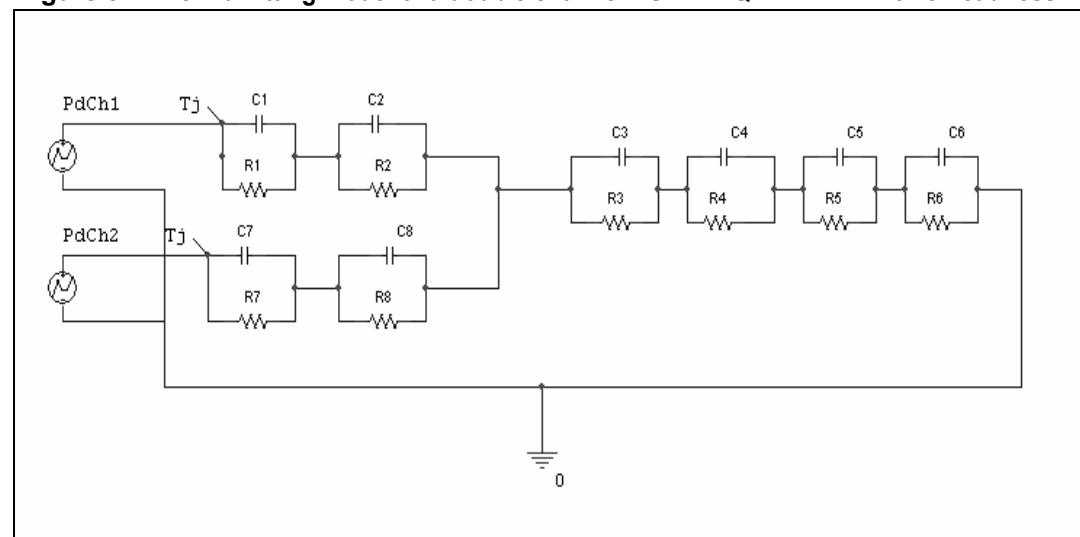
Figure 29.  $R_{thj-amb}$  Vs. PCB copper area in open box free air condition (one channel ON)



**Figure 30. PQFN - 12x12 Power lead-less package thermal impedance junction ambient single pulse (one channel ON)**



**Figure 31. Thermal fitting model of a double channel HSD in PQFN - 12x12 Power lead-less<sup>(b)</sup>**



- b. The fitting model is a simplified thermal tool and is valid for transient evolutions where the embedded protections (power limitation or thermal cycling during thermal shutdown) are not triggered.

**Equation 2: pulse calculation formula**

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where  $\delta = t_p/T$

**Table 16. Thermal parameters for PQFN - 12x12 Power lead-less**

| Area/island (cm <sup>2</sup> ) | Footprint | 4    | 8    | 16   |
|--------------------------------|-----------|------|------|------|
| R1 (°C/W)                      | 0.3       |      |      |      |
| R2 (°C/W)                      | 0.15      |      |      |      |
| R3 (°C/W)                      | 4.2       |      |      |      |
| R4 (°C/W)                      | 9.6       | 9.4  | 9.2  | 9    |
| R5 (°C/W)                      | 15.1      | 10.5 | 8.5  | 5.5  |
| R6 (°C/W)                      | 16.7      | 12   | 9    | 6    |
| R7 (°C/W)                      | 0.3       |      |      |      |
| R8 (°C/W)                      | 0.15      |      |      |      |
| C1 (W.s/°C)                    | 0.021     |      |      |      |
| C2 (W.s/°C)                    | 0.015     |      |      |      |
| C3 (W.s/°C)                    | 0.2       |      |      |      |
| C4 (W.s/°C)                    | 1.9       | 2.2  | 2.32 | 2.45 |
| C5 (W.s/°C)                    | 2.45      | 7.3  | 13.7 | 20   |
| C6 (W.s/°C)                    | 11.85     | 22   | 25   | 30   |
| C7 (W.s/°C)                    | 0.021     |      |      |      |
| C8 (W.s/°C)                    | 0.015     |      |      |      |

## 5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com).  
ECOPACK® is an ST trademark.

### 5.1 MultiPowerSO-30 package information

Figure 32. MultiPowerSO-30 package outline

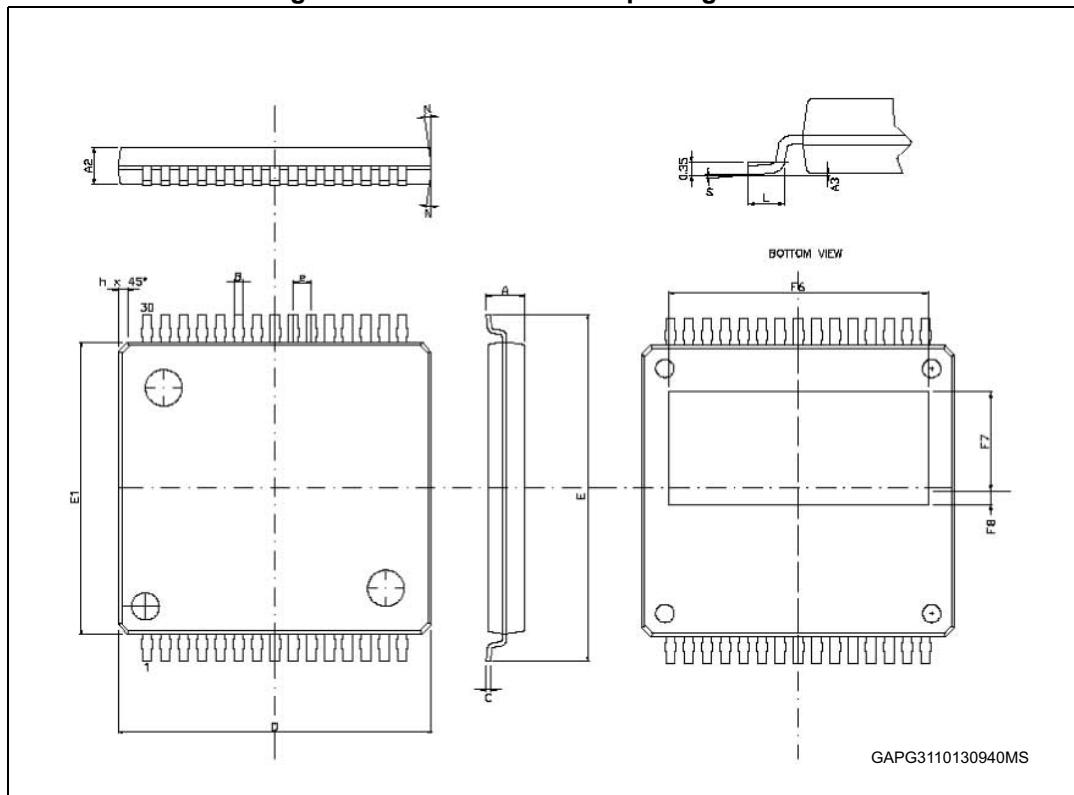


Table 17. MultiPowerSO-30 mechanical data

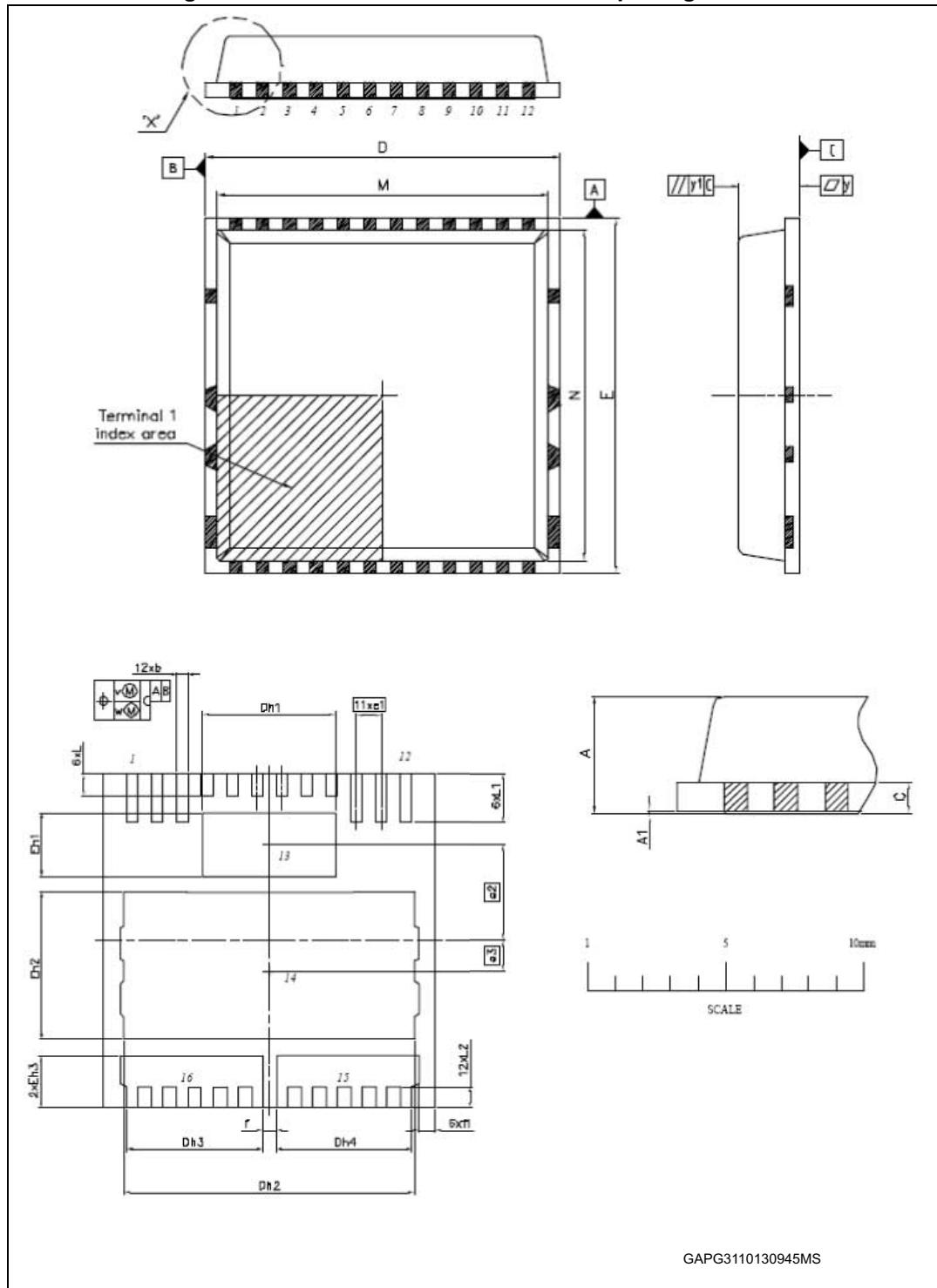
| Symbol | Millimeters |      |      |
|--------|-------------|------|------|
|        | Min.        | Typ. | Max. |
| A      |             |      | 2.35 |
| A2     | 1.85        |      | 2.25 |
| A3     | 0           |      | 0.1  |
| B      | 0.42        |      | 0.58 |
| C      | 0.23        |      | 0.32 |
| D      | 17.1        | 17.2 | 17.3 |

**Table 17. MultiPowerSO-30 mechanical data (continued)**

| Symbol | Millimeters |      |        |
|--------|-------------|------|--------|
|        | Min.        | Typ. | Max.   |
| E      | 18.85       |      | 19.15  |
| E1     | 15.9        | 16   | 16.1   |
| "e"    | 1           |      |        |
| F6     |             | 14.3 |        |
| F7     |             | 5.45 |        |
| F8     |             | 0.73 |        |
| L      | 0.8         |      | 1.15   |
| N      |             |      | 10 Deg |
| S      | 0 Deg       |      | 7 Deg  |

## 5.2 PQFN - 12x12 Power lead-less package information

Figure 33. PQFN - 12x12 Power lead-less package outline



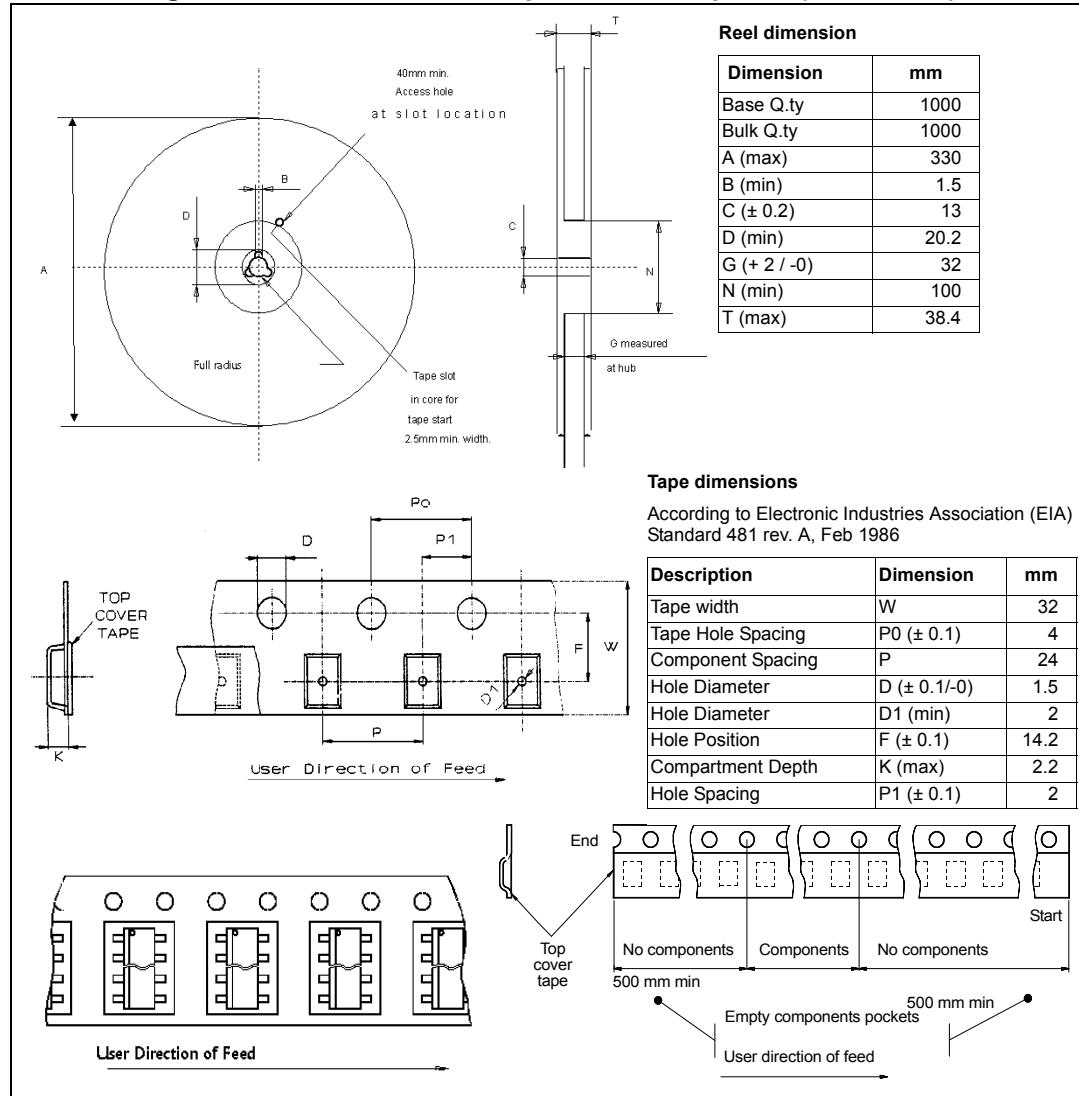
**Table 18. PQFN - 12x12 Power lead-less mechanical data**

| Symbol | Millimeters |      |       |
|--------|-------------|------|-------|
|        | Min.        | Typ. | Max.  |
| A      | 2           |      | 2.2   |
| A1     | 0           |      | 0.05  |
| b      | 0.35        |      | 0.47  |
| C      |             | 0.50 |       |
| D      | 11.90       |      | 12.10 |
| Dh1    | 4.65        |      | 4.95  |
| Dh2    | 10.45       |      | 10.65 |
| Dh3    | 4.80        |      | 5     |
| Dh4    | 4.80        |      | 5     |
| E      | 11.90       |      | 12.10 |
| Eh1    | 2.15        |      | 2.45  |
| Eh2    | 5.15        |      | 5.45  |
| Eh3    | 1.70        |      | 2     |
| e1     |             | 0.90 |       |
| e2     |             | 3.45 |       |
| e3     |             | 1.10 |       |
| f      |             | 0.50 |       |
| f1     |             | 0.60 |       |
| L      | 0.75        |      | 0.95  |
| L1     | 1.65        |      | 1.90  |
| L2     | 0.76        |      | 0.78  |
| M      | 11.10       |      | 11.30 |
| N      | 11.10       |      | 11.30 |
| v      |             | 0.1  |       |
| w      |             | 0.05 |       |
| y      |             | 0.05 |       |
| y1     |             | 0.1  |       |

## 5.3 MultiPowerSO-30 packing information

The devices are packed in tape and reel shipments (see [Table 1: Device summary](#)).

**Figure 34. MultiPowerSO-30 tape and reel shipment (suffix “TR”)**



## 5.4 PQFN - 12x12 Power lead-less packing information

The devices can be packed in tray or tape and reel shipments (see [Table 1: Device summary](#)).

**Figure 35. PQFN - 12x12 Power lead-less tray shipment (no suffix)**

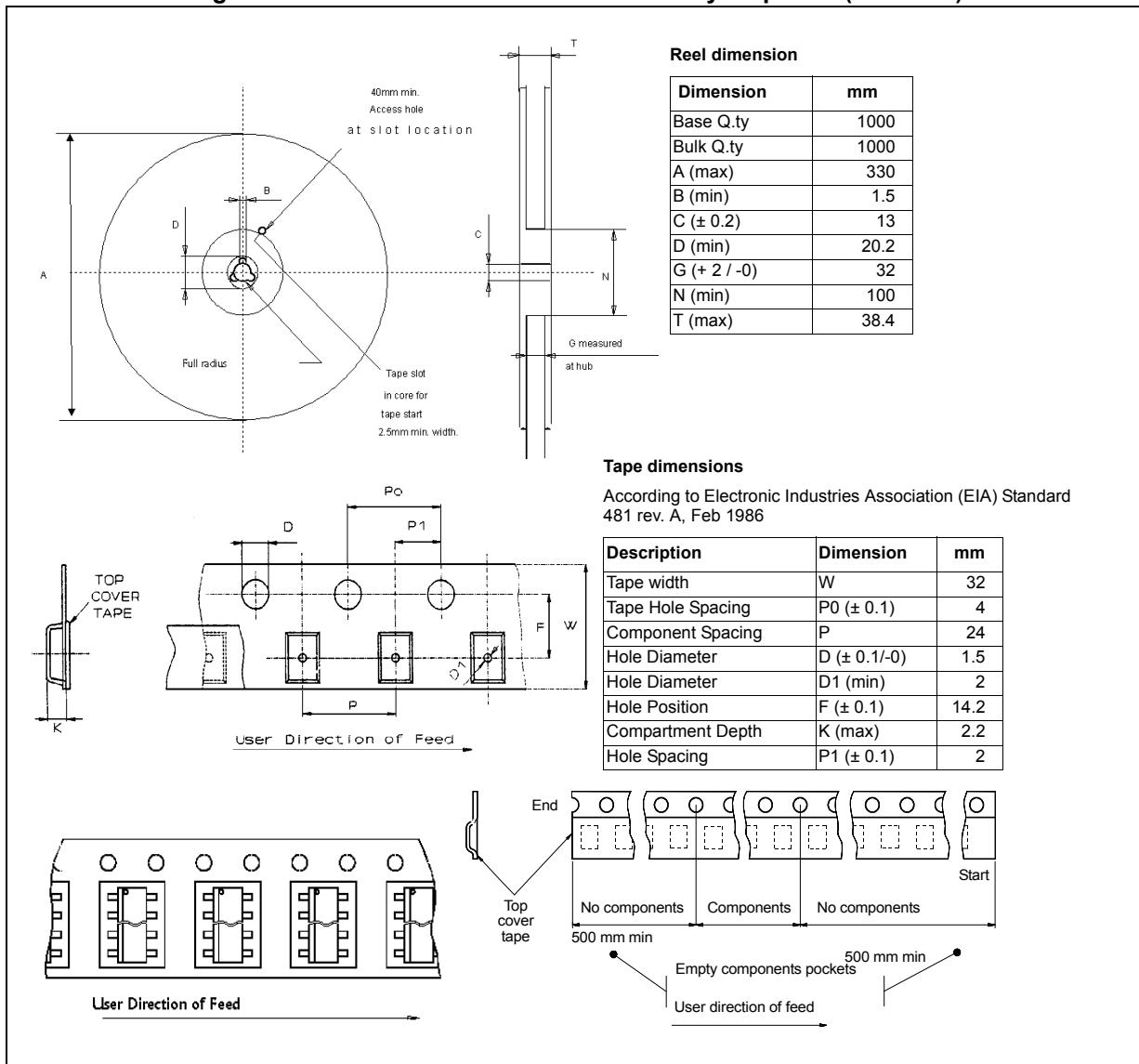
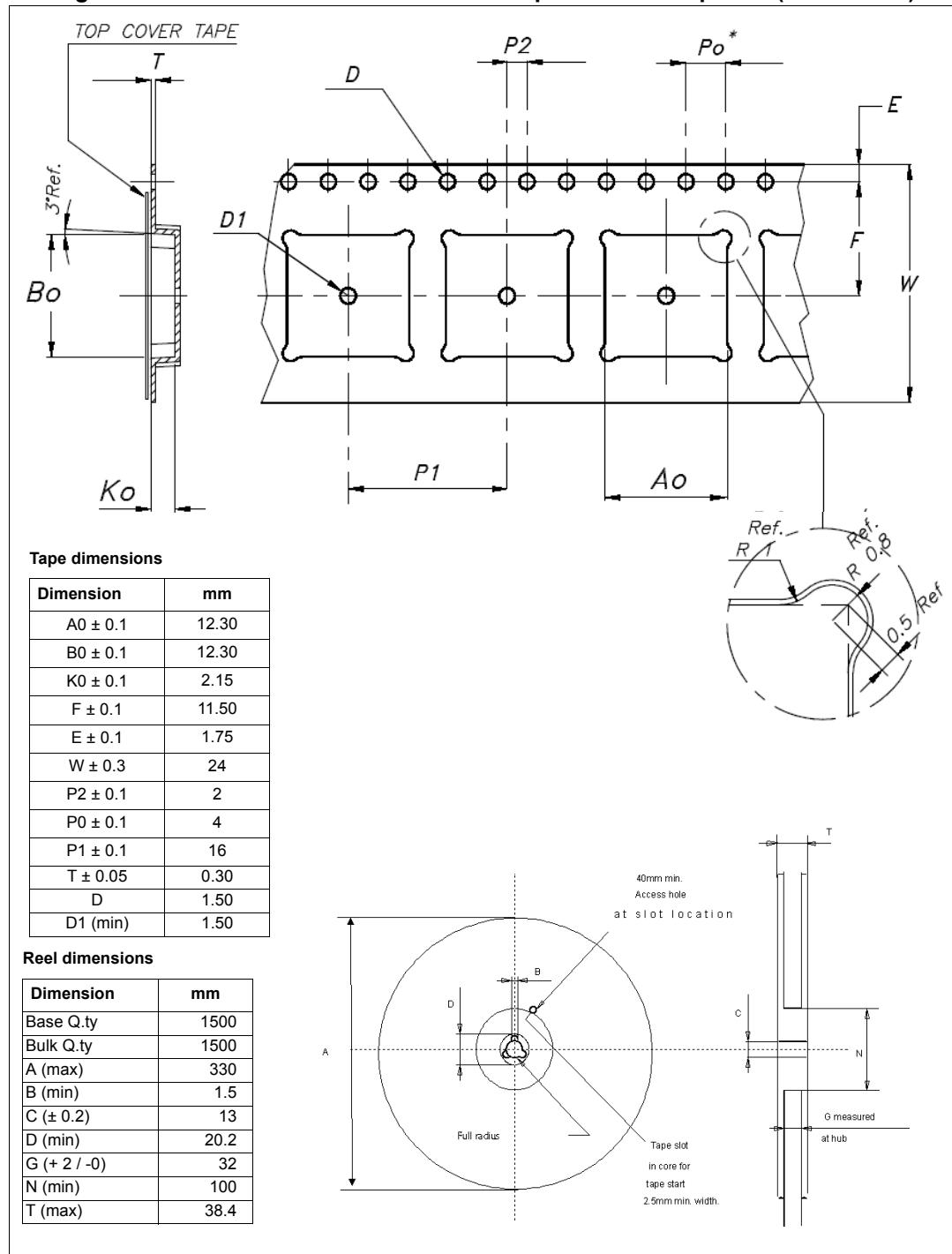


Figure 36. PQFN - 12x12 Power lead-less tape and reel shipment (suffix "TR")



## 6 Revision history

**Table 19. Document revision history**

| Date        | Revision | Changes  |
|-------------|----------|--|
| 15-Sep-2003 | 1        | Initial release.   |
| 21-Jun-2004 | 2        | MultiPowerSO-30 package insertion.   |
| 22-Mar-2006 | 3        | Major general update   |
| 02-Jul-2007 | 4        | Document converted into new ST corporate template.<br>Contents and lists of tables and figures added.<br><i>Section 3.3: Maximum demagnetization energy (VCC = 13.5 V)</i> added.<br><i>Section 5: Package and packing information</i> updated   |
| 29-Oct-2007 | 5        | <i>Section Table 12.: Electrical transient requirements (part 1)</i> - Added note 3: "Suppressed load dump (pulse 5b) is withstood with a minimum load connected as specified in <i>Table 4.: Absolute maximum ratings</i> ."  |
| 24-Sep-2013 | 6        | Updated disclaimer.  |
| 28-Oct-2013 | 7        | Updated footnote 2 into the <i>Table 12: Electrical transient requirements (part 1)</i> and <i>Table 13: Electrical transient requirements (part 2)</i> .  |
| 11-Jan-2017 | 8        | <ul style="list-style-type: none"> <li>– Removed all information relative to tube packing of the product</li> <li>– Modified <i>Section 5: Package information</i>.</li> <li>– Added AEC-Q100 qualified in the Features section</li> <li>– Minor text edits throughout the document</li> </ul> |



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