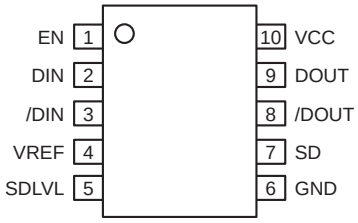
PACKAGE/ORDERING INFORMATION



10-Pin MSOP (K10-1)

Ordering Information

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY88933VKC	K10-1	Commercial	933V	Sn-Pb
SY88933VKCTR(1)	K10-1	Commercial	933V	Sn-Pb
SY88933VKI	K10-1	Industrial	933V	Sn-Pb
SY88933VKITR(1)	K10-1	Industrial	933V	Sn-Pb
SY88933VKG(2)	K10-1	Industrial	933V with Pb-Free bar-line indicator	Pb-Free NiPdAu
SY88933VKGTR(1, 2)	K10-1	Industrial	933V with Pb-Free bar-line indicator	Pb-Free NiPdAu

Note:

1. Tape and Reel.
2. Pb-Free package is recommended for new designs.

PIN DESCRIPTION

Pin Number	Pin Name	Type	Pin Function
1	EN	TTL Input: Default is high.	Enable: Asserts true data output when high.
2	DIN	Data Input	True data input.
3	/DIN	Data Input	Complementary data input.
4	VREF		Reference voltage: capacitor here to V_{CC} helps stabilize SD_{LVL}.
5	SDLVL	Input	Signal-Detect Level Set: a resistor from this pin to V_{CC} sets the threshold for the data input amplitude at which SD will be asserted.
6	GND	Ground	Device ground.
7	SD	Open-collector TTL output w/ internal 6.75kΩ pull-up resistor	Signal-Detect: asserts high when the data input amplitude rises above the threshold set by SD_{LVL}.
8	/DOUT	PECL Output	Complementary data output.
9	DOUT	PECL Output	True data output.
10	VCC	Power Supply	Positive power supply.

Absolute Maximum Ratings(Note 1)

Supply Voltage (V_{CC}) ..... 0V to +7.0V
Input Voltage (D_{IN}, /D_{IN}) ..... 0 to V_{CC}
Output Current (I_{OUT})
  Continuous 50mA
  Surge 100mA
EN Voltage ..... 0 to V_{CC}
V_{REF} Current ..... –800µA to +500µA
SD_{LVL} Voltage ..... V_{REF} to V_{CC}
Storage Temperature (T_S) ..... –55°C to +125°C

Operating Ratings(Note 2)

Supply Voltage (V_{CC}) ..... +3.0V to +3.6V or
..... +4.5V to +5.5V
Ambient Temperature (T_A), **Note 3** ..... –40°C to +85°C
Junction Temperature (T_J), **Note 3** ..... –40°C to +120°C
Package Thermal Resistance
  MSOP
    (θ_{JA}) Still-Air ..... 113°C/W

Note 1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect device reliability.

Note 2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.

Note 3. Commercial devices are guaranteed from 0°C to +85°C ambient temperature.

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 3.0V to 3.6V or 4.5V to 5.5V; R_{LOAD} = 50Ω to V_{CC}–2V; T_A = –40°C to +85°C; typical values at V_{CC} = 3.3V, T_A = 25°C.

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{CC}	Power Supply Current	No output load		22	42	mA
SD_{LVL}	SD_{LVL} Voltage		V_{REF}		V_{CC}	V
V_{IH}	EN Input HIGH Voltage		2.0			V
V_{IL}	EN Input LOW Voltage				0.8	V
I_{IH}	EN Input HIGH Current	V_{IN} = 2.7V V_{IN} = V_{CC}			20 100	µA µA
I_{IL}	EN Input LOW Current	V_{IN} = 0.5V	–0.3			mA
V_{OH}	SD Output HIGH Level	V_{CC} ≥ 3.3V V_{CC} < 3.3V	2.4 2.0			V V
V_{OL}	SD Output LOW Level	I_{OL} = +2mA			0.5	V
V_{OH}	PECL Output HIGH Voltage	50Ω to V_{CC}–2V output load	V_{CC}–1.085	V_{CC}–0.955	V_{CC}–0.880	V
V_{OL}	PECL Output LOW Voltage	50Ω to V_{CC}–2V output load	V_{CC}–1.830	V_{CC}–1.705	V_{CC}–1.555	V
V_{OFFSET}	Differential Output Offset				±160	mV
V_{IHCMR}	Common Mode Range	**Note 1**	GND +2.0		V_{CC}	V
V_{REF}	Reference Voltage	**Note 2**	V_{CC}–1.38	V_{CC}–1.32	V_{CC}–1.26	V

Note 1. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

Note 2. The current provided into or from V_{REF} must be limited to 800µA source and 500µA sink.

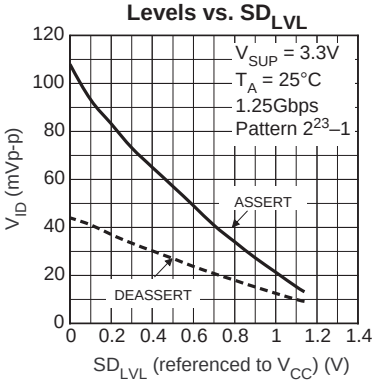
AC ELECTRICAL CHARACTERISTICS

V_{CC} = 3.0V to 3.6V or 4.5V to 5.5V; R_{LOAD} = 50Ω to V_{CC}–2V; T_A = –40°C to +85°C; typical values at V_{CC} = 3.3V, T_A = 25°C.

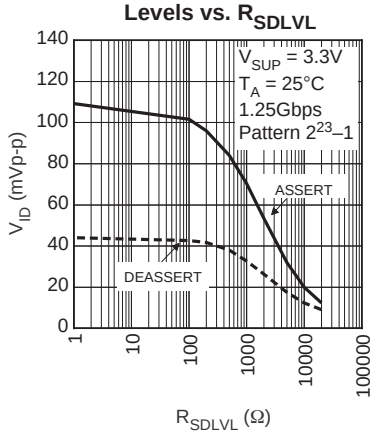
Symbol	Parameter	Condition	Min	Typ	Max	Units
HYS	SD Hysteresis	electrical signal	2	4.6	8	dB
t_{OFF}	SD Release Time			0.1	0.5	µs
t_{ON}	SD Assert Time			0.2	0.5	µs
V_{ID}	Differential Input Voltage Swing		5		1800	mV_{PP}
V_{OD}	Differential Output Voltage Swing	$V_{ID} \geq 18mV_{PP}$ $V_{ID} = 5mV_{PP}$		1500 400		mV_{PP} mV_{PP}
V_{SR}	SD Sensitivity Range		5		50	mV_{PP}
$A_{V(Diff)}$	Differential Voltage Gain			38		dB
$B_{–3dB}$	3dB Bandwidth		1			GHz
S_{21}	Single-Ended Small-Signal Gain		26	32		dB
t_r, t_f	Differential Output Rise/Fall Time (20% to 80%)	$V_{ID} > 100mV_{PP}$ and 50Ω to V_{CC} – 2V load			260	ps

TYPICAL OPERATING CHARACTERISTICS

SD Assert and Deassert Levels vs. SD_{LVL}



SD Assert and Deassert Levels vs. R_{SDLVL}



DETAILED DESCRIPTION

The SY88933V low-power limiting post amplifier operates from a single +3.3V or +5V power supply, over temperatures from –40°C to +85°C. Signals with data rates up to 1.25Gbps and as small as 5mVp-p can be amplified. Figure 1 shows the allowed input voltage swing. The SY88933V generates an SD output. SD_{LVL} sets the sensitivity of the input amplitude detection.

Input Amplifier/Buffer

Figure 2 shows a simplified schematic of the SY88933V's input stage. The high-sensitivity of the input amplifier allows signals as small as $5mV_{PP}$ to be detected and amplified. The input amplifier allows input signals as large as $1800mV_{PP}$. Input signals are linearly amplified with a typically 38dB differential voltage gain. Since it is a limiting amplifier, the SY88933V outputs typically $1500mV_{PP}$ voltage-limited waveforms for input signals that are greater than $18mV_{PP}$. Applications requiring the SY88933V to operate with high-gain should have the upstream TIA placed as close as possible to the SY88933V's input pins to ensure the best performance of the device.

Output Buffer

The SY88933V's PECL output buffer is designed to drive 50Ω lines. The output buffer requires appropriate termination for proper operation. An external 50Ω resistor to V_{CC}–2V for each output pin provides this. Figure 3 shows a simplified schematic of the output stage and includes an appropriate termination method.

Signal-Detect

The SY88933V generates a chatter-free SD open-collector TTL output with internal 6.75kΩ pullup resistor as shown in Figure 4. SD is used to determine that the input amplitude is large enough to be considered a valid input. SD asserts high if the input amplitude rises above the threshold set by SD_{LVL} and deasserts low otherwise. SD can be fed back to the enable (EN) input to maintain output stability under a loss of signal condition. EN deasserts the true output signal without removing the input signals. Typically, 4.6dB SD hysteresis is provided to prevent chattering.

Signal-Detect Level Set

A programmable SD level set pin (SD_{LVL}) sets the threshold of the input amplitude detection. Connecting an external resistor between V_{CC} and SD_{LVL} sets the voltage at SD_{LVL}. This voltages ranges from V_{CC} to V_{REF}. The external resistor creates a voltage divider between V_{CC} and V_{REF} as shown in Figure 5. If desired, an appropriate external voltage may be applied rather than using a resistor. The smaller the external resistor, implying a smaller voltage difference from SD_{LVL} to V_{CC}, the smaller the SD sensitivity. Hence, larger input amplitude is required to assert SD. "Typical Operating Characteristics" shows the relationship between the input amplitude detection sensitivity and the SD_{LVL} voltage.

Hysteresis

The SY88933V provides typically 4.6dB SD electrical hysteresis. By definition, a power ratio measured in dB is 10log(power ratio). Power is calculated as V^2_{IN}/R for an electrical signal. Hence, the same ratio can be stated as 20log(voltage ratio). While in linear mode, the electrical voltage input changes linearly with the optical power and hence the ratios change linearly. Therefore, the optical hysteresis in dB is half the electrical hysteresis in dB given in the datasheet. The SY88933V provides typically 2.3dB SD optical hysteresis. As the SY88933V is an electrical device, this datasheet refers to hysteresis in electrical terms. With 6dB SD hysteresis, a voltage factor of two is required to assert or deassert SD.

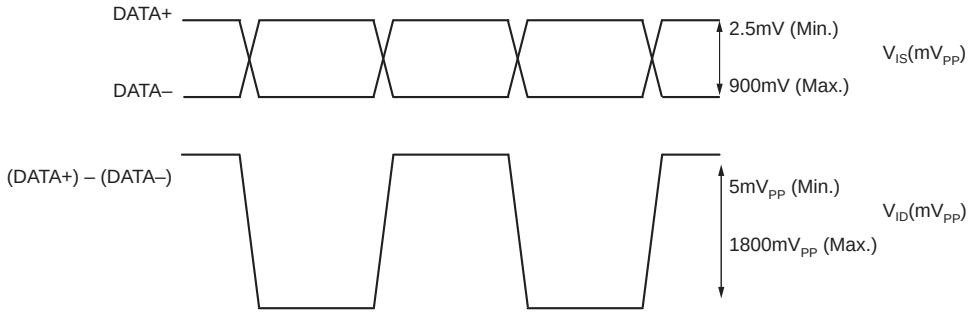


Figure 1. V_{IS} and V_{ID} Definitions

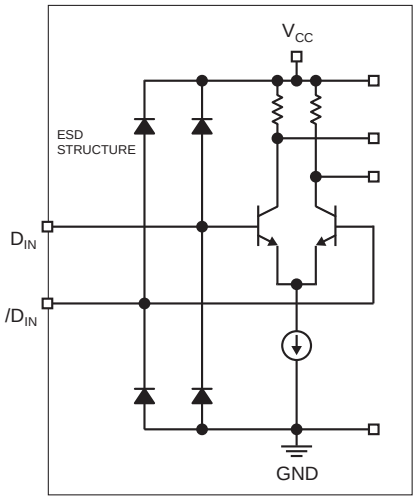


Figure 2. Input Structure

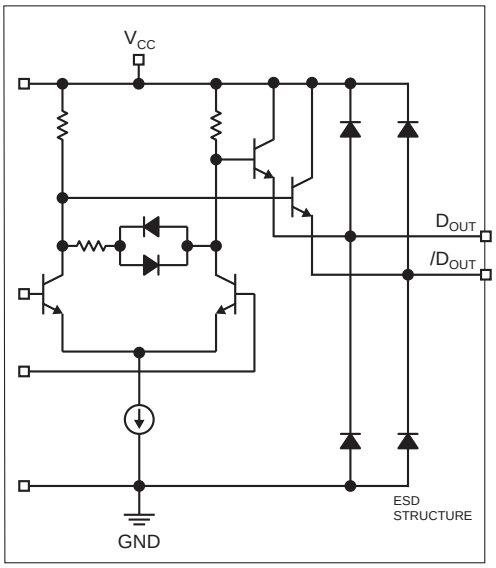


Figure 3. Output Structure

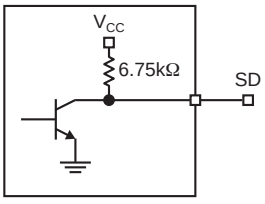


Figure 4. SD Output Structure

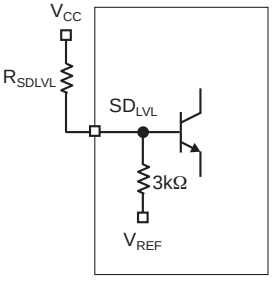
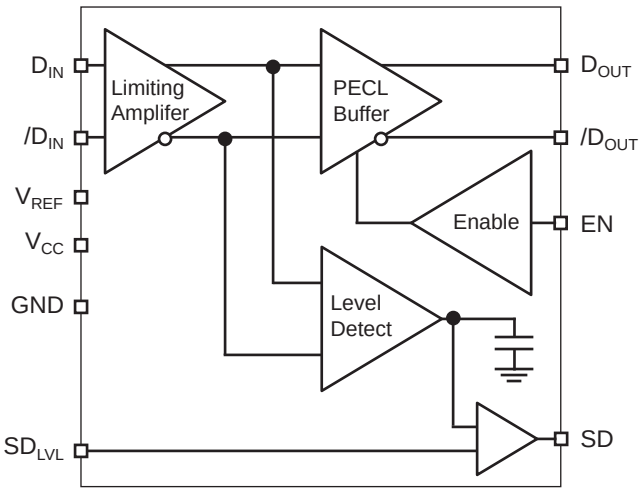


Figure 5. SD_{LVL} Setting Circuit

FUNCTIONAL BLOCK DIAGRAM



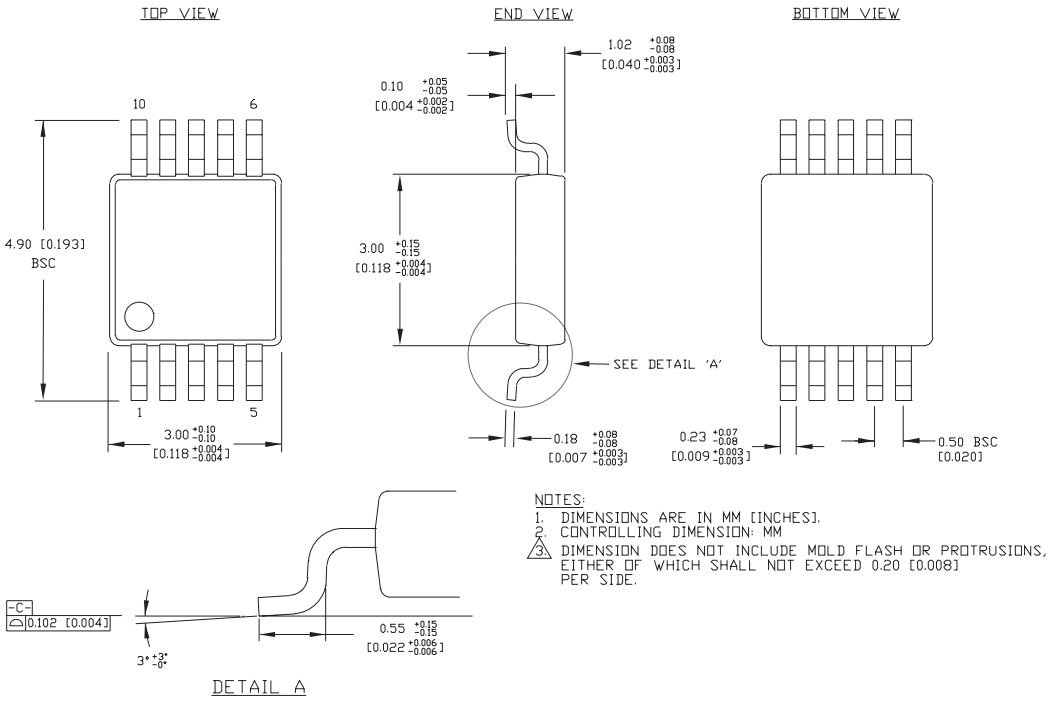
DESIGN PROCEDURE

Layout and PCB Design

Since the SY88933V is a high-frequency component, performance can be largely determined by the board layout and design. A common problem with high-gain amplifiers is the feedback from the large swing outputs to the input via the power supply.

The SY88933V's ground pin should be connected to the circuit board ground. Use multiple PCB vias close to the part to connect to ground. Avoid long, inductive runs which can degrade performance.

10-PIN MSOP (K10-1)



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