



# 512 Kbit / 1 Mbit / 2 Mbit / 4 Mbit Multi-Purpose Flash SST39LF512 / SST39LF010 / SST39LF020 / SST39LF040 SST39VF512 / SST39VF010 / SST39VF020 / SST39VF040

## Data Sheet

### Device Operation

Commands are used to initiate the memory operation functions of the device. Commands are written to the device using standard microprocessor write sequences. A command is written by asserting WE# low while keeping CE# low. The address bus is latched on the falling edge of WE# or CE#, whichever occurs last. The data bus is latched on the rising edge of WE# or CE#, whichever occurs first.

### Read

The Read operation of the SST39LF512/010/020/040 and SST39VF512/010/020/040 device is controlled by CE# and OE#, both have to be low for the system to obtain data from the outputs. CE# is used for device selection. When CE# is high, the chip is deselected and only standby power is consumed. OE# is the output control and is used to gate data from the output pins. The data bus is in high impedance state when either CE# or OE# is high. Refer to the Read cycle timing diagram for further details (Figure 5).

### Byte-Program Operation

The SST39LF512/010/020/040 and SST39VF512/010/020/040 are programmed on a byte-by-byte basis. Before programming, the sector where the byte exists must be fully erased. The Program operation is accomplished in three steps. The first step is the three-byte load sequence for Software Data Protection. The second step is to load byte address and byte data. During the Byte-Program operation, the addresses are latched on the falling edge of either CE# or WE#, whichever occurs last. The data is latched on the rising edge of either CE# or WE#, whichever occurs first. The third step is the internal Program operation which is initiated after the rising edge of the fourth WE# or CE#, whichever occurs first. The Program operation, once initiated, will be completed, within 20  $\mu$ s. See Figures 6 and 7 for WE# and CE# controlled Program operation timing diagrams and Figure 16 for flowcharts. During the Program operation, the only valid reads are Data# Polling and Toggle Bit. During the internal Program operation, the host is free to perform additional tasks. Any commands written during the internal Program operation will be ignored.

### Sector-Erase Operation

The Sector-Erase operation allows the system to erase the device on a sector-by-sector basis. The sector architecture is based on uniform sector size of 4 KByte. The Sector-Erase operation is initiated by executing a six-byte command sequence with Sector-Erase command (30H) and sector address (SA) in the last bus cycle. The sector address is latched on the falling edge of the sixth WE# pulse, while the command (30H) is latched on the rising

edge of the sixth WE# pulse. The internal Erase operation begins after the sixth WE# pulse. The End-of-Erase can be determined using either Data# Polling or Toggle Bit methods. See Figure 10 for timing waveforms. Any commands written during the Sector-Erase operation will be ignored.

### Chip-Erase Operation

The SST39LF512/010/020/040 and SST39VF512/010/020/040 devices provide a Chip-Erase operation, which allows the user to erase the entire memory array to the '1's state. This is useful when the entire device must be quickly erased.

The Chip-Erase operation is initiated by executing a six-byte Software Data Protection command sequence with Chip-Erase command (10H) with address 5555H in the last byte sequence. The internal Erase operation begins with the rising edge of the sixth WE# or CE#, whichever occurs first. During the internal Erase operation, the only valid read is Toggle Bit or Data# Polling. See Table 4 for the command sequence, Figure 11 for timing diagram, and Figure 19 for the flowchart. Any commands written during the Chip-Erase operation will be ignored.

### Write Operation Status Detection

The SST39LF512/010/020/040 and SST39VF512/010/020/040 devices provide two software means to detect the completion of a Write (Program or Erase) cycle, in order to optimize the system write cycle time. The software detection includes two status bits: Data# Polling (DQ<sub>7</sub>) and Toggle Bit (DQ<sub>6</sub>). The End-of-Write detection mode is enabled after the rising edge of WE# which initiates the internal Program or Erase operation.

The actual completion of the nonvolatile write is asynchronous with the system; therefore, either a Data# Polling or Toggle Bit read may be simultaneous with the completion of the Write cycle. If this occurs, the system may possibly get an erroneous result, i.e., valid data may appear to conflict with either DQ<sub>7</sub> or DQ<sub>6</sub>. In order to prevent spurious rejection, if an erroneous result occurs, the software routine should include a loop to read the accessed location an additional two (2) times. If both reads are valid, then the device has completed the Write cycle, otherwise the rejection is valid.



## Data# Polling (DQ<sub>7</sub>)

When the SST39LF512/010/020/040 and SST39VF512/010/020/040 are in the internal Program operation, any attempt to read DQ<sub>7</sub> will produce the complement of the true data. Once the Program operation is completed, DQ<sub>7</sub> will produce true data. Note that even though DQ<sub>7</sub> may have valid data immediately following completion of an internal Write operation, the remaining data outputs may still be invalid: valid data on the entire data bus will appear in subsequent successive Read cycles after an interval of 1  $\mu$ s. During internal Erase operation, any attempt to read DQ<sub>7</sub> will produce a "0". Once the internal Erase operation is completed, DQ<sub>7</sub> will produce a "1". The Data# Polling is valid after the rising edge of fourth WE# (or CE#) pulse for Program operation. For Sector- or Chip-Erase, the Data# Polling is valid after the rising edge of sixth WE# (or CE#) pulse. See Figure 8 for Data# Polling timing diagram and Figure 17 for a flowchart.

## Toggle Bit (DQ<sub>6</sub>)

During the internal Program or Erase operation, any consecutive attempts to read DQ<sub>6</sub> will produce alternating '0's and '1's, i.e., toggling between 0 and 1. When the internal Program or Erase operation is completed, the toggling will stop. The device is then ready for the next operation. The Toggle Bit is valid after the rising edge of fourth WE# (or CE#) pulse for Program operation. For Sector- or Chip-Erase, the Toggle Bit is valid after the rising edge of sixth WE# (or CE#) pulse. See Figure 9 for Toggle Bit timing diagram and Figure 17 for a flowchart.

## Data Protection

The SST39LF512/010/020/040 and SST39VF512/010/020/040 provide both hardware and software features to protect nonvolatile data from inadvertent writes.

## Hardware Data Protection

**Noise/Glitch Protection:** A WE# or CE# pulse of less than 5 ns will not initiate a Write cycle.

**V<sub>DD</sub> Power Up/Down Detection:** The Write operation is inhibited when V<sub>DD</sub> is less than 1.5V.

**Write Inhibit Mode:** Forcing OE# low, CE# high, or WE# high will inhibit the Write operation. This prevents inadvertent writes during power-up or power-down.

## Software Data Protection (SDP)

The SST39LF512/010/020/040 and SST39VF512/010/020/040 provide the JEDEC approved Software Data Protection scheme for all data alteration operation, i.e., Program and Erase. Any Program operation requires the inclusion of a series of three-byte sequence. The three-byte load sequence is used to initiate the Program operation, providing optimal protection from inadvertent Write operations, e.g., during the system power-up or power-down. Any Erase operation requires the inclusion of six-byte load sequence. These devices are shipped with the Software Data Protection permanently enabled. See Table 4 for the specific software command codes. During SDP command sequence, invalid commands will abort the device to read mode, within T<sub>RC</sub>.

## Product Identification

The Product Identification mode identifies the devices as the SST39LF/VF512, SST39LF/VF010, SST39LF/VF020 and SST39LF/VF040 and manufacturer as SST. This mode may be accessed by software operations. Users may use the Software Product Identification operation to identify the part (i.e., using the device ID) when using multiple manufacturers in the same socket. For details, see Table 4 for software operation, Figure 12 for the Software ID Entry and Read timing diagram, and Figure 18 for the Software ID entry command sequence flowchart.

**TABLE 1: PRODUCT IDENTIFICATION**

	Address	Data
Manufacturer's ID	0000H	BFH
Device ID		
SST39LF/VF512	0001H	D4H
SST39LF/VF010	0001H	D5H
SST39LF/VF020	0001H	D6H
SST39LF/VF040	0001H	D7H

T1.1 1150

## Product Identification Mode Exit/Reset

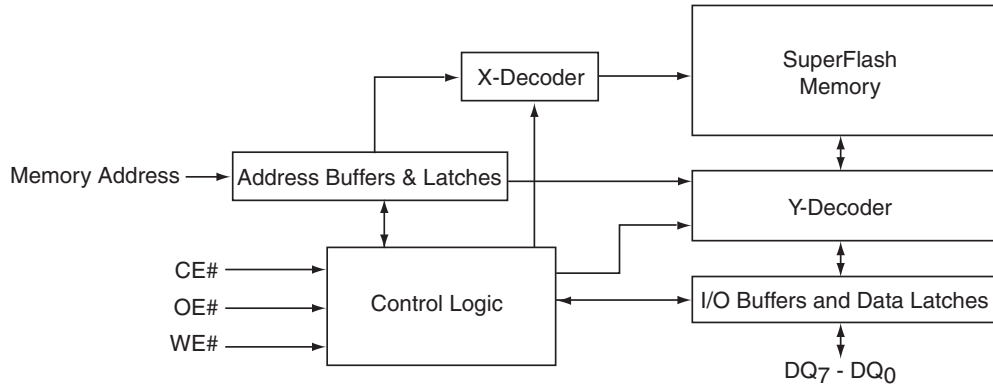
In order to return to the standard Read mode, the Software Product Identification mode must be exited. Exit is accomplished by issuing the Software ID Exit command sequence, which returns the device to the Read operation. Please note that the Software ID Exit command is ignored during an internal Program or Erase operation. See Table 4 for software command codes, Figure 13 for timing waveform, and Figure 18 for a flowchart.



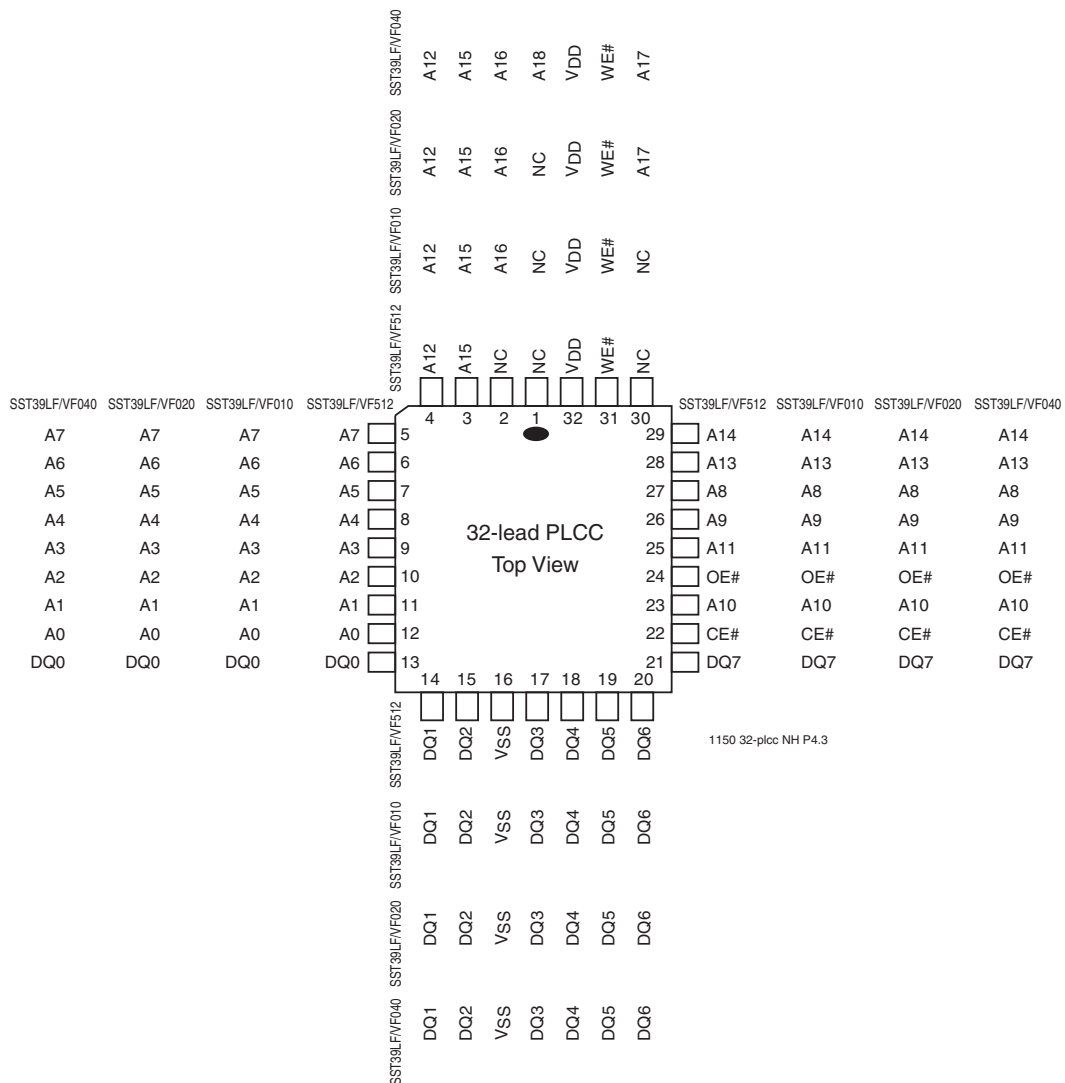
# 512 Kbit / 1 Mbit / 2 Mbit / 4 Mbit Multi-Purpose Flash SST39LF512 / SST39LF010 / SST39LF020 / SST39LF040 SST39VF512 / SST39VF010 / SST39VF020 / SST39VF040

## Data Sheet

### FUNCTIONAL BLOCK DIAGRAM



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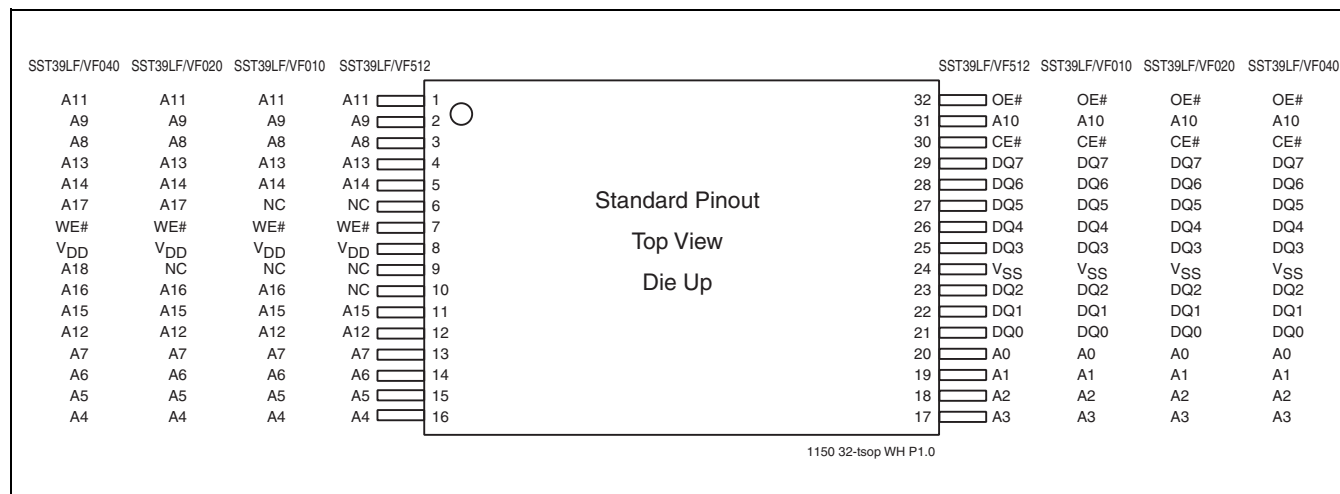
1150 32-plcc NH P4.3

FIGURE 1: PIN ASSIGNMENTS FOR 32-LEAD PLCC

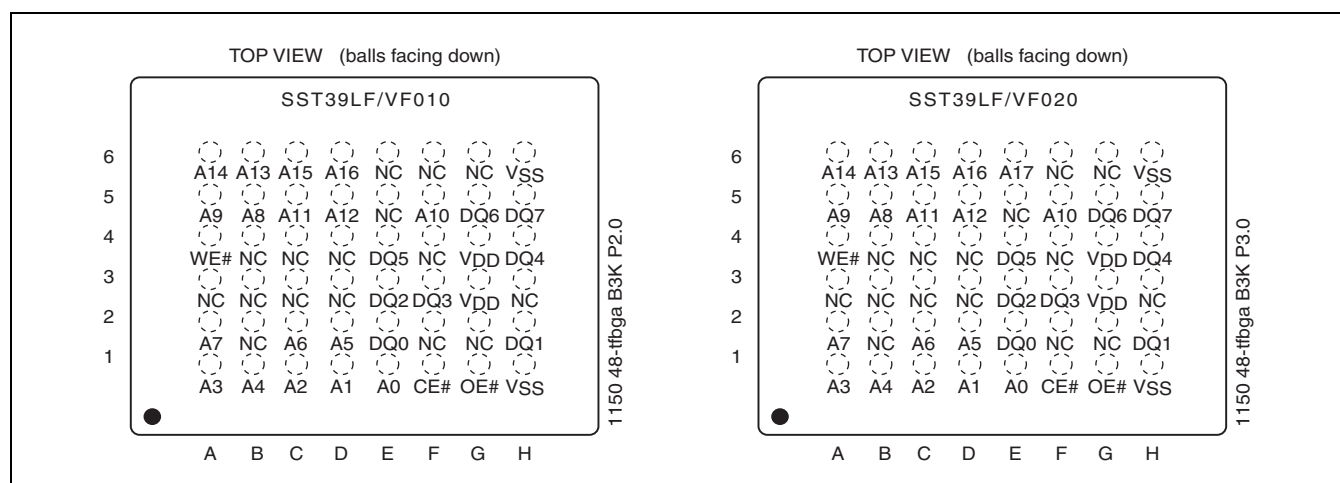
**512 Kbit / 1 Mbit / 2 Mbit / 4 Mbit Multi-Purpose Flash**  
**SST39LF512 / SST39LF010 / SST39LF020 / SST39LF040**  
**SST39VF512 / SST39VF010 / SST39VF020 / SST39VF040**



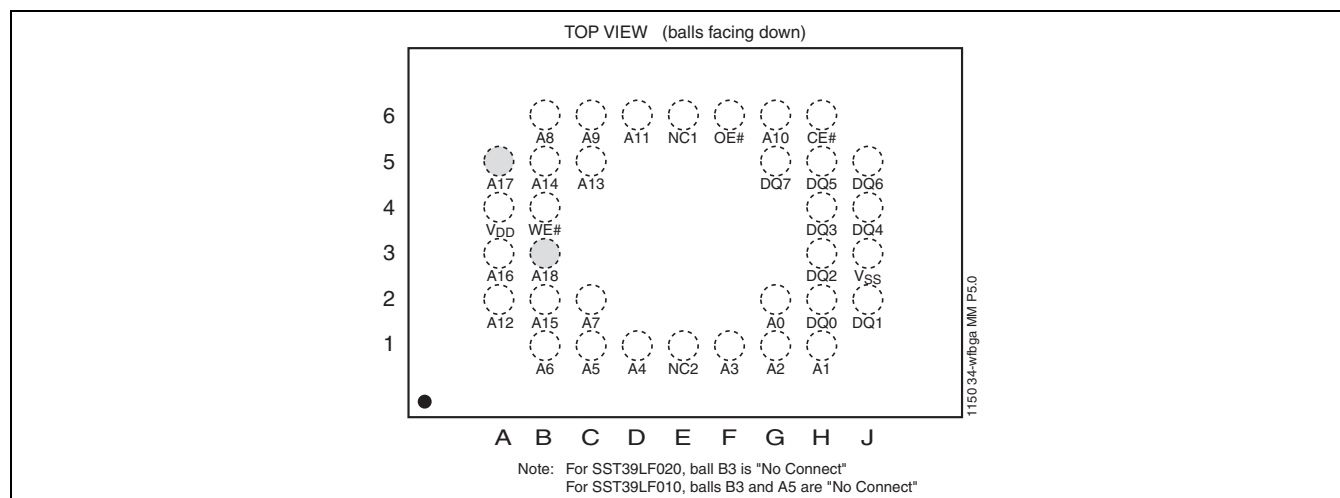
Data Sheet



**FIGURE 2: PIN ASSIGNMENTS FOR 32-LEAD TSOP (8MM X 14MM)**



**FIGURE 3: PIN ASSIGNMENT FOR 48-BALL TFBGA (6MM X 8MM) FOR 1 MBIT AND 2 MBIT**



**FIGURE 4: PIN ASSIGNMENT FOR 34-BALL WFBGA (4MM X 6MM) FOR 1 MBIT AND 2 MBIT**



# 512 Kbit / 1 Mbit / 2 Mbit / 4 Mbit Multi-Purpose Flash SST39LF512 / SST39LF010 / SST39LF020 / SST39LF040 SST39VF512 / SST39VF010 / SST39VF020 / SST39VF040

## Data Sheet

**TABLE 2: PIN DESCRIPTION**

Symbol	Pin Name	Functions
$A_{MS}^1-A_0$	Address Inputs	To provide memory addresses. During Sector-Erase $A_{MS}-A_{12}$ address lines will select the sector. During Block-Erase $A_{MS}-A_{16}$ address lines will select the block.
$DQ_7-DQ_0$	Data Input/output	To output data during Read cycles and receive input data during Write cycles. Data is internally latched during a Write cycle. The outputs are in tri-state when OE# or CE# is high.
CE#	Chip Enable	To activate the device when CE# is low.
OE#	Output Enable	To gate the data output buffers.
WE#	Write Enable	To control the Write operations.
$V_{DD}$	Power Supply	To provide power supply voltage: 3.0-3.6V for SST39LF512/010/020/040 2.7-3.6V for SST39VF512/010/020/040
$V_{SS}$	Ground	
NC	No Connection	Unconnected pins.

T2.1 1150

1.  $A_{MS}$  = Most significant address

$A_{MS}$  =  $A_{15}$  for SST39LF/VF512,  $A_{16}$  for SST39LF/VF010,  $A_{17}$  for SST39LF/VF020, and  $A_{18}$  for SST39LF/VF040

**TABLE 3: OPERATION MODES SELECTION**

Mode	CE#	OE#	WE#	DQ	Address
Read	$V_{IL}$	$V_{IL}$	$V_{IH}$	$D_{OUT}$	$A_{IN}$
Program	$V_{IL}$	$V_{IH}$	$V_{IL}$	$D_{IN}$	$A_{IN}$
Erase	$V_{IL}$	$V_{IH}$	$V_{IL}$	$X^1$	Sector address, XXH for Chip-Erase
Standby	$V_{IH}$	X	X	High Z	X
Write Inhibit	X	$V_{IL}$	X	High Z/ $D_{OUT}$	X
	X	X	$V_{IH}$	High Z/ $D_{OUT}$	X
Product Identification					
Software Mode	$V_{IL}$	$V_{IL}$	$V_{IH}$		See Table 4

T3.4 1150

1. X can be  $V_{IL}$  or  $V_{IH}$ , but no other value.

**512 Kbit / 1 Mbit / 2 Mbit / 4 Mbit Multi-Purpose Flash**  
**SST39LF512 / SST39LF010 / SST39LF020 / SST39LF040**  
**SST39VF512 / SST39VF010 / SST39VF020 / SST39VF040**



Data Sheet

**TABLE 4: SOFTWARE COMMAND SEQUENCE**

Command Sequence	1st Bus Write Cycle		2nd Bus Write Cycle		3rd Bus Write Cycle		4th Bus Write Cycle		5th Bus Write Cycle		6th Bus Write Cycle	
	Addr <sup>1</sup>	Data	Addr <sup>1</sup>	Data	Addr <sup>1</sup>	Data	Addr <sup>1</sup>	Data	Addr <sup>1</sup>	Data	Addr <sup>1</sup>	Data
Byte-Program	5555H	AAH	2AAAH	55H	5555H	A0H	BA <sup>2</sup>	Data				
Sector-Erase	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	SA <sub>X</sub> <sup>3</sup>	30H
Chip-Erase	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	5555H	10H
Software ID Entry <sup>4,5</sup>	5555H	AAH	2AAAH	55H	5555H	90H						
Software ID Exit <sup>6</sup>	XXH	F0H										
Software ID Exit <sup>6</sup>	5555H	AAH	2AAAH	55H	5555H	F0H						

T4.2 1150

- Address format A<sub>14</sub>-A<sub>0</sub> (Hex),  
 Address A<sub>15</sub> can be V<sub>IL</sub> or V<sub>IH</sub>, but no other value, for the Command sequence for SST39LF/VF512.  
 Addresses A<sub>MS</sub>-A<sub>15</sub> can be V<sub>IL</sub> or V<sub>IH</sub>, but no other value, for the Command sequence.  
 A<sub>MS</sub> = Most significant address  
 A<sub>MS</sub> = A<sub>15</sub> for SST39LF/VF512, A<sub>16</sub> for SST39LF/VF010, A<sub>17</sub> for SST39LF/VF020, and A<sub>18</sub> for SST39LF/VF040
- BA = Program Byte address
- SA<sub>X</sub> for Sector-Erase; uses A<sub>MS</sub>-A<sub>12</sub> address lines
- The device does not remain in Software Product ID mode if powered down.
- With A<sub>MS</sub>-A<sub>1</sub> = 0; SST Manufacturer's ID = BFH, is read with A<sub>0</sub> = 0,  
 SST39LF/VF512 Device ID = D4H, is read with A<sub>0</sub> = 1  
 SST39LF/VF010 Device ID = D5H, is read with A<sub>0</sub> = 1  
 SST39LF/VF020 Device ID = D6H, is read with A<sub>0</sub> = 1  
 SST39LF/VF040 Device ID = D7H, is read with A<sub>0</sub> = 1
- Both Software ID Exit operations are equivalent

**Absolute Maximum Stress Ratings** (Applied conditions greater than those listed under "Absolute Maximum Stress Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
D. C. Voltage on Any Pin to Ground Potential	-0.5V to V <sub>DD</sub> +0.5V
Transient Voltage (<20 ns) on Any Pin to Ground Potential	-2.0V to V <sub>DD</sub> +2.0V
Voltage on A <sub>9</sub> Pin to Ground Potential	-0.5V to 13.2V
Package Power Dissipation Capability (Ta = 25°C)	1.0W
Output Short Circuit Current <sup>1</sup>	50 mA

- Outputs shorted for no more than one second. No more than one output shorted at a time.

**OPERATING RANGE FOR SST39LF512/010/020/040**

Range	Ambient Temp	V <sub>DD</sub>
Commercial	0°C to +70°C	3.0-3.6V

**OPERATING RANGE FOR SST39VF512/010/020/040**

Range	Ambient Temp	V <sub>DD</sub>
Commercial	0°C to +70°C	2.7-3.6V
Industrial	-40°C to +85°C	2.7-3.6V

**AC CONDITIONS OF TEST**

Input Rise/Fall Time	5 ns
Output Load	
C <sub>L</sub> =	30 pF for SST39LF512/010/020/040
C <sub>L</sub> =	100 pF for SST39VF512/010/020/040
See Figures 14 and 15	



# 512 Kbit / 1 Mbit / 2 Mbit / 4 Mbit Multi-Purpose Flash SST39LF512 / SST39LF010 / SST39LF020 / SST39LF040 SST39VF512 / SST39VF010 / SST39VF020 / SST39VF040

## Data Sheet

**TABLE 5: DC OPERATING CHARACTERISTICS**

$V_{DD} = 3.0\text{-}3.6\text{V}$  FOR SST39LF512/010/020/040 AND  $2.7\text{-}3.6\text{V}$  FOR SST39VF512/010/020/040<sup>1</sup>

Symbol	Parameter	Limits			Test Conditions
		Min	Max	Units	
$I_{DD}$	Power Supply Current				Address input= $V_{ILT}/V_{IHT}$ , at $f=1/T_{RC}$ Min $V_{DD}=V_{DD}$ Max
	Read <sup>2</sup>		20	mA	$CE\#=V_{IL}$ , $OE\#=WE\#=V_{IH}$ , all I/Os open
	Program and Erase <sup>3</sup>		30	mA	$CE\#=WE\#=V_{IL}$ , $OE\#=V_{IH}$
$I_{SB}$	Standby $V_{DD}$ Current		15	$\mu\text{A}$	$CE\#=V_{IHC}$ , $V_{DD}=V_{DD}$ Max
$I_{LI}$	Input Leakage Current		1	$\mu\text{A}$	$V_{IN}=\text{GND}$ to $V_{DD}$ , $V_{DD}=V_{DD}$ Max
$I_{LO}$	Output Leakage Current		10	$\mu\text{A}$	$V_{OUT}=\text{GND}$ to $V_{DD}$ , $V_{DD}=V_{DD}$ Max
$V_{IL}$	Input Low Voltage		0.8	V	$V_{DD}=V_{DD}$ Min
$V_{IH}$	Input High Voltage	$0.7V_{DD}$		V	$V_{DD}=V_{DD}$ Max
$V_{IHC}$	Input High Voltage (CMOS)	$V_{DD}-0.3$		V	$V_{DD}=V_{DD}$ Max
$V_{OL}$	Output Low Voltage		0.2	V	$I_{OL}=100\text{ }\mu\text{A}$ , $V_{DD}=V_{DD}$ Min
$V_{OH}$	Output High Voltage	$V_{DD}-0.2$		V	$I_{OH}=-100\text{ }\mu\text{A}$ , $V_{DD}=V_{DD}$ Min

T5.7 1150

1. Typical conditions for the Active Current shown on the front data sheet page are average values at 25°C (room temperature), and  $V_{DD} = 3\text{V}$  for VF devices. Not 100% tested.
2. Values are for 70 ns conditions. See the *Multi-Purpose Flash Power Rating* application note for further information.
3. 30 mA max for Erase operations in the industrial temperature range.

**TABLE 6: RECOMMENDED SYSTEM POWER-UP TIMINGS**

Symbol	Parameter	Minimum	Units
$T_{PU-READ}^1$	Power-up to Read Operation	100	$\mu\text{s}$
$T_{PU-WRITE}^1$	Power-up to Program/Erase Operation	100	$\mu\text{s}$

T6.1 1150

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

**TABLE 7: CAPACITANCE ( $T_a = 25^\circ\text{C}$ ,  $f=1\text{ Mhz}$ , other pins open)**

Parameter	Description	Test Condition	Maximum
$C_{I/O}^1$	I/O Pin Capacitance	$V_{I/O} = 0\text{V}$	12 pF
$C_{IN}^1$	Input Capacitance	$V_{IN} = 0\text{V}$	6 pF

T7.0 1150

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

**TABLE 8: RELIABILITY CHARACTERISTICS**

Symbol	Parameter	Minimum Specification	Units	Test Method
$N_{END}^{1,2}$	Endurance	10,000	Cycles	JEDEC Standard A117
$T_{DR}^1$	Data Retention	100	Years	JEDEC Standard A103
$I_{LTH}^1$	Latch Up	$100 + I_{DD}$	mA	JEDEC Standard 78

T8.3 1150

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.
2.  $N_{END}$  endurance rating is qualified as a 10,000 cycle minimum for the whole device. A sector- or block-level rating would result in a higher minimum specification.





## AC CHARACTERISTICS

**TABLE 9: READ CYCLE TIMING PARAMETERS**

$V_{DD} = 3.0\text{-}3.6\text{V}$  FOR SST39LF512/010/020/040 AND  $2.7\text{-}3.6\text{V}$  FOR SST39VF512/010/020/040

Symbol	Parameter	SST39LF512-45 SST39LF010-45 SST39LF020-45 SST39LF040-45		SST39LF020-55 SST39LF040-55		SST39VF512-70 SST39VF010-70 SST39VF020-70 SST39VF040-70		SST39VF512-90 SST39VF010-90 SST39VF020-90 SST39VF040-90		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
$T_{RC}$	Read Cycle Time	45		55		70		90		ns
$T_{CE}$	Chip Enable Access Time		45		55		70		90	ns
$T_{AA}$	Address Access Time		45		55		70		90	ns
$T_{OE}$	Output Enable Access Time		30		30		35		45	ns
$T_{CLZ}^1$	CE# Low to Active Output	0		0		0		0		ns
$T_{OLZ}^1$	OE# Low to Active Output	0		0		0		0		ns
$T_{CHZ}^1$	CE# High to High-Z Output		15		15		25		30	ns
$T_{OHZ}^1$	OE# High to High-Z Output		15		15		25		30	ns
$T_{OH}^1$	Output Hold from Address Change	0		0		0		0		ns

T9.2 1150

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

**TABLE 10: PROGRAM/ERASE CYCLE TIMING PARAMETERS**

Symbol	Parameter	Min	Max	Units
$T_{BP}$	Byte-Program Time		20	$\mu\text{s}$
$T_{AS}$	Address Setup Time	0		ns
$T_{AH}$	Address Hold Time	30		ns
$T_{CS}$	WE# and CE# Setup Time	0		ns
$T_{CH}$	WE# and CE# Hold Time	0		ns
$T_{OES}$	OE# High Setup Time	0		ns
$T_{OEh}$	OE# High Hold Time	10		ns
$T_{CP}$	CE# Pulse Width	40		ns
$T_{WP}$	WE# Pulse Width	40		ns
$T_{WPH}^1$	WE# Pulse Width High	30		ns
$T_{CPH}^1$	CE# Pulse Width High	30		ns
$T_{DS}$	Data Setup Time	40		ns
$T_{DH}^1$	Data Hold Time	0		ns
$T_{IDA}^1$	Software ID Access and Exit Time		150	ns
$T_{SE}$	Sector-Erase		25	ms
$T_{SCE}$	Chip-Erase		100	ms

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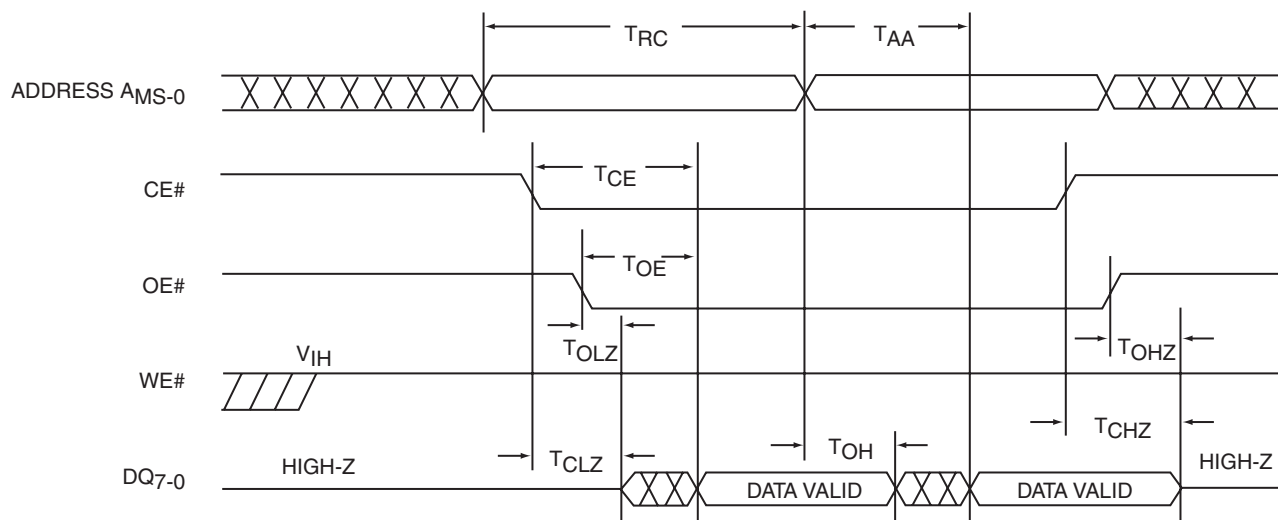
1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.





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SST39VF512 / SST39VF010 / SST39VF020 / SST39VF040

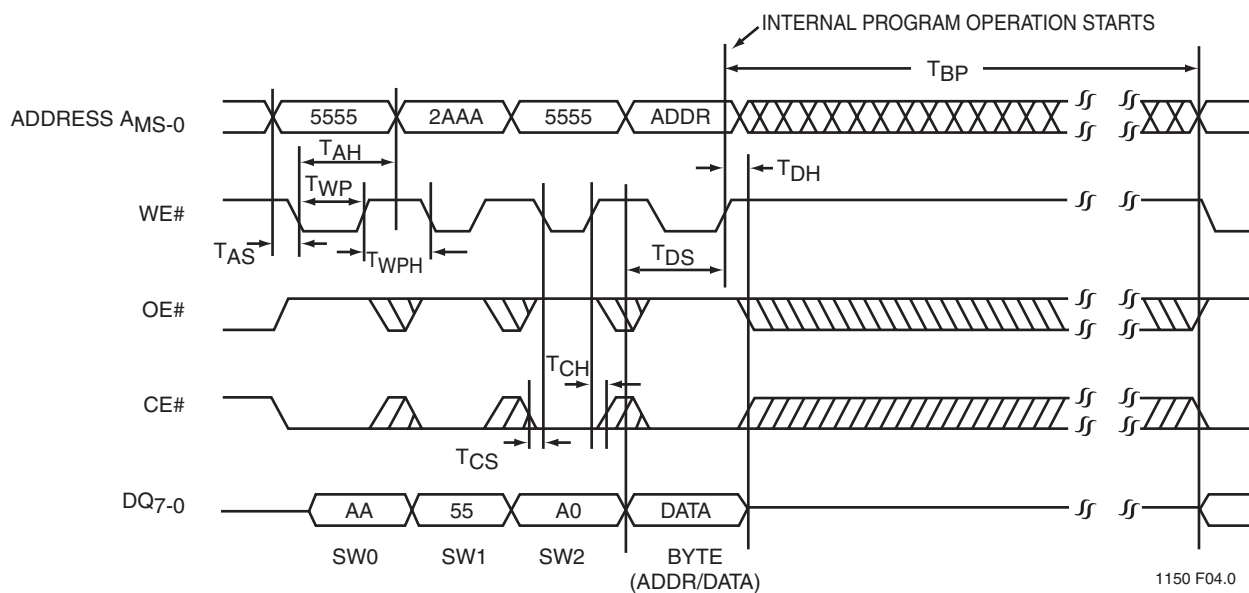
Data Sheet



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Note: A<sub>MS</sub> = Most significant address  
A<sub>MS</sub> = A<sub>15</sub> for SST39LF/VF512, A<sub>16</sub> for SST39LF/VF010,  
A<sub>17</sub> for SST39LF/VF020 and A<sub>18</sub> for SST39LF/VF040

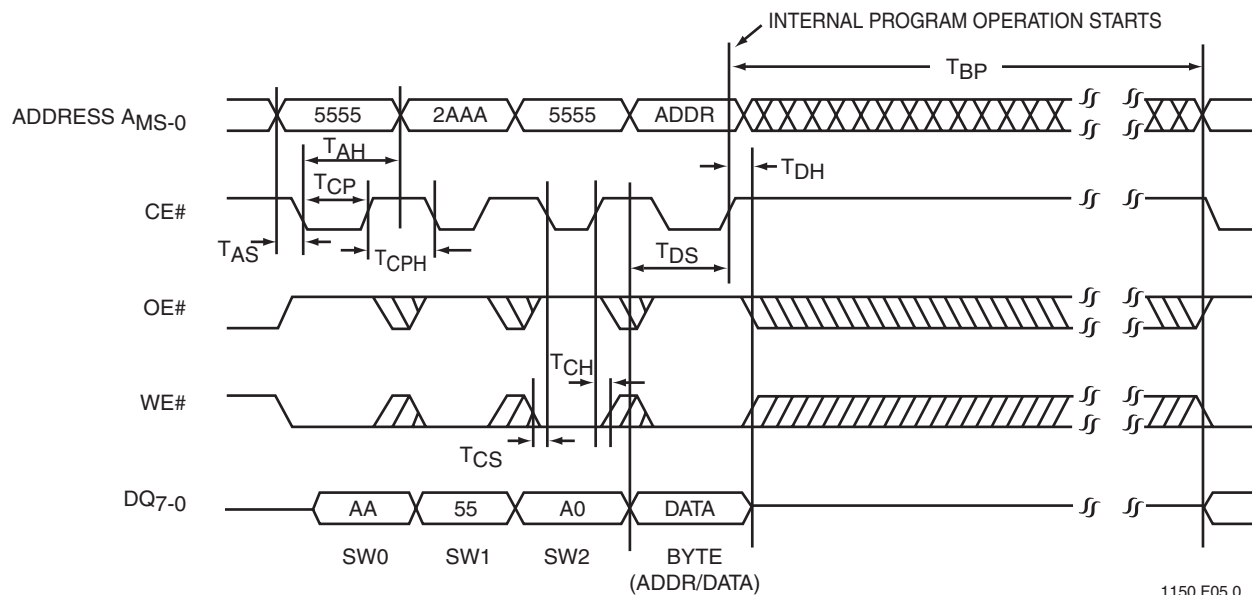
FIGURE 5: READ CYCLE TIMING DIAGRAM



1150 F04.0

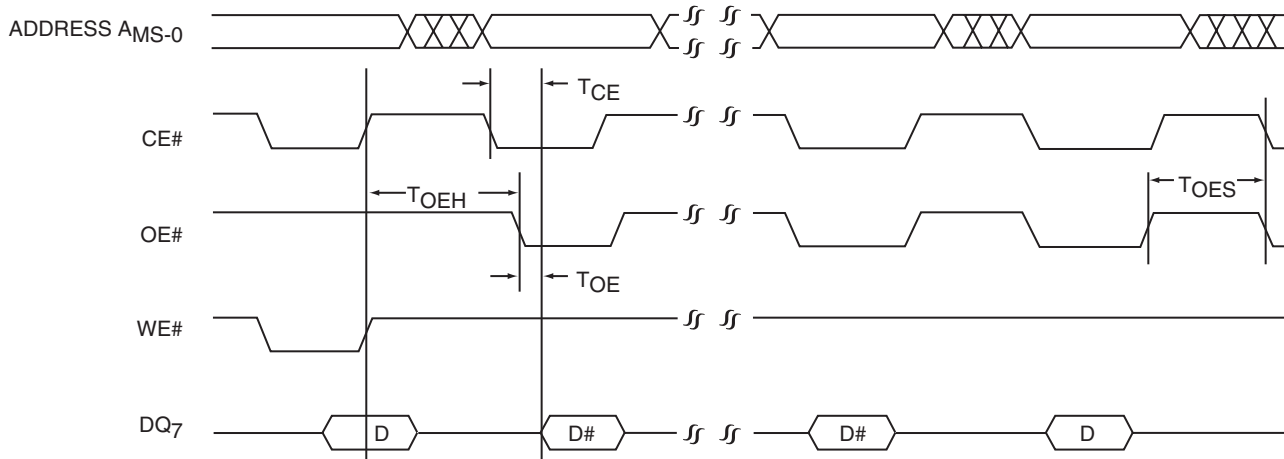
Note: A<sub>MS</sub> = Most significant address  
A<sub>MS</sub> = A<sub>15</sub> for SST39LF/VF512, A<sub>16</sub> for SST39LF/VF010,  
A<sub>17</sub> for SST39LF/VF020 and A<sub>18</sub> for SST39LF/VF040

FIGURE 6: WE# CONTROLLED PROGRAM CYCLE TIMING DIAGRAM



Note:  $A_{MS}$  = Most significant address  
 $A_{MS}$  =  $A_{15}$  for SST39LF/VF512,  $A_{16}$  for SST39LF/VF010,  
 $A_{17}$  for SST39LF/VF020 and  $A_{18}$  for SST39LF/VF040

FIGURE 7: CE# CONTROLLED PROGRAM CYCLE TIMING DIAGRAM



Note:  $A_{MS}$  = Most significant address  
 $A_{MS}$  =  $A_{15}$  for SST39LF/VF512,  $A_{16}$  for SST39LF/VF010,  
 $A_{17}$  for SST39LF/VF020 and  $A_{18}$  for SST39LF/VF040

FIGURE 8: DATA# POLLING TIMING DIAGRAM



512 Kbit / 1 Mbit / 2 Mbit / 4 Mbit Multi-Purpose Flash  
SST39LF512 / SST39LF010 / SST39LF020 / SST39LF040  
SST39VF512 / SST39VF010 / SST39VF020 / SST39VF040

Data Sheet

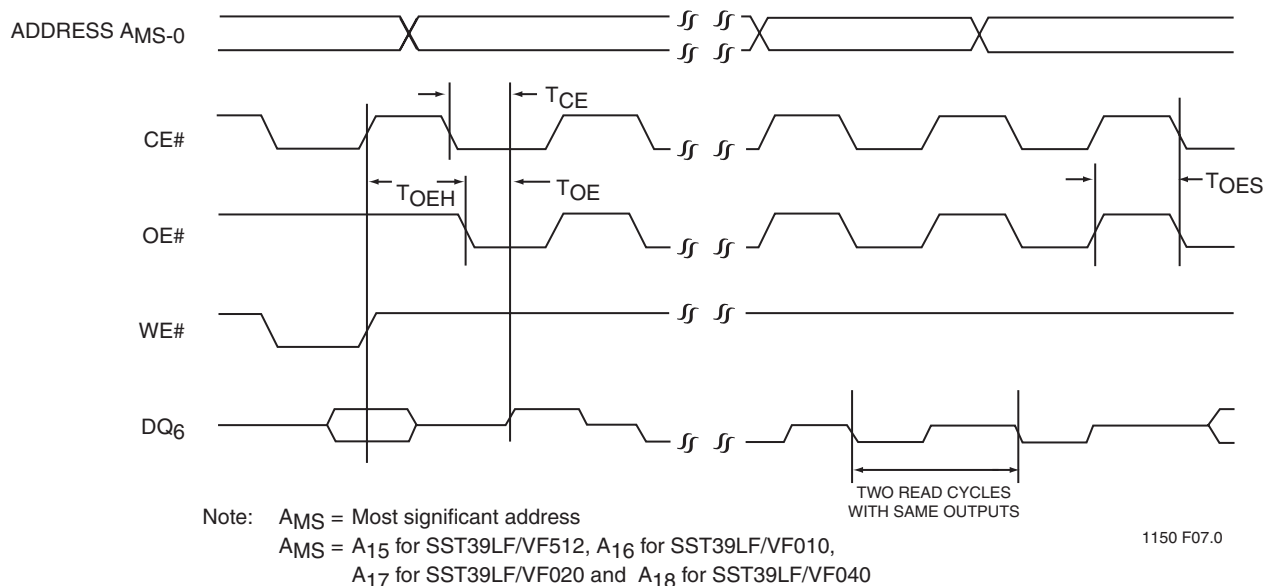


FIGURE 9: TOGGLE BIT TIMING DIAGRAM

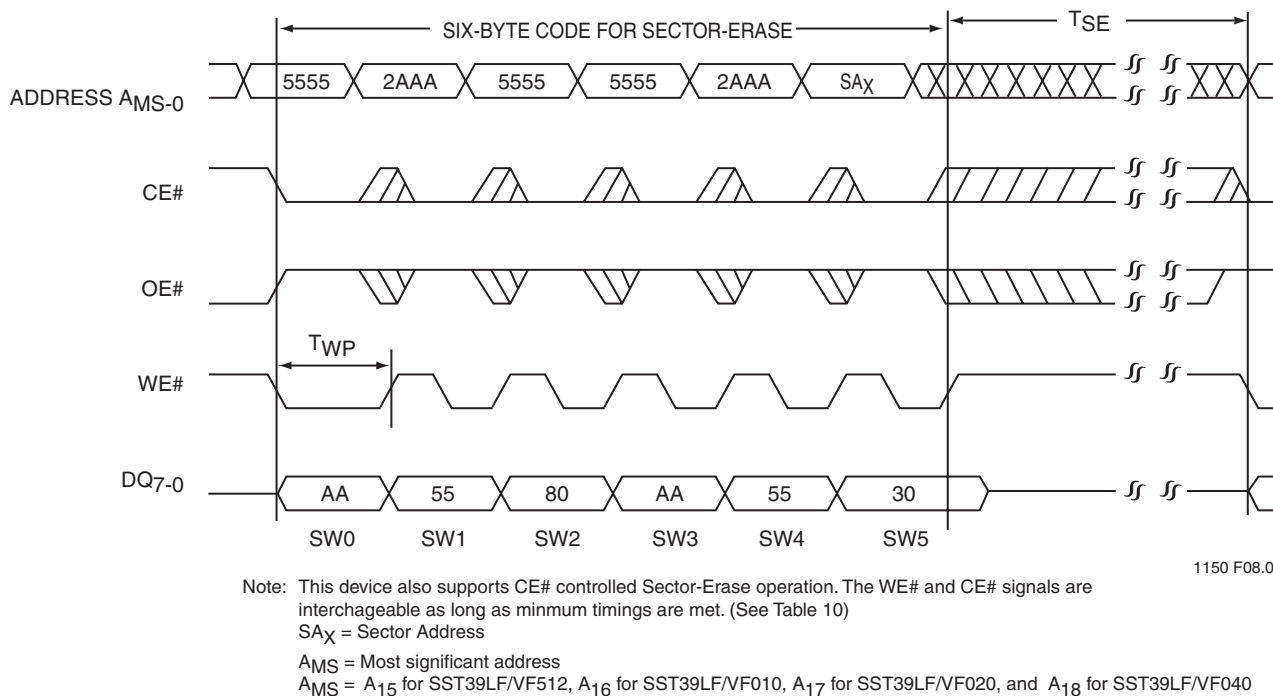
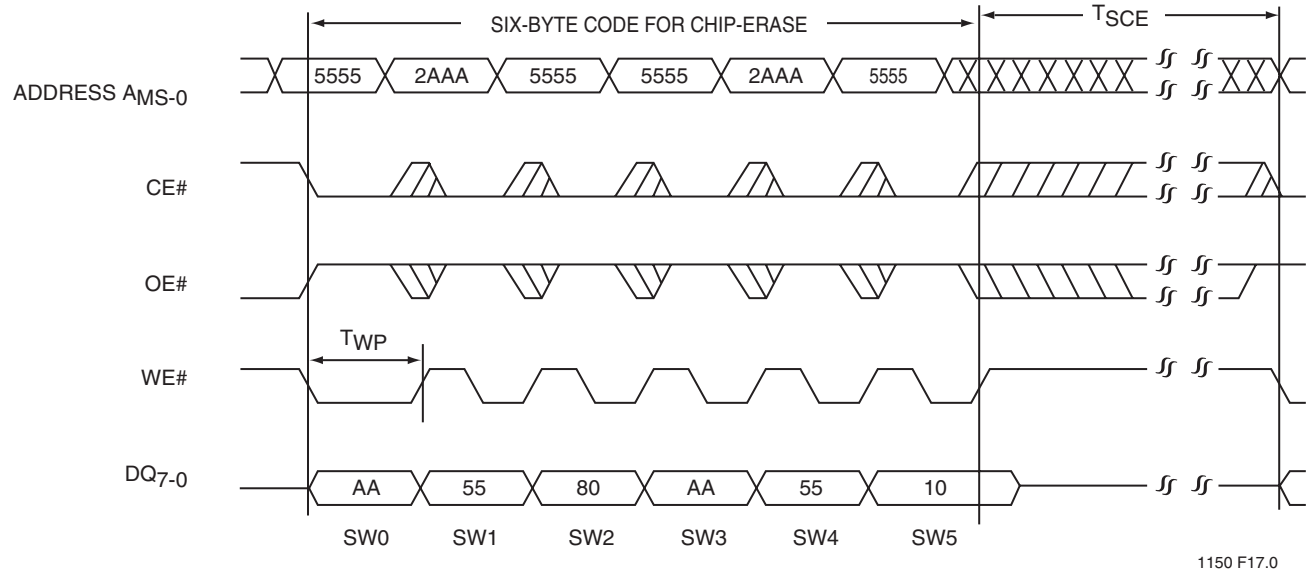
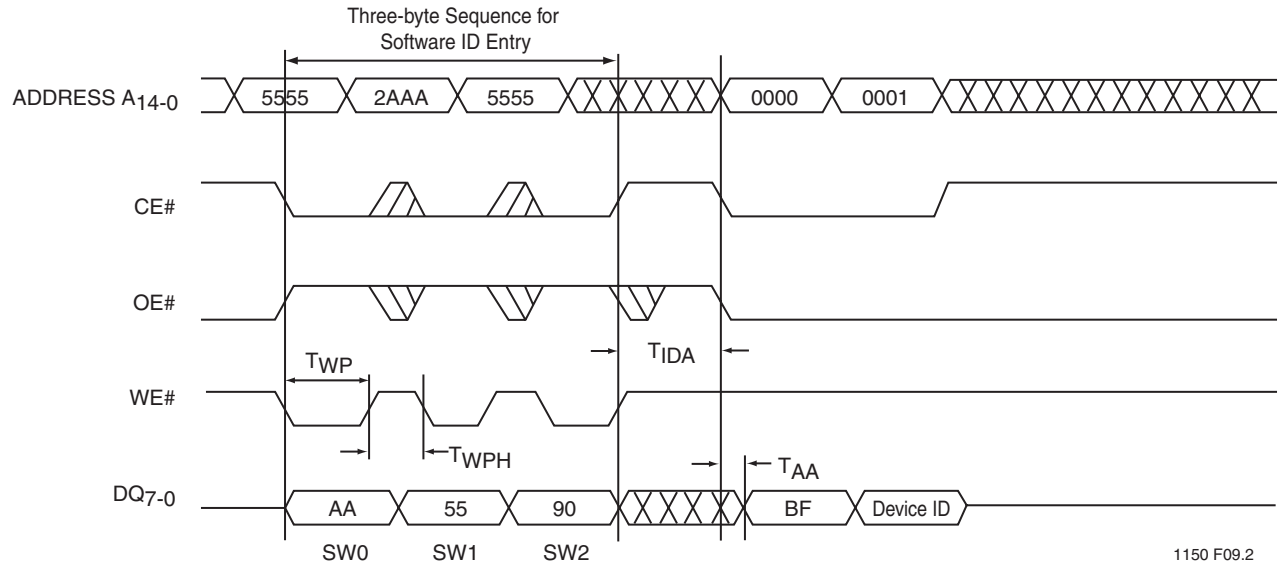


FIGURE 10: WE# CONTROLLED SECTOR-ERASE TIMING DIAGRAM



Note: This device also supports CE# controlled Chip-Erase operation. The WE# and CE# signals are interchangeable as long as minimum timings are met. (See Table 10)  
AMS = Most significant address  
AMS = A<sub>15</sub> for SST39LF/VF512, A<sub>16</sub> for SST39LF/VF010, A<sub>17</sub> for SST39LF/VF020, and A<sub>18</sub> for SST39LF/VF040

FIGURE 11: WE# CONTROLLED CHIP-ERASE TIMING DIAGRAM



Note: Device ID = D4H for SST39LF/VF512, D5H for SST39LF/VF010, D6H for SST39LF/VF020, and D7H for SST39LF/VF040.

FIGURE 12: SOFTWARE ID ENTRY AND READ



512 Kbit / 1 Mbit / 2 Mbit / 4 Mbit Multi-Purpose Flash  
SST39LF512 / SST39LF010 / SST39LF020 / SST39LF040  
SST39VF512 / SST39VF010 / SST39VF020 / SST39VF040

Data Sheet

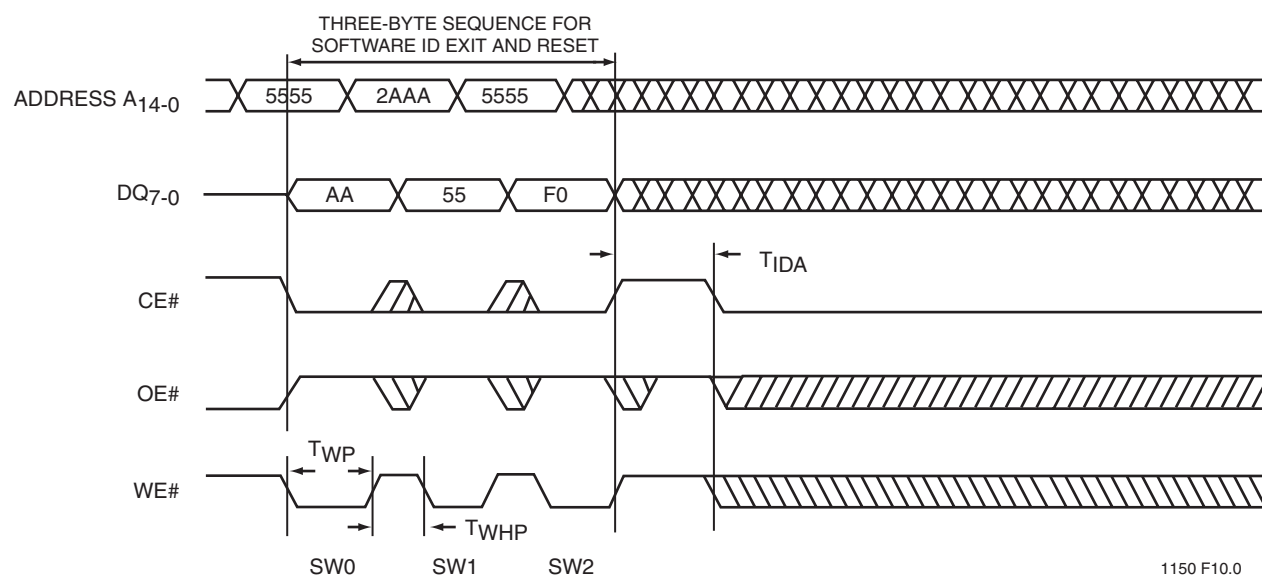
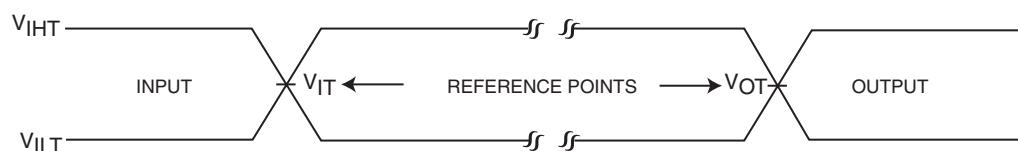


FIGURE 13: SOFTWARE ID EXIT AND RESET

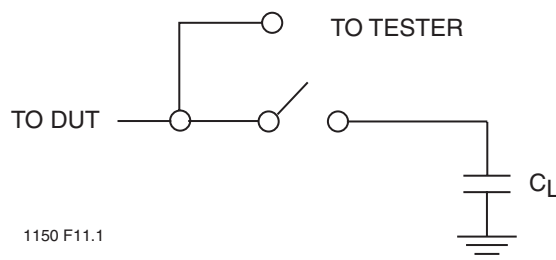


1150 F12.1

AC test inputs are driven at  $V_{IHT}$  ( $0.9 V_{DD}$ ) for a logic "1" and  $V_{ILT}$  ( $0.1 V_{DD}$ ) for a logic "0". Measurement reference points for inputs and outputs are  $V_{IT}$  ( $0.5 V_{DD}$ ) and  $V_{OT}$  ( $0.5 V_{DD}$ ). Input rise and fall times ( $10\% \leftrightarrow 90\%$ ) are  $< 5$  ns.

**Note:**  $V_{IT}$  -  $V_{INPUT}$  Test  
 $V_{OT}$  -  $V_{OUTPUT}$  Test  
 $V_{IHT}$  -  $V_{INPUT}$  HIGH Test  
 $V_{ILT}$  -  $V_{INPUT}$  LOW Test

FIGURE 14: AC INPUT/OUTPUT REFERENCE WAVEFORMS



1150 F11.1

FIGURE 15: A TEST LOAD EXAMPLE



512 Kbit / 1 Mbit / 2 Mbit / 4 Mbit Multi-Purpose Flash  
SST39LF512 / SST39LF010 / SST39LF020 / SST39LF040  
SST39VF512 / SST39VF010 / SST39VF020 / SST39VF040

Data Sheet

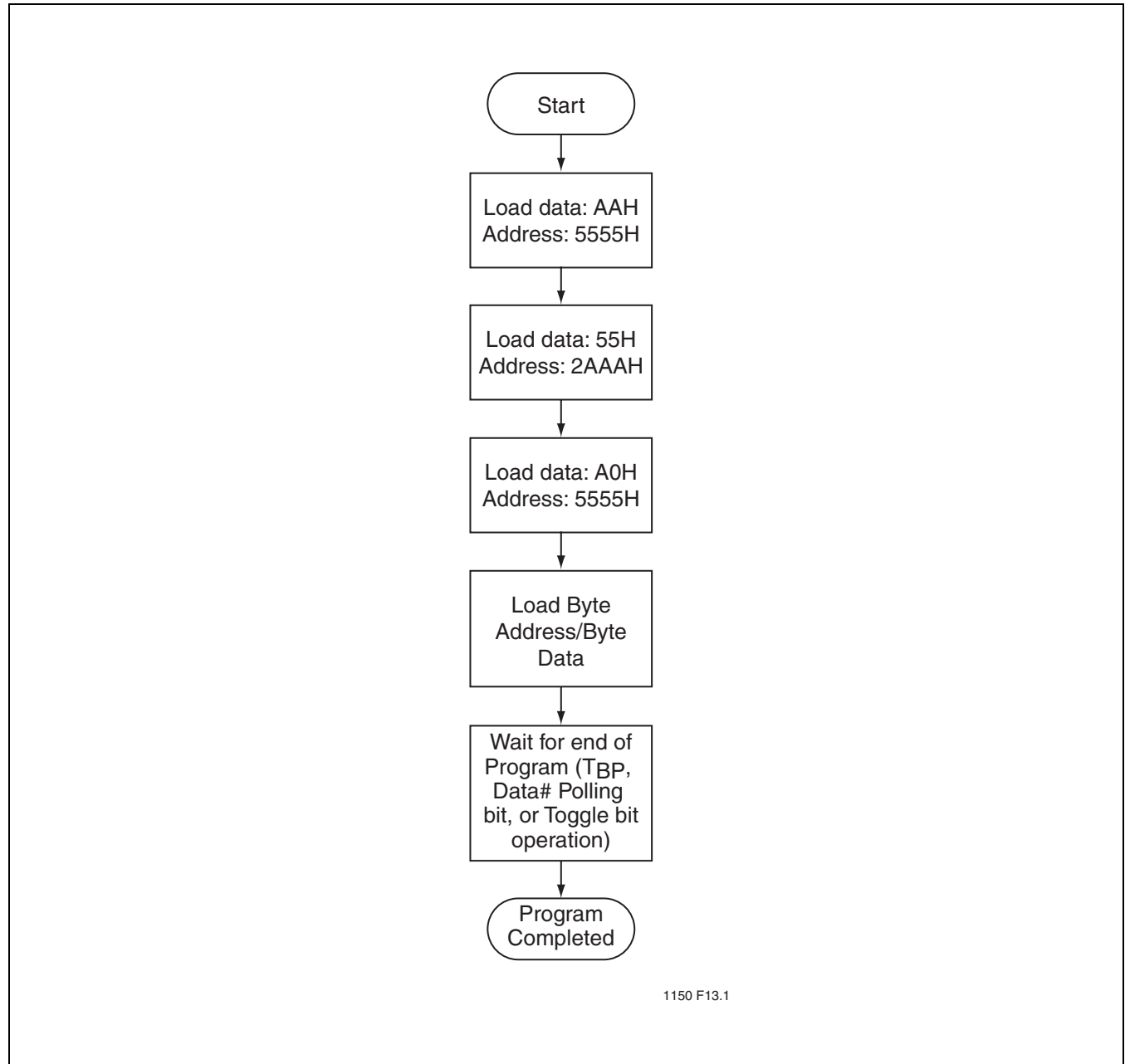
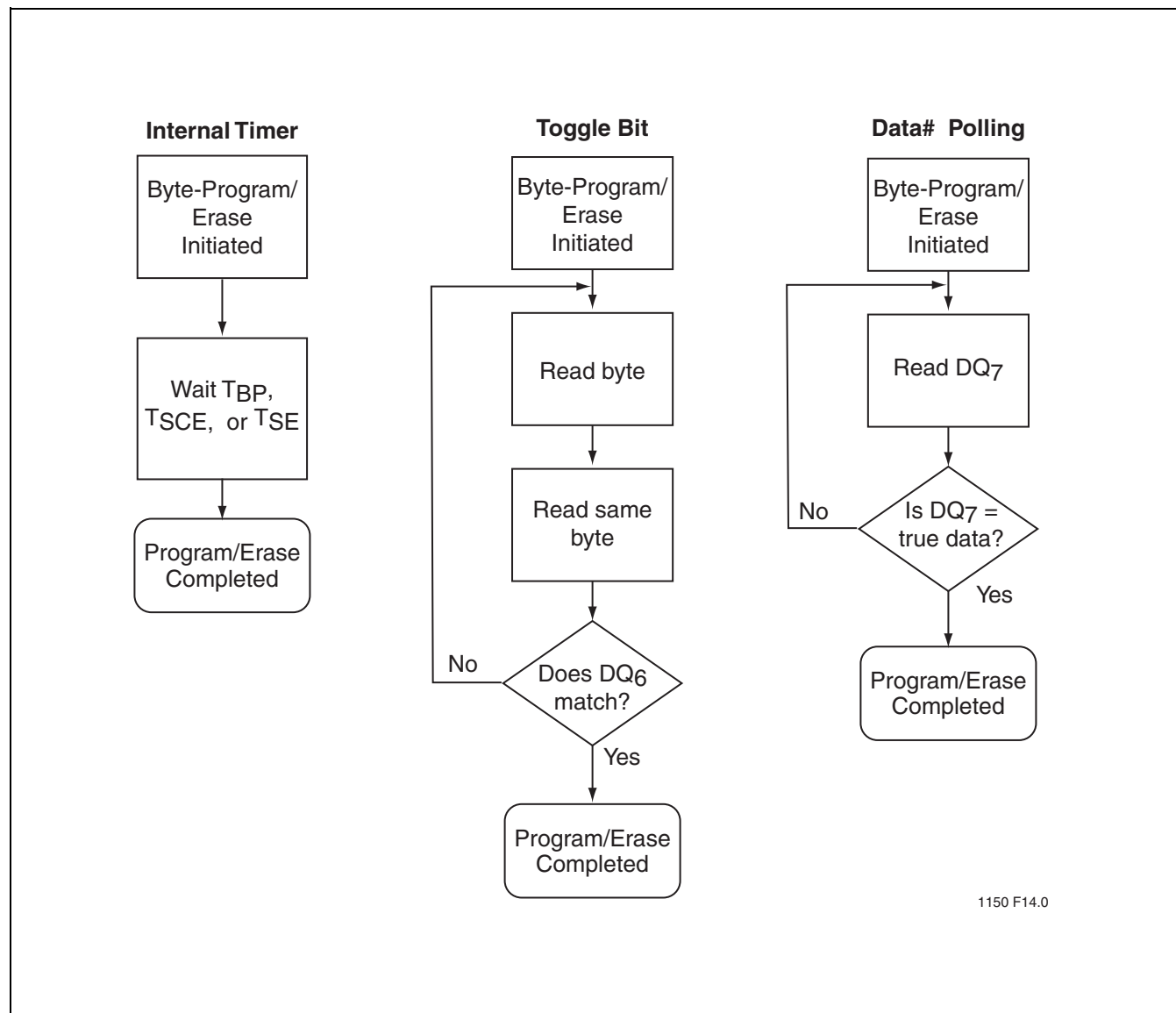


FIGURE 16: BYTE-PROGRAM ALGORITHM





1150 F14.0

FIGURE 17: WAIT OPTIONS

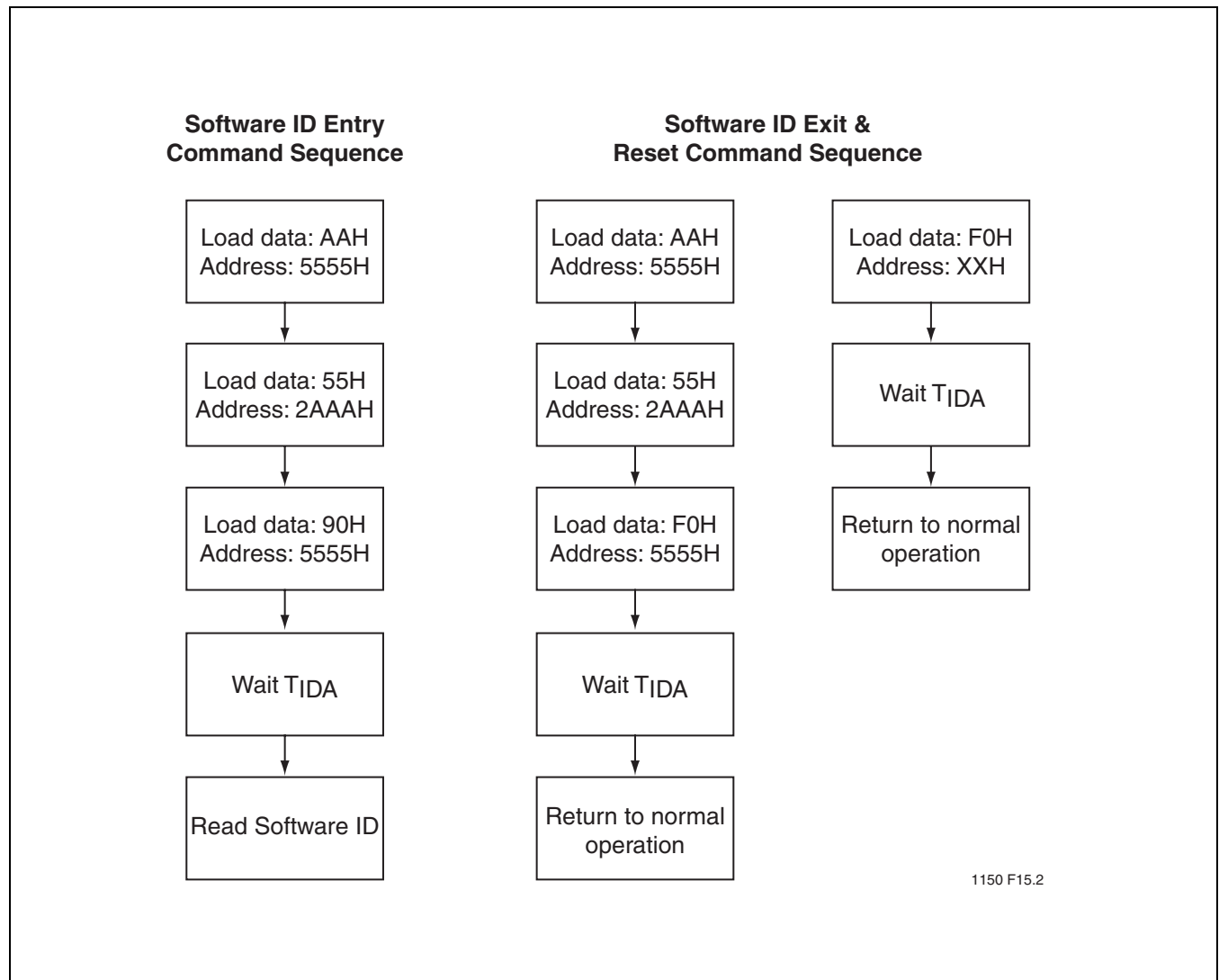


FIGURE 18: SOFTWARE ID COMMAND FLOWCHARTS

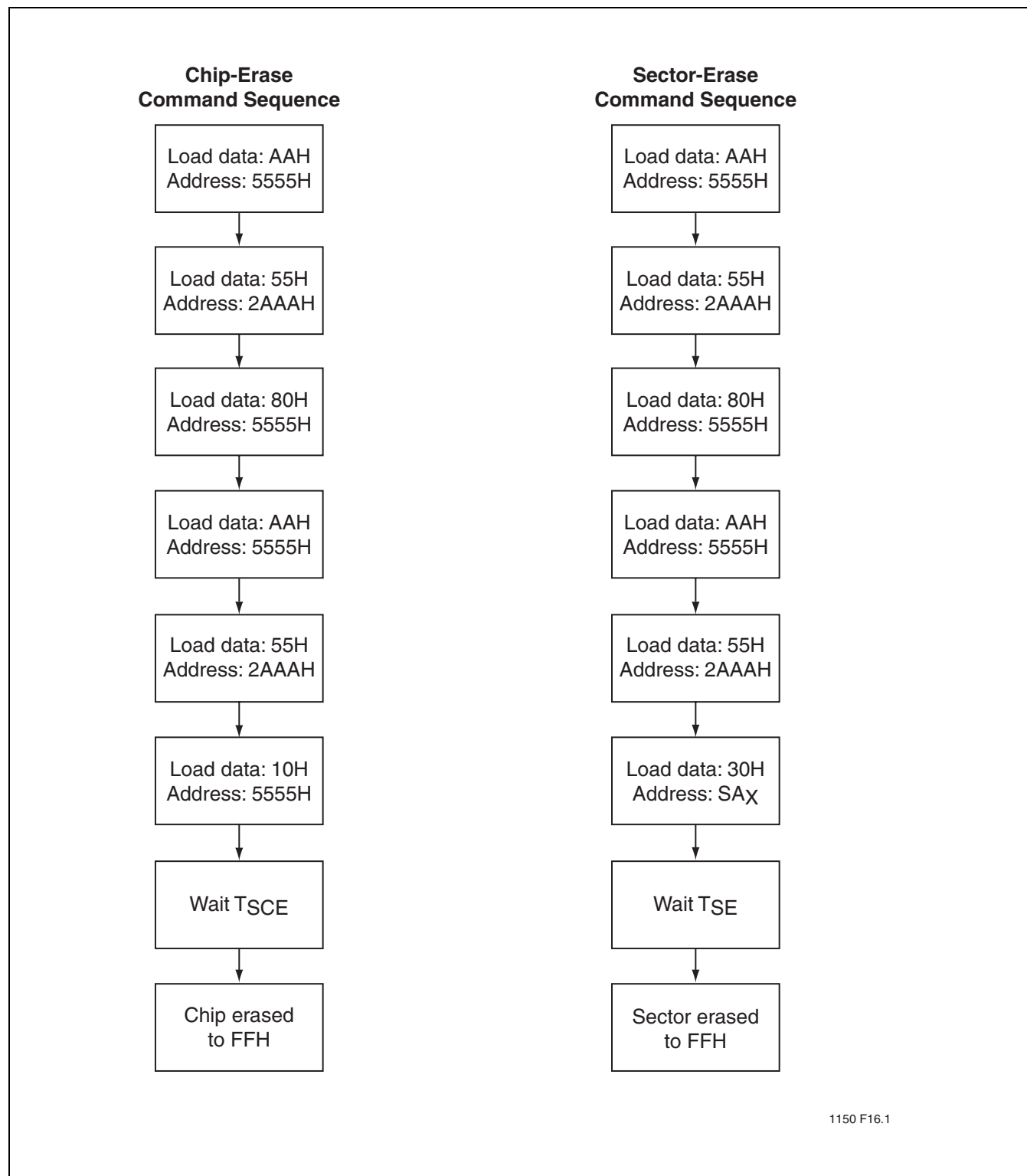


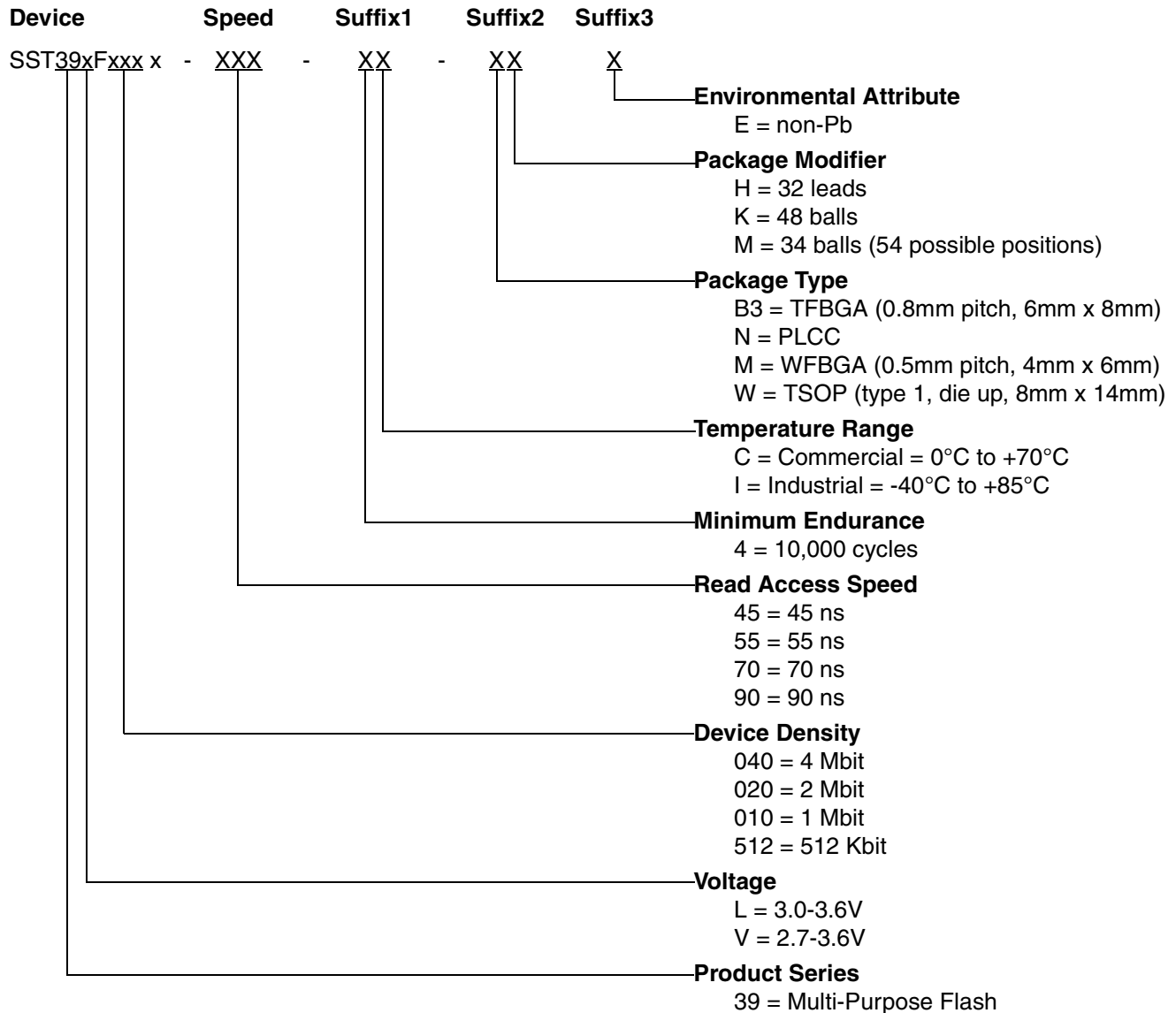
FIGURE 19: ERASE COMMAND SEQUENCE



512 Kbit / 1 Mbit / 2 Mbit / 4 Mbit Multi-Purpose Flash  
SST39LF512 / SST39LF010 / SST39LF020 / SST39LF040  
SST39VF512 / SST39VF010 / SST39VF020 / SST39VF040

Data Sheet

PRODUCT ORDERING INFORMATION



**512 Kbit / 1 Mbit / 2 Mbit / 4 Mbit Multi-Purpose Flash**  
**SST39LF512 / SST39LF010 / SST39LF020 / SST39LF040**  
**SST39VF512 / SST39VF010 / SST39VF020 / SST39VF040**



Data Sheet

**Valid combinations for SST39LF512**

SST39LF512-45-4C-NH    SST39LF512-45-4C-WH

**Valid combinations for SST39VF512**

SST39VF512-70-4C-NH    SST39VF512-70-4C-WH  
 SST39VF512-90-4C-NH<sup>†</sup>    SST39VF512-90-4C-WH<sup>†</sup>  
 SST39VF512-70-4I-NH    SST39VF512-70-4I-WH  
 SST39VF512-90-4I-NH<sup>†</sup>    SST39VF512-90-4I-WH<sup>†</sup>

**Valid combinations for SST39LF010**

SST39LF010-45-4C-NH    SST39LF010-45-4C-WH    SST39LF010-45-4C-B3K    SST39LF010-45-4C-MM

**Valid combinations for SST39VF010**

SST39VF010-70-4C-NH    SST39VF010-70-4C-WH    SST39VF010-70-4C-B3K  
 SST39VF010-90-4C-NH<sup>†</sup>    SST39VF010-90-4C-WH<sup>†</sup>    SST39VF010-90-4C-B3K<sup>†</sup>  
 SST39VF010-70-4I-NH    SST39VF010-70-4I-WH    SST39VF010-70-4I-B3K  
 SST39VF010-90-4I-NH<sup>†</sup>    SST39VF010-90-4I-WH<sup>†</sup>    SST39VF010-90-4I-B3K<sup>†</sup>

**Valid combinations for SST39LF020**

SST39LF020-45-4C-NH    SST39LF020-45-4C-WH    SST39LF020-45-4C-B3K    SST39LF020-45-4C-MM  
 SST39LF020-55-4C-NH    SST39LF020-55-4C-WH

**Valid combinations for SST39VF020**

SST39VF020-70-4C-NH    SST39VF020-70-4C-WH    SST39VF020-70-4C-B3K  
 SST39VF020-90-4C-NH<sup>†</sup>    SST39VF020-90-4C-WH<sup>†</sup>    SST39VF020-90-4C-B3K<sup>†</sup>  
 SST39VF020-70-4I-NH    SST39VF020-70-4I-WH    SST39VF020-70-4I-B3K  
 SST39VF020-90-4I-NH<sup>†</sup>    SST39VF020-90-4I-WH<sup>†</sup>    SST39VF020-90-4I-B3K<sup>†</sup>

**Valid combinations for SST39LF040**

SST39LF040-45-4C-NH    SST39LF040-45-4C-WH  
 SST39LF040-55-4C-NH    SST39LF040-55-4C-WH

**Valid combinations for SST39VF040**

SST39VF040-70-4C-NH    SST39VF040-70-4C-WH  
 SST39VF040-90-4C-NH<sup>†</sup>    SST39VF040-90-4C-WH<sup>†</sup>  
 SST39VF040-70-4I-NH    SST39VF040-70-4I-WH  
 SST39VF040-90-4I-NH<sup>†</sup>    SST39VF040-90-4I-WH<sup>†</sup>

**Note:** Valid combinations are those products in mass production or will be in mass production. Consult your SST sales representative to confirm availability of valid combinations and to determine availability of new combinations.

<sup>†</sup> These 90 ns parts will be phased out and replaced by 70 ns parts in 2004.  
 Customers should use 70 ns parts for new designs and qualifications.

**Non-Pb:** All devices in this data sheet are also offered in non-Pb (no lead added) packages.

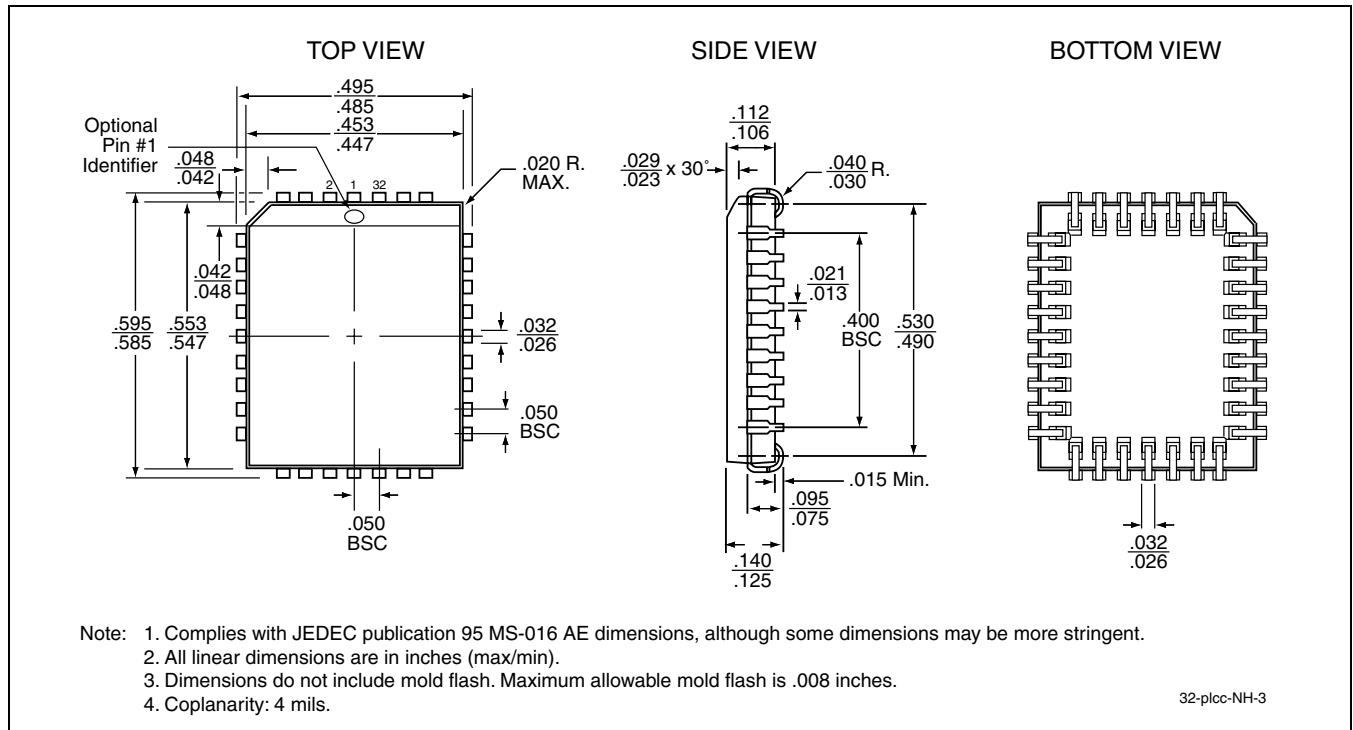
The non-Pb part number is simply the standard part number with the letter "E" added to the end of the package code.  
 The non-Pb package codes corresponding to the packages listed above are NHE, WHE, B3KE, and MME.



512 Kbit / 1 Mbit / 2 Mbit / 4 Mbit Multi-Purpose Flash  
SST39LF512 / SST39LF010 / SST39LF020 / SST39LF040  
SST39VF512 / SST39VF010 / SST39VF020 / SST39VF040

Data Sheet

PACKAGING DIAGRAMS

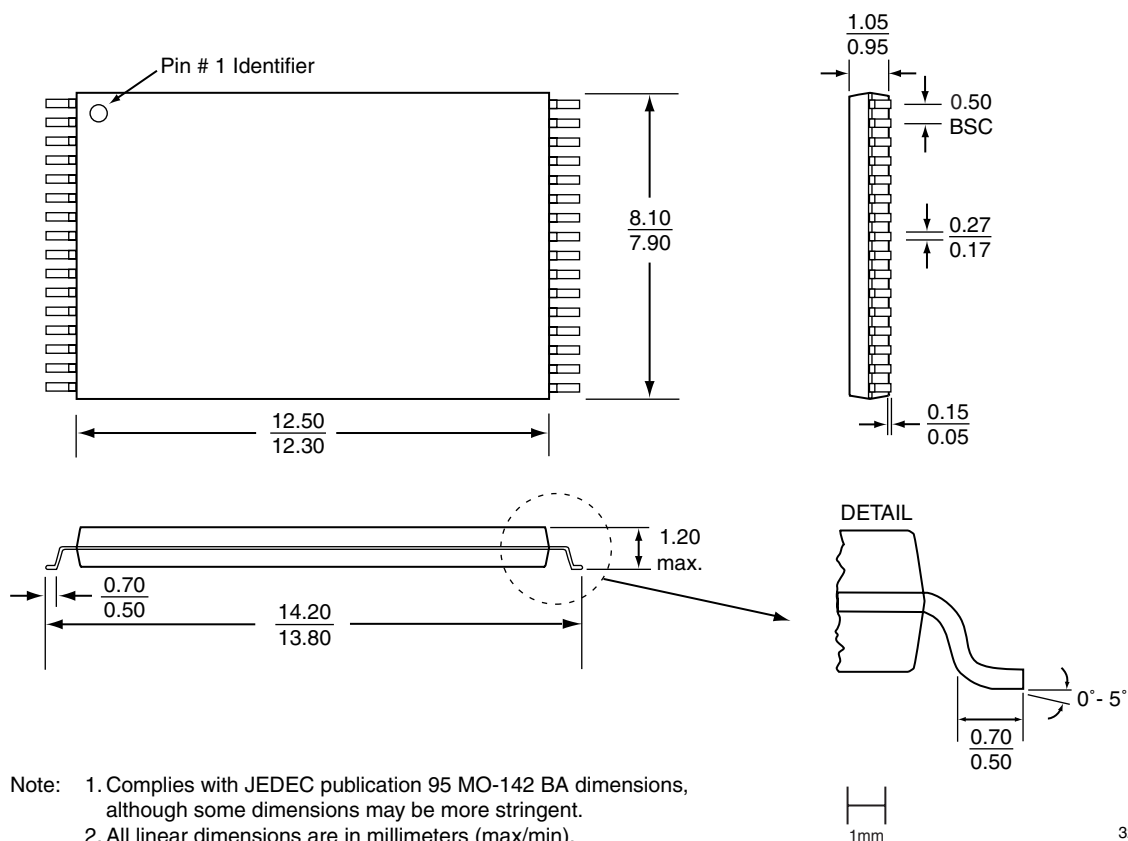


**32-LEAD PLASTIC LEAD CHIP CARRIER (PLCC)**  
**SST PACKAGE CODE: NH**

512 Kbit / 1 Mbit / 2 Mbit / 4 Mbit Multi-Purpose Flash  
SST39LF512 / SST39LF010 / SST39LF020 / SST39LF040  
SST39VF512 / SST39VF010 / SST39VF020 / SST39VF040



Data Sheet



- Note:
1. Complies with JEDEC publication 95 MO-142 BA dimensions, although some dimensions may be more stringent.
  2. All linear dimensions are in millimeters (max/min).
  3. Coplanarity: 0.1 mm
  4. Maximum allowable mold flash is 0.15 mm at the package ends, and 0.25 mm between leads.

32-tsop-WH-7

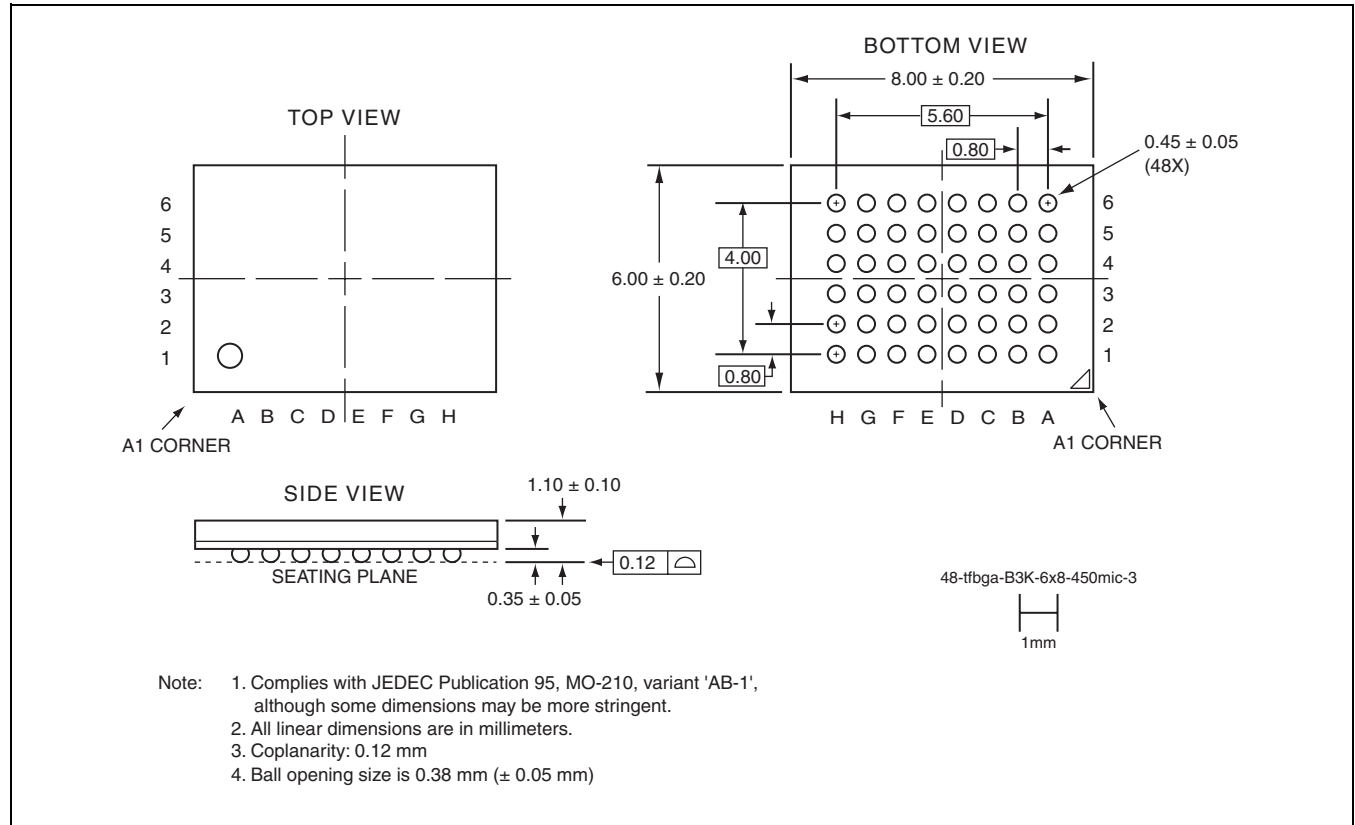
**32-LEAD THIN SMALL OUTLINE PACKAGE (TSOP) 8MM X 14MM**  
**SST PACKAGE CODE: WH**



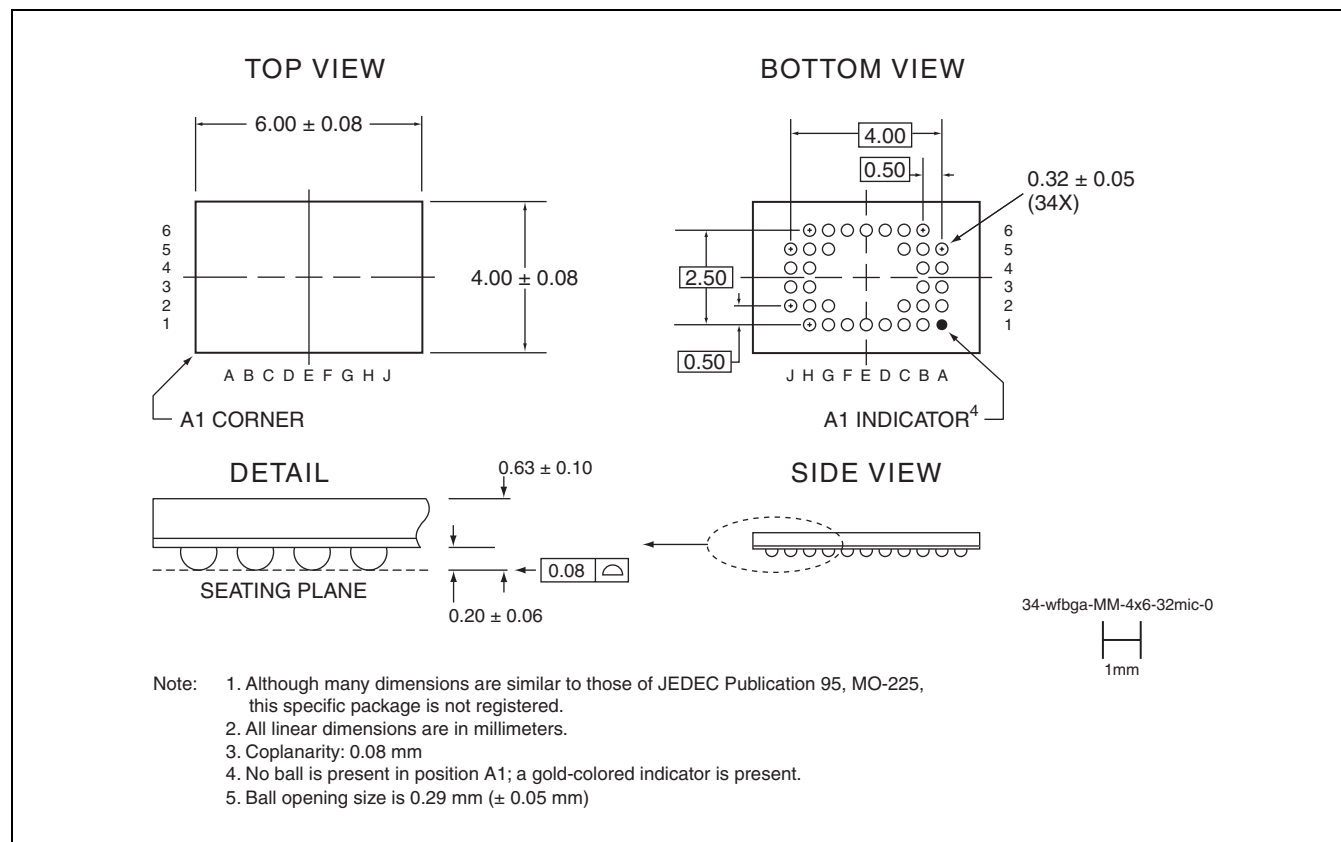


**512 Kbit / 1 Mbit / 2 Mbit / 4 Mbit Multi-Purpose Flash**  
**SST39LF512 / SST39LF010 / SST39LF020 / SST39LF040**  
**SST39VF512 / SST39VF010 / SST39VF020 / SST39VF040**

Data Sheet



**48-BALL THIN-PROFILE, FINE-PITCH BALL GRID ARRAY (TFBGA) 6MM X 8MM**  
**SST PACKAGE CODE: B3K**



**34-BALL VERY-VERY-THIN-PROFILE, FINE-PITCH BALL GRID ARRAY (WFBGA) 4MM X 6MM**  
**SST PACKAGE CODE: MM**

**TABLE 11: REVISION HISTORY**

Number	Description	Date
01	• 2000 Data Book	Feb 2000
02	• Changed speed from 45 ns to 55 ns for the SST39LF020 and SST39LF040	Aug 2000
03	• 2002 Data Book: Reintroduced the 45 ns parts for the SST39LF020 and SST39LF040	Feb 2002
04	• Added the B3K package for the 2 Mbit devices • Added footnote in Table 5 to indicate I <sub>DD</sub> Write is 30 mA max for Erase operations in the industrial temperature range.	Oct 2002
05	• Changes to Table 5 on page 8 – Added footnote for MPF power usage and Typical conditions – Clarified the Test Conditions for Power Supply Current and Read parameters – Clarified I <sub>DD</sub> Write to be Program and Erase – Corrected I <sub>DD</sub> Program and Erase from 20 mA to 30 mA • Part number changes - see page 21 for additional information	Mar 2003
06	• Added new “MM” Micro-Package MPNs for 1M and 2M LF parts- see page 21	Oct 2003