Revision History

Revision	Release Date	Change Description
2.0.0	6/4/10	Reformat of datasheet
3.0.0	4/14/15	Change of specs to match industry standards [ECN 1517-08]
3.0.1	4/12/19	Updated to MaxLinear format. Updated ordering information and moved to end. Added Note 1 to Absolute Maxmimum Ratings and Note 2 to Electrical Characteristics table. Corrected active low pin names. Obsolete SP708R removed.
3.0.2	9/10/19	Corrected typo in $\overline{PFO}$ pin description.

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Specifications

Absolute Maximum Ratings

Important: These are stress rating only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum ratings conditions for extended periods of time may affect reliability.

Table 1: Absolute Maximum Ratings

Parameter	Minimum	Maximum	Units
V_{CC}	-0.3	6.0	V
All Other Inputs(1)	-0.3	V_{CC} + 0.3V	V
Input Current			
VCC		20	mA
GND		20	mA
Output Current			
All Outputs		20	mA
Continuous Power Dissipation			
SO (derate 5.88mW/°C above 70°C)		471	mW
Mini SO (derate 4.10mW/°C above 70°C)		330	mW
Storage temperature	-65	160	°C
Lead temperature (soldering, 10 sec)		300	°C

1. The input voltage limits on PFI, WDI and $\overline{MR}$ can be exceeded if the input current is less than 10mA.

ESD Ratings

Table 2: ESD Ratings

Parameter	Value	Units
HBM (Human Body Model)	2	kV

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Electrical Characteristics

Unless otherwise noted, V_{CC} = 2.7V to 5.5V (SP706R), V_{CC} = 3.15V to 5.5V (SP70xS), V_{CC} = 3.0V to 5.5V (SP70xT), $T_A = T_{MIN}$ to T_{MAX}, typical at 25°C.

Table 3: Electrical Characteristics

Parameter		Test Condition	Minimum	Typical	Maximum	Units
Operating voltage range			1.0		5.5	V
Supply current I_{SUPPLY}		$\overline{MR}$ = V_{CC} or floating, WDI floating, V_{CC} = 3.3V		25	40	µA
		$\overline{MR}$ = V_{CC} or floating, V_{CC} = 5.5V		40	80	
Reset threshold		SP706R	2.55	2.63	2.70	V
		SP706S, SP708S	2.85	2.93	3.00	
		SP706T, SP708T	3.00	3.08	3.15	
Reset threshold hysteresis(2)				20		mV
Reset pulse width t_{RS}(2)			140	200	280	ms
RESET Output Voltage	V_{OH}	$V_{RST(MAX)} < V_{CC} < 3.6V$, I_{SOURCE} = 500µA	0.8 x V_{CC}			V
	V_{OL}	$V_{RST(MAX)} < V_{CC} < 3.6V$, I_{SINK} = 1.2mA			0.3	
	V_{OH}	4.5V < V_{CC} < 5.5V, I_{SOURCE} = 800µA	V_{CC} - 1.5			
	V_{OL}	4.5V < V_{CC} < 5.5V, I_{SINK} = 3.2mA			0.4	
RESET Output Voltage	V_{OH}	$V_{RST(MAX)} < V_{CC} < 3.6V$, I_{SOURCE} = 215µA	V_{CC} - 0.6			V
	V_{OL}	$V_{RST(MAX)} < V_{CC} < 3.6V$, I_{SINK} = 1.2mA			0.3	
	V_{OH}	4.5V < V_{CC} < 5.5V, I_{SOURCE} = 800µA	V_{CC} - 1.5			
	V_{OL}	4.5V < V_{CC} < 5.5V, I_{SINK} = 3.2mA			0.4	
Watchdog timeout period t_{WD}		V_{CC} < 3.6V	1.00	1.60	2.25	s
WDI pulse width t_{WP}(1)		V_{IL} = 0.4V, V_{IH} = 0.8 x V_{CC}	50			ns
WDI Input Threshold	V_{IL}	$V_{RST(MAX)} < V_{CC} < 3.6V$			0.6	V
	V_{IH}	$V_{RST(MAX)} < V_{CC} < 3.6V$	0.7 x V_{CC}			
	V_{IL}	V_{CC} = 5V			0.8	
	V_{IH}	V_{CC} = 5V	3.5			
WDI input current		WDI = 0V or WDI = V_{CC}	-1	0.02	1	µA
$\overline{WDO}$ Output Voltage	V_{IL}	$V_{RST(MAX)} < V_{CC} < 3.6V$, I_{SOURCE} = 500µA	0.8 x V_{CC}			V
	V_{IH}	$V_{RST(MAX)} < V_{CC} < 3.6V$, I_{SINK} = 1.2mA			0.3	
	V_{IL}	4.5V < V_{CC} < 5.5V, I_{SOURCE} = 800µA	V_{CC} - 1.5			
	V_{IH}	4.5V < V_{CC} < 5.5V, I_{SINK} = 3.2mA			0.4	
$\overline{MR}$ Pull-up current		$\overline{MR}$ = 0V, $V_{RST(MAX)} < V_{CC} < 3.6V$	25	70	250	µA
		$\overline{MR}$ = 0V, 4.5V < V_{CC} < 5.5V	100	250	600	
$\overline{MR}$ pulse width t_{MR}		$V_{RST(MAX)} < V_{CC} < 3.6V$	500			ns
		4.5V < V_{CC} < 5.5V	150			

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Table 3: Electrical Characteristics

Parameter		Test Condition	Minimum	Typical	Maximum	Units
$\overline{MR}$ input threshold	V_{IL}	$V_{RST(MAX)} < V_{CC} < 3.6V$			0.6	V
	V_{IH}	$V_{RST(MAX)} < V_{CC} < 3.6V$	0.7 x V_{CC}			
	V_{IL}	$4.5V < V_{CC} < 5.5V$			0.8	
	V_{IH}	$4.5V < V_{CC} < 5.5V$	2.0			
$\overline{MR}$ to reset out delay t_{MD}		$V_{RST(MAX)} < V_{CC} < 3.6V$			750	ns
		$4.5V < V_{CC} < 5.5V$			250	
PFI Input Threshold		V_{CC} = 3.0V - SP706R, PFI falling V_{CC} = 3.3V - SP70xS/T, PFI falling	1.20	1.25	1.30	V
PFI input current		V_{PFI} = 1.36V	-200.00	0.01	200.00	nA
$\overline{PFO}$ Output Voltage	V_{IL}	$V_{RST(MAX)} < V_{CC} < 3.6V$, I_{SOURCE} = 500uA	0.8 x V_{CC}			V
	V_{IH}	$V_{RST(MAX)} < V_{CC} < 3.6V$, I_{SINK} = 1.2mA			0.3	
	V_{IL}	$4.5V < V_{CC} < 5.5V$, I_{SOURCE} = 800µA	V_{CC} - 1.5			
	V_{IH}	$4.5V < V_{CC} < 5.5V$, I_{SINK} = 3.2mA			0.4	

1. WDI minimum rise / fall time is 1us.
2. Applies to both $\overline{RESET}$ in the SP706R, SP706S and SP706T and RESET in the SP708S and SP708T.

Block Diagrams

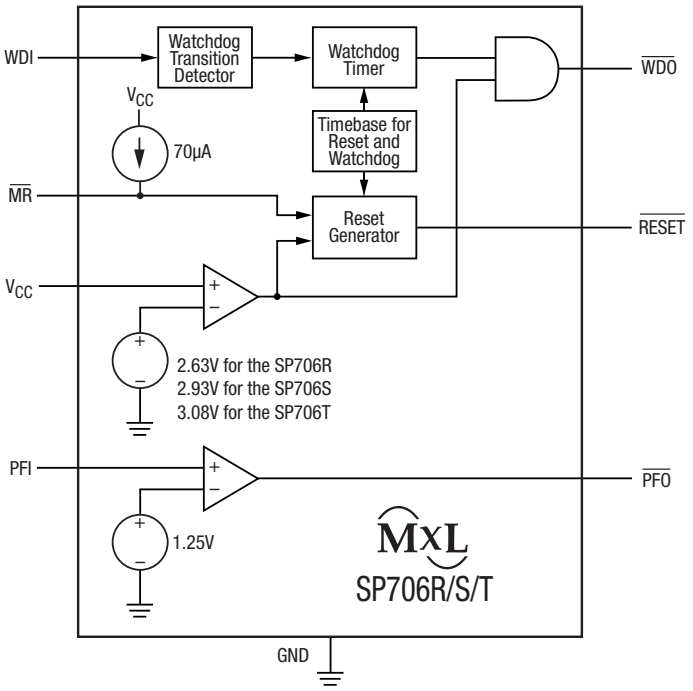

Figure 1: SP706R / SP706S / SP706T Block Diagram

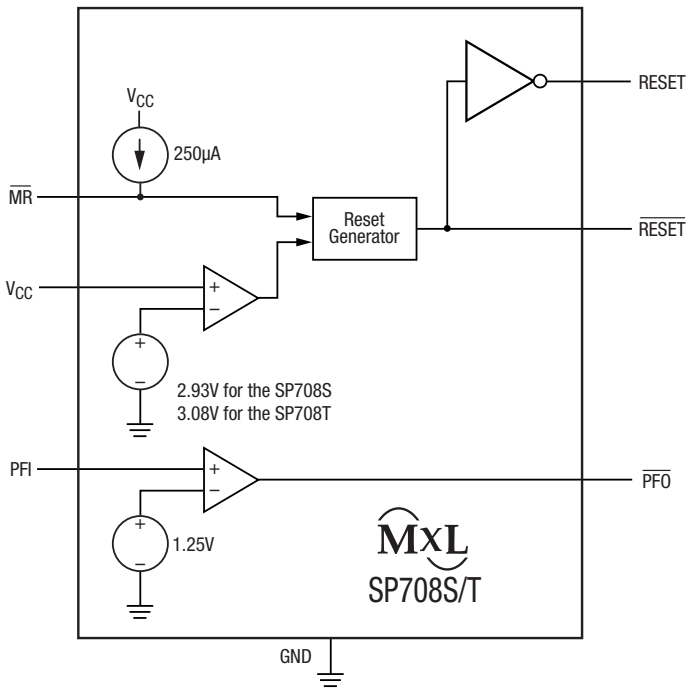

Figure 2: SP708S / SP708T Block Diagram

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Pin Information

Pin Configurations

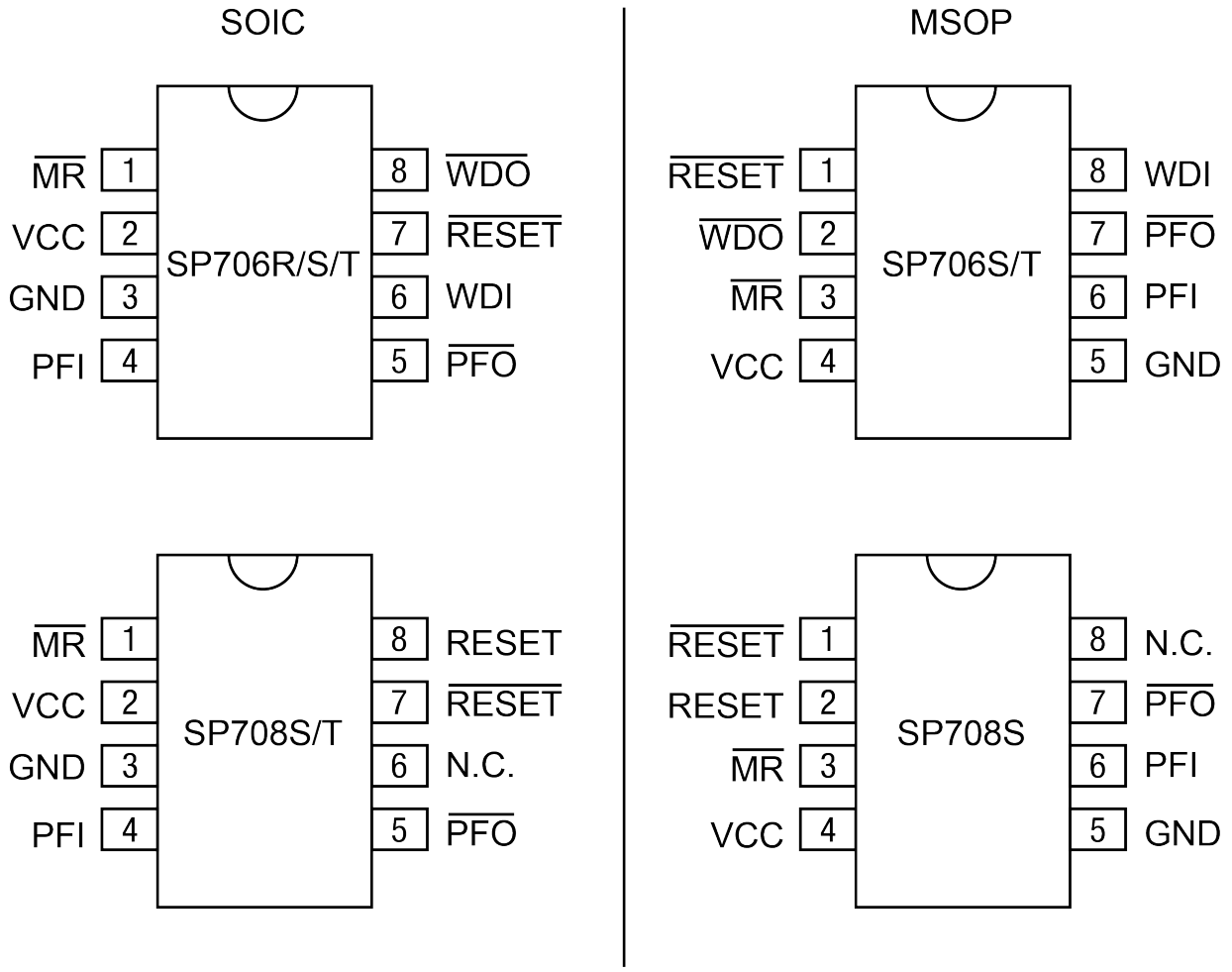

Figure 3: SP706R, SP706S, SP706T, SP708S and SP708T Pin Assignments

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Table 4: Pin Description

Name	Pin Number				Description
	SP706R, SP706S, SP706T		SP708S, SP708T		
	SOIC	MSOP	SOIC	MSOP	
$\overline{MR}$	1	3	1	3	Manual Reset This input triggers a reset pulse when pulled below 0.8V. This active LOW input has an internal 70µA pull-up current. It can be driven from a TTL or CMOS logic line or shorted to ground with a switch.
VCC	2	4	2	4	Voltage input
GND	3	5	3	5	Ground reference for all signals
PFI	4	6	4	6	Power-Fail Input When this voltage monitor input is less than 1.25V, PFO goes LOW. Connect PFI to ground or V_{CC} when not in use.
$\overline{PFO}$	5	7	5	7	Power-Fail Output This output is HIGH until PFI is less than 1.25V.
WDI	6	8	-	-	Watchdog Input If this input remains HIGH or LOW for 1.6s, the internal watchdog timer times out and $\overline{WDO}$ goes LOW. Floating WDI or connecting WDI to a high-impedance tri-state buffer disables the watchdog feature. The internal watchdog timer clears whenever RESET is asserted, WDI is tri-stated, or whenever WDI sees a rising or falling edge.
N.C.	-	-	6	8	No Connect
$\overline{RESET}$	7	1	7	1	Active-LOW RESET Output This output pulses LOW for 200ms when triggered and stays LOW whenever V_{CC} is below the reset threshold. It remains LOW for 200ms after V_{CC} rises above the reset threshold or $\overline{MR}$ goes from LOW to HIGH. A watchdog timeout will not trigger RESET unless $\overline{WDO}$ is connected to $\overline{MR}$.
$\overline{WDO}$	8	2	-	-	Watchdog Output This output pulls LOW when the internal watchdog timer finishes its 1.6s count and does not go HIGH again until the watchdog is cleared. $\overline{WDO}$ also goes LOW during low-line conditions. Whenever V_{CC} is below the reset threshold, $\overline{WDO}$ stays LOW. However, unlike RESET, $\overline{WDO}$ does not have a minimum pulse width. As soon as V_{CC} is above the reset threshold, $\overline{WDO}$ goes HIGH with no delay.
RESET	-	-	8	2	Active-HIGH RESET Output This output is the complement of $\overline{RESET}$. Whenever RESET is HIGH, $\overline{RESET}$ is LOW and vice-versa. Note that the SP708S / SP708T has a reset output only.

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Typical Performance Characteristics

All data taken at V_{CC} = 2.7V to 5.5V (SP706R), V_{CC} = 3.15V to 5.5V (SP70xS), V_{CC} = 3.0V to 5.5V (SP70xT), T_A = 25°C, unless otherwise indicated.

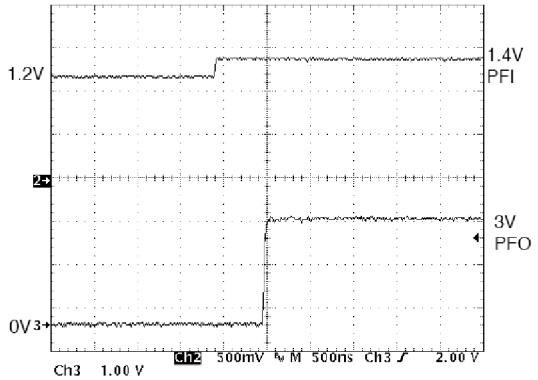

Figure 4: Power-Fail Comparator De-Assertion Response Time

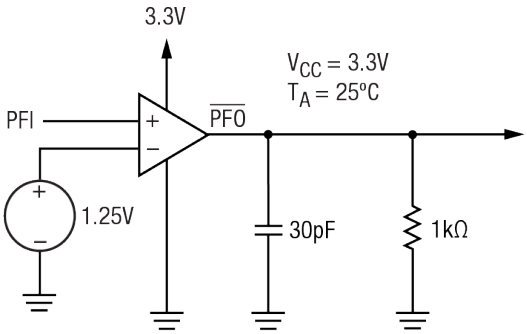

Figure 5: Power-Fail Comparator De-Assertion Response Time Circuit

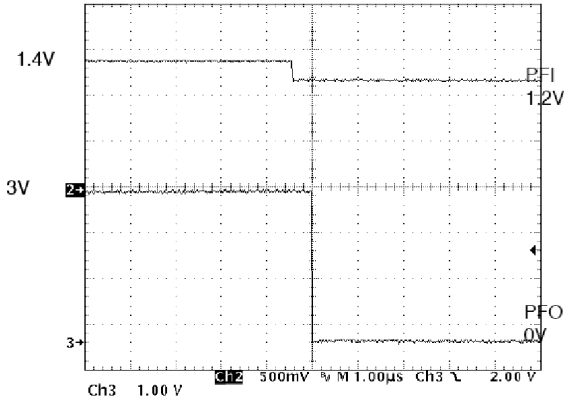

Figure 6: Power-Fail Comparator Assertion Response Time

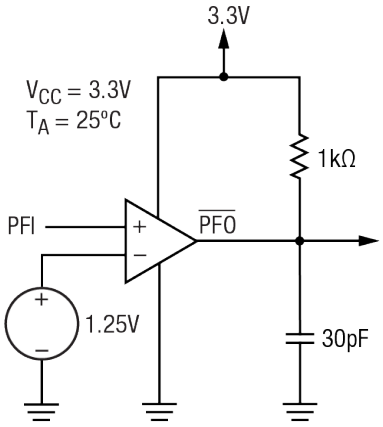

Figure 7: Power-Fail Comparator Assertion Response Time Circuit

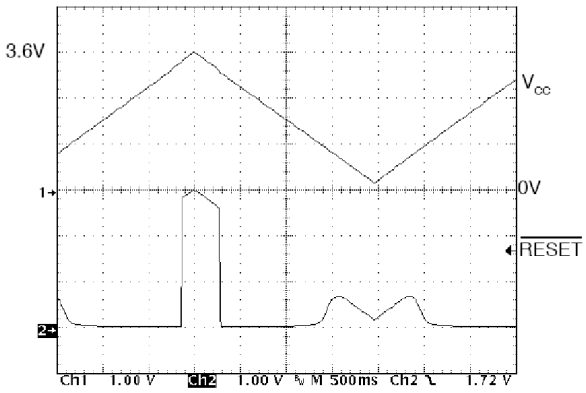

Figure 8: SP706 RESET Output Voltage vs. Supply Voltage

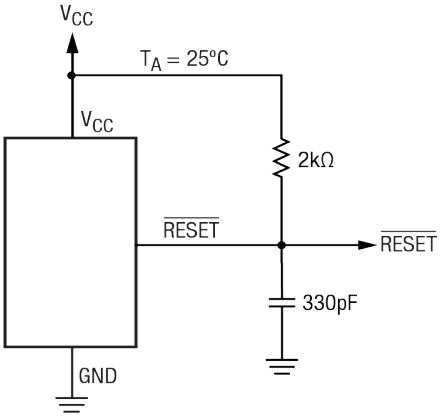

Figure 9: SP706 RESET Output Voltage vs. Supply Voltage Circuit

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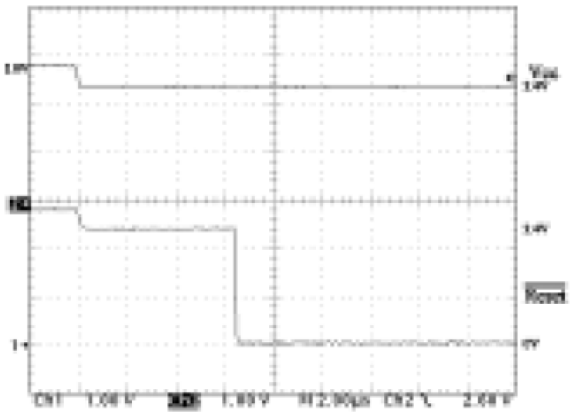

Figure 10: SP706 RESET Response Time

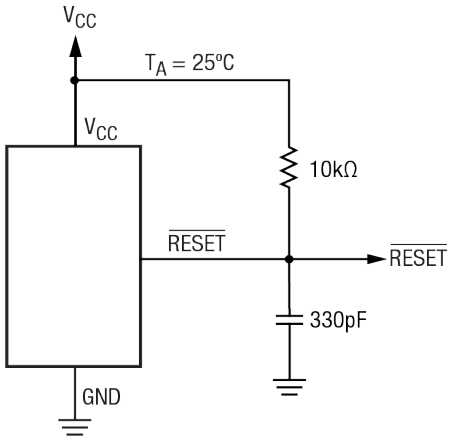

Figure 11: SP706 RESET Response Time Circuit

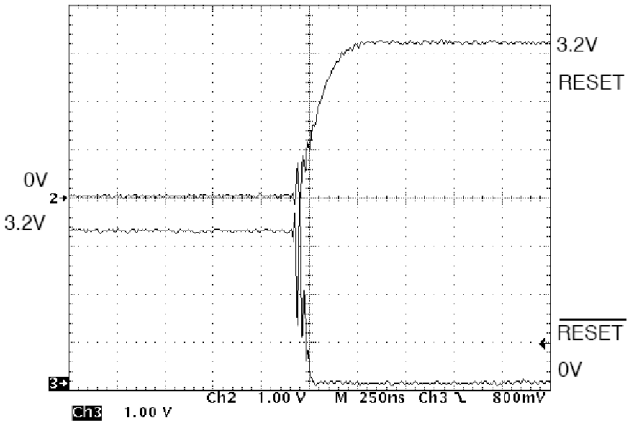

Figure 12: SP708 RESET and RESET Assertion

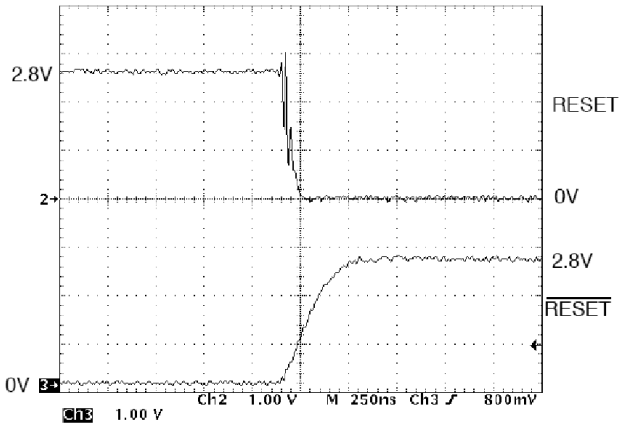

Figure 13: SP708 RESET and RESET De-Assertion

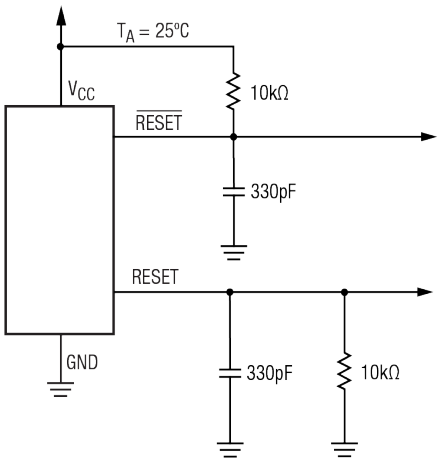

Figure 14: SP708 RESET and RESET Assertion and De-Assertion Circuit

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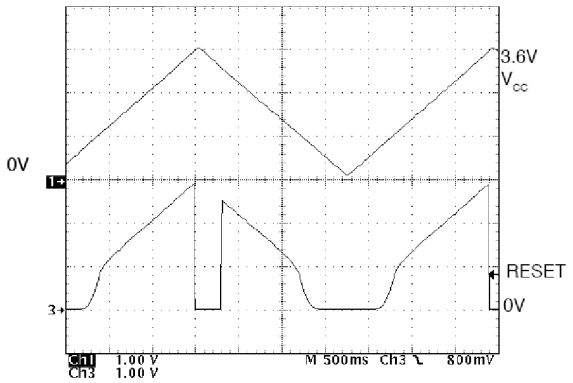

Figure 15: SP708 RESET Output Voltage vs. Supply Voltage

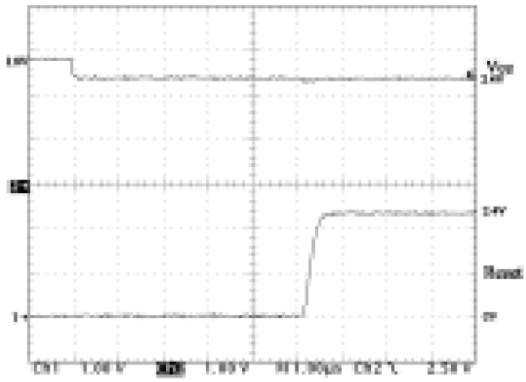

Figure 16: SP708 RESET Response Time

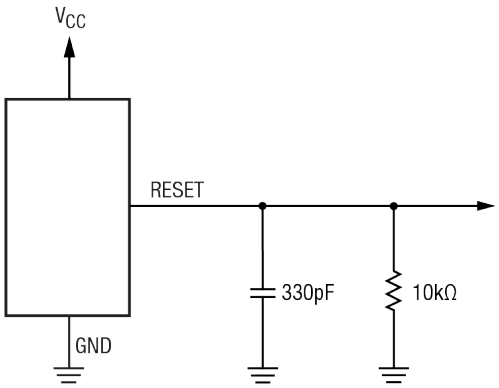

Figure 17: SP708 RESET Output Voltage vs. Supply Voltage and RESET Response Time Circuit

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Features

The SP706R/S/T and SP708S/T series provides four key functions:

1. A reset output during power-up, power-down and brownout conditions.

2. An independent watchdog output that goes LOW if the watchdog input has not been toggled within 1.6 seconds.

3. A 1.25V threshold detector for power-fail warning, low battery detection, or monitoring a power supply other than +3.3V / +3.0V.

4. An active-LOW manual-reset that allows RESET to be triggered by a pushbutton switch.

The SP706S/T devices are the same as the SP708S/T devices except for the active-HIGH RESET substitution of the watchdog timer.

Theory of Operation

The SP706R/S/T - SP708S/T series is a microprocessor (µP) supervisory circuit that monitors the power supplied to digital circuits such as microprocessors, microcontrollers or memory. The series is an ideal solution for portable, battery-powered equipment that requires power supply monitoring. Implementing this series will reduce the number of components and overall complexity. The watchdog functions of this product family will continuously oversee the operational status of a system. The operational features and benefits of the SP706R/S/T - SP708S/T series are described in more detail below.

RESET Output

A microprocessor's reset input starts the µP in a known state. The SP706R/S/T - SP708S/T series asserts reset during power-up and prevents code execution errors during power down or brownout conditions.

On power-up, once V_{CC} reaches 1V, RESET is a guaranteed logic LOW of 0.4V or less. As V_{CC} rises, RESET stays LOW. When V_{CC} rises above the reset threshold, an internal timer releases RESET after 200ms. RESET pulses LOW whenever V_{CC} dips below the reset threshold, such as in a brownout condition. When a brownout condition occurs in the middle of a previously initiated reset pulse, the pulse continues for at least another 140ms. On power down, once V_{CC} falls below the reset threshold, RESET stays LOW and is guaranteed to be 0.4V or less until V_{CC} drops below 1V.

The active-HIGH RESET output is simply the complement of the RESET output and is guaranteed to be valid with V_{CC} down to 1.1V. Some µPs, such as Intel's 80C51, require an active-HIGH reset pulse.

Watchdog Timer

The SP706R/S/T - SP708S/T watchdog circuit monitors the µP's activity. If the µP does not toggle the watchdog input (WDI) within 1.6 seconds and WDI is not tri-stated, $\overline{WDO}$ goes LOW. As long as RESET is asserted or the WDI input is tri-stated, the watchdog timer will stay cleared and will not count. As soon as RESET is released and WDI is driven HIGH or LOW, the timer will start counting. Pulses as short as 50ns can be detected.

Typically, $\overline{WDO}$ will be connected to the non-maskable interrupt input (NMI) of a µP. When V_{CC} drops below the reset threshold, $\overline{WDO}$ will go LOW whether or not the watchdog timer had timed out. Normally this would trigger an NMI but RESET goes LOW simultaneously and thus overrides the NMI.

If WDI is left unconnected, $\overline{WDO}$ can be used as a low-line output. Since floating WDI disables the internal timer, $\overline{WDO}$ goes LOW only when V_{CC} falls below the reset threshold, thus functioning as a low-line output.

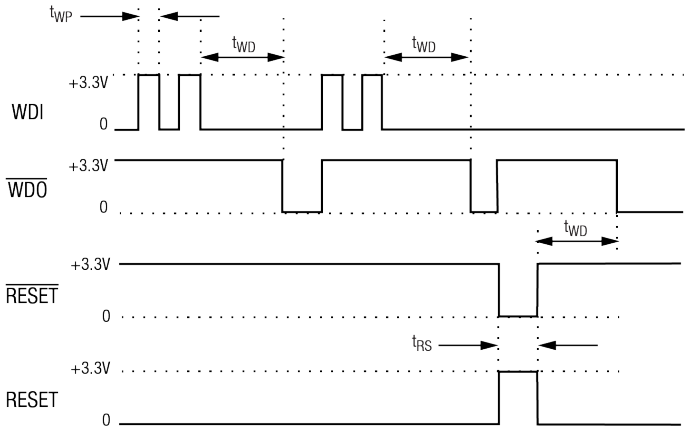

Figure 18: Watchdog Timing Waveforms

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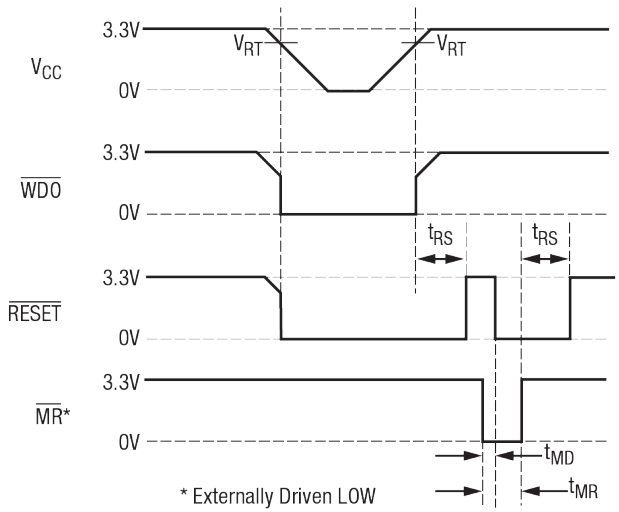

Figure 19: Timing Diagrams with WDI tri-stated

Power-Fail Comparator

The power-fail comparator can be used for various purposes because its output and non inverting input are not internally connected. The inverting input is internally connected to a 1.25V reference.

To build an early-warning circuit for power failure, connect the PFI pin to a voltage divider as shown in Figure 20. Choose the voltage divider ratio so that the voltage at PFI falls below 1.25V just before the +5V regulator drops out. Use PFO to interrupt the µP so it can prepare for an orderly power-down.

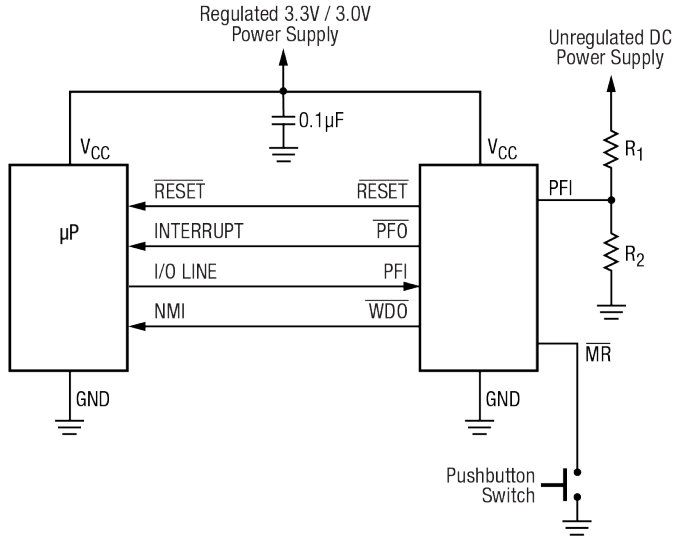

Figure 20: Typical Operating Circuit

Manual Reset

The manual-reset input ($\overline{MR}$) allows RESET to be triggered by a pushbutton switch. The switch is effectively debounced by the 140ms minimum RESET pulse width. $\overline{MR}$ is TTL/CMOS logic compatible, so it can be driven by an external logic line. $\overline{MR}$ can be used to force a watchdog timeout to generate a RESET pulse in the SP706R/S/T-SP708S/T. Simply connect $\overline{WDO}$ to $\overline{MR}$.

Ensuring a Valid Reset Output Down to V_{CC} = 0V

When V_{CC} falls below 1V, the RESET output no longer sinks current, it becomes an open circuit. High-impedance CMOS logic inputs can drift to undetermined voltages if left undriven. If a pull-down resistor is added to the RESET pin, any stray charge or leakage currents will be shunted to ground, holding RESET LOW. The resistor value is not critical. It should be about 100kΩ, large enough not to load RESET and small enough to pull RESET to ground.

Monitoring Voltages Other Than the Unregulated DC Input

Monitor voltages other than the unregulated DC by connecting a voltage divider to PFI and adjusting the ratio appropriately. If required, add hysteresis by connecting a resistor (with a value approximately 10 times the sum of the two resistors in the potential divider network) between PFI and $\overline{PFO}$. A capacitor between PFI and GND will reduce the power-fail circuit's sensitivity to high-frequency noise on the line being monitored. RESET can be used to monitor voltages other than the +3.3V / +3.0V V_{CC} line. Connect $\overline{PFO}$ to $\overline{MR}$ to initiate a RESET pulse when PFI drops below 1.25V. Figure 21 shows the SP706R/S/T - SP708S/T series configured to assert RESET when the +3.3V / 3.0V supply falls below the RESET threshold, or when the +12V supply falls below approximately 11V.

Monitoring a Negative Voltage Supply

The power-fail comparator can also monitor a negative supply rail, shown in Figure 22. When the negative rail is good (a negative voltage of large magnitude), $\overline{PFO}$ is LOW. By adding the resistors and transistor as shown, a HIGH $\overline{PFO}$ triggers RESET. As long as $\overline{PFO}$ remains HIGH, the

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SP706R/S/T - SP708S/T series will keep RESET asserted (where $\overline{RESET}$ = LOW and RESET = HIGH). Note that this circuit's accuracy depends on the PFI threshold tolerance, the V_{CC} line, and the resistors.

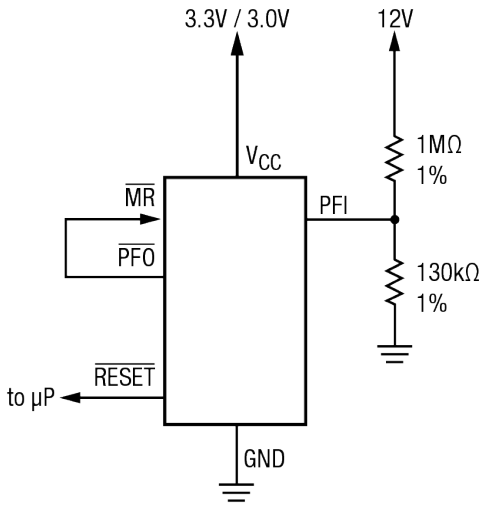
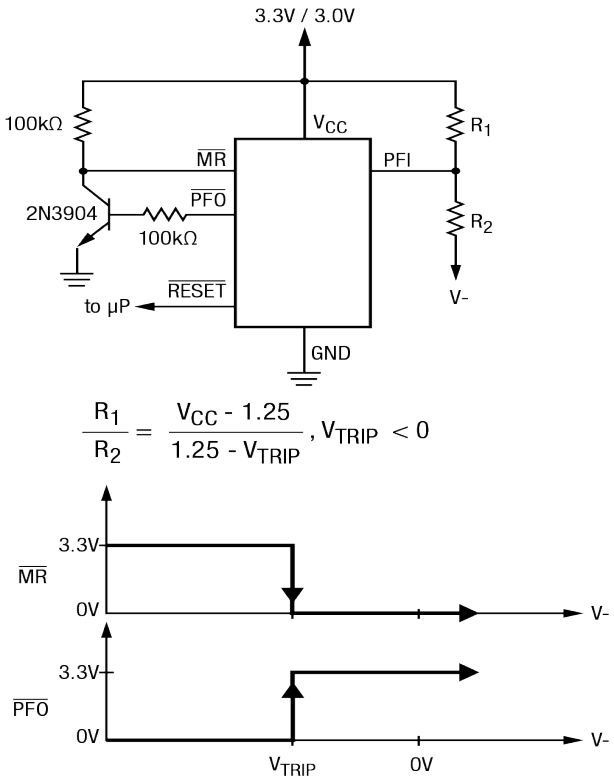


Figure 21: Monitoring +3.3V / +3.0V and +12V Power Supplies



$$\frac{R_1}{R_2} = \frac{V_{CC} - 1.25}{1.25 - V_{TRIP}}, V_{TRIP} < 0$$

Figure 22: Monitoring a Negative Voltage Supply

Interfacing to µPs with Bidirectional Reset Pins

µPs with bidirectional RESET pins, such as the Motorola 68HC11 series, can contend with the SP706/708 RESET output. If, for example, the RESET output is driven HIGH and the µP wants to pull it LOW, indeterminate logic levels may result. To correct this, connect a 4.7kΩ resistor between the RESET output and the µP reset I/O, as shown if Figure 23. Buffer the RESET output to other system components.

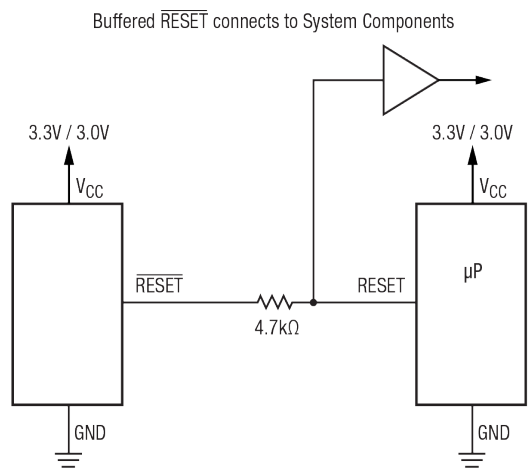


Figure 23: Interfacing to Microprocessors with Bidirectional RESET I/O (SP706)

Negative-Going V_{CC} Transient

While issuing resets to the µP during power-up, power-down and brownout conditions, these supervisors are relatively immune to short duration negative-going V_{CC} transients (glitches). It is usually undesirable to reset the µP when V_{CC} experiences only small glitches.

Figure 24 shows maximum transient duration vs. reset-comparator overdrive, for which reset pulses are not generated. The data was generated using negative-going V_{CC} pulses, starting at 3.3V and ending below the reset threshold by the magnitude indicated (reset comparator overdrive). The graph shows the maximum pulse width a negative-going V_{CC} transient may typically have without causing a reset pulse to be issued. As the amplitude of the transient increases (i.e. goes farther below the reset threshold), the maximum allowable pulse width decreases. Typically, a V_{CC} transient that goes 100mV below the reset threshold and lasts for 40µs or less will not cause a reset pulse to be issued. A 100nF bypass capacitor mounted close to the VCC pin provides additional transient immunity.

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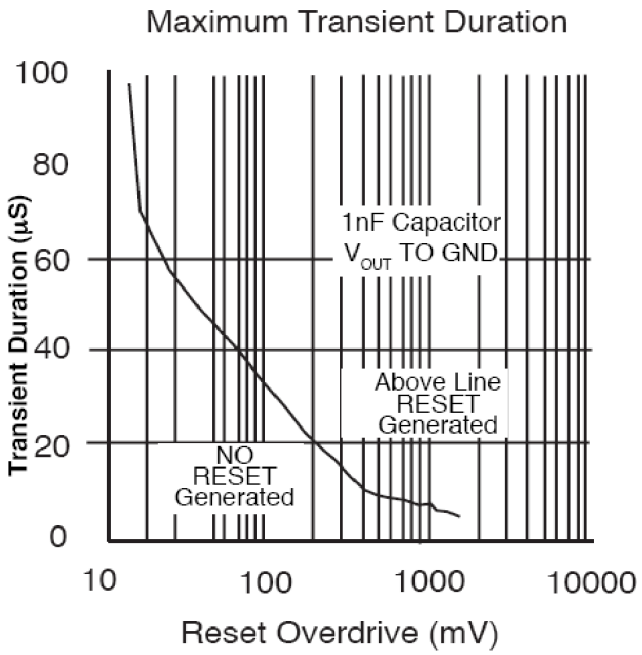

Figure 24: Maximum Transient Duration without Causing a Reset Pulse vs. Reset Comparator Overdrive

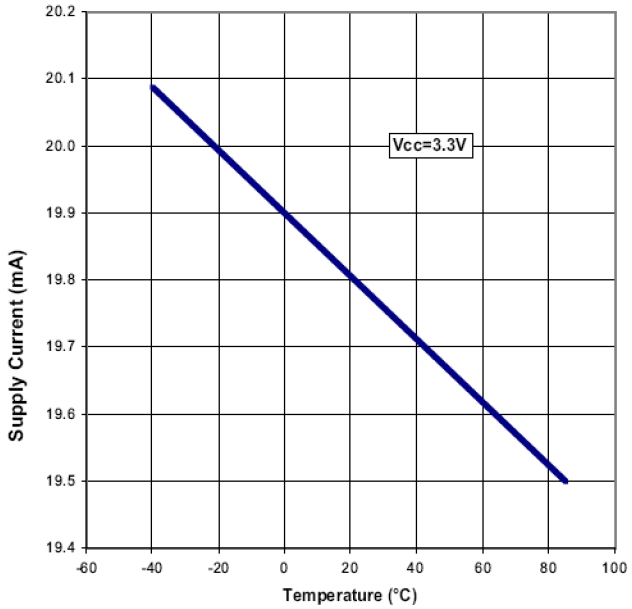

Figure 25: Supply Current vs. Temperature

Applications

The SP706R/S/T - SP708S/T series offers unmatched performance and the lowest power consumption for these industry standard devices. Refer to Figure 25 and Figure 26 for supply current performance characteristics rated against temperature and supply voltages.

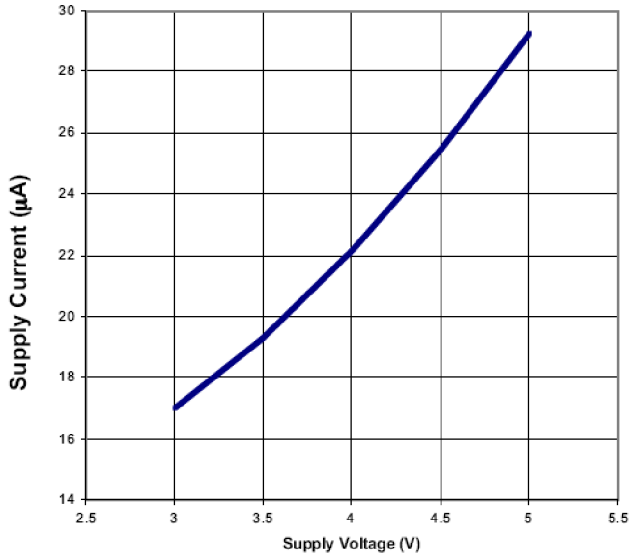

Figure 26: Supply Current vs. Supply Voltage

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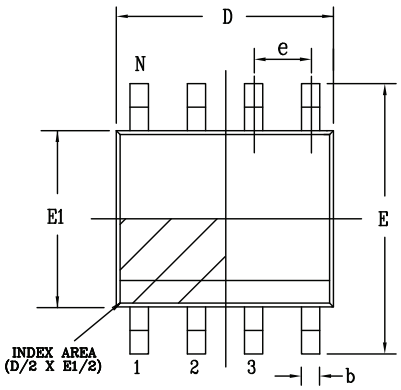
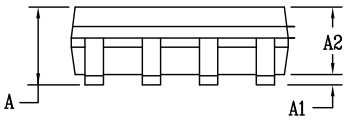
Mechanical Dimensions

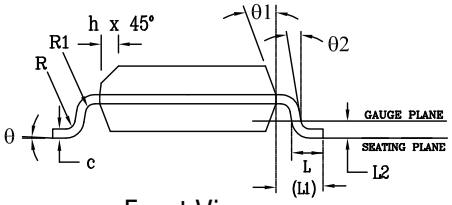
NSOIC8

Top View





Side View



Front View

PACKAGE OUTLINE NSOIC .150" BODY JEDEC MS-012 VARIATION AA						
SYMBOLS	COMMON DIMENSIONS IN MM (Control Unit)			COMMON DIMENSIONS IN INCH (Reference Unit)		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.35	—	1.75	0.053	—	0.069
A1	0.10	—	0.25	0.004	—	0.010
A2	1.25	—	1.65	0.049	—	0.065
b	0.31	—	0.51	0.012	—	0.020
c	0.17	—	0.25	0.007	—	0.010
E	6.00 BSC			0.236 BSC		
E1	3.90 BSC			0.154 BSC		
e	1.27 BSC			0.050 BSC		
h	0.25	—	0.50	0.010	—	0.020
L	0.40	—	1.27	0.016	—	0.050
L1	1.04 REF			0.041 REF		
L2	0.25 BSC			0.010 BSC		
R	0.07	—	—	0.003	—	—
R1	0.07	—	—	0.003	—	—
q	0°	—	8°	0°	—	8°
q1	5°	—	15°	5°	—	15°
q2	0°	—	—	0°	—	—
D	4.90 BSC			0.193 BSC		
N	8					

Drawing No: POD-00000108
Revision: A

Figure 27: Mechanical Dimensions, NSOIC8

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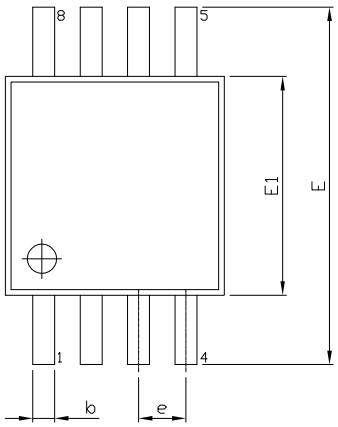
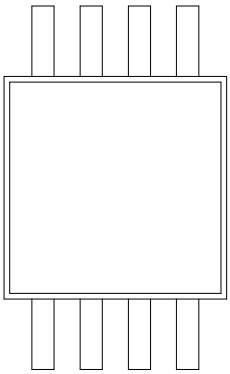
Mechanical Dimensions

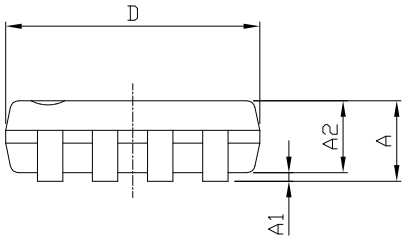
MSOP8

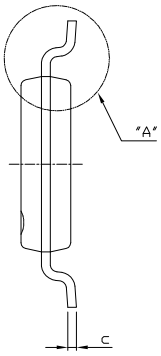


TOP VIEW



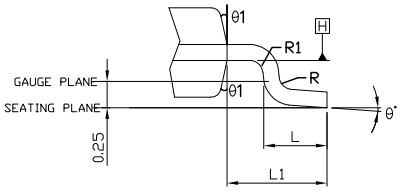
BOTTOM VIEW





DIM / SYMBOL	MIN	NOM	MAX
A	–	–	1.10
A1	0.05	–	0.15
A2	0.75	0.85	0.95
b	0.22	–	0.38
c	0.08		0.23
D	3.00 BSC		
E	4.90 BSC		
E1	3.00 BSC		
e	0.65 BSC		
L	0.40	0.60	0.80
L1	0.95 REF		
θ	0	–	8
θ1	0	–	15
R	0.07	–	–
R1	0.07	–	–

TERMINAL DETAILS



DETAIL A

SIDE VIEW

- ALL DIMENSIONS ARE IN MILLIMETERS, ANGLES ARE IN DEGREES.
- DIMENSIONS AND TOLERANCE PER JEDEC MO-187F.

Drawing No.: POD-00000127

Revision: B

Figure 28: Mechanical Dimensions, MSOP8

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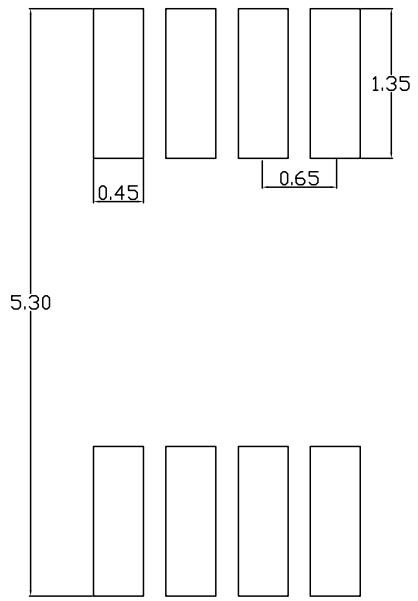
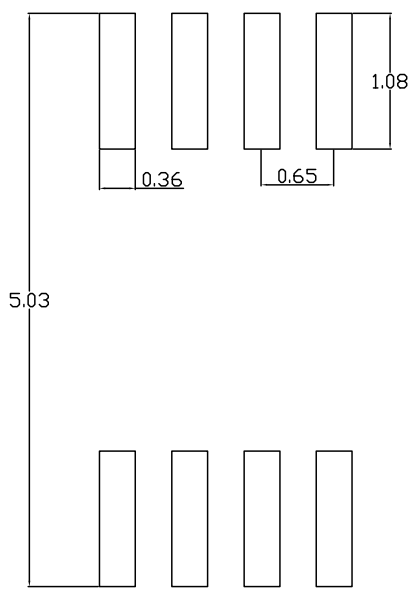
Recommended Land Pattern and Stencil

MSOP8



TYPICAL RECOMMENDED LAND PATTERN



TYPICAL RECOMMENDED STENCIL

Drawing No.: POD-00000127

Revision: B

Figure 29: Recommended Land Pattern and Stencil, MSOP8

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Ordering Information

Table 5: Ordering Information[1]

Ordering Part Number	Operating Temperature Range	Lead-Free	Package	Packaging Method
SP706R/S/T				
SP706RCN-L/TR	0°C ≤ T_A ≤ 70°C	Yes[2]	NSOIC8	Tape and Reel
SP706REN-L/TR	-40°C ≤ T_A ≤ 85°C			
SP706SCU-L/TR	0°C ≤ T_A ≤ 70°C		MSOP8	
SP706SEN-L/TR	-40°C ≤ T_A ≤ 85°C		NSOIC8	
SP706TCN-L/TR	0°C ≤ T_A ≤ 70°C			
SP706TEN-L/TR	-40°C ≤ T_A ≤ 85°C			
SP706TEU-L/TR			MSOP8	
SP708S/T				
SP708SEN-L/TR	-40°C ≤ T_A ≤ 85°C	Yes[2]	NSOIC8	Tape and Reel
SP708TEN-L/TR				

1. Refer to www.maxlinearar.com/SP706R, www.maxlinearar.com/SP706S, www.maxlinearar.com/SP706T, www.maxlinearar.com/SP708S, and www.maxlinearar.com/SP708T for most up-to-date Ordering Information.

2. Visit www.maxlinear.com for additional information on Environmental Rating.

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