ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

Supply Input Voltage (V_{IN}) .... -2V to 7V
Output Voltage (V_{OUT})........................... -0.6 to (V_{IN} +1V)
Enable Input Voltage (V_{EN}) .... -2V to 7V
Storage Temperature........................... -65°C to +150°C
Power Dissipation .... Internally Limited[1]
Lead Temperature (Soldering, 5 sec) .... 260°C

OPERATING RATINGS

Input Voltage Range V_{IN}............................ +2.5V to +6V
Enable Input Voltage (V_{EN}) .... 0V to 6V
Junction Temperature Range ....-40°C to 125°C
Thermal Resistance ....
SOT-23-5 (θ_{JA}) ....191°C/W
DFN-8 (θ_{JA}) .... 59°C/W

Note 1: Maximum power dissipation can be calculated using the formula: $PD = (T_J(max) - T_A) / \theta_{JA}$, where $T_J(max)$ is the junction temperature, T_A is the ambient temperature and θ_{JA} is the junction-to-ambient thermal resistance. θ_{JC} is 6°C/W for this package. Exceeding the maximum allowable power dissipation will result in excessive die temperature and the regulator will go into thermal shutdown mode.

ELECTRICAL SPECIFICATIONS

Specifications with standard type are for an Operating Junction Temperature of T_J = 25°C only; limits applying over the full Operating Junction Temperature range are denoted by a "•". Minimum and Maximum limits are guaranteed through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise indicated, V_{IN} = (V_{OUT} + 1V), V_{OUT} = 5V for Adjustable version, C_{IN} = 1.0µF, C_{OUT} = 1.0µF and I_L = 100µA, T_J= 25°C.

Parameter	Min.	Typ.	Max.	Units		Conditions
Output Voltage Accuracy, (V_O)	-2		2	%		Variation from specified V_{OUT}
	-3		3		•	
Reference Voltage	1.213	1.250	1.287	V	•	Adjustable version only
Output Voltage Temperature Coefficient[2] ($\Delta V_O/\Delta T$)		60		ppm/°C		
Minimum Supply Voltage		2.50 2.55 2.70 3.00	2.70 2.80 2.95 3.50	V V V V		I_L = 100µA I_L = 50mA I_L = 100mA I_C = 200mA
Line Regulation, ($\Delta V_O/V_{IN}$)		0.03	0.2	%/V	•	V_{IN} = (V_{OUT} + 1V) to 6V
Load Regulation[3] ($\Delta V_O/V_O$)		0.07 0.14	0.25 0.50	% %	• •	I_L = 0.1mA to 100mA, SP6200 I_L = 0.1mA to 200mA, SP6201
SP6200-1.5V & 1.8 Load Reg. SP6201-1.5V & 1.8 Load Reg.		0.3 0.3	1 1	% %		I_L = 0.1mA to 100mA, V_{IN} = 2.95V I_L = 0.1mA to 200mA, V_{IN} = 3.5V
Dropout Voltage[4] ($V_{IN} - V_O$) (Not applicable to voltage options below 2.7V)		0.2	4	mV		I_L = 100µA
			7		•	
		70	120	mV		I_L = 50mA
			160		•	
		160	250	mV		I_L = 100mA
			300		•	
		320	400	mV		I_L = 200mA, SP6201 Only
			500		•	
Shutdown Quiescent Current (I_{GND})		0.01	1	µA	•	$V_{EN} \geq 0.4V$
Ground Pin Current[5] (I_{GND})		28	40	µA		$V_{EN} \geq 2.0V$, I_L = 100 µA
			45		•	
		110	200	µA		$V_{EN} \geq 2.0V$, I_L = 100 mA, SP6200 only (for 1.5 & 1.8, V_{IN} = 2.95)
			250		•	
		200	400	µA		$V_{EN} \geq 2.0V$, I_L = 200mA, SP6201 Only (for 1.5 & 1.8, V_{IN} = 3.5)
			500		•	
Power Supply Rejection Ratio, (PSRR)		78		dB		Frequency = 100Hz, I_L = 10mA
		40				Frequency = 400Hz, I_L = 10mA
Current Limit, (I_{CL})	100	140	200	mA	•	SP6200

Parameter	Min.	Typ.	Max.	Units		Conditions
	300	420	600		•	SP6201
Thermal Limit		162		°C		Turns On
		147				Turns Off
Thermal Regulation[6] ($\Delta V_O/\Delta P_D$)		0.05		%/W		
Output Noise, (e_{NO})		150		µVrms		I_L = 50mA, C_L = 1µF 0.1µF from V_{OUT} to Adj. 10Hz to 100kHz
ENABLE INPUT						
Enable Input Logic-Low Voltage, (V_{IL})			0.4	V	•	Regulator Shutdown
Enable Input Logic-High Voltage, (V_{IH})	1.6			V	•	Regulator Enabled
Enable Input Current, (I_{IL}), (I_{IH})		0.01	1	µA	•	V_{IL} < 0.4V
		0.01	1	µA	•	V_{IH} > 2.0V
Reset Not Output	-2	-4	-6	%		Threshold

Note 2: Output voltage temperature coefficient is defined as the worst case voltage change divided by the totaltemperature range.
Note 3: Load Regulation is measured at constant junction temperature using low duty cycle pulse testing. Parts are tested for load regulation in the load range; from 0.1mA to 100mA, SP6200; from 0.1mA to 200mA, SP6201. Changes in output voltage due to heating effects are covered by the thermal regulation specification. Not applicable to output voltages less than 2.5V.
Note 4: Dropout Voltage is defined as the input to output differential at which the output voltage drops 2% below its nominal value measured at 1V differential. Not applicable to output voltages less than 2.7V.
Note 5: Ground pin current is the regulator quiescent current. The total current drawn from the supply is the sum of the load current plus the ground pin current.
Note 6: Thermal regulation is defined as the change in output voltage at a time "t" after a change in power dissipation is applied, excluding load or line regulation effects. Specifications are for a 100mA load pulse at V_{IN} = 6V for t = 10ms.

BLOCK DIAGRAMS

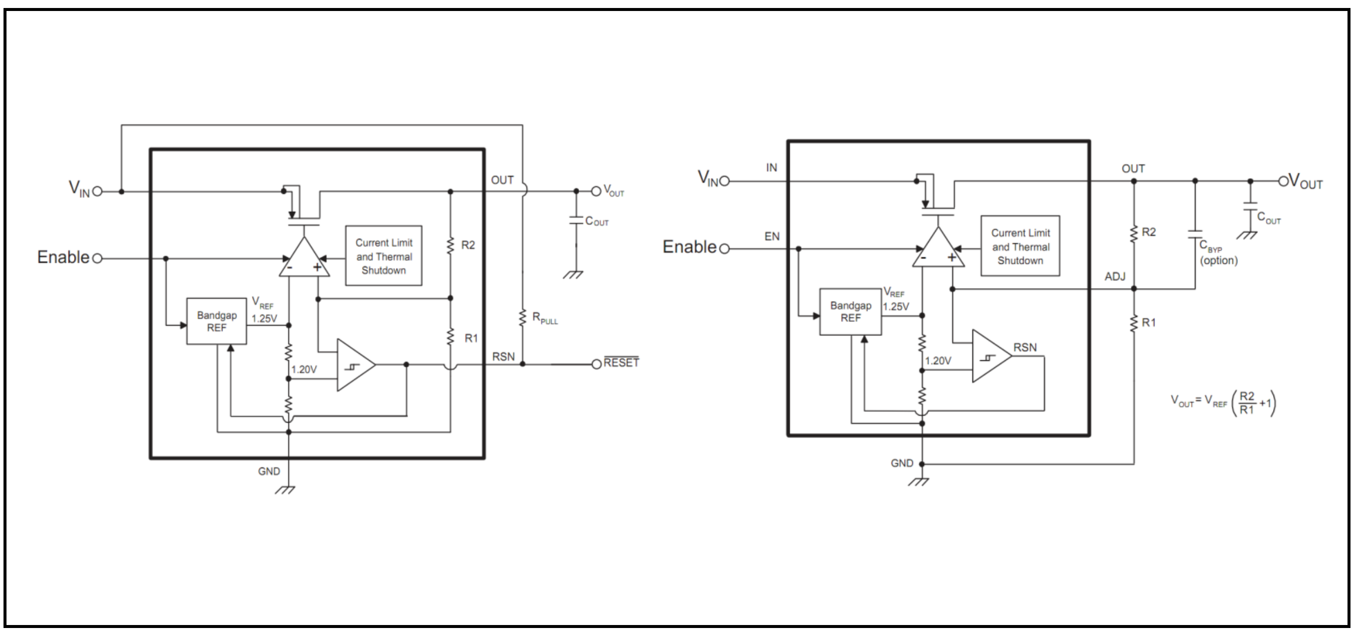


Fig. 2: Fixed Voltage and Adjustable Regulators

Adjustable versions are obsolete

PIN ASSIGNMENT

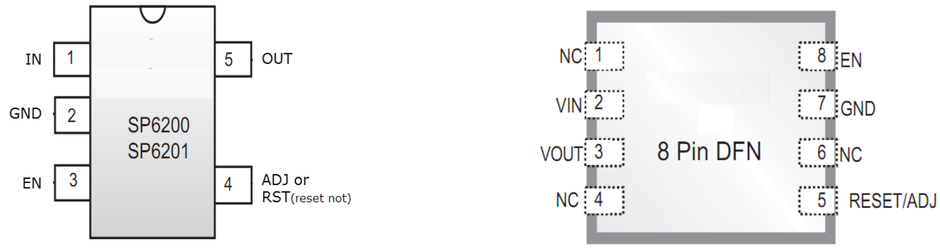


Fig. 3: SP6200 / SP6201 Pin Assignment

DFN-8 version is obsolete

PIN DESCRIPTION

SOT 23-5

Name	SOT-23-5	Description
IN	1	Power Supply Input
GND	2	Ground Terminal
EN	3	Enable/Shutdown Input – CMOS or TTL compatible Input - Logic high = enable - Logic low = shutdown
RST(Reset not)/ADJ	4	Reset/Power Good - Fixed voltage option: Open Drain indicating that V_{OUT} is good. Adjustable Input – Adjustable voltage option: Adjustable regulator feedback input. Connect to a resistive voltage-Divider network.
OUT	5	Regulator Output Voltage

8 PIN DFN **DFN-8 version is obsolete**

Name	DFN-8	Description
NC	1	No Connect
V_{IN}	2	Power Supply Input
V_{OUT}	3	Regulator Output Voltage
NC	4	No Connect
RESET/ADJ	5	Reset/Power Good - Fixed voltage option: Open Drain indicating that V_{OUT} is good. Adjustable Input – Adjustable voltage option: Adjustable regulator feedback input. Connect to a resistive voltage-Divider network.
NC	6	No Connect
NC	7	No Connect
EN	8	Enable/Shutdown Input – CMOS or TTL compatible Input - Logic high = enable Logic low = shutdown

ORDERING INFORMATION[(1), (2)]

Part Number	Temperature Range	Package	Packing Method	Voltage Option	Lead Free[(3)]
SP6201EM5-L-1-8/TR	-40°C ≤ T_J ≤ +125°C	SOT-23-5	Tape & Reel	1.8V	Yes
SP6201EM5-L-3-0/TR	-40°C ≤ T_J ≤ +125°C	SOT-23-5	Tape & Reel	3.0V	Yes
SP6201EM5-L-3-3/TR	-40°C ≤ T_J ≤ +125°C	SOT-23-5	Tape & Reel	3.3V	Yes
SP6201EM5-L-5-0/TR	-40°C ≤ T_J ≤ +125°C	SOT-23-5	Tape & Reel	5.0V	Yes

NOTES:

1. Refer to www.maxlinear.com/SP6201 for most up-to-date Ordering Information.
2. SP6200 (100mA), SP6201 adjustable versions and SP6201 DFN-8 versions are obsolete.
3. Visit www.maxlinear.com for additional information on Environmental Rating.

TYPICAL PERFORMANCE CHARACTERISTICS

All data taken at 25°C, V_{IN} = 5.5V, I_O = 0.1mA, C_{IN} = C_{OUT} = 1µF, unless otherwise specified - Schematic and BOM from Application Information section of this datasheet.

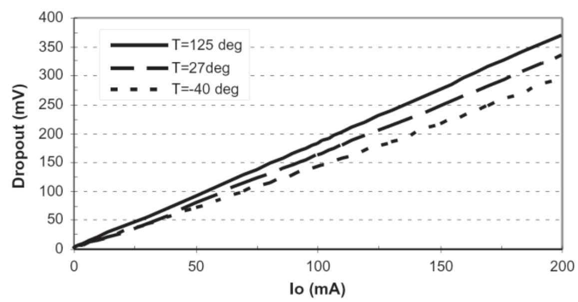


Fig. 4: Dropout vs. Io (SP6201 fixed 3.0V)

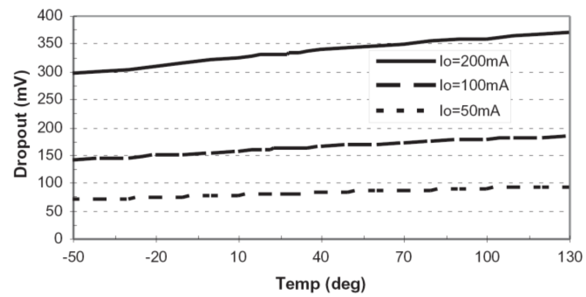


Fig. 5: Dropout vs. Temp (SP6201 fixed 3.0V)

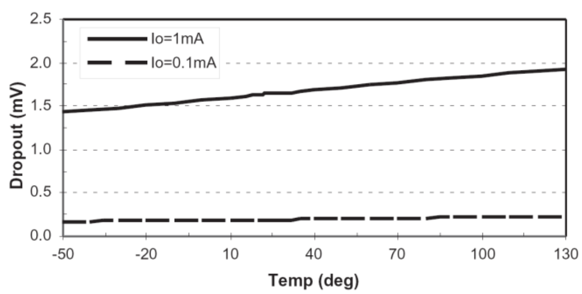


Fig. 6: Dropout vs. Temp (SP6201 fixed 3.0V)

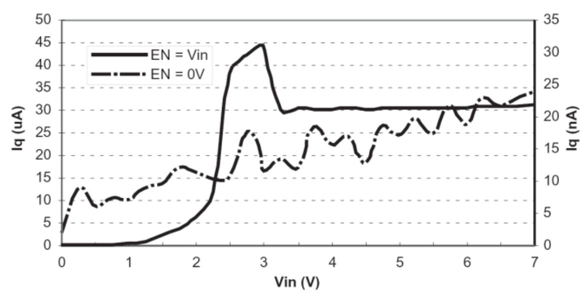


Fig. 7: Iq vs. Vin (fixed 3.0V, I_O=0µA)

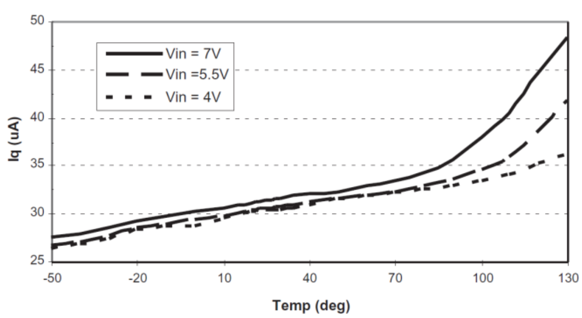


Fig. 8: I_q vs. Temp (SP6201 fixed 3.0V, EN=Vin, I_O=0uA)

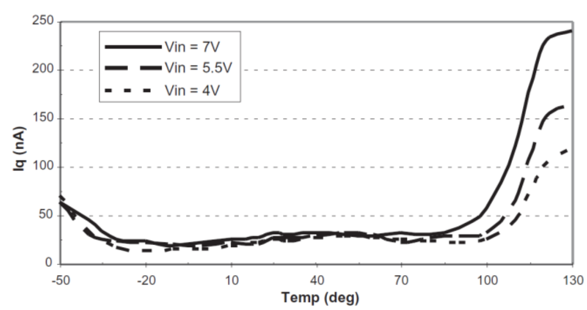


Fig. 9: I_q vs. Temp (SP6201 fixed 3.0V, EN=0V, I_O=0uA)

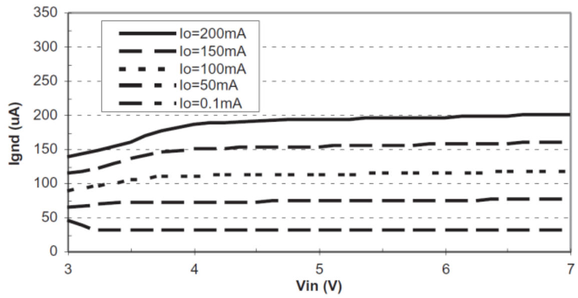


Fig. 10: I_{GND} vs. V_{IN} (SP6201 fixed 3.0V)

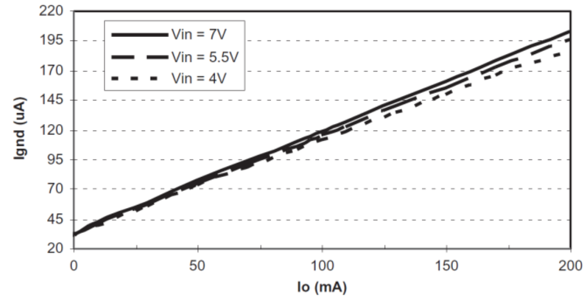


Fig. 11: I_{GND} vs. I_O (SP6201 fixed 3.0V)

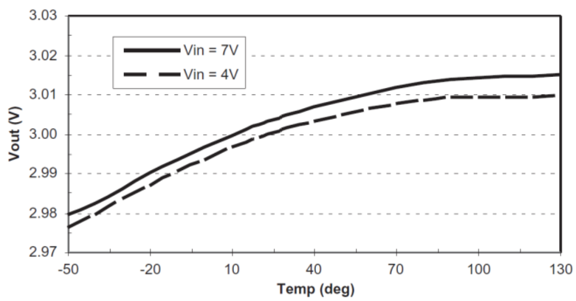


Fig. 12: V_{OUT} vs. Temp (fixed 3.0V)

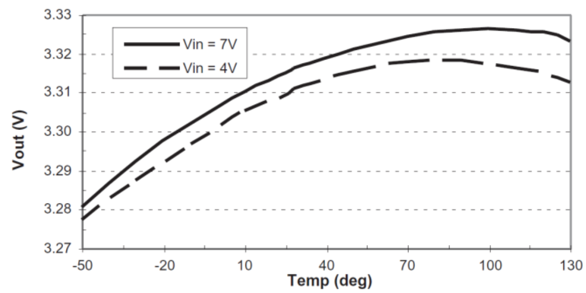


Fig. 13: V_{OUT} vs. Temp (fixed 3.3V)

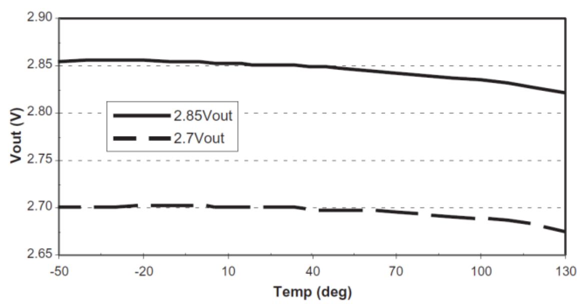


Fig. 14: V_{OUT} vs. Temp (adjustable)

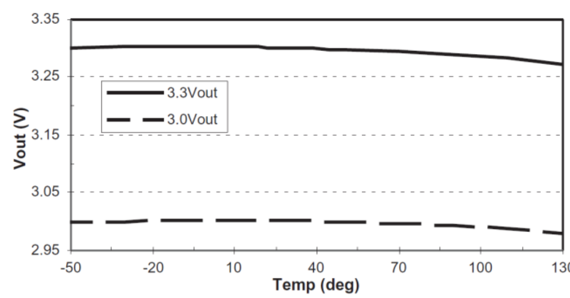


Fig. 15: V_{OUT} vs. Temp (adjustable)

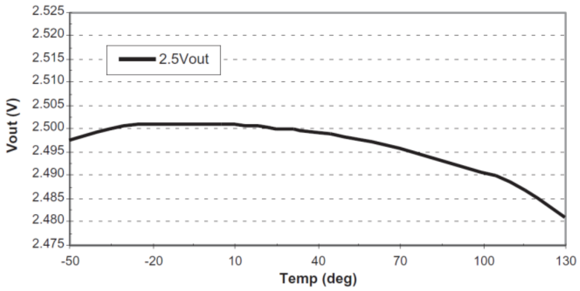


Fig. 16: V_{OUT} vs. Temp (adjustable)

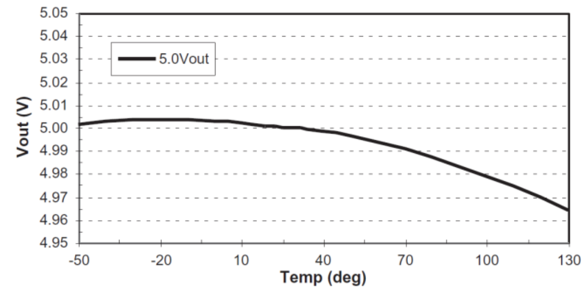


Fig. 17: V_{OUT} vs. Temp (adjustable)

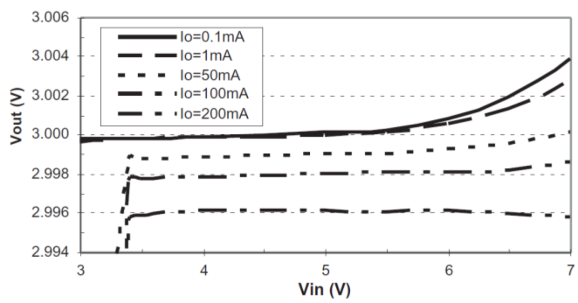


Fig. 18: Line Regulation (SP6201 fixed 3.0V)

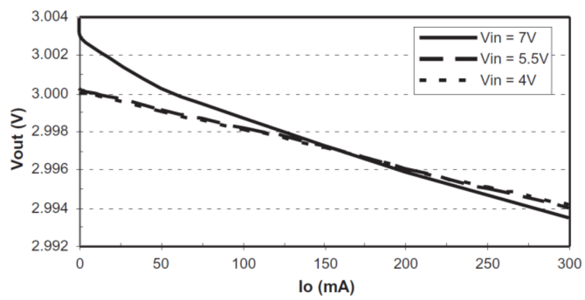


Fig. 19: Load Regulation (SP6201 fixed 3.0V)

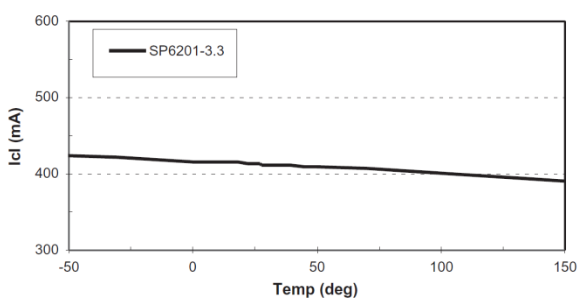


Fig. 20: Current Limit vs. Temp (fixed 3.3V, V_{IN}=4V)

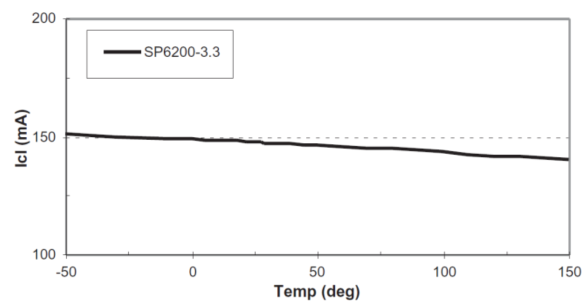


Fig. 21: Current Limit vs. Temp (fixed 3.3V, V_{IN}=4V)

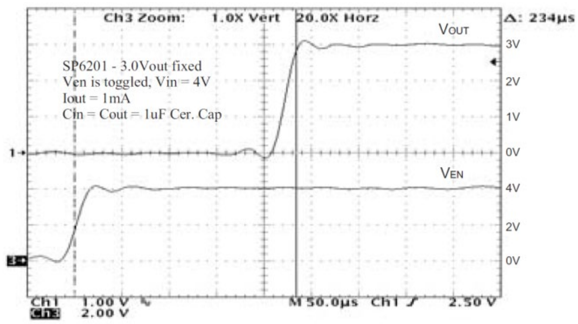


Fig. 22: Turn on time, I_O=1mA, $4V_{IN}$

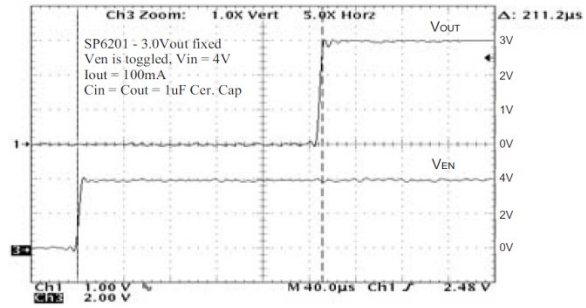


Fig. 23: Turn on time, I_O=100mA, $4V_{IN}$

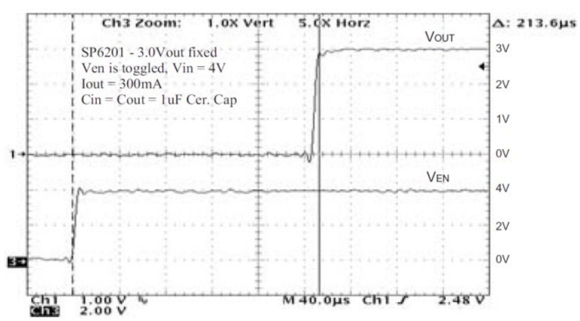


Fig. 24: Turn on time, I_O=300mA, $4V_{IN}$

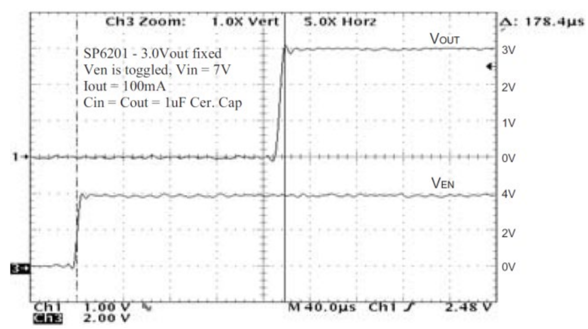


Fig. 25: Turn on time, I_O=100mA, $7V_{IN}$

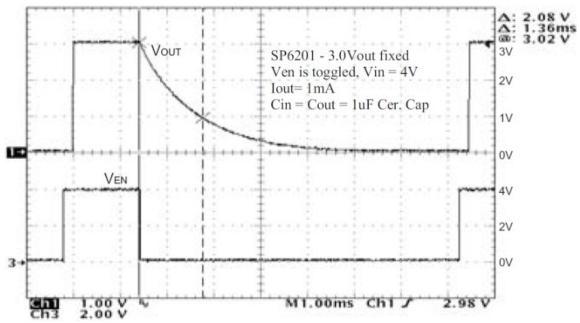


Fig. 26: Turn off time, I_O=1mA, $4V_{IN}$

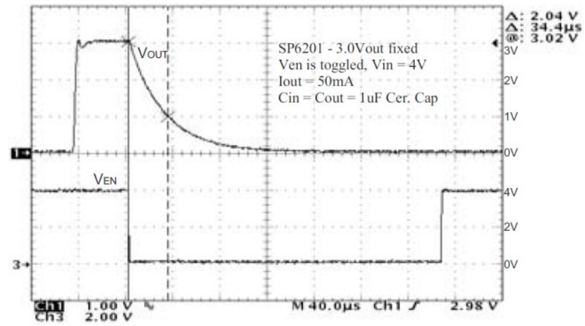


Fig. 27: Turn off time, I_O=50mA, $4V_{IN}$

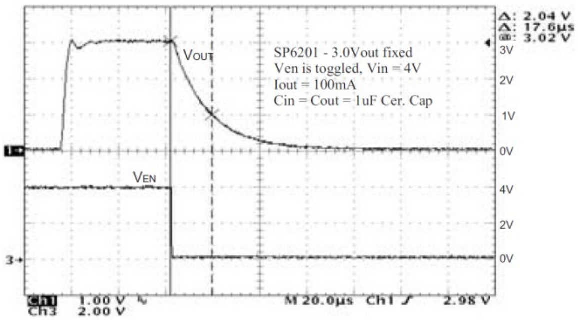


Fig. 28: Turn off time, I_O=100mA, $4V_{IN}$

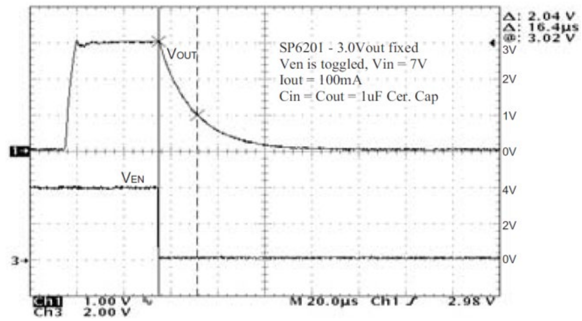


Fig. 29: Turn off time, I_O=100mA, $7V_{IN}$

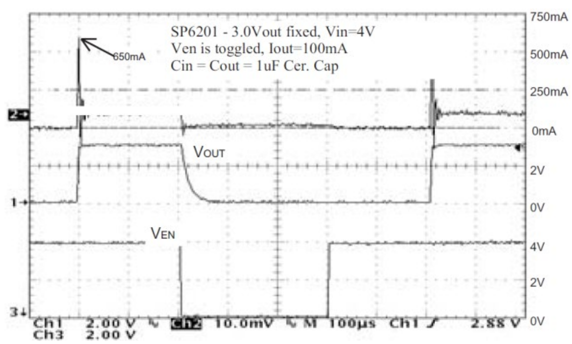


Fig. 30: Inrush Current, I_O=100mA

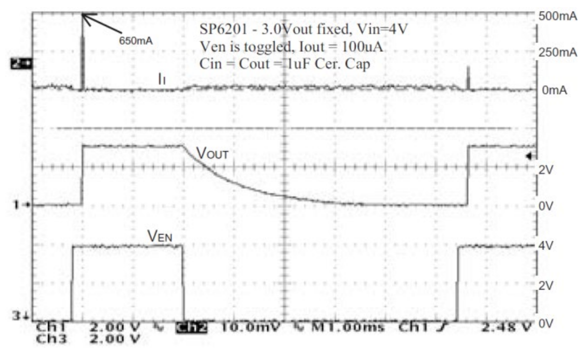


Fig. 31: Inrush Current, I_O=100μA

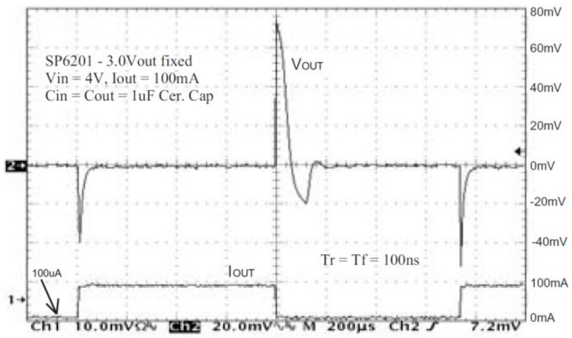


Fig. 32: Load Transient Response, 100mA step, $4V_{IN}$

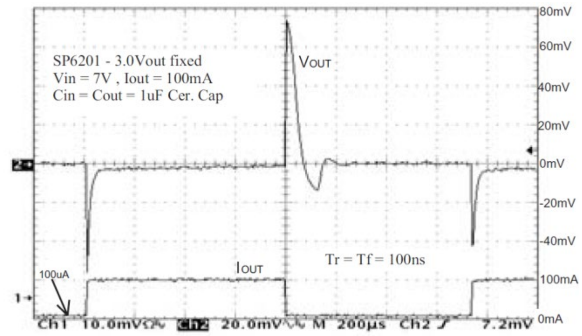


Fig. 33: Load Transient Response, 100mA step, $7V_{IN}$

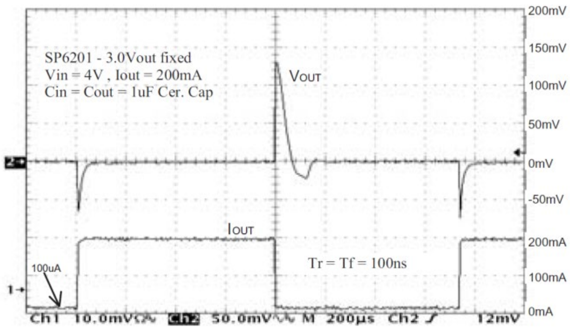


Fig. 34: Load Transient Response, 200mA step, $4V_{IN}$

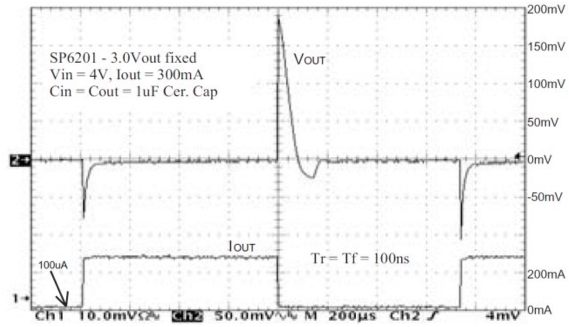


Fig. 35: Load Transient Response, 300mA step, $4V_{IN}$

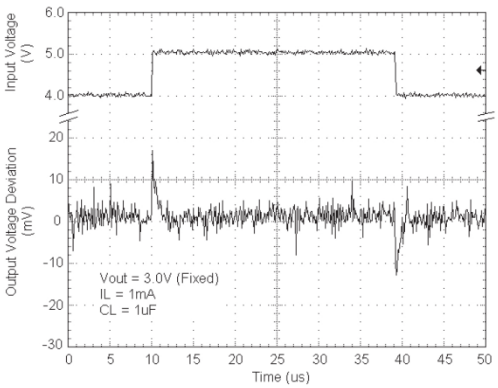


Fig. 36: Line Transient Response

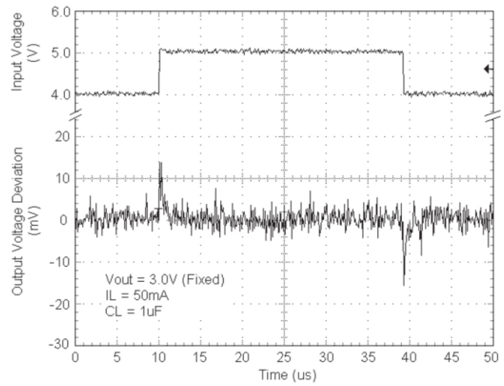


Fig. 37: Line Transient Response

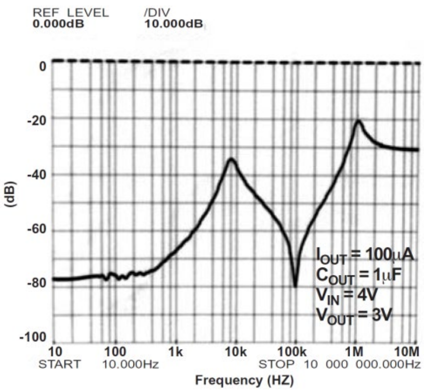


Fig. 38: Power Supply Rejection Ratio

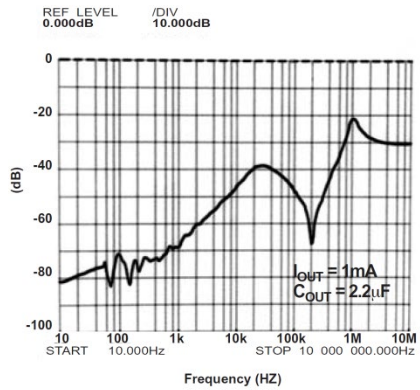


Fig. 39: Power Supply Rejection Ratio

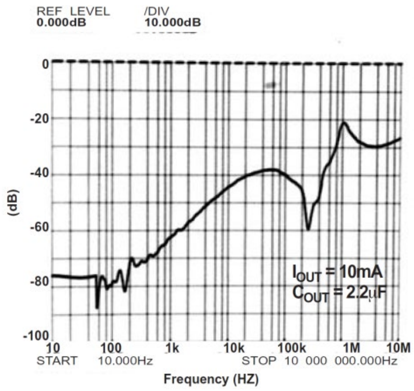


Fig. 40: Power Supply Rejection Ratio

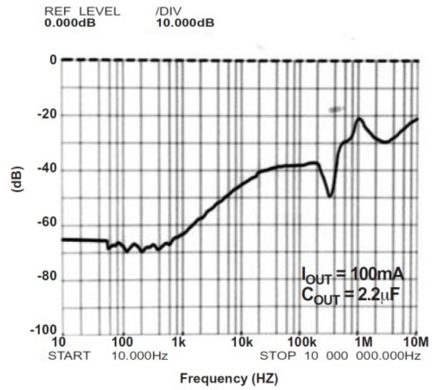


Fig. 41: Power Supply Rejection Ratio

THEORY OF OPERATION

GENERAL OVERVIEW

The SP6200 and SP6201 are CMOS LDOs designed to meet a broad range of applications that require accuracy, speed and ease of use. These LDOs offer extremely low quiescent current which only increases slightly under load, thus providing advantages in ground current performance over bipolar LDOs. The LDOs handle an extremely wide load range and guarantee stability with a 1µF ceramic output capacitor. They have excellent low frequency PSRR, not found in other CMOS LDOs and thus offer exceptional Line Regulation. High frequency PSRR is better than 40dB up to 400kHz. Load Regulation is excellent and temperature stability is comparable to bipolar LDOs. Thus, overall system accuracy is maintained under all DC and AC conditions. Enable feature is provided on all versions. A Vout good indicator (RSN pin) is provided in all the fixed output voltage devices. An adjustable output version is also available. Current Limit and Thermal protection is provided internally and is well controlled.

ARCHITECTURE

The SP6200 and SP6201 are only different in their current limit threshold. The SP6200 has a current limit of 140mA, while the SP6201 current limit is 420mA. The SP6201 can provide pulsed load current of 300mA. The LDOs have a two stage amplifier which handles an extremely wide load range (10µA to 300mA) and guarantees stability with a 1µF ceramic load capacitor. The LDO amplifier has excellent gain and thus touts PSRR performance not found in other CMOS LDOs. The amplifier guarantees no overshoot on power up or while enabled through the EN pin. The amplifier also contains an active pull down, so that when the load is removed quickly the output voltage transient is minimal; thus output deviation due to load transient is small and fairly well matched when connecting and disconnecting the load.

An accurate 1.250V bandgap reference is bootstrapped to the output in fixed output versions of 2.7V and higher. This increases both the low frequency and high frequency PSRR. The adjustable version also has the bandgap reference bootstrapped to the output, thus the lowest externally programmable output voltage is 2.7V. The 2.5V fixed output version has the bandgap always connected to the Vin pin. Unlike many LDOs, the bandgap reference is not brought out for filtering by the user. This tradeoff was made to maintain good PSRR at high frequency (PSRR can be degraded in a system due to switching noise coupling into this pin). Also, often leakages of the bypass capacitor or other components cause an error on this high impedance bandgap node. Thus, this tradeoff has been made with "ease of use" in mind.

PROTECTION

Current limit behavior is very well controlled, providing less than 10% variation in the current limit threshold over the entire temperature range for both SP6200 and SP6201. The SP6200 has a current limit of 140mA, while the SP6201 has a current limit of 420mA. Thermal shutdown activates at 162°C and deactivates at 147°C. Thermal shutdown is very repeatable with only a 2 to 3 degree variation from device to device. Thermal shutdown changes by only 1 to 2 degrees with Vin change from 4V to 7V.

ENABLE (SHUTDOWN NOT) INPUT

The LDOs are turned off by pulling the EN pin low and turned on by pulling it high. If it is not necessary to shut down the LDO, the EN (pin 3) should be tied to IN (pin 1) to keep the regulator output on at all time. The enable threshold is 0.9V and does not change more than 100mV over the entire temperature and V_{IN} voltage range. The lot to lot variations in Enable Threshold are also within 100mV. Shutdown current is guaranteed to be <1µA without requiring the user to pull enable all the way to 0V. Standard TTL or CMOS levels will transition the device from totally on to totally off.

RESET NOT (V_{OUT} GOOD) OUTPUT

An accurate V_{OUT} good indicator is provided on all the fixed output version devices, pin 4 (RSN), Figure 1. This is an open drain, logic output that can be used to hold a microprocessor or microcontroller in a RESET condition when its power supplied by V_{OUT} is 4% out of nominal regulation. A 1% hysteresis is included in the Reset Not function, so that false alarms are not issued as a result of LDO's output noise. The Reset Not function reacts in 10 to 50µs.

ADJUSTABLE OUTPUT VERSION

The adjustable version can be programmed to any voltage from 2.7V to 6V for the industrial temperature range; 2.5V to 6V for the commercial temperature range. The output cannot be programmed below 2.5V due a headroom restriction. Since the bandgap is bootstrapped to the output, the output voltage must be above the minimum bandgap supply voltage. The bandgap requires 2.7V or greater at -40°C and requires 2.5V or greater at 0°C. The regulator's output can be adjusted to a specific output voltage by using two external resistors, see block diagram. The resistor's set the output voltage based on the following equation:

$$V_{OUT} = 1.25 \times \left(1 + \frac{R_2}{R_1}\right)$$

Resistor values are not critical because the ADJ node has a high input impedance, but for best results use resistors of 470kΩ or less. A capacitor from ADJ to V_{OUT} pin provides improved noise performance as is shown in the following plot.

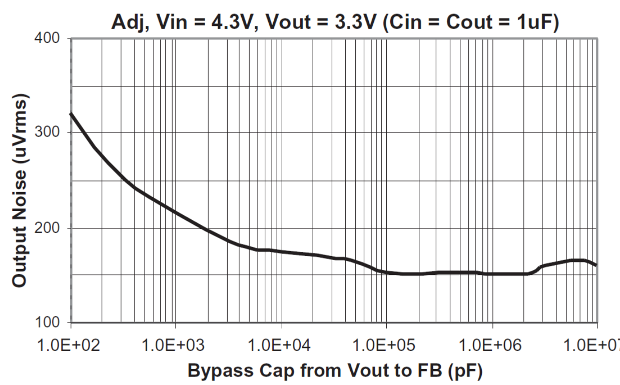


Fig. 42: Noise Performance 10Hz to 100kHz

INPUT CAPACITOR

A small capacitor, 1µF or higher, is required from V_{IN} to GND to create a high frequency bypass for the LDO amplifier. Any ceramic or tantalum capacitor may be used at the input. Capacitor ESR (effective series resistance) should be smaller than 3Ω.

OUTPUT CAPACITOR

An output capacitor is required between V_{OUT} and GND to prevent oscillation; a capacitance as low as 0.22µF can fulfill stability requirements in most applications. A 1µF capacitor will ensure unconditional stability from no load to full load over the entire input voltage, output voltage and temperature range. Larger capacitor values improve the regulator's transient response. The output capacitor value may be increased without limit. The output capacitor should have an ESR (effective series resistance) below 5Ω and a resonant frequency above 1MHz.

No Load Stability

The SP6200/SP6201 will remain stable and in regulation with no external load (other than the internal voltage driver) unlike many other voltage regulators. This is especially important in CMOS RAM keep-alive applications.

Thermal Considerations

The SP6200 is designed to provide 100mA of continuous current, while the SP6201 will provide 200mA of continuous current. Maximum power dissipation can be calculated based on the output current and the voltage drop across the part. To determine the maximum power dissipation in the package, use the junction-to-ambient thermal resistance of the device and the following basic equation:

$$P_D = \frac{(T_{J(MAX)} - T_A)}{\Theta_{JA}}$$

$T_{J(MAX)}$ is the maximum junction temperature of the die and is 125°C. T_A is the ambient operating. θ_{JA} is the junction-to-ambient thermal resistance for the regulator and is layout dependent.
The actual power dissipation of the regulator circuit can be determined using one simple equation:

$$P_D = \frac{125°C - 25°C}{191°C/W} = 0.52W$$

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_{GND} \cong (V_{IN} - V_{OUT}) \times I_{OUT}$$

Substituting $P_{D(max)}$ for P_D and solving for the operating conditions that are critical to the application will give the maximum operating conditions for the regulator circuit. For example, if we are operating the SP6201- 3.0V at room temperature, with a SOT-23-5 package on a 4 layer standard board we can determine the maximum input voltage for a set output current.

$$P_D = \frac{125°C - 25°C}{191°C/W} = 0.52W$$

To prevent the device from entering thermal shutdown, maximum power dissipation cannot be exceeded. Using the output voltage of 3.0V and an output current of 200mA, the maximum input voltage can be determined. Ground pin current can be taken from the electrical spec's table (I_{GND}=200μA at I_{OUT}=200mA). The maximum input voltage is determined as follows:

$$0.52W = (V_{IN} - 3.0V) \times 200mA + (V_{IN} \times 0.2mA)$$

Solving for V_{IN}, we get:

$$V_{IN} = \frac{0.52W + 0.6W}{200.2mA}$$

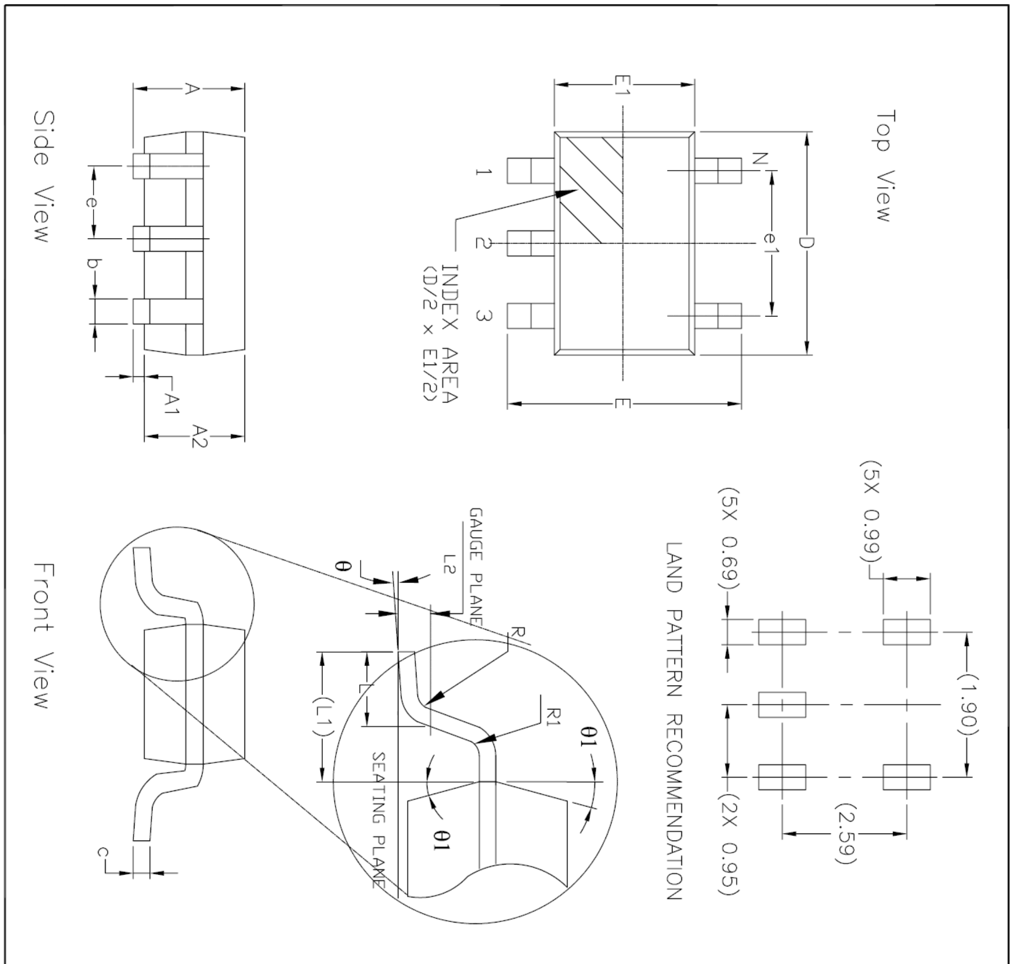
After calculations, we find that the maximum input voltage of a 3.0V application at 200mA of output current in an SOT-23-5 package is 5.59V.

Dual-Supply Operation

When used in dual supply systems where the regulator load is returned to a negative supply, the output voltage must be diode clamped to ground.

PACKAGE SPECIFICATION

5 PIN SOT-23



5 Pin SOT-23 JEDEC MO-178 Variation AA

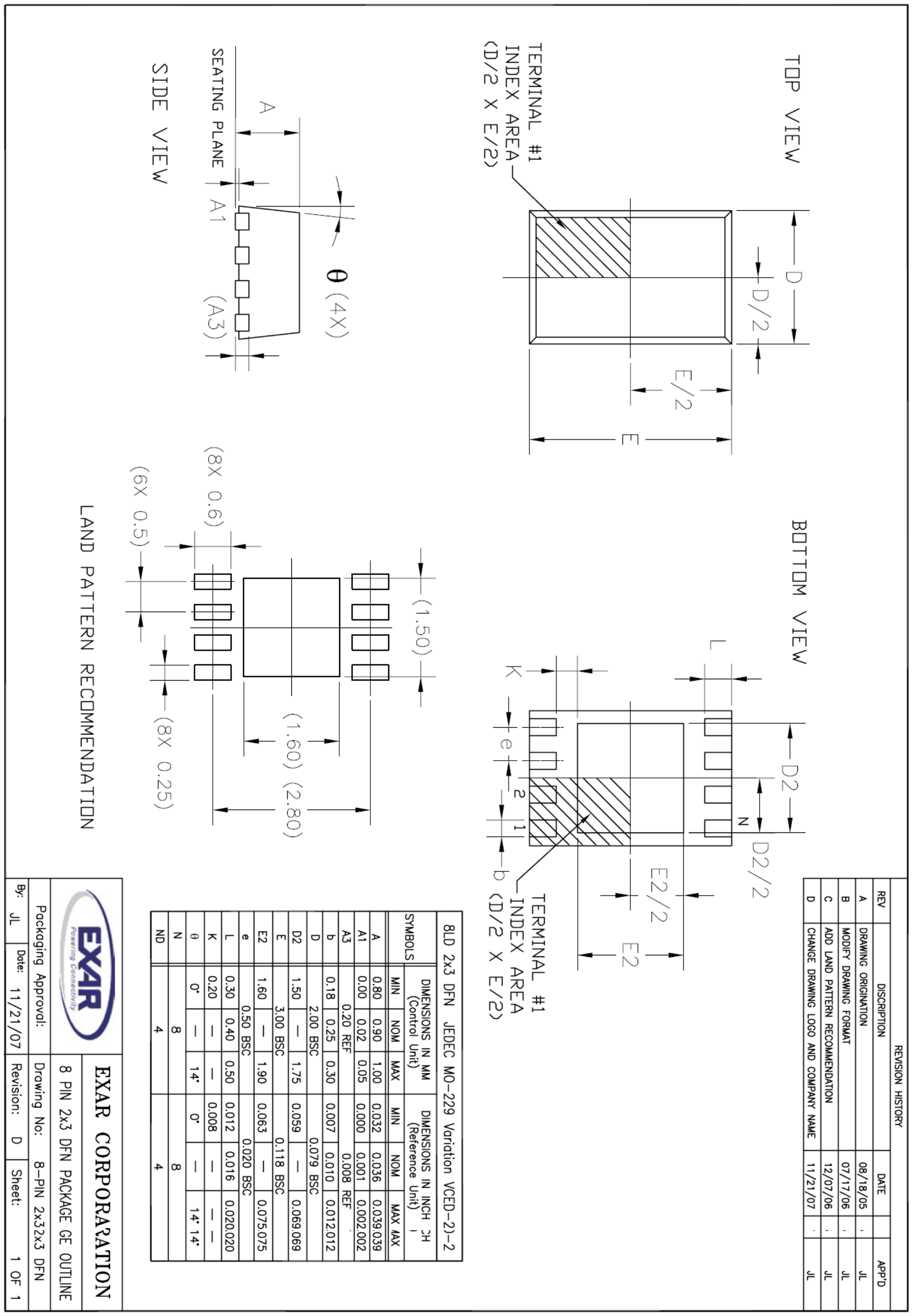
SYMBOLS	DIMENSIONS IN MM (Control Unit) MIN	NOM	MAX	DIMENSIONS IN INCH (Reference Unit) MIN	NOM	MAX
A	—	—	1.45	—	—	0.057
A1	0.00	—	0.15	0.000	—	0.006
A2	0.90	1.15	1.30	0.036	0.045	0.051
b	0.30	—	0.50	0.012	—	0.020
c	0.08	—	0.22	0.003	—	0.009
D		2.90 BSC			0.115 BSC	
E		2.80 BSC			0.111 BSC	
E1		1.60 BSC			0.063 BSC	
e		0.95 BSC			0.038 BSC	
e1		1.90 BSC			0.075 BSC	
L	0.30	0.45	0.60	0.012	0.018	0.024
L1		0.60 REF			0.024 REF	
L2		0.25 BSC			0.010 BSC	
R	0.10	—	—	0.004	—	—
R1	0.10	—	0.25	0.004	—	0.010
θ	0°	4°	8°	0°	4°	8°
θ1	5°	10°	15°	5°	10°	15°
N		5			5	

REVISION HISTORY

REV.	DESCRIPTION	DATE	APP'D
A	DRAWING ORIGINATION	10/3/05	JL
B	DRAWING FORMAT MODIFICATION	07/25/06	JL
C	ADD LAND PATTERN RECOMMENDATION	11/02/06	JL
D	CHANGE DRAWING LOGO AND COMPANY NAME	11/21/07	JL

EXAR CORPORATION
5 PIN SOT-23 PACKAGE OUTLINE
Packaging Approval:
Drawing No: 5-PIN SOT-23
By: JL Date: 11/21/07 Revision: D Sheet: 1 OF 1

8-PIN DFN DFN-8 version is obsolete



REVISION HISTORY			
REV	DESCRIPTION	DATE	APP'D
A	DRAWING ORIGINATION	08/18/05	JL
B	MODIFY DRAWING FORMAT	07/17/06	JL
C	ADD LAND PATTERN RECOMMENDATION	12/07/06	JL
D	CHANGE DRAWING LOGO AND COMPANY NAME	11/21/07	JL

8LD 2x3 DFN JEDEC MO-229 Variation VCED-2)-2

SYMBOLS	DIMENSIONS IN MM (Control Unit)			DIMENSIONS IN INCH (Reference Unit)		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.90	1.00	0.032	0.036	0.039
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3		0.20 REF			0.008 REF	
b	0.18	0.25	0.30	0.007	0.010	0.012
D		2.00 BSC			0.079 BSC	
D2	1.50	—	1.75	0.059	—	0.069
E		3.00 BSC			0.118 BSC	
E2	1.60	—	1.90	0.063	—	0.075
e		0.50 BSC			0.020 BSC	
L	0.30	0.40	0.50	0.012	0.016	0.020
K	0.20	—	—	0.008	—	—
θ	0°	—	14°	0°	—	14°
N		8			8	
ND		4			4	

REVISION HISTORY

Revision	Date	Description
2.0.0	03/28/2012	Reformatted Data Sheet Includes top package marking update.
2.1.0	05/29/2012	Corrected typographical error on page 1.
2.1.1	01/23/20	Updated to MaxLinear logo. Updated Ordering Information.

CORPORATE HEADQUARTERS:

5966 La Place Court

Suite 100

Carlsbad, CA 92008

Tel.: +1 (760) 692-0711

Fax: +1 (760) 444-8598

www.maxlinear.com